EXAR

DATABOOK

- TELECOMMUNICATION
- DATA COMMUNICATION
- MASS STORAGE
- ADVANCED CONSUMER
- STRATEGIC CAPABILITIES

EXAR
the analog plus company

DATABOOK

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Commitment to Customer Satisfaction

One of the founding principles of EXAR has been to focus on customer satisfaction through unsurpassed service and quality. Every individual at EXAR takes this principle as a personal commitment, assuring that quality and reliability are built into all our products from inception through production.

It is this very commitment which has given EXAR worldwide recognition as a dependable supplier of mixed-signal application-specific and custom integrated circuits to the communication and computer peripheral markets. This commitment along with our "analog plus" design expertise using in-house bipolar, CMOS, EEPROM and BiCMOS technologies, has increasingly made us the vendor of choice by customers seeking total system solutions.

I view this corporate dedication to quality, advanced technologies and service as the foundation to a mutually beneficial long term relationship with you, our valued customer.



Nob Hatta
President

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SO Availability List

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XR-215	Monolithic Phase-Locked Loop	Japanese SO (MD)
XR-C277	Low Voltage Receiver	JEDEC SO (D)
XR-501	R/W Preamplifier for 3 Terminal Recording Heads	JEDEC SO (D), PLCC (CJ)
XR-501R	R/W Preamplifier for 3 Terminal Recording Heads	JEDEC SO (D), PLCC (CJ)
XR-505	5V Low Power Single Supply Disk Drive R/W Preamplifier	JEDEC SO (D), PLCC (CJ)
XR-505R	5V Low Power Single Supply Disk Drive R/W Preamplifier	JEDEC SO (D), PLCC (CJ)
XR-507	5V, R/W Preamplifier for 3 Terminal Recording Heads	Japanese SO (K)
XR-507R	5V, R/W Preamplifier for 3 Terminal Recording Heads	Japanese SO (K)
XR-510A	R/W Preamplifier for 3 Terminal Recording Heads	JEDEC SO (D), PLCC (CJ)
XR-510AR	R/W Preamplifier for 3 Terminal Recording Heads	JEDEC SO (D), PLCC (CJ)
XR-532A	Low Power Data Synchronizer /2,7 RLL ENDEC	JEDEC SO (D), PLCC (CJ)
XR-541	Pulse Detector	JEDEC SO (D). PLCC (CJ) PQFP (Q)
XR-L555	Micropower Timing Circuit	Japanese SO (MD)
XR-567	Monolithic Tone Decoder	Japanese SO (MD)
XR-L567	Micropower Tone Decoder	Japanese SO (MD)
XR-1001/1008	General Purpose Low Pass Filters	JEDEC SO (D)
XR-1010	Second Order Switched Capacitor Filter	JEDEC SO (D)
XR-1016	Seventh Order Switched Capacitor Filter	JEDEC SOL (D)
XR-2100	V.21 Modem	PLCC (CJ)
XR-2135A	Bell/CCITT Type Data Buffer	JEDEC SOL (D)
XR-2206	Monolithic Function Generator	JEDEC SO (MD)
XR-2207	Voltage Controlled Oscillator	JEDEC SO (D)
XR-2211	FSK Demodulator/Tone Decoder	JEDEC SO (D), Japanese SO (MD)
XR-2321	V.23/V.21 Modem	PLCC (CJ), JEDEC SO (CD)
XR-2400	V.22bis Modem	PLCC (CJ), QFP (CQ)
XR-2403B	Enhanced MNP 5 Modem Microcontroller	PLCC (CJ)
XR-2442	V.42, MNP 2-5 Modem Controller	PLCC (CJ), QFP (CQ)
XR-2443	V.42bis, MNP 2-5 Modem Controller	PLCC (CJ), QFP (CQ)
XR-2900	FAX Data Modem	PLCC (CJ), QFP (CQ)
XR-2942	Fax/ Data V.42, MNP 2-5 Modem Controller	PLCC (CJ), QFP (CQ)

SO Availability List

PART NO.	DESCRIPTION	SO PACKAGE (SUFFIX)
XR-2943	Fax/ Data V.42bis, MNP 2-5 Modem Controller	PLCC (CJ), QFP (CQ)
XR-4151	Voltage-to-Frequency Converter	Japanese SO (MD)
XR-4610/4610R	R/W Preamplifier for 2 Terminal Heads	JEDEC SO (D)
XR-8073	Micropower Step-up Switching Regulator	JEDEC SO (D)
XR-T56L22	Low Power PCM Receiver/Repeater	JEDEC SO (D)
XR-T5650	PCM Line Receiver & Clock Recovery Circuit	JEDEC SO (D)
XR-T5675	PCM Line Driver	JEDEC SO (D)
XR-T5684	CMOS Digital T1 Line Interface	PLCC
XR-T5690	T1/ISDN Primary Rate Framer	PLCC (CJ)
XR-T5691	T1/ISDN Primary Rate Framer	PLCC (CJ)
XR-T7295	DS3 / STS-1 Integrated Line Receiver	SOJ (IW)
XR-T7296	DS3 / STS-1 Integrated Line Transmitter	SOJ (IW)
XR-8038	Precision Waveform Generator	Japanese SO (MD)
XR-9010/9010R	5V R/W Preamplifier for 3 Terminal Recording Heads	JEDEC SO (D)
XR-9022	5V Low Pass Filter with Differentiator and Pulse Slimming	JEDEC SO (D) Japanese SO (MD)
XR-9030	5V R/W Preamplifier for 2 Terminal Recording Heads	JEDEC SO (D)
XR-9040	5V Disk Drive Pulse Detector	PQFP (D)
XR-9050	1,7 RLL Data Separator & ENDEC with Write Precompensation	PLCC (J) JEDEC SO (D)
XR-9080	Frequency Synthesizer 1,7 RLL Data Seperator & ENDEC	PQFP (Q) 52
XR-T56188	T1 / CEPT Jitter Attenuator	SOIC (CD, ID)
XR-T56189	T1 / CEPT High Speed Jitter Attenuator	SOIC (CD, ID)
XR-16C450	CMOS UART	PLCC (CJ)
XR-16C452	CMOS DUART with Parallel Printer Port	PLCC (CJ)
XR-16C550	CMOS DUART with FIFO	PLCC (CJ)
XR-16C552	CMOS DUART with Parallel Printer Port &FIFO	PLCC (CJ)
XR-T66100	Caller I.D. Receiver I.C.	SOIC (CD)
XR-68C681	CMOS Dual Channel UART (DUART)	PLCC (CJ, J) CLCC (ML)
XR-82C684	CMOS Quad Channel UART (QUART)	PLCC (CJ, J)
XR-88C681	CMOS Dual Channel UART (DUART)	PLCC (CJ, J) CLCC (ML)

Product Ordering Information
(for products introduced prior to 1989)

PART IDENTIFICATION		DEFINITION OF SYMBOLS:
XR Manufacturer's Prefix	XXXXX Basic Type	M = Military Grade Part, Ceramic Package Only are guaranteed to operate over military temperature range. Consult factory for level of high rel screening N = Prime Grade Part, Ceramic Package P = Prime Grade Part, Plastic Package
GRADE M = Military N = Prime Electrical P = Prime Electrical C = Commercial F = 4.75 V to 15 V Operating V = 4.75 V to 6 V Voltage Ranges K = Kit	**PACKAGE TYPE** N = Ceramic Dual-in-Line P = Plastic Dual-in-Line MD = Plastic SOIC (Surface Mount) Q = Quad Package	N, P, CN, and CP parts are electricaly identical and operate over 0°C to +70°C unless otherwise stated. In addition, N and P parts generally have operating parameters more tightly controlled than the CN or CP parts.

For details, consult EXAR Sales Headquarters
or your Sales/Technical Representatives.

Example

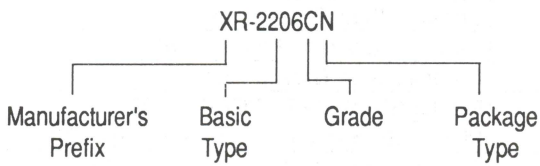


TABLE 1. OPERATING TEMPERATURE RANGE

Designator	DESCRIPTION
C	COMMERCIAL (0 deg C TO 70 deg C)
W	As specified on data sheet
I	INDUSTRIAL (-40 deg C to +85 deg C)
M	MILITARY (-55 deg C to +125 deg C)

TABLE 2. PACKAGE DESCRIPTION

Designator	DESCRIPTION
P	Plastic Dual In Line (PDIP)
N	Ceramic Dual In Line (CDIP)
J	Plastic Leaded Chip Carrier (PLCC)
L	Ceramic Leadless Chip Carrier (LCC)
D	JEDEC Plastic Small Outline (SOIC)
Q	Plastic Quad Flat Pack (Metric QFP)
K	EIAJ Plastic Small Outline (SOP)
H	Hybrid
R	Ceramic Side Brazed DIP
S	Ceramic Brazed J-lead Carrier
T	Ceramic Side Brazed SOIC
V	Plastic Shrink QFP (SQFP or VQFP)
Z	Plastic Staggered In Line Package (ZIP)
Y	Plastic Single In Line Package (SIP)
U	Plastic Shrink SOP (SSOP)
W	JEDEC Plastic J-bend Small Outline (SOJ)
E	Ceramic J-lead Quad Package (J-CQUAD)
C	Die (Chip)
F	Wafer
I,O,X	Not Used

TABLE 3. PACKAGE VARIATION

VARIATION	DESCRIPTION
P(A)22	22ld 300 mils PDIP
PB22	22ld 400 mils PDIP
P(A)24	24ld 600 mils PDIP
PB24	24ld 300 mils PDIP
N(A)24	24ld 600 mils CDIP
NB24	24ld 400 mils CDIP
NC24	24ld 300 mils CDIP
D(A)16	16ld 300 mils SOIC
DB16	16ld 150 mils SOIC
Q(A)44	JEDEC 44LD QFP
QB44	EIAJ 44LD QFP
Q(A)64	JEDEC 64LD QFP
QB64	EIAJ 64LD QFP
Q(A)80	JEDEC 80LD QFP
QB80	EIAJ 80LD QFP

TABLE 4. SCREEN LEVEL

SCREENING	PLASTIC			CERAMIC			REMARK
	STD	XL2	XL3	STD	XL5	XL6	
Pre cap Internal Visual	per XR Std	per XR Std	per XR Std	per XR Std	per XR Std	per XR Std	100%
Fine Leak				1% AQL	1% AQL	1% AQL	
Gross Leak				100%	100%	100%	
Pre Burn In Electrical		OPTIONAL	OPTIONAL		OPTIONAL	OPTIONAL	Per Device Spec
Burn In		48 hours	160 hours		48 hours	160 hours	
Final Electrical	100%	100%	100%	100%	100%	100%	Per Device Spec
AQL Sample	0.10%	0.10%	0.10%	0.10%	0.10%	0.10%	
External Visual	per XR Std	per XR Std	per XR Std	per XR Std	per XR Std	per XR Std	100%
QA Plant Clearance	100%	100%	100%	100%	100%	100%	

Cross Reference Guide

The following guide is provided to assist you in determining the EXAR part number equivalent to industry standard products from various manufacturers. The level of interchangeability is indicated in the accompanying note as described below:

No reference note: "Direct replacement"
Note (1): "Pin compatible - pin-for-pin compatible device but specifications may differ. Consult datasheet for suitability
Note (2): "Functional equivalent" - functional equivalent, but may not be pin-for-pin compatible. Consult datasheet for suitability.

Competitor	Competitor Part Number	EXAR Part Number	Note
Dallas Semiconductor	DS2176	XR-T5691	
	DS2180A	XR-T5690	
Gould/AMI	S3528	XR-1015	(2)
	S3528	XR-1016	(2)
	S3541	XR-1020A	(2)
Harris	ICM7555	XR-L555	(1)
	ICM7556	XR-L556	(1)
	ICM7240	XR-2240	(1)
	ICM8240	XR-2240	(1)
	ICM8038	XR-8038	(1)
	CP82C50A	XR-16C450	(1)
	HF10	XR-1010	(1)
	HA5002	XR-117	

Cross Reference Guide

Competitor	Competitor Part Number	EXAR Part Number	Note
Linear Technology	LTC1060	XR-1010	(1)
	LTC1062	XR-1015	(2)
Maxim	MF10	XR-1010	(1)
	ICM7240	XR-2240	
	ICM7242	XR-2242	(1)
	MC34072	XR-34072	
	MC34074	XR-34074	
	MC2681	XR-88C681	(1)
	MC68681	XR-68C681	
	MC34118	XR-T65118	
	MC34119	XR-T65119	
National	LM146/346	XR-146/346	
	LM567	XR-567	
	MF4C-100	XR-1001	(1)
	MF4C-50	XR-1002	(1)
	MF4C-100	XR-1003	(1)
	MF4C-50	XR-1004	(1)
	MF4C-100	XR-1005	(1)
	MF4C-50	XR-1006	(1)
	MF4C-1007	XR-1007	(1)
	MF4C-1008	XR-1008	(2)
	MF10	XR-1010	(1)
	LM1524/3524	XR-1524/3524	
	NS16C450	XR-16C450	
	µA2240	XR-2240	

Cross Reference Guide

Competitor	Competitor Part Number	EXAR Part Number	Note
Raytheon	XR2207	XR-2207	
	XR2211	XR-2211	
	RC4136	XR-4136	
	RC4151	XR-4151	
	RC5532/5532A	XR-5532/5532A	
	RC5534/5534A	XR-5534/5534A	
Reticon	RU5621/22	XR-1010	(2)
	RF5609	XR-1015	(2)
	RF56009	XR-1016	(2)
	RF5651	XR-1020A	(2)
Signetics	NE567	XR-567	
	SG3524	XR-3524	
	NE5532	XR-5532	
	NE5534	XR-5534	
	SCN2681	XR-88C681	(1)
	SCN2692	XR-88C681	
	SCN68681	XR-68C681	
Silicon Systems	SSI32R117	XR-117	
	SSI32R501	XR-501	
	SSI32R511	XR-511	
	SSI32P541	XR-541	
	SSID5321	XR-532	
Silicon General	SG1524/3524	XR-1524/3524	
Texas Instruments	µA2240	XR-2240	
	SG3524	XR-3524	
	RC4136	XR-4136	
	NE5532	XR-5532	
	NE5534	XR-5534	

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TELECOMMUNICATION APPLICATION NOTES

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SECTION 2

Product Selection Guide

Part Number	Description	Product Features	Technology	Supply Voltages	Package
PCM Repeaters					
XR-C240	Monolithic PCM Repeater	Recovers and Regenerates AMI Encoded Data 1 Port ALBO 13.5mA Supply Current 2,048 MBPS (6300 ft) Operation Pulsed Clock Recovery	Bipolar	+8.2V ± 5% +4.3V ± 5%	16 Pin Ceramic
XR-C262 XR-C262Z (Improved ALBO)	Monolithic PCM Repeater	Recovers and Regenerates AMI Encoded Data 15mA Supply Current 2.048 MBPS (6300 ft) Operation Pulsed Clock Recovery Automatic Zero Input Shutdown	Bipolar	+6.8V ± 5%	16 Pin Ceramic
XR-C277	High Performance Low Power Repeater	Recovers and Regenerates AMI Encoded Data 1 ALBO Port 13mA Supply Current 2.048 MBPS (6300 ft) Operation Pulsed/Locked Clock Recovery	Bipolar	+6.3V ± 5% +4.3V ± 5%	16 Pin Ceramic
XR-TM044H		Line Equalization Optimized to 1.544 MPBS Complete ALBO Circuitry Smoothing ALBO Filter Network Fixed Gain and Compensation Network Improved Crosstalk and Noise Through Simplified Layout	Hybrid	+5V ± 10%	16 Pin Ceramic
XR-T5600 T5620	High Performance PCM Repeater	Recovers and Regenerates AMI Encoded Data Triple Matched ALBO Ports 22mA Supply Current 2.37 MBPS (6300 ft) Operation Pulsed Clock Extraction	Bipolar	+5.1V ± 5%	18 Pin Ceramic Plastic
XR-T5720	High Performance Crystal Clock Repeater	Recovers and Regenerates AMI Encoded Data Triple Matched ALBO Ports 22mA Supply Current 2.37 MBPS (6300 ft) Operation Crystal Clock Extraction	Bipolar	+5.1V ± 5%	18 Pin Ceramic Plastic
XR-T56L22	High Performance, Long Haul PCM Repeater	Extracts +Data, –Data & Clock Dynamic Range: 5 to 42dB Very Low Power (8.75mA Max) Applications: T1, CEPT Double Matched ALBO Ports Operating Range: –40°C to +85°C Internal Shunt Regulator Internal Adjustable Phase Shift Circuit	Bipolar	+5V ± 5%	18 Pin Ceramic Plastic S.O.P.

TELECOMMUNICATION

Part Number	Description	Product Features	Technology	Supply Voltages	Package
PCM Line Interface					
XR-T5681	Short Distance, Low Power PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB Balanced or Unbalanced Receiver Inputs All TTL Compatible Interface LC Clock Extraction Applications: Up to 3MBPS Supply Current: 35mA	Bipolar	+5V ± 5%	18 Pin Ceramic
XR-T5683	Short Distance, High Freq. PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB Balanced or Unbalanced Receiver Inputs All TTL Compatible Interface LC Clock Extraction Applications: Up to 8.448MBPS Supply Current: 40mA	Bipolar	+5V ± 5%	18 Pin Ceramic
XR-T5684	Short Distance DSX-1 PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB (DSx-1 Interface) Accepts Balanced or Unbalanced Inputs TTL Compatible Interfaces No LC Tuning Required Meets Bell Pub 62411, Pub 43802 and G.703 Transmitter Equalizer From 0 to 655 feet	CMOS	+5V ± 5%	8 Pin Ceramic Plastic S.O.P.
XR-T56188	T1/CEPT Jitter Attenuator	Reduces jitter present on clock and data for T1 and CEPT lines. Meets jitter templates for TR62411, TR-TSY-000170, G.735, and G.742 Selectable buffer size:144, 32, 16, 8 Disable pin Pin to pin and functionally compatible to DS2188	CMOS	5V±10%	Plastic, SOIC
XR-T56189	T1/CEPT High Speed Jitter Attenuator	Reduces jitter present on clock and data for T1 and CEPT lines up to 144Ulpp. Meets jitter templates for TR64211, TR-TSY-000170, G.735 and G.742. Selectable buffer size:144, 32, 16, 8 Disable pin option Pint to pin and functionally compatible to DS2188 Maximum Data Rate (8.5MHz)	CMOS	5V±10%	Plastic, SOIC
XR-T56L85	Short Distance, Single Ended PCM Line Interface	Receiver and Transmitter in One Package Dynamic Range: 0 to 10dB Receiver Accepts: Transformer Input Capacitive Coupled Single Coaxial Input TTL Compatible Inputs LC Clock Extraction Applications: T1. CEPT Very Low Power (14mA Typ) Pin Compatible with XR-T5683	Bipolar	+5V ± 5%	18 Pin Ceramic Plastic S.O.P.
XR-T6164	Codirectional G.703 CCITT Line Interface	Analog IC (Short Line Transceiver Function Adaptive Detection Threshold Dual High Current Line Drivers Loss of Signal Alarm	Bipolar	+5V ± 5%	16 Pin Ceramic

Part Number	Description	Product Features	Technology	Supply Voltages	Package
PCM Line Interface (continued)					
XR-T6165 XR-T6166	Codirectional G.703 CCITT Line Interface	Digital IC (Digital Data Processor) Converters 64kbit/s Data to 2.048MBPS Data and Vice Versa Recovers Both Clock and Octet Timing Performs Byte Insertion and Deletion Programmable Loss of Lock Alarm AMI Coding and Bipolar Violation Insertion	CMOS	+5V ± 5%	22 Pin Ceramic
XR-T7295	DS3/SONET STS-1 Integrated Line Receiver	DS3 & STS-1 receive interface Integrated equalization and timing recovery Loss of signal and loss of lock alarms Variable input sensitivity control. Compliance to AT&T Pub 54014, ANSI Standard T1.102-1989, compatibility bulletin119, CCITT G.703 and G.824 and TR-TSY-000449.	CMOS	+5V±5%	Plastic, SOIC
XR-T7296	DS3/SONET STS-1 Integrated Line	Fully integrated transmit interface for T3 or E3 Integrated pulse shaping circuit for line length select . Build-in B3ZS/HDB3 encoder and decoder Bipolar violation and error-rate output Integrated Driver monitor circuit	Bipolar	+5V±5%	Plastic, SOIC
Framers/Coders					
XR-T5690	Serial T1 Framer	Supports 12 Frame and 24 frame/ Superframe Pin Compatible to: DS2180 B8ZS, B7 Stuffing and Zero Suppression Modes Operates in Hardware or Serial Processor Mode 0, 2, 4 and 16 State Robed Bit Signaling Modes Clear and Non-Clear DS0 Channels on DS1 Link Alarm Generation and Detection Receive Error Detection and Counting	CMOS	+5V ± 5%	40 Pin Plastic 44 Pin PLCC
XR-T5691	Receive Buffer	Synchronize T1 Data Streams to System Clocks Two Frame Buffer Depth Frame Slip Output at Frame Boundaries Buffer Recentering Capability Recommended Operating Frequency: 1.544 and 2.048 MBPS Interfaces to Parallel and Serial Backplanes Robbed-bit Signaling Extraction and Buffering Inhibits Signaling Updates During Alarm or Slip Conditions Integration Feature "Debounces" Signaling Pin Compatible to: DS2176	CMOS	+5V ± 5%	24 Pin Plastic PLCC

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Part Number	Description	Product Features	Technology	Supply Voltages	Package
Coder/Decoder					
XR-T5670	B8ZS/AMI Line Transcoder	B8ZS/AMI Coding and Decoding Max Frequency: 6MHz Complies to Tech Advisory 69 Code Error Detector Looptest Capability All Ones Alarm Indicator	CMOS	+5V ± 5%	16 Pin Ceramic Plastic
Loopback Circuits					
XR-T2713	Loopback Detector	Loopback Detector According to Bell Pub 4300 Detection Band: 2713 or 2813 ± 15Hz Detection Level: –32dB Complementary Output Signal Low Power (2mA @ 12V) 4 or 20 minutes Time Out	CMOS	+5V ± 5%	16 Pin Plastic
Drivers/Receivers					
XR-T3588 XR-T3589	V.35 Line Driver/Receiver	CCITT V.35 & Bell 306 Compatible Interface Driver Inputs and Receiver Output are TTL High Common Mode Voltage Range 10MBPS Operation Capability Individual Power Down Capability	Bipolar	+5V ± 5%	18 Pin Ceramic 14 Pin Ceramic
XR-T5650	Long Distance PCM Line Receiver	Extracts +Data, –Data & Clock Dynamic Range 10 to 36dB Applications: T1, CEPT Double Matched ALSO Ports	Bipolar	+5V ± 5%	18 Pin Ceramic
XR-T5675	PCM Line Driver	High Speed Switching Dual Matched Driver Outputs TTL or DTL Compatible Inputs 50mA Output Current Capability Current Consumption: 18mA	Bipolar	+5V ± 5%	8 Pin Ceramic Plastic
XR-T5676	Low Power PCM Line Receiver	Low Power T1/CEPT Receiver Up to 2.048 MBPS Operation TTL Compatible Interface Inputs: Balanced Transformer Capacitively Coupled Single Coaxial	Bipolar	+5V ± 10%	Ceramic Plastic SOIC
Telephone Circuits					
XR-T65118	Voice Switched Speakerphone Circuit	Attenuator Gain Range: 52dB Improved Sensitivity: 4 Point Signal Sensing Background Noise Monitor on Transmit and Receive Sides Mute Feature with Externally Adjustable Microphone Amplifier Gain Chip Disable for Active/Standby Operation On Board Filter Pinned Out for User Defined Function Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence Compatible with the XR-T34119 Speaker Amplifier	Bipolar	+5V ± 10%	Plastic SOIC

Part Number	Description	Product Features	Technology	Supply Voltages	Package
Telephone Circuits (continued)					
XR-T65119	Low Power Audio	Low Quiescent Supply Current (2.7mA Typical-Battery Powered Applications) Chip Disable Input for Power Down Applications Low Power Down Quiescent Current (65µA typical) Wide Range Drive Capability (8-100 ohms) Low Harmonic Distortion (0.5% typical) Adjustable Gain (0 to 46dB for Voice Band)	Bipolar	+5V ± 10%	Plastic SOIC
XR-T66100	Caller Identification Receiver IC	On-chip ring detector and ring qualifier Power down operation On-chip Band-pass filter (Bell 202 compliant) FSK Demodulator with energy detect High input sensitivity (-35 dBm) Low current consumption in power down mode	CMOS	5V±10%	Plastic SOIC

Monolithic PCM Repeater

GENERAL DESCRIPTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rate on T1-type PCM lines.

The XR-C240 monolithic IC is packaged in a hermetic 16-pin DIP package, and is designed to operate over a temperature range of –40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic-Lin- Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance, along with significant savings in power consumption and system cost.

FEATURES

Contains all Active Components of PCM Repeater
On-Chip ALBO Port
High-Current Output Drivers
Low-Power Consumption
Increased Reliability over Discrete Designs
2 Megabit Operation Capability

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 MBPS Systems

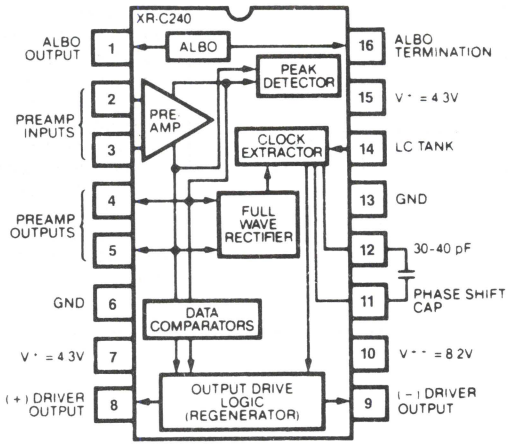
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Supply Voltage	–0.5 to 10V
Input Voltage (Except Pin 1, 16)	–0.5 to +7V
Input Voltage (Pin 7, 16)	–0.5 to +0.5V
Data Output Voltage (Pin 8, 9)	+20V
Voltage Surge (Pin 2, 3, 8, 9) (10 msec only)	50V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C240	Ceramic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-C240 contains all the active circuits required to build one side of a T1 or 2 MBPS PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36dB at 772kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier Automatic Line Build Out (ABLO), clock and data threshold detector circuits contained within the XR-C240. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO ports and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by driving an injection locked oscillator tuned to 1.544MHz. The oscillator's sinusoidal waveform is amplified and phase shifted by 90 degrees with the help of a capacitor between Pins 11 and 12.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

(Measured at 25°C with VCC1 = 8.2V, VCC2 = 4.3V, unless specified otherwise.)

PARAMETERS	LIMITS MIN	LIMITS MAX	UNIT	CONDITIONS
Supply Voltage				
VCC1	7.79	8.61	V	Measured at Pin 10
VCC2	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current				
I_A	1.1	2.5	mA	
I_B	6	11	mA	Supply = 8.2V
Total Current	7.9	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	dB	
Input Bias Current, I_B		4	µA	
Input Offset Current, I_{OS}		2	µA	
Input Impedance, R_{in}	50		kΩ	
Comparator Thresholds				
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	Measured Differentially Across Pins 4 and 5
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	µA	
"One" Signal Current	80	220	µA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	−18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero.
Output Drive Section				
				Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100Ω
Low Output Voltage	0.65	0.95	V	Referenced to Pin 7, I_L = 30mA
Output Leakage Current		50	µ A	
Output Pulse				
Maximum Pulse Width Error		±30	ns	
Rise and Fall Times		80	ns	

High-Performance PCM Repeater

GENERAL DESCRIPTION

The XR-C262 is a high-performance monolithic repeater IC for pulse-code modulated (PCM) telephone lines. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rates on T1-type PCM lines.

The XR-C262 operates with a single 6.8 volt power supply, and with a typical supply current of 13mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to their "off" state automatically, when there is no input signal present.

FEATURES

Contains all Necessary Active Components of a PCM Repeater
Uses L-C Tank for Clock Recovery
Low-Voltage Operation (6.8 volts)
Low-Current Drain (13mA, typical)
High-Current Bipolar Output Drivers
On-Chip ALBO Equalizer
Automatic Zero-input Shutdown
Increased Reliability Over Discrete Designs
2 Megabit Operation Capability

APPLICATIONS

PCM Repeater for T1 Systems
Repeater for 2 MBPS PCM Systems

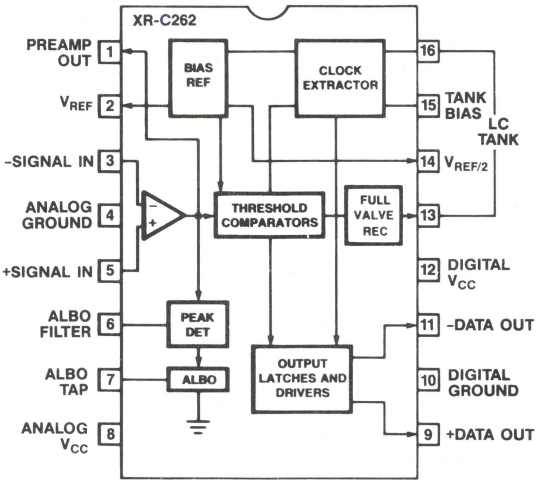
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Supply Voltage	–0.5 to +10V
Input Voltage (Except Pin 6, 7)	–0.5 to +7V
Input Voltage (Pin 6, 7)	–0.5 to +0.5V
Data Output Voltage (Pin 9, 11)	+20V
Voltage Surge (Pin 3, 5, 9, 11) (10 msec only)	50V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262	Ceramic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-C262 contains all the active functions required to build one side of a T1 or 2 MBPS PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 MBPS. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36dB at 772kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier Automatic Line Build Out (ALBO), clock and data threshold detector circuits contained within the XR-C262. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO port and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544MHz.

Data is sampled and stored in the output data latches. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurrence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC} = 6.8V$, $T_A = -40°C$ to $+85°C$.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	–15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	µA	Measured at Pin 16
Comparator Thresholds					
ALBO Threshold	0.75	0.9	1.1	V	Measured at Pin 1 relative to Pin 14
Clock Threshold	0.323	0.4	0.517	V	
Data Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					
Output High Swing	5.9	6.8		V	Measured at Pins 9 and 11
Output Low Swing	0.6	0.7	0.9	V	$R_L = 400Ω$
Leakage Current			100	µA	$I_L = 15mA$
Output Pulse Width	294	324	354	nsec	Measured with output in off state
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

High-Performance PCM Repeater

GENERAL DESCRIPTION

The XR-C262Z is a high-performance monolithic repeater IC for pulse-code modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rate on T1-type PCM lines.

The XR-C262Z operates with a single 6.8 volt power supply, and with a typical supply current of 13mA. It provides bipolar output drive with high-current handling capability. The clock extractor section of XR-C262Z uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to their "off" state automatically, when there is no input signal present.

FEATURES

Contains all Necessary Active Components of a PCM Repeater
Uses L-C Tank for Clock Recovery
Low-Voltage Operation (6.8 volts)
Low-Current Drain (13mA, typical)
High-Current Bipolar Output Drivers
On-Chip ALBO Port
Automatic Zero-Input Shutdown
Increased Reliability Over Discrete Designs
2 Megabit Operation Capability
Pin-to-Pin Compatible with XR-C262 with Improved Switching Characteristics

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 MBPS Systems

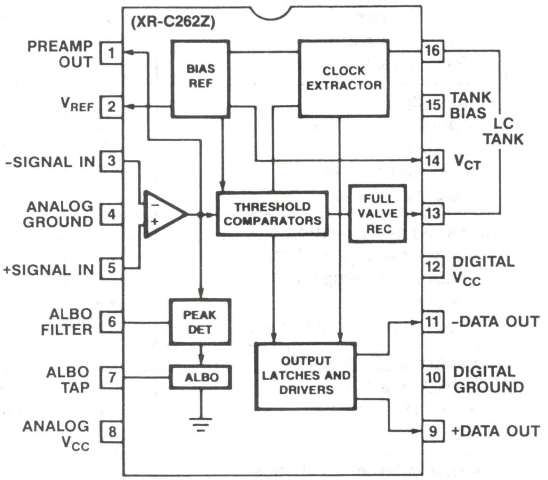
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Supply Voltage	–0.5 to +10V
Input Voltage (Except Pin 6, 7)	–0.5 to +7V
Input Voltage (Pin 6, 7)	–0.5 to +0.5V
Data Output Voltage (Pin 9, 11)	+20V
Voltage Surge (Pin 3, 5, 9, 11) (10 msec only)	50V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262Z	Ceramic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-C262Z contains all the active functions required to build one side of a T1 or 2 MBPS PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 MBPS. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36dB at 772kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier Automatic Line Build Out (ALBO), clock and data threshold detector circuits contained within the XR-C262Z. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO ports and its associated ALBO network.

Incoming pulse stream is full Wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by Pulsing a tank circuit tuned to 1.544MHz.

Data is sampled and stored in the output data latches. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 6.8V, T_A = –40°C to +85°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Current					
Digital Current	6	10	13	mA	Measured at Pin 12
Analog Current	1.5	3.5	5	mA	Measured at Pin 8
Total Current		13	15	mA	
Preamplifier					
Input Offset Voltage	–15		+15	mV	Measured between Pins 3 & 5
Open Loop Gain	58	69	76	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.8	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			4.0	V	Measured at Pin 13
Clock Bias	3.8	4		V	Measured at Pin 15
Clock Source Input Current		0.5	4	µA	Measured at Pin 16
Comparator Thresholds					
ALBO Threshold	0.75	0.9	1.1	V	Measured at Pin 1 relative to Pin 14
Clock Threshold	0.323	0.4	0.517	V	
Data Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.0	5.45	5.65	V	Measured at Pin 2
Divider Center Tap	2.5	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	3	mA	Drive Current available at Pin 6
Output Driver Section					Measured at Pins 9 & 11
Output High Swing	5.9	6.8		V	R_L = 400Ω
Output Low Swing	0.5	0.7	1.0	V	I_L = 15mA
Leakage Current			100	µA	Measured with output in off state
Output Pulse Width	298	324	350	nsec	
Output Rise Time			80	nsec	
Output Fall Time			80	nsec	
Pulse Width Unbalance			15	nsec	

Low-Voltage PCM Repeater

GENERAL DESCRIPTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rate on T1-type PCM lines. It is packaged in a hermetic 16-Pin CERDIP package and is designed to operate over a temperature range of –40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system, including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltage (6.3 volts and 4.3 volts) with a supply current of less than 13mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance, along with significant savings in power consumption and system cost.

The XR-C277-5F is an improved version of XR-C277 with an internal feedback that improved the phase gain margin which enables the system to be more stable and less sensitive to PC board layouts.

Other versions of the XR-C277-5F are XR-C277-F and XR-C277-FL. XR-C277-F is an AC tested device of XR-C277-5F at 2 Mbit while XR-C277-FL Is the equivalent at 1.544 MBPS.

FEATURES

Contains all the Active Components of a PCM Repeater
Low-Voltage Operation (6.3 volts)
Low-Power Dissipation (13mA)
On-Chip ALBO Port
High-Current Output Drivers
Increased Reliability over Discrete Designs
2 Megabit Operation Capability
Pin-Compatible with XR-C240

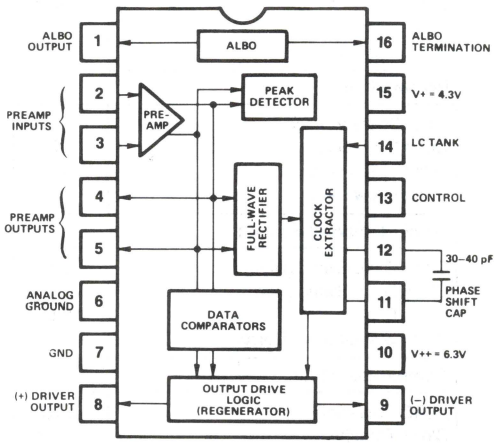
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage	–0.5 to +10V
Input Voltage (Except Pin 1, 16)	–0.5 to +7V
Input Voltage (Pin 1, 16)	–0.5 to +0.5V
Data Output Voltage (Pin 8, 9)	20V
Voltage Surge (Pin 2, 3, 8, 9) (10 msec only)	50V

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C277	Ceramic	–40°C to +85°C
XR-C277-5F	Ceramic	–40°C to +85°C
XR-C277-F	Ceramic	–40°C to +85°C
XR-C277-FL	Ceramic	–40°C to +85°C

SYSTEM DESCRIPTION

The XR-C277 contains all the active circuits required to build one side of a T1 or 2 MBPS PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 MBPS. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36dB at 772kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6} the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier Automatic Line Build Out (ALBO), clock and data threshold detector circuits contained within the XR-C277. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO port and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544MHz. Either injection locking or pulsed tank type clock extraction are possible with the XR-C277. By grounding Pin 13, the circuit works in the injection lock mode. Floating (open) Pin 13 switches the XR-C277 to a pulse tank mode. The oscillator's sinusoidal waveform is amplified and phase shifted by 90 degrees with the help of a capacitor between Pins 11 and 12.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: +25°C, VCC1 = 6.3V ± 5%, VCC2 = 4.4V ± 5%, unless specified otherwise.

PARAMETERS	LIMITS MIN	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
Supply Current					
I_A		3.5		mA	Measured at Pin 10
I_B		7.5		mA	Measured at Pin 15
Total Current	8	11	13	mA	$(I_A + I_B)$
Preamplifier					
Input Offset Voltage		1.5	15	mV	Measured at Pins 2 and 3
Input Bias Current		0.3	4	µA	Measured at Pins 2 and 3
Voltage Gain	44	48	51	dB	Single-ended Gain
Preamp Output Swing					Measured at Pins 4 and 5
High Swing	3.45	3.6	3.75	V	Maximum Voltage Swing
Low Swing	1.25	1.4	1.55	V	Minimum Voltage Swing
Output DC Level	2.47	2.55	2.72	V	
ALBO Section					
ALBO "Off" Voltage		10	75	mV	Measured from Pin 1 and 16 to Ground
ALBO "On" Voltage	0.6	0.87	1.1	V	Measured at Pin 1
ALBO "On Voltage	1.2	1.5	2.1	V	Measured at Pin 16
ALBO Threshold	1.35	1.50	1.65	V	Measured Differentially Across Pins 4 and 5
Differential Threshold	–75		+75	mV	Threshold Difference for Polarity Reversal at Pins 4 and 5
ALBO "On" Impedance		5	10	Ω	Measured at Pin 1
ALBO "Off" Impedance	20	50		kΩ	Measured at Pin 1
Comparator Thresholds					
Clock Threshold	68	73	78	%	% of ALBO Threshold
Data Threshold	47	50	53	%	% of ALBO Threshold
Clock Extractor					
Oscillator Current	10	14	20	µA	
Tank Drive Impedance		50		kΩ	
Recommended OSC. Q	100				
$I_{injection}/I_{OSC}$	6.0	7	7.5		
Output Driver					
Low Output Voltage	0.65	0.75	0.95	V	Measured at Pins 8 and 9 I_L = 15mA
Output "Off" Current		5	100	µA	V_{out} = 20V
Output Pulse					
Max. Pulse Width Error			±30	nsec	
Rise Time			80	nsec	
Full Time			80	nsec	

T1 Repeater Equalization Hybrid Module

GENERAL DESCRIPTION

The TM-044H is a passive equalizer module designed for use in conjunction with the XR-C277 repeater/receiver family. The TM-044H provides a complete solution for T1 PCM line repeater or line termination units. Using hybrid technology, the TM-044H replaces 17 precision external components normally required for T1 line equalization (up to 36 dB of cable loss), with automatic line build out (ALBO) and filter network. This simple front stage network provides space saving, enhanced performance, increased reliability and reduction in manufacturing costs.

FEATURES

Line Equalization Optimized to 2.048 MBPS
Complete ALBO Circuitry
Smoothing ALBO Filter Network
Fixed Gain and Compensation Network
Improved Crosstalk and Noise Through Simplified Layout

APPLICATIONS

T1 PCM Line Repeaters and Receivers
CPI
DMI
T1 Test and Maintenance Equipment

ABSOLUTE MAXIMUM RATINGS

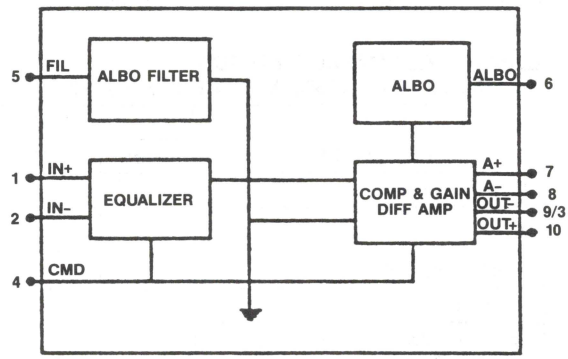
Storage Temperature Range	–55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
TM-044H	Ceramic Hybrid	–40°C to +85°C

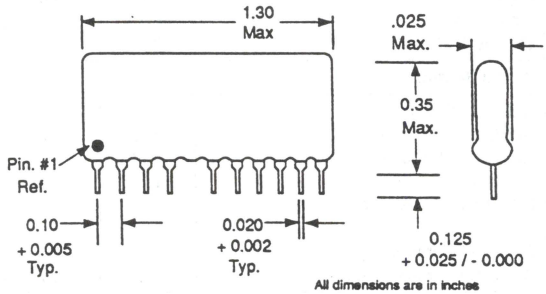
PIN ASSIGNMENT

BLOCK DIAGRAM



SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF TM-044H

DIMENSIONS



All dimensions are in inches

SYSTEM DESCRIPTION

The equalizer module includes all the front end circuitry necessary to equalize the incoming bipolar signals, which are attenuated and distorted due to the transmission medium. It is the function of the equalizer when working with the preamplifier of the repeater to provide the necessary amount of gain and phase equalization, so that the attenuated incoming data can be faithfully extracted and regenerated. In addition, the network band limits the input signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable bundle.

The ALBO Network is providing an Automatic-Gain-Control for the preamplifier in the feedback loop, such that all input signals applied to the preamplifier will appear to be transmitted from the same cable length, which is usually set at 6,000 ft. The TM-044H also includes our ALBO filter that determines the ALBO time constant for optimum performance.

Other circuits included in the module is a preamplifier gain adjustment network and a simple high pass filter that further reduces any noise on the signals before they are applied to the input of the repeater. The preamplifier gain is set at around 40dB and this enables the preamplifier to recover signals which have been attenuated more than 36dB.

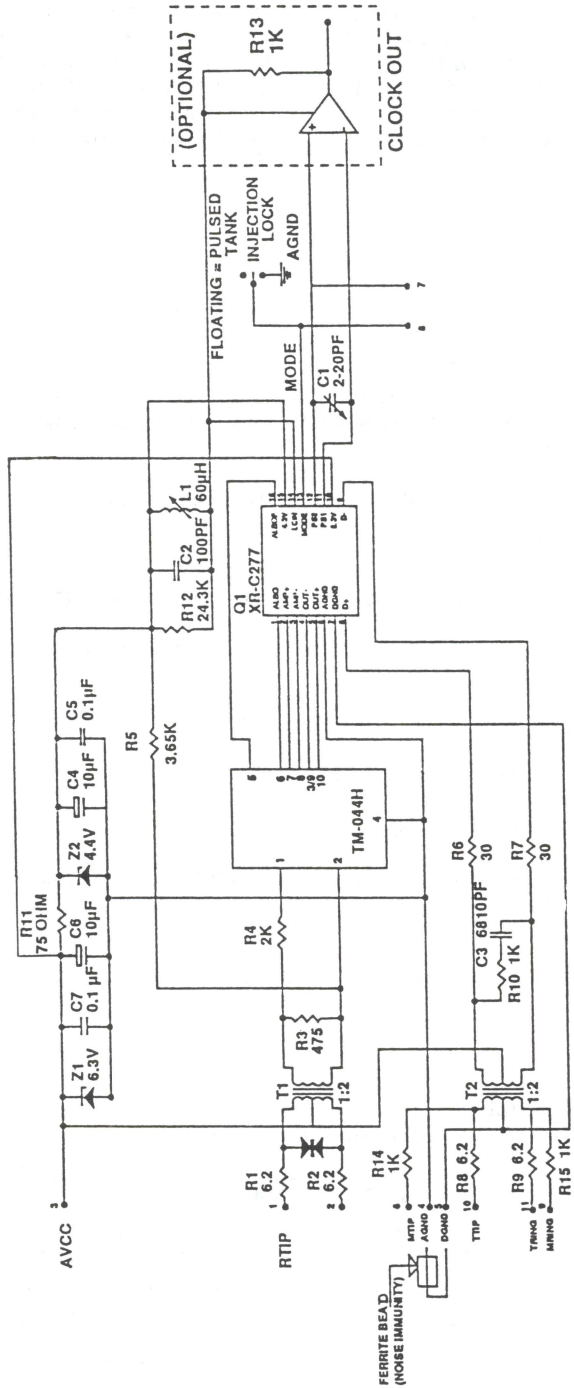
PIN DESCRIPTION

Pins	Name	Description
1-2		Network Input Pins. These two pins connect directly to the secondary side of the isolation transformer. A line termination resistor to mini mize reflections and possibly a trimming resistor may be required to maximize performance.
3		This Output pin is connected directly to the negative pre- amplifier output. (XR-C277 pin 4).
4		Ground. (XR-C277 pin 6).
5		Automatic Line Build Out (ALBO) smoothing filter input pin. (XR-C277 pin 16).
6		This input is part at the ALBO feedback network and connect directly to the ALBO output port. (XR-C277 pin 1).
7		Preamplifier negative input pin. (XR-C277 pin 2).
8		Preamplifier positive input pin. (XR-C277 pin 3).
9		Same as pin 3. (XR-C277 pin 4).
10		This pin connects to the pre-amplifier negative output pin and determines the preamplifier gain. (XR-C277 pin 5).

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	UNIT	MIN	TYP	MAX	CONDITIONS
f-in	Input Frequency	MHz		2.048		
Zin	Input Impedance	kΩ	3			
t-ALBO	ALBO Time Constant	ns		20		
f-ALBO	ALBO Pole	kHz		60		


(OPTIONAL)
R13
1K
CLOCK OUT
FLOATING = PULSED TANK
INJECTION LOCK
AGND
MODE
C1
2-20PF
L1
60µH
C2
100PF
R12
24.3K
Q1
XR-C277
R5
3.65K
C5
0.1µF
C4
10µF
Z2
4.4V
R11
75 OHM
C6
10µF
C7
0.1 µF
Z1
6.3V
TM-044H
R4
2K
R3
475
T1
1:2
R1
6.2
R2
6.2
R14
1K
R6
30
R7
30
C3
6810PF
R10
1K
T2
1:2
R8
6.2
R9
6.2
R15
1K
AVCC
RTIP
FERRITE BEAD
(NOISE IMMUNITY)

Triple ALBO PCM Repeater

GENERAL DESCRIPTION

The XR-T5600/T5620 is a bipolar monolithic repeater IC designed for PCM carrier systems operating at 1.544 MBPS (T1), 2 MBPS, or 2.37 MBPS (T148C). it provides all of the active circuits required for one side of a PCM repeater.

FEATURES

Single 5.1V Power Supply
Less than 10ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports
2 MBPS Capability

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
European 2 MBPS PCM Repeater
T1C PCM Repeater (requires external preamplifier)

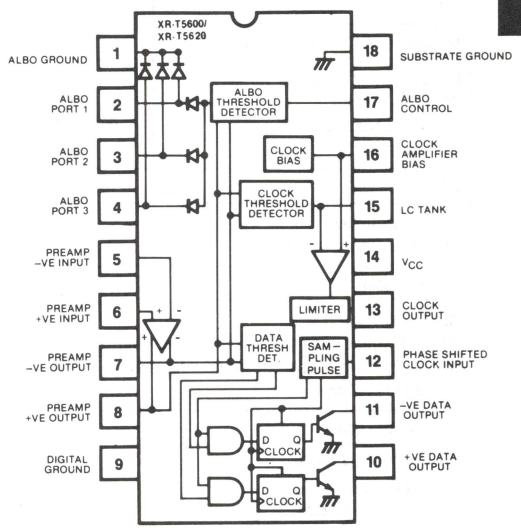
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply voltage	–0.5 to +10V
Supply Voltage Surge (10ms)	+25V
Input Voltage (except Pin 2, 3, 4, 17)	–0.5 to 7V
Input Voltage (Pin 2, 3, 4, 17)	–0.5 to +0.5V
Data Output Voltage (Pin 10, 11)	20V
Voltage Surge (Pin 5, 6, 10, 11) (10 msec only)	50V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5600	Plastic	–40°C to 85°C
XR-T5620	Plastic or Ceramic	–40°C to 85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-T5600/T5620 performs most of the functions required for one side of a PCM repeater operating at 2 Mbit/s or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build Out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into the external tank coil at Pin 15. The sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488ns) in the latches. They appear as half-width output pulses at Pins 10 and 11.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5.1V \pm 5\%$, unless specified otherwise (see Figure 1).

PARAMETERS	PINS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Current	14		22	30	mA	
Data Output Leakage Current	10, 11		0	100	µA	$V_{pull\text{-}up} = 15V$, $V_{CC} = 5.35V$
ALBO Port Off Voltage	2, 3, 4		0	0.1	V	
Amplifier Pin Voltage	5, 6, 7, 8	2.4	2.9	3.4	V	
Dynamic Characteristics Amplifier						
Output Offset Voltage		–50	0	50	mV	$R_S = 8.2k\Omega$
AC Gain @ 1MHz		47	50	53	dB	
Input Impedance		20			kΩ	
Output Impedance				200	Ω	
ALBO						
ALBO Off Impedance		20		25	kΩ	
ALBO On Impedance				25	Ω	
Thresholds						
ALBO Threshold		1.4	1.5	1.6	V	
Clock Threshold as % of ALBO Threshold		68		80	%	
DATA Threshold as % of ALBO Threshold		42		49	%	
Clock Drive Current		0.7		1.4	mA	At $V_O = V_{ALBO}$ Threshold
Output Stages						$R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$
Output Pulse Rise Time				40	ns	
Output Pulse Fall Time				40	ns	
Output Pulse Width		224	244	264	ns	
Output Pulse Width Differential		–10		+10	ns	
Buffer Gate Voltage (Low)		0.65		0.95	V	
Buffer Gate Voltage Differential		–0.15		0.15	V	

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise stated, all characteristics shall apply over the operating temperature range of –40°C to +85°C with V_{CC} = 5.1V ± 5%, all voltages referred to ground = 0V.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
General (Ref. Figure 2)							
I_S	Supply Current	14		22	30	mA	
I_{LD}	Data Output Leakage Current	10, 11		6	100	µA	From V_S (See Note 1)
	Amplifier Pin Voltages	5, 6, 7, 8	2.4	2.9	3.4	V	
	ALBO Ports Off Voltage	2, 3, 4		0	0.1	V	
Note: 1) V_S=15V, V_{CC} = 5.35V							
Amplifier (Ref. Figure 2, Only Pins 1, 9, 10 . . . 18 connected)							
	Input Offset Voltage	5 & 6	–10		+10	mV	R_S = 8.2kΩ (See Note 1)
	Input Bias Current	5 & 6	0		5	µA	R_S = 8.2kΩ (See Note 1)
	Input Offset Current	5 & 6	–1		1	µA	R_S = 8.2kΩ (See Note 1)
	Output Offset Voltage	7 & 8	–50	0	50	mV	R_S = 8.2kΩ (See Note 1)
	Common Mode Rejection Ratio	7 & 8	30			dB	V_{CC} ± 10%
	Output Voltage Swing	7 & 8	2.2			V	
Note: 1) R_S = Source Resistance							
Clock Amplifier (Ref. Figure 2, Disconnect Pin 15 from Pin 16)							
	Input Offset Voltage	15 & 16	0.5		6	mV	R_S = 10kΩ *(See Note 1)*
	Input Bias Current	15 & 16			10	µA	T = 25°C *(See Note 2)*
	Max. Output Voltage	13	0.7			V	*(See Note 3)*
	Min. Output Voltage	13	0.7			V	*(See Note 4*
	Max./Min. Output Voltage Difference	—	0.7		50	mV	*(See Note 5)*

Notes:
1. R_S = Source resistance, Pin 15 positive with respect to Pin 16
2. Pin 15 = Pin 16 = 3.6V
3. Pin 15 = 2.6V, Pin 16 = 3.6V
4. Pin 15 = 4.6V, Pin 16 = 3.6V
5. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
ALBO (Ref. Figure 2)							
	On Current	1	3			mA	V_8–V_7 = ±1.75V
	Drive Current	17	0.4		1.4	mA	V_8–V_7 = ±1.75V
	Resistance Pin 17 to Ground		35	50	70	kΩ	Not Powered

DYNAMIC CHARACTERISTICS

Amplifier (Ref. Figure 3)							
Ao	AC Gain @ 1MHz	5 to 8	47	50	53	dB	
Z_{in}	Input Impedance	5	20			kΩ	(See Note 1)
Z_{out}	Output Impedance	7, 8			200	Ω	(See Note 2)

Notes: 1) At 1MHz, AC ground Pins 7 and 8, disconnect 51Ω resistor, allow for in-circuit R, C
2) At 1MHz, use Figure 2

Clock Amplifier (Ref. Figure 3)							
A_o	AC Gain	15,16 to 13	32			dB	(See Note 1
BW	–3dB Bandwidth	15,16 to 13	10			MHz	(See Note 2)
t_d	Delay	15 to 13	8		12	ns	(See Note 3)
Z_{out}	Output Impedance	13			200	Ω	(See Note 4)

Notes: 1) Remove dc offset, at 2.048MHz, Pin 13 = 1Vpk-pk sine wave
2) Remove dc offset, Pin 13 = 1Vpk-pk sine wave
3) Remove dc offset, Pin 15 = 2Vpk-pk sine wave; delay from Pin 15 negative-going zero crossover to Pin 13 positive edge
4) Remove dc offset, at 2.048MHz

ALBO (Ref. Figure 2)							
	Off Impedance	2,3,4	20			kΩ	(See Note 1)
	Intermediate Impedance Difference	2,3,4			5	%	(See Note 2)
	On Impedance	2,3,4			25	Ω	(See Note 3)
	Transconductance	7/8 to 1			0.03	dB	(See Note 4)

Notes: 1) At 1MHz, allow for in-circuit R, C
2) At 1MHz, V_8–V_7 adjusted for current at Pin 1 = 100μA
3) At 1MHz, V_8–V_7 adjusted for ±1.75V
4) At 1MHz, change in V_8–V_7 for current at Pin 1 = 10μA to 100μA

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
Threshold Voltages (Ref. Figure 3)							
	ALBO Threshold +ve	8-7	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold –ve	7-8	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold Difference	—	–5	0	5	%	(See Note 3)
	Clock Drive on Current (peak) +ve	18		1.0	1.4	mA	(See Note 4)
	Clock Drive on Current (peak) –ve	18		1.0	1.3	mA	(See Note 5)
	Clock Drive on Current Difference	—	–5	0	5	%	(See Note 3)
	Clock Threshold +ve	87	68		80	%	(See Notes 1, 6, 8)
	Clock Threshold –ve	7-8	68		80	%	(See Notes 1, 7, 8)
	Clock Threshold Difference	—	–5	0	5	%	(See Note 3)
	Data Threshold +ve	8-7	44	46	48	%	(See Notes 1, 8, 9, 11)
	Data Threshold –ve	7-8	44	46	48	%	(See Notes 1, 8, 10, 11)
	Data Threshold Difference	—	–3	0	3	%	(See Note 3)

Notes:

1) Pk/pk voltage at Pins 7 and 8 of a 1MHz sine wave derived through amplifier and measured differentially
2) Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3mA
3) Calculation only percentage difference calculated from $\left(\frac{\text{higher value}}{\text{lower value}} - 1\right) \times 100\ \%$
4) V_8–V_7 adjusted to ALBO threshold +ve voltage, ref. Pin 16 = 3.6V
5) V_7–V_8 adjusted to ALBO threshold –ve voltage, ref. Pin 16 = 3.6V
6) V_8–V_7 adjusted to peak current at Pin 18 = 1/2 (clock drive on current peak +ve)
7) V_7–V_8 adjusted to peak current at Pin 18 = 1/2 (clock drive on current peak –ve)
8) Figure taken as a percentage of lower ALBO threshold
9) V_8–V_7 increased until 1MHz PRF on counter at Pin 10
10) V_7–V_8 increased until 1MHz PRF on counter at Pin 11
11) With 2,048MHz 2Vpk-pk sine wave to Pin 15 with 180µH parallel with 36Ω to Pin 16 = 3.6V

Output Stages (Ref. Figure 3. Use 180µ inductor between Pins 15 and 16. Apply 2.048MHz 2Vpk/pk to Pin 15.)							
t_r	Output Pulse Rise Time +ve	10			40	ns	10%–90%
t_r	Output Pulse Rise Time -ve	11			40	ns	10%–90%
t_f	Output Pulse Fall Time +ve	10			40	ns	10%–90%
t_f	Output Pulse Fall Time -ve	11			40	ns	10%–90%
t_w	Output Pulse Width +ve	10	224	244	264	ns	at 50%
	Output Pulse Width -ve	11	224	244	264	ns	at 50%
Δt_w	Output Pulse Width Difference	—	–10		10	ns	
V_{OL}	Buffer Gate Voltage (low) +ve	10	0.65		0.95	V	
V_{OL}	Buffer Gate Voltage (low) -ve	11	0.65		0.95	V	
ΔV_{OL}	Buffer Gate Voltage Difference	—	–0.15		0.15	V	

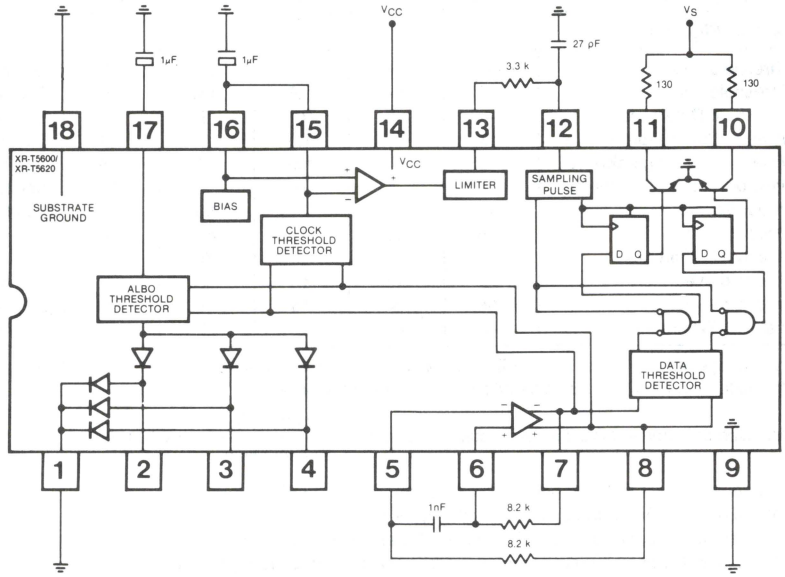


Figure 2. D.C. Parameter Test Circuit

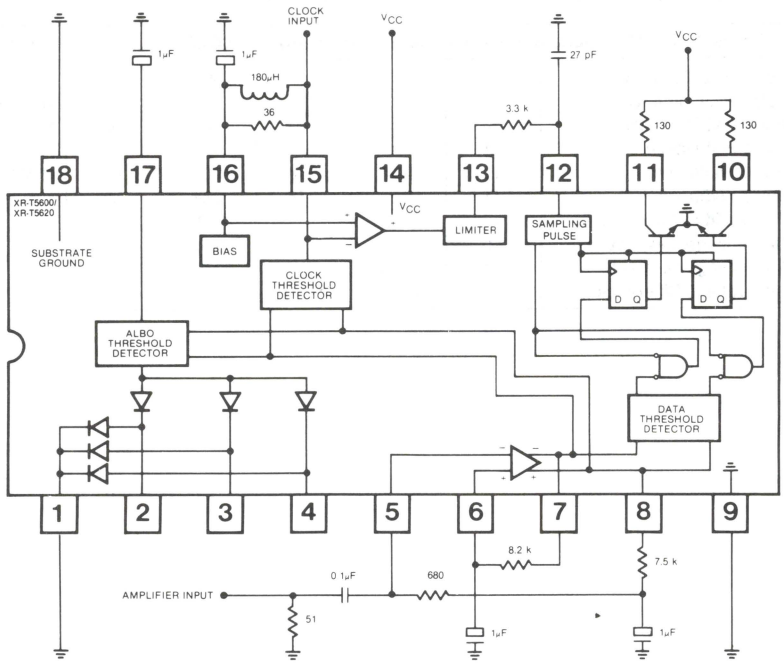


Figure 3. A.C. Parameter Test Circuit

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
Sample Pulse Width (Ref. Figure 4, C_Y = 27pF)							
	Sample Pulse width			10		ns	(See Notes 1 . . . 5)

Notes:
1) The sample pulse width is the period during which the output latches are opened to accept a signal above the data hold at Pin 7 or 8 and cause a half-width output pulse at Pin 11 or 10 respectively.
2) Sample pulse width is specified with a 2.048MHz TTL waveform at clock input (Pin 15) and a 2,400MHz Schottky TTL waveform at amplifier input in the circuit of Figure 4. Figure 7 shows the relevant IC waveforms.
3) Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through output circuit to frequency counter.
4) Sample pulse width = X ns + (0,1 x measured frequency in kHz) ns where X is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5) X to be within the range of 10nx < X < 12ns. THis requires HF layout techniques with the amplifier operated closed loop.

Sample Pulse Generator Input Waveform (Pin 12 — Ref. Figure 4, C_Y = 40pF)							
	Output Pulse Frequency	10, 11	1.024 −100	1.024	1.024 +100	MHz ppm	(See Note 1)

Note:
1) With 2.048MHz ± 100ppm TTLwaveform at clock input. With half of above waveform frequency at amplifier input.

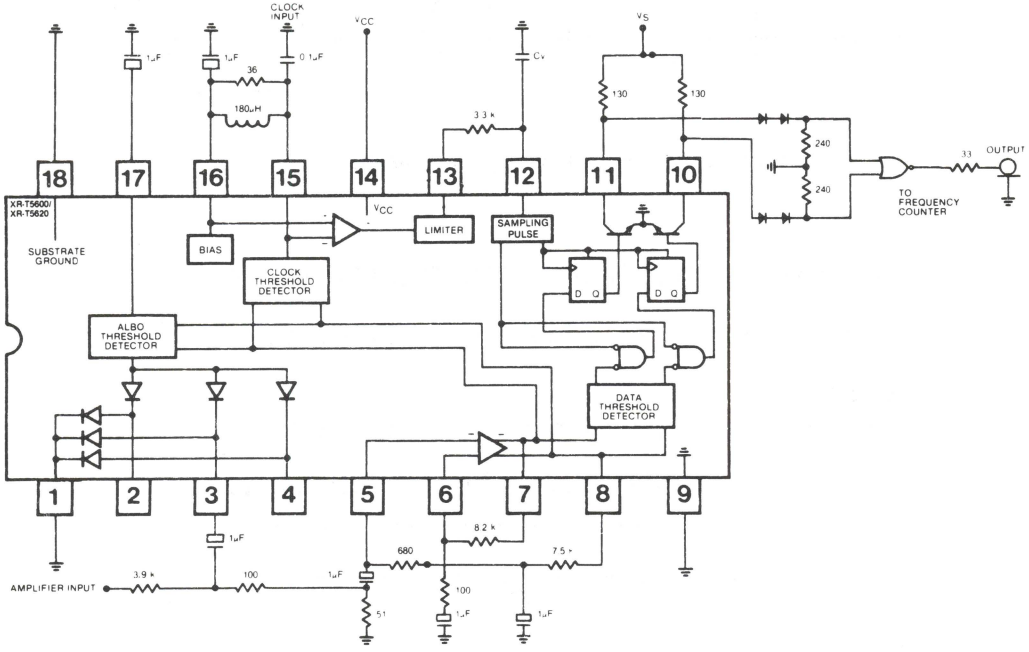


Figure 4. Sampling Pulse Test Circuit

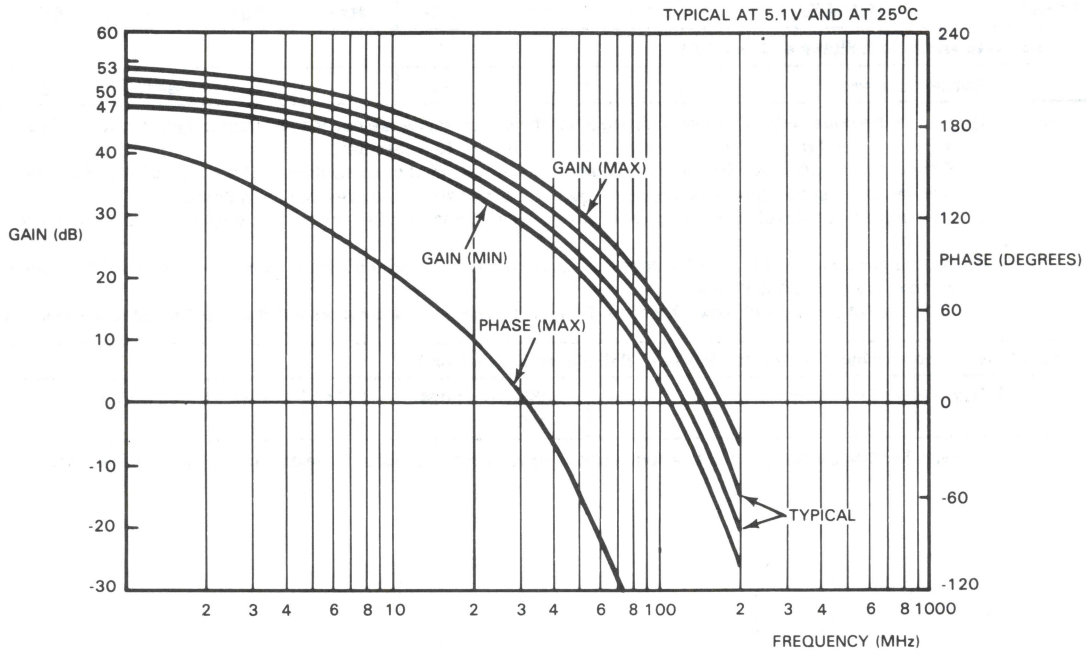


Figure 5. Typical and Limiting Values of Gain and Phase

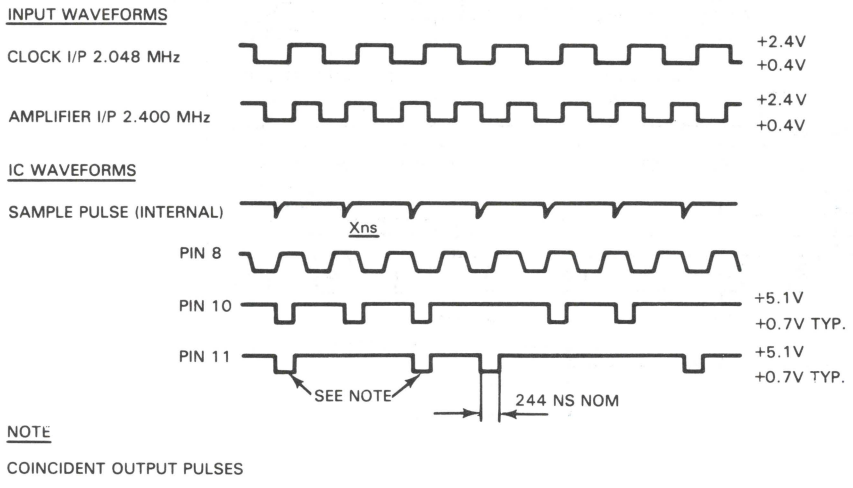
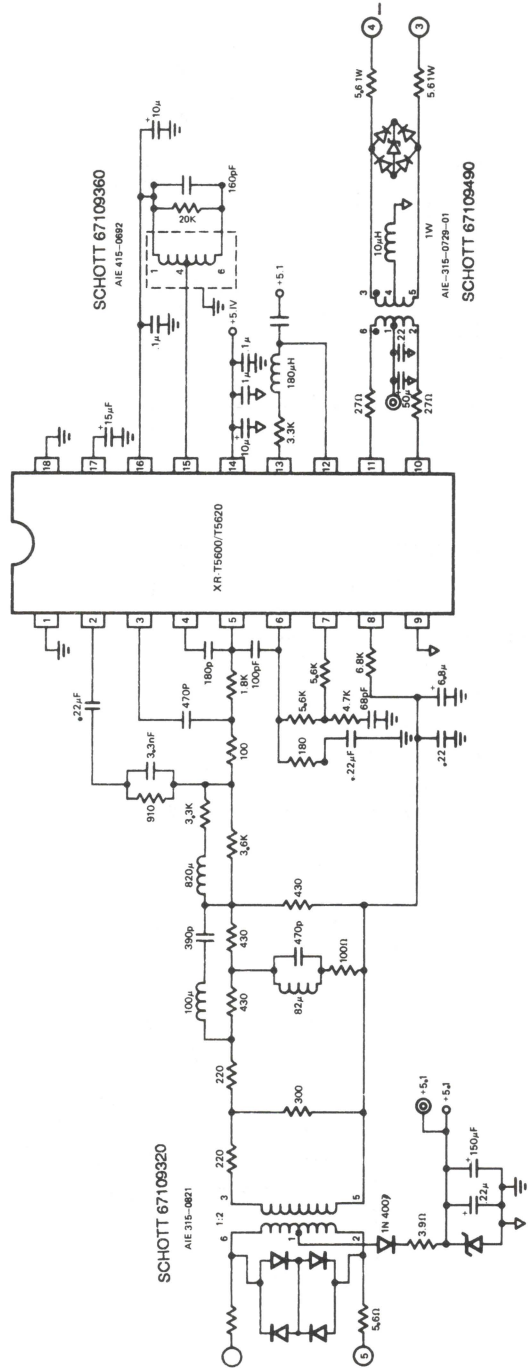
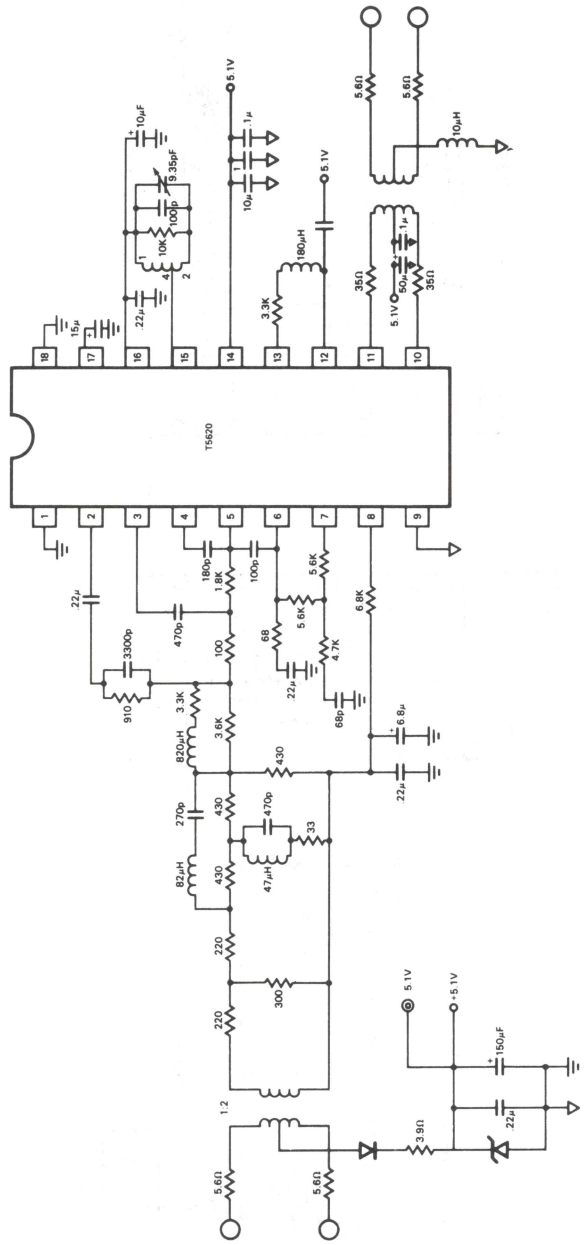


Figure 6. IC Waveforms for Measuring Sampling Pulse Width



T5600/T5620 1.544 MBITS/SEC REPEATER APPLICATION CIRCUIT



T5620 2.048 MBITS/S PCM REPEATER APPLICATION CIRCUIT

PCM Line Repeater

GENERAL DESCRIPTION

The XR-T5720 is a bipolar monolithic repeater IC that provides all the active circuits required for one side of a PCM repeater. The IC is designed for clock extraction by using a crystal filter.

The primary applications of the XR-T5720 are T1 (1.544 C), T148C (2.37MBPS), and European 2MBPS PCM repeater.

A tank circuit clock extraction version of XR-T5720 is available as XR-T5600/T5620.

FEATURES

Crystal Clock Extraction
Single 5.1V Power Supply
Less than 10ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
T1C PCM Repeater (requires external preamplifier)
European 2 MBPS PCM Repeater

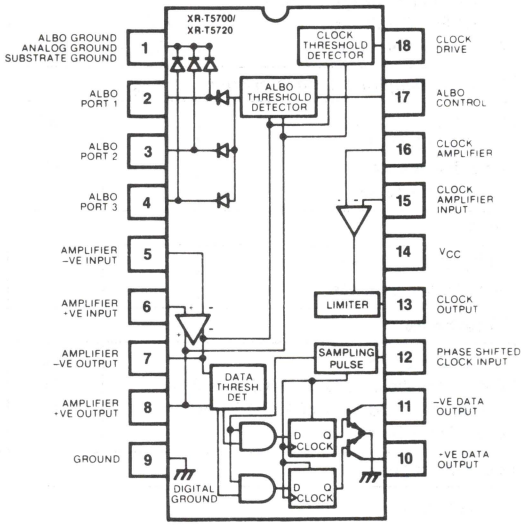
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage	–0.5 to +10V
Supply Voltage Surge (10ms)	+25V
Input Voltage(except Pins 2, 3, 4, 17)	–0.5 to 7V
Input Voltage (Pins 2, 3, 4, 17)	–0.5 to 0.5V
Data Output Voltage (Pins 10, 11)	20V
Voltage Surge (Pins 5, 6, 10, 11) (10 msec only)	50V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5720	Ceramic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-T5720 performs most of the functions required for one side of a PCM repeater operating at 2MBPS or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build Out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into an open collector output (Pin 18). A crystal filter is connected from Pin 18 to clock amplifier input Pins 16 and 15, the sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488ns for 2 MBPS) in the latches. They appear as half-width output pulses at Pins 10 and 11.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5.1V \pm 5\%$, unless specified otherwise (see Figure 1).

PARAMETERS	PINS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
General						
Supply Current	14		22	30	mA	
Data Output Leakage Current	10, 11		0	100	µA	$V_{pull\text{-}up} = 15V$, $V_{CC} = 5.35V$
ALBO Port Off Voltage	2, 3, 4		0	0.1	V	
Amplifier Pin Voltage	5, 6, 7, 8	2.4	2.9	3.4	V	
Dynamic Amplifier Characteristics						
Output Offset Voltage		–50	0	50	mV	$R_S = 8.2k\Omega$
AC Gain @ 1MHz		47	50	53	dB	
Input Impedance		20			kΩ	
Output Impedance				200	Ω	
ALBO						
ALBO Off Impedance		20		25	kΩ	
ALBO On Impedance				25	Ω	
Thresholds						
ALBO Threshold		1.4	1.5	1.6	V	
Clock Threshold as % of ALBO Threshold		68		80	%	
DATA Threshold as % of ALBO Threshold		42		49	%	
Clock Drive Current		0.7		1.4	mA	At $V_O = V_{ALBO}$ Threshold
Output Stages						$R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$
Output Pulse Rise Time				40	ns	
Output Pulse Fall Time				40	ns	
Output Pulse Width		224	244	264	ns	
Output Pulse Width Differential		–10		+10	ns	
Buffer Gate Voltage (Low)		0.65		0.95	V	
Buffer Gate Voltage Differential		–0.15		0.15	V	

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise stated, all characteristics shall apply over the operating temperature range of –40°C to +85°C with V_{CC} = 5.1V ± 5%, all voltages referred to ground = 0V.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
General Characterstics (Ref. Figure 2)							
I_S	Supply Current	14		22	30	mA	
I_{LD}	Data Output Leakage Current	10, 11			100	µA	From V_S (See Note 1)
	Amplifier Pin Voltages	5, 6, 7, 8	2.4	2.9	3.4	V	
	ALBO Ports Off Voltage	2, 3, 4		0	0.1	V	
Amplifier (Ref. Figure 2, Only Pins 1, 9, 10 . . . 18 Connected)							
	Input Offset Voltage	5 & 6	–10		+10	mV	R_S = 8.2kΩ (See Note 1)
	Input Bias Current	5 & 6	0		5	µA	R_S = 8.2kΩ (See Note 1)
	Input Offset Current	5 & 6	–1		1	µA	R_S = 8.2kΩ (See Note 1)
	Output Offset Voltage	7 & 8	–50	0	–50	mV	R_S = 8.2kΩ (See Note 1)
	Common Mode Rejection Ratio	7 & 8	30			dB	V_{CM} ± 0.3V
	Power Supply Rejection Ratio	7 & 8	30			dB	V_{CC} ± 10
	Output Voltage Swing	7 & 8	2.2			V	
Clock Amplifier (Ref. Figure 2, Disconnect Pin 15 from Pin 16)							
	Input Offset Voltage	15 & 16	0.5		6	mV	R_S = kΩ (See Note 1)
	Input Bias Current	15 & 16			10	µA	T = 25°C (See Note 2)
	Max. Output Voltage	13	0.7			V	(See Note 3)
	Min. Output Voltage	13	0.7			V	(See Note 4)
	Max./Min. Output Voltage Difference	—			50	mV	(See Note 5)

Note: 1) V_S = 15V, V_{CC} = 5.35V

Note: 1) R_S = Source Resistance

Notes:
1. R_S = Source resistance, Pin 15 positive with respect to Pin 16
2. Pin 15 = Pin 16 = 3.6V
3. Pin 15 = 2.6V, Pin 16 = 3.6V
4. Pin 15 = 4.6V, Pin 16 = 3.6V
5. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
ALBO (Ref. Figure 2)							
	On Current	1	3			mA	V_8–V_7 = ±1.75V
	Drive Current	17	0.4		1.4	mA	V_8–V_7 = ±1.75V
	Resistance Pin 17 to Ground		35	50	70	kΩ	Not Powered

DYNAMIC CHARACTERISTICS

Amplifier (Ref. Figure 3)							
Ao	AC Gain @ 1MHz	5 to 8	47	50	53	dB	
Z_{in}	Input Impedance	5	20			kΩ	(See Note 1)
Z_{out}	Output Impedance	7, 8			200	Ω	(See Note 2)

Notes: 1) At 2MHz, AC ground Pins 7 and 8, disconnect 51Ω resistor. Allow for in-circuit R, C
2) At 1MHz, use Figure 2

Clock Amplifier (Ref. Figure 3)							
A_o	AC Gain	15,16 to 13	32			dB	(See Note 1
BW	–3dB Bandwidth	15,16 to 13	10			MHz	(See Note 2)
	Delay	15,16 to 13	8		12	ns	(See Note 3)
	Output Impedance	13			200	Ω	(See Note 4)

Notes: 1) Remove dc offset, at 2.048MHz, Pin 13 = 1Vpk-pk sine wave
2) Remove dc offset, Pin 13 = 1Vpk-pk sine wave
3) Remove dc offset, Pin 15 = 2Vpk-pk sine wave. Delay from Pin 15 negative-going zero crossover to Pin 13 positive edge
4) Remove dc offset, at 2.048MHz

ALBO (Ref. Figure 2)							
	Off Impedance	2,3,4	20			kΩ	(See Note 1)
	Intermediate Impedance Difference	2,3,4			5	%	(See Note 2)
	On Impedance	2,3,4			25	Ω	(See Note 3)
	Transconductance	7/8 to 1			0.03	dB	(See Note 4)

Notes: 1) At 1MHz, allow for in-circuit R, C
2) At 1MHz, V_8–V_7 adjusted for current at Pin 1 = 100μA
3) At 1MHz, V_8–V_7 adjusted for ±1.75V
4) At 1MHz, change in V_8–V_7 for current at Pin 1 = 10μA to 100μA

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
Threshold Voltages (Ref. Figure 3)							
	ALBO Threshold +ve	8-7	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold –ve	7-8	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold Difference	—	–5	0	5	%	(See Note 3)
	Clock Drive on Current (Peak) +ve	18	0.65	1.0	1.4	mA	(See Note 4)
	Clock Drive on Current (Peak) –ve	18	0.65	1.0	1.3	mA	(See Note 5)
	Clock Drive on Current Difference	—	–5	0	5	%	(See Note 3)
	Clock Threshold +ve	8-7	68		80	%	(See Notes 1, 6, 8)
	Clock Threshold –ve	7-8	68		80	%	(See Notes 1, 7, 8)
	Clock Threshold Difference	—	–5	0	5	%	(See Note 3)
	Data Threshold +ve	8-7	44	46	48	%	(See Notes 1, 8, 9, 11)
	Data Threshold –ve	7-8	44	46	48	%	(See Notes 1, 8, 10, 11)
	Data Threshold Difference	—	–3	0	3	%	(See Note 3)

Notes:

1) Pk/pk voltage at Pins 7 and 8 of a 1MHz sine wave derived through amplifier and measured differentially
2) Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3mA
3) Calculation only percentage difference calculated from $\left(\frac{\text{higher value}}{\text{lower value}} - 1\right) \times 100\ \%$
4) V_8–V_7 adjusted to ALBO threshold +ve voltage (ref. Pin 16 = 3.6V)
5) V_7–V_8 adjusted to ALBO threshold –ve voltage (ref. Pin 16 = 3.6V)
6) V_8–V_7 adjusted to peak current at Pin 18 = 1/2 (clock drive on current peak +ve)
7) V_7–V_8 adjusted to peak current at Pin 18 = 1/2 (clock drive on current peak –ve)
8) Figure taken as a percentage of lower ALBO threshold
9) V_8–V_7 increased until 1MHz PRF on counter at Pin 10
10) V_7–V_8 increased until 1MHz PRF on counter at Pin 11
11) With 2,048MHz 2Vpk-pk sine wave to Pin 15 with 180µH in parallel with 36Ω to Pin 16 = 3.6V

Output Stages (Ref. Figure 3. Use 180µH inductor between Pins 15 and 16. Apply 2.048MHz 2Vpk/pk to Pin 15.)							
t_r	Output Pulse Rise Time +ve	10			40	ns	10%–90%
t_r	Output Pulse Rise Time –ve	11			40	ns	10%–90%
t_f	Output Pulse Fall Time +ve	10			40	ns	10%–90%
t_f	Output Pulse Fall Time –ve	11			40	ns	10%–90%
t_w	Output Pulse Width +ve	10	224	244	264	ns	at 50%
t_w	Output Pulse Width –ve	11	224	244	264	ns	at 50%
Yt_w	Output Pulse Width Difference	—	–10		10	ns	
V_{OL}	Buffer Gate Voltage (low) +ve	10	0.65		0.95	V	
V_{OL}	Buffer Gate Voltage (low) –ve	11	0.65		0.95	V	
bV_{OL}	Buffer Gate Voltage Difference	—	–0.15		0.15	V	

Note: 1) Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
Sample Pulse Width (Ref. Figure 4, C_Y = 27pF)							
	Sample Pulse width	—		10	20	ns	(See Notes 1 . . . 5)

Notes:
1) The sample pulse width is the period during which the output latches are opened to accept a signal above the data threshold at Pin 7 or 8 and cause a half-width output pulse at Pin 11 or 10 respectively.
2) Sample pulse width is specified with a 2.048MHz TTL waveform at clock input (Pin 15) and a 2,400MHz Schottky TTL waveform at amplifier input in the circuit of Figure 5. Figure 7 shows the relevant IC waveforms.
3) Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through output circuit to frequency counter.
4) Sample pulse width = Xns + (0, 1 x measured frequency in kHz) ns where X is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5) X to be within the range of 10ns < X < 12ns. THis requires HF layout techniques with the amplifier operated closed loop.

Sample Pulse Generator Input Waveform (Pin 12 — Ref. Figure 4, C_Y = 40pF)							
	Output Pulse Frequency	10, 11	1.024 −100	1.024	1.024 +100	MHz ppm	(See Note 1)

Note:
1) Width 2.048MHz ± 100ppm TTLwaveform at clock input with half of above waveform frequency at amplifier input.

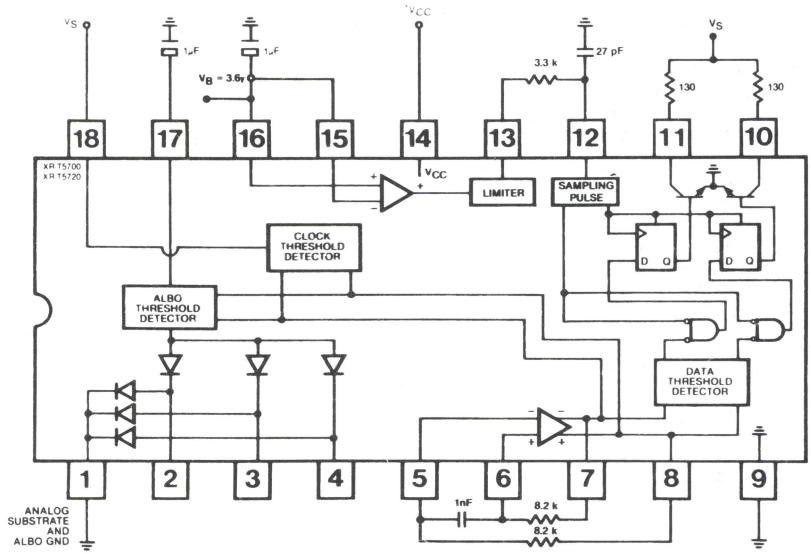


Figure 2. D.C. Parameter Test Circuit

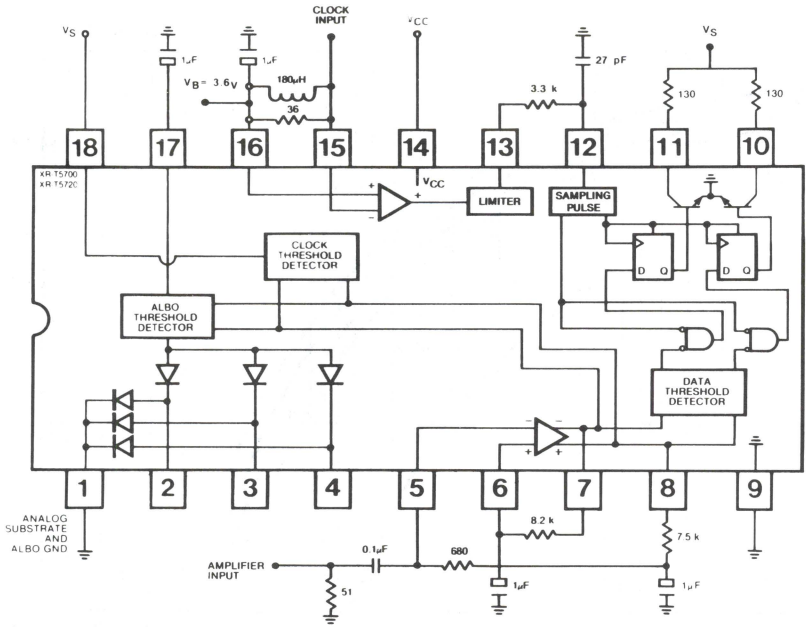


Figure 3. A.C. Parameter Test Circuit

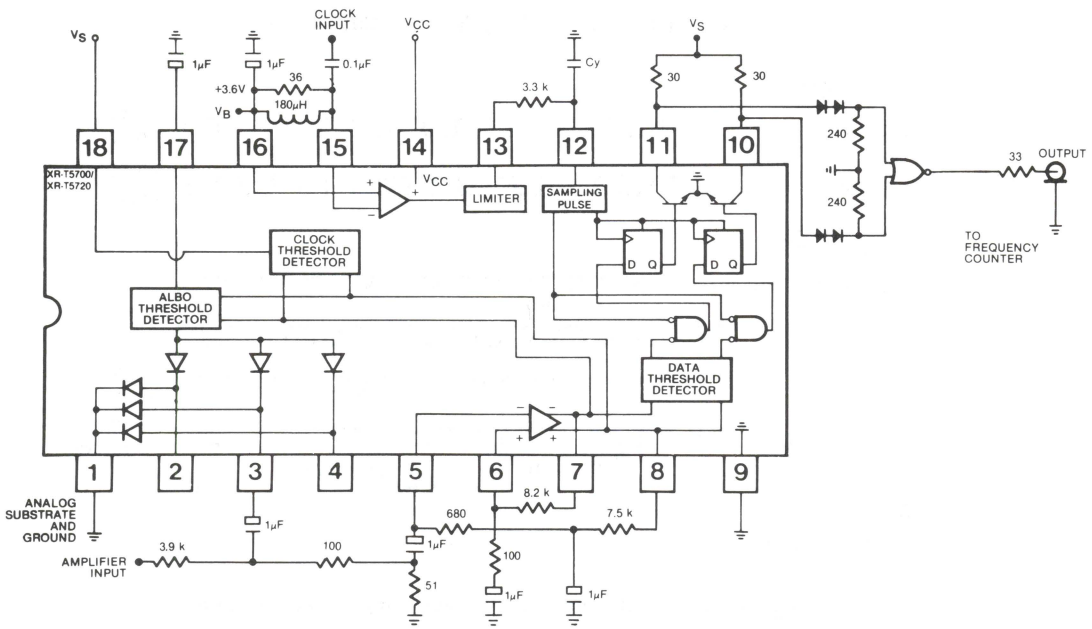


Figure 4. Sampling Pulse Test Circuit

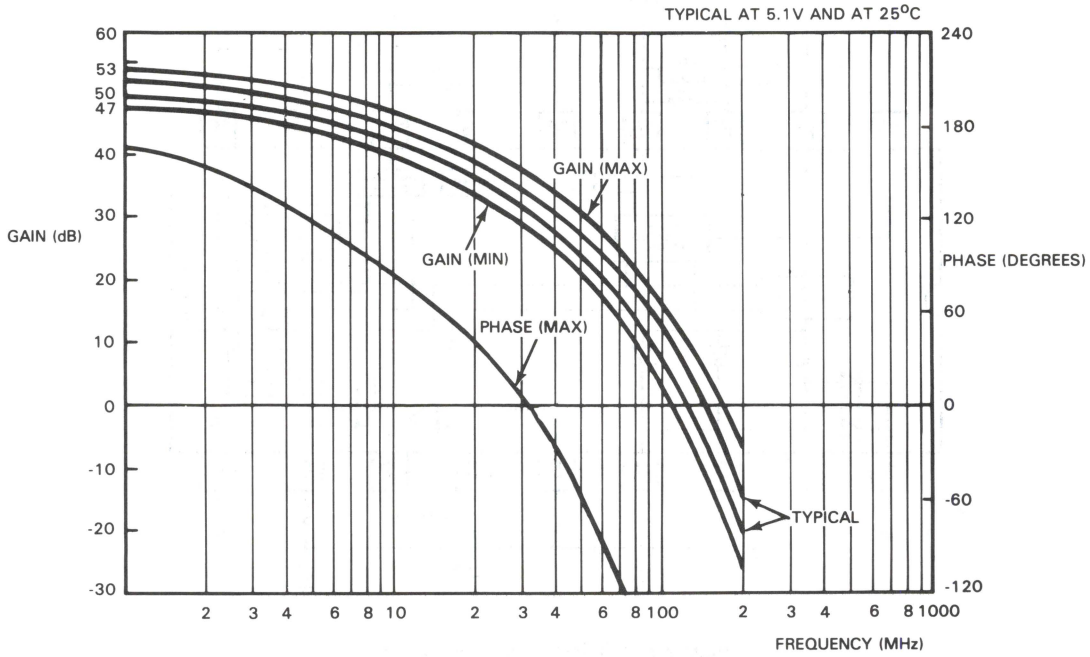


Figure 5. Typical and Limiting Values of Gain and Phase

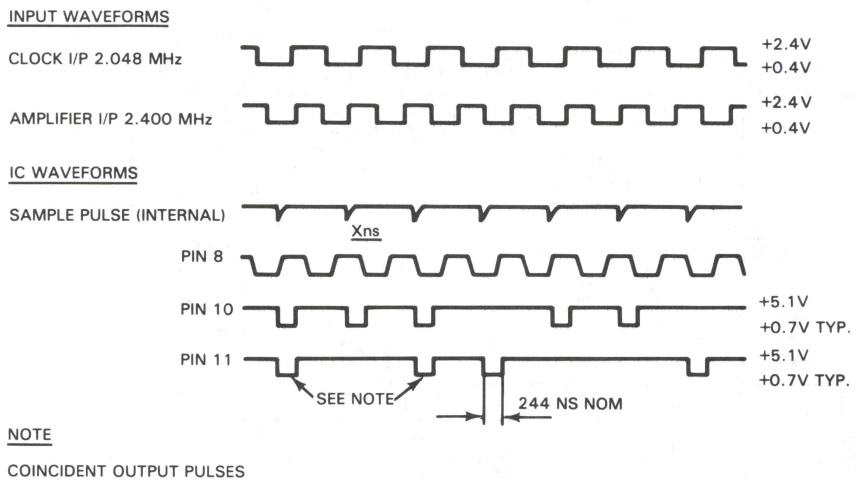
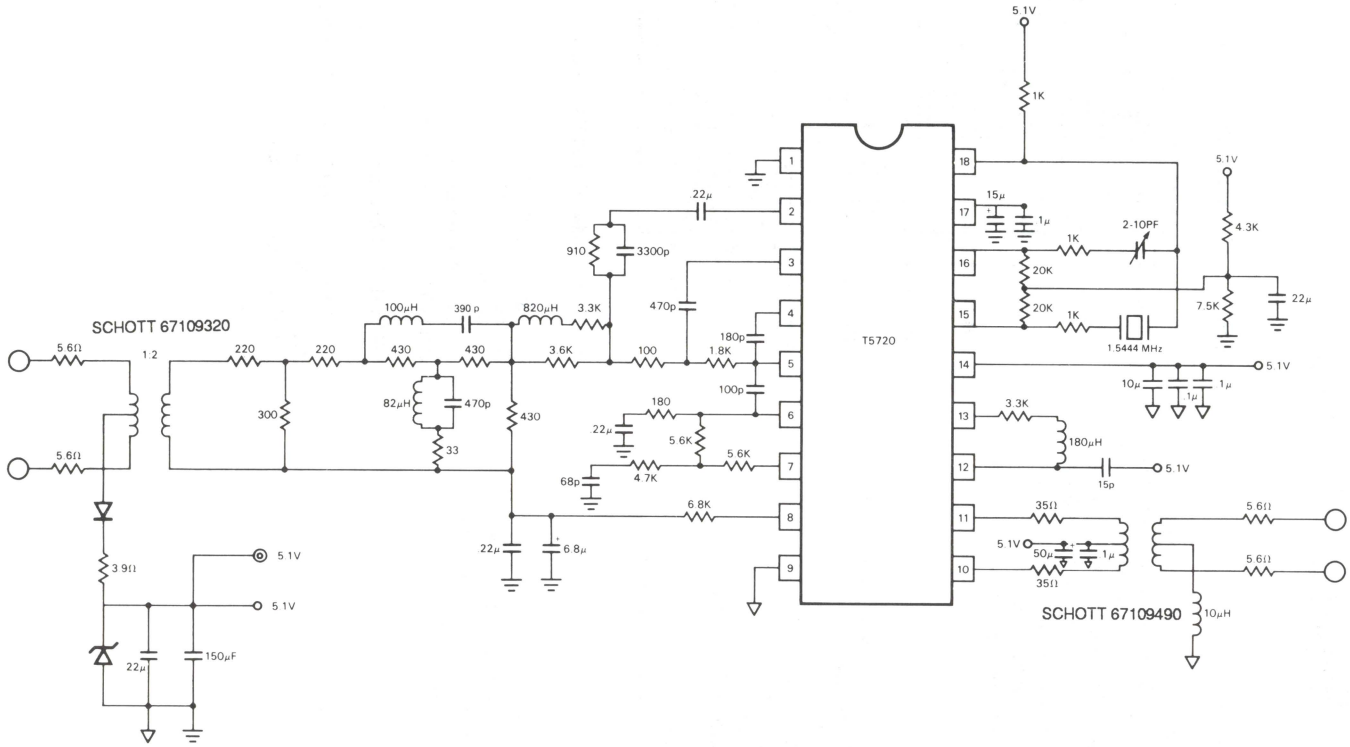


Figure 6. IC Waveforms for Measuring Sampling Pulse Width



T5720 1.544 MBITS/S HIGH Q PCM REPEATER APPLICATION CIRCUIT

Low Power Repeater/Receiver

GENERAL DESCRIPTION

The XR-T56L22 is a very low power monolithic repeater/receiver IC designed for PCM carrier systems operating between 1.544 Mbps and 2.37 Mbps. The IC provides all the active circuitry required to implement one side of a PCM repeater. The XR-T56L22 features on chip adjustable phase shifting, an extracted clock output and an on-board shunt regulator. The very low power consumption of the device makes it ideal for long haul "tandem" repeater applications.

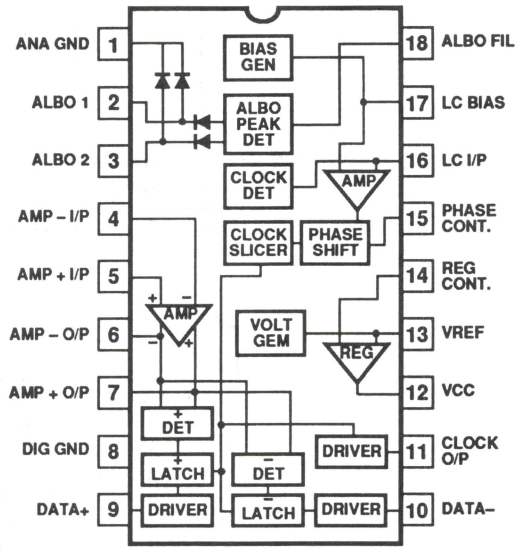
FEATURES

Contains All The Active Components For A Long Haul PCM Repeater Or Receiver
Low Voltage Operation (5.1V)
Low Power Consumption (8.75mA Max)
2 Mbps Operation Capability
Dual Matched ALBO Ports
Internal Adjustable Phase Shift Circuitry
Extracted Clock Output
Internal Shunt Regulator
Temperature Independent Current Biasing

APPLICATIONS

T1 PCM Repeater/Receiver
T148C PCM Repeater/Receiver
European 2.048 Mbps PCM Repeater/Receiver
Digital Multiplexers, CSU's, Switching Equipment
ISDN Compatible Equipment: Fax Machines, Computers etc.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Supply Voltage	–0.5 to 7V
Supply Voltage Surge (10ms)	+25V
Data Output Voltage (Pin 9, 10)	+12V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T56L22IP	Plastic	–40°C to +85°C
XR-T56L22IN	Ceramic	–40°C to +85°C
XR-T56L22ID	SOIC	–40°C to +85°C

PIN DESCRIPTION

Pin #	Name	Description
1	ANA GND	Ground for analog sections of IC and substrate.
2	ALBO 1	ALBO PORT 1 output. Port impedance varies between 25Ω and 20kΩ proportional to input signal level.
3	ALBO 2	ALBO PORT 2 output. Similar to pin 2.
4	AMP – I/P	Inverting input of signal preamp R_{IN} > 20kΩ.
5	AMP + I/P	Non-inverting input of signal preamp. R_{IN} > 20kΩ.
6	AMP – O/P	Inverting output of signal preamp. Rout < 200Ω. DC level typically 3.2V.
7	AMP + O/P	Non-inverting output of signal preamp. Similar to pin 6.
8	DIG GND	Ground for digital portion of IC.
9	DATA+	Positive data driver output (open collector). V_{OL} < 0.95V @ I_{OUT} = 32mA.
10	DATA–	Negative data driver output (open collector). V_{OL} < 0.95V @ I_{OUT} = 32mA.
11	CLOCK O/P	Phase shifted clock output (open collector). Decouple to GND with 0.1μF if not required. With $R_{pull-up}$ = 1K, V_{OL} < 1.1V @ Iout = 4mA.
12	V_{CC}	Input pin of shunt regulator and supply pin for IC. For voltage feed applications the regulator must be disabled and a 5V ± 5% supply connected. For line feed a current of 48-120mA is required. I_{CC} < 8.75mA @ R_{ON}, ALBO = 25Ω typical.
13	V_{REF}	Output voltage of internal reference of shunt regulator. For parallel operation of regulators should be tied to pin 13 of 2nd T56L22 device. V_{REF} approximately $V_{CC}/2$. Decouple to GND with 0.1μF.
14	REG CONT	Input voltage of shunt regulator amp. To inhibit regulator, pin should be tied to ground. For line feed operation decouple to GND with 0.1μF. For parallel operation of regulators tie pin 14 of 2nd T56L22 device. V_{REG} approximately V_{REF}.
15	PHASE CONT	Phase shift adjust input. A resistor to GND from the pin allows adjustment of phase shift from 90° to approximately 0°. R_P typical 1.8K to 1K. V_{phase} typical 340mV.
16	LC I/P	Clock amplifier input. Pulsed with current from clock comparator. Connect LC tank between 16, 17 for clock recovery. I_{ckon} = –110μA typical.
17	LC BIAS	Clock amplifier reference voltage. VLC = 3.6V typical.
18	ALBO FIL	Control pin for ALBO ports. Voltage developed across a capacitor on this pin defines ALBO on impedance V_{ALBO} = 1.5V typical.

SYSTEM DESCRIPTION

With reference to the functional block diagram, the basic operation of the XR-T56L22 may be described as follows: The received bipolar signal, is applied to a linear amplifier and automatic equalizer. These circuits provide the necessary amount of gain and phase equalization to recover the transmitted data, and band limit the signal, to optimize repeater performance for near-end crosstalk produced by other systems operating within the same cable bundle.

The preamplifier output signals which are balanced and of opposite phase, are applied to the clock extraction and pulse regenerator circuits. Here they are rectified and then applied to a high Q resonant circuit which extracts the 1.544/2.048 Mbps frequency component from the received signal. This signal is then sliced and fed to an adjustable phase shift circuit. A second slicer is used to control the time at which the output signals from the preamplifier are sampled by the pulse regenerator circuits. The phase shifted clock signal is made available as an output from the circuit for interface applications. The clock phase adjustment is performed with a single pin using an external resistor. Adjustment of the position of the clock sampling edge by the phase shift circuit allows performance of the pulse regenerator to be optimized. The pulse regenerator performs the sampling and data slicing to regenerate the appropriate output pulse. These pulses are applied to an external output transformer to create the bipolar signal that drives the next section of twisted pair.

ELECTRICAL CHARACTERISTICS

Test Conditions: –40°C to +85°C, V_{CC} = 5.1V ± 5%, unless otherwise specified — refer to test circuit (Fig 6).

PARAMETERS	PIN	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
Supply Voltage	12	4.85		5.35	V	Pin 12,13 to V_{CC}, Note 1
Supply Current	12		7	8.75	mA	
Data Output Leakage Current	9,10			100	µA	$V_{pull\text{-}up}$ = 8V V_{CC} = 5.35V, Note 1
ALBO Port Off Voltage	2,3			0.1	V	
Amplifier Pin Voltage	4,5 6,7	2.7	3.2	3.7	V	
AMPLIFIER						
Input Impedance	4,5	40			KΩ	
Input Offset Voltage	4,5	–10		+10	mV	R_S = 8.2K, Note 1
Input Bias Current	4,5			5	µA	"
Input Offset Current	4,5	–1		+1	µA	"
Output Offset Voltage	6,7	–50		+50	mV	"
Common Mode Rejection Ratio	4,5,6,7	40			dB	
Output Voltage Swing	6,7	1.9			V	
CLOCK AMPLIFIER						
Input Offset Voltage	17,16	0.5		6	mV	R_S = 10K, Note 1
Input Bias Current	17,16			5	µA	Note 2
AC Gain		40			dB	
–3dB Bandwidth		10			MHz	
Delay			35		nS	
ALBO						
ALBO Filter Resistance	18-1	31		57	KΩ	
ALBO Impedance Match	2,3			10	%	
On Current	1	1.3		2.4	mA	
Drive Current	18	0.4		1.4	mA	
Maximum On Impedance	2,3-1			25	Ω	Note 1
Minimum Off Impedance	2,3-1	20			KΩ	"

Note: 1) Internal Regulator disabled.

Note: 1) Source Resistance

Notes: 1) R_S = Source resistance Pin 16 positive with respect to Pin 17
2) Pin 16 = Pin 17 = 3.6V

Note: 1) f_{test} = 1MHz

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = –40°C to +85°C, V_{CC} = 5.1V ± 5% unless otherwise specified — refer to test circuit (Fig 6).

PARAMETERS	PIN	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES						
ALBO Threshold +Ve	7,6	1.4		1.6	V	Notes 1 & 2
ALBO Threshold -Ve	7,6	1.4		1.6	V	Notes 1 & 2
ALBO Threshold Difference		–3		+3	%	Note 3
Clock Drive on Current +Ve		80		140	µA	Note 4
Clock Drive on Current -Ve		80		140	µA	Note 4
Clock Drive Difference		–3		+3	%	Note 3
Clock Threshold +Ve	7,6	69		79	%	Note 5
Clock Threshold -Ve	7,6	69		79	%	Note 5
Clock Threshold Difference		–3		+3	%	Note 3
Data Threshold +Ve	7,6	41		50	%	Note 5
Data Threshold -Ve	7,6	41		50	%	Note 5
Data Threshold Difference		–3		+3	%	Note 3

Notes: 1) Pk/pk voltage at Pins 6 and 7 of a 1MHz sine wave derived through amplifier and measured differentially.

2) Pk/pk voltage at Pins 6 and 7 adjusted for a current increase of 2mA at pin 1.

3) Calculation only: percentage difference = $\left[\frac{\text{higher value}}{\text{lower value}}\right] - 1 \times 100\%$

4) $V_6 - V_7$ adjusted to ALBO threshold voltage (Pin 16 = 3.6V)

5) Figure taken as a percentage of ALBO threshold

DATA OUTPUT STAGES						
Output Pulse Rise Time +Ve (Tr)	9			40	nS	10%-90% Note 1
Output Pulse Rise -Time –Ve (Tr)	10			40	nS	"
Output Pulse Fall Time +Ve (Tf)	9			40	nS	"
Output Pulse Fall Time –Ve (Tf)	10			40	nS	"
Output Pulse Width +Ve (Tw)	9	224		264	nS	at 50%
Output Pulse Width –Ve (Tw)	10	224		264	nS	"
Output Pulse Width Difference (dTw)		–12		+12	nS	"
Output Voltage (low) (V_{OL})	9,10	0.6		0.95	V	Note 1
Output Voltage Difference (V_{OL})	9,10	–0.15		+0.15	V	"

Note: 1) Using a 130Ω pull up resistor between 9, 10 and V_{CC} and 15pF capacitance to GND.

CLOCK OUTPUT STAGE						
Output Pulse Rise Time (Tr)	11			40	nS	Note 1
Output Pulse Fall Time (Tf)	11			40	nS	
Output Pulse Width (Tw)	11	224		264	nS	
Output Voltage Low (V_{OL})	11			1.1	V	

Note: 1) Using a 2K pull up resistor between 11 and Vcc and 15pF capacitance to GND.

SHUNT REGULATOR						
Output Voltage	12	4.85	5.1	5.35	V	Pin 13, 14 floating
Voltage Regulation Over Temp.	12		–0.02		%/°C	"
Load Regulation	12			0.027	%/mA	1mA to 100mA load

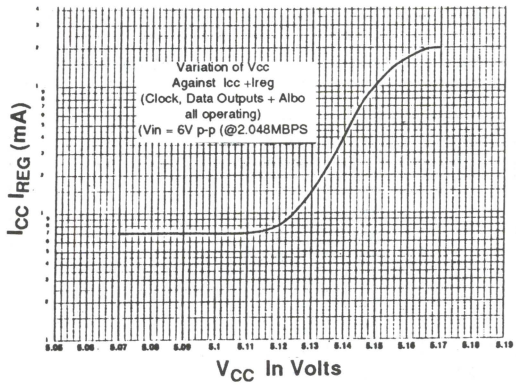


Figure 1. Regulator Output Voltage Versus Current (I_{CC} + I_{REG})

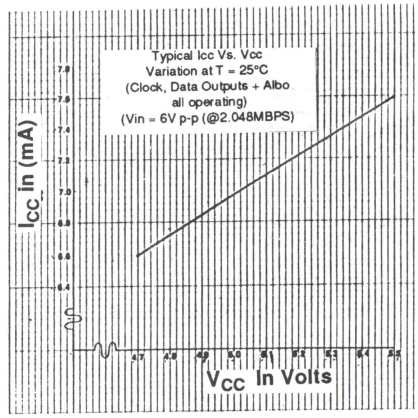


Figure 2. Supply Current Variation with V_{CC} (Regulator Inhibited)

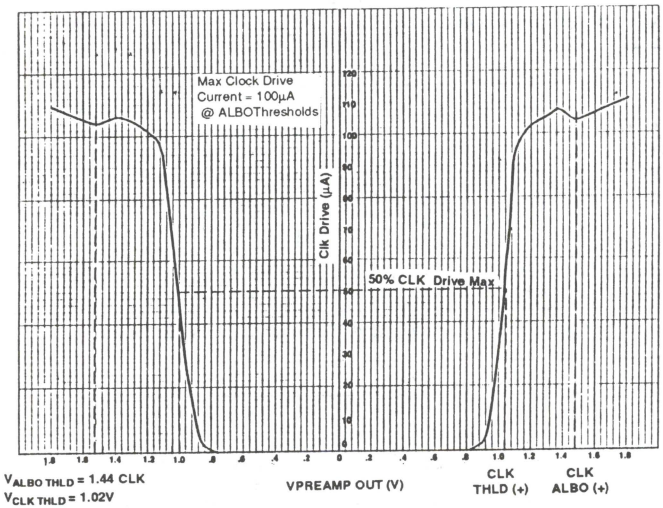


Figure 3. Clock Drive Current Against Preamp Output Voltage

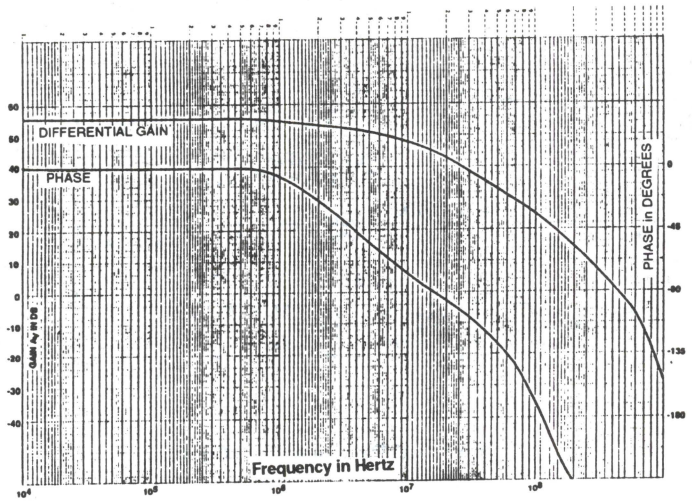


Figure 4. Preamp Gain/Phase Characteristics

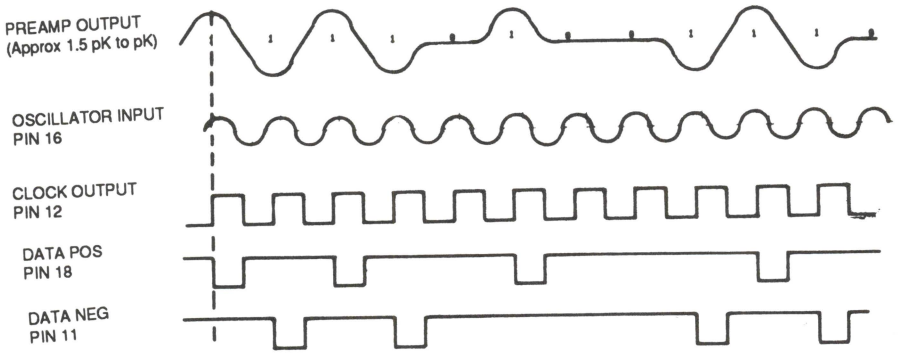


Figure 5. Typical T56L22 Waveforms

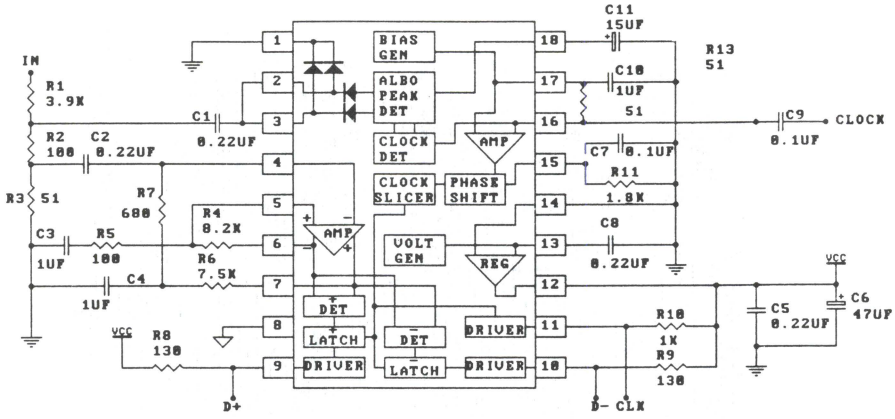
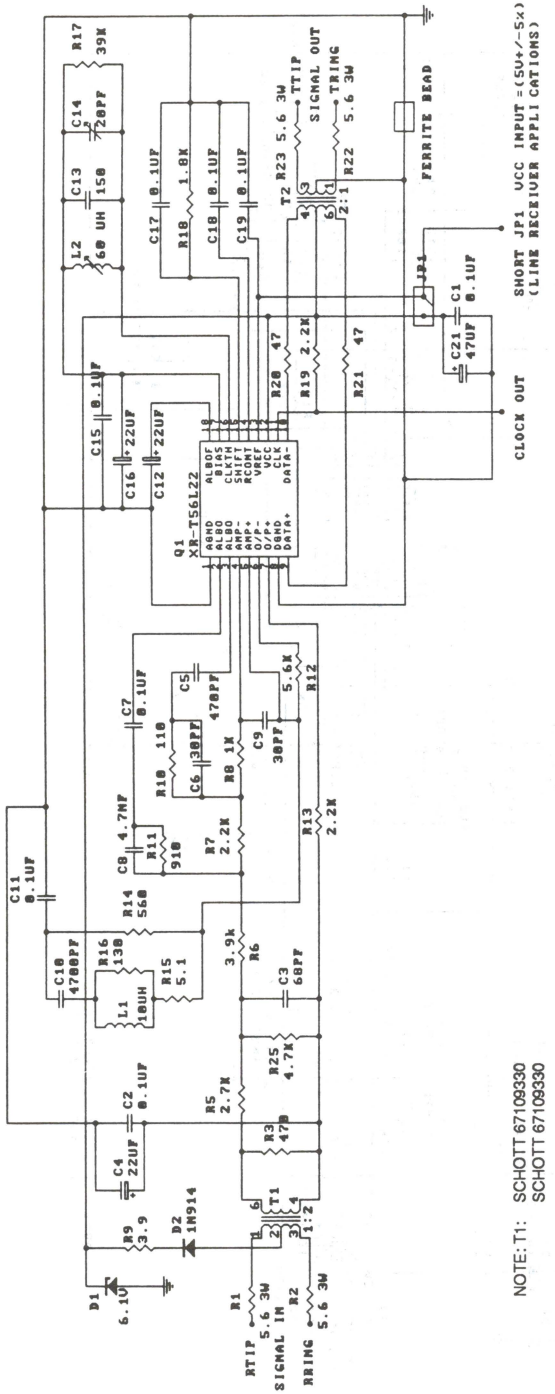
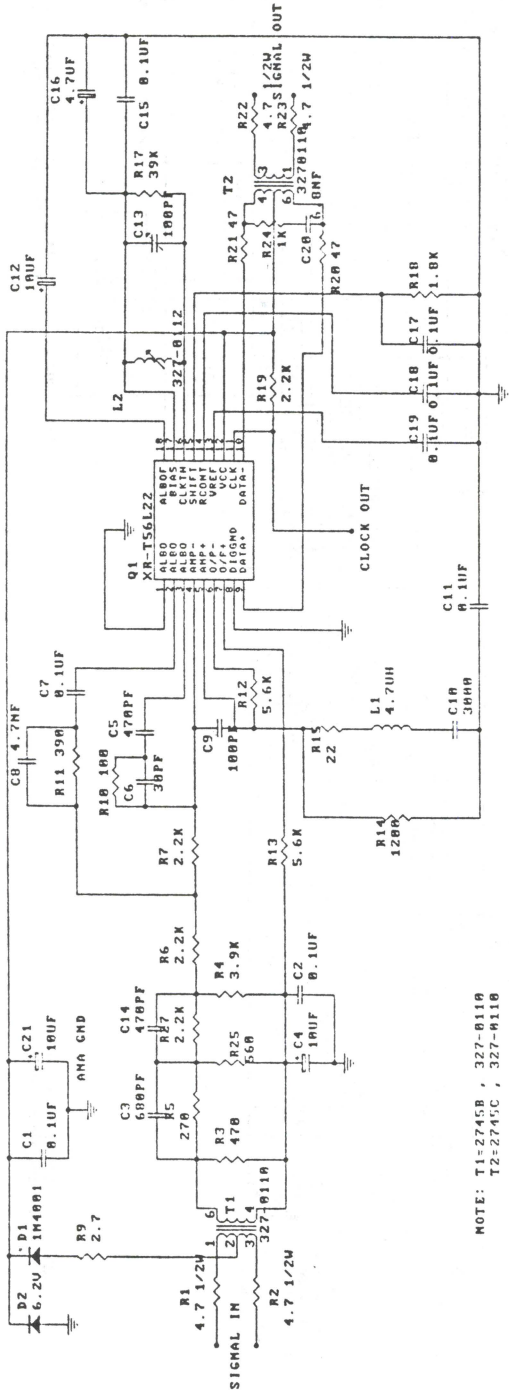


Figure 6. AC Parameter Test Circuit



Typical Application for the XR-T56L22 at 1.544 MBPs.



Typical Application for the XR-T56L22 at 2.048 MBps

PCM Transceiver Chip

GENERAL DESCRIPTION

The XR-T5681 is a PCM transceiver chip. It consists of both transmit and receive circuitry in a CERDIP 18 pin package. The transceiver is designed for short line application (< –10dB) such as in digital multiplexed interfacing and digital PBX environments. The maximum frequency of operation is 3 MBPS so it covers T1, T148C, and Europe's 2.048 MBPS PCM system.

FEATURES

Single +5.0V Supply
Receiver Can Accept Either Balanced or Unbalanced Inputs
TTL Compatible Interface
Transmitter and Receiver in One Package

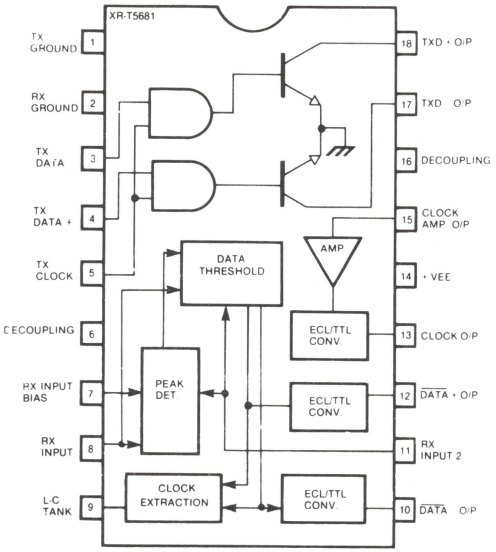
APPLICATIONS

T1, T148C, and 2.048 MBPS PCM Line Interface
CPI
DMI

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20V
Storage Temperature	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5681	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The functions of the circuit terminals are defined in the Functional Block Diagram. At the receive direction, the incoming bipolar signal which has been attentuated and distorted by the cable is applied to the input of the peak detector. The variable threshold voltage produced by the peak detector controls the data comparator for positive and negative rails signal extractions. Timing information is obtained by means of a full wave rectifier and an L-C resonant circuit turned at the appropriate frequency. All data and clock outputs are LSTTL compatible.

At the transmitter, the outputs have two identical non-saturating open collector stages which can drive the output line transformer directly with a maximum current of 40mA. Full width, TTL compatible, positive and negative rail signals at the inputs and a 50% duty cycle TTL clock are needed to form the bipolar line signal at the secondary of the transformer. The output signal conforms to CCITT G.703 recommendation. A circuit diagram connected for 2.048 MBPS line interface application is shown in Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0V, T_A = 0°C to +70°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC Supply	+4.75	+5.0	+5.25	V	
Supply Current		35.0	46.0	mA	T_X Drivers Open
Tank Drive Current	1.5	2.0	2.5	mA	Measured at Pin 9,
Clock O/P/Low Level		0.3	0.8	V	Measured at Pin 13, I_{OL} = 1.0mA
Clock O/P/High Level	3.0	4.3		V	Measured at Pin 13, I_{OH} = 400µA
Data O/P/Low Level		0.4	0.8	V	Measured at Pins 10, 12, I_{OL} = 1.0mA
Data O/P/High Level	3.0	4.5		V	Measured at Pin 10,12, I_{OH} = 400µA
Transmitter O/P/Low Level	0.6		0.95	V	Measured at Pin 13,15, I_{OL} = 40mA
Transmitter O/P/Current Sink			40	mA	Measured at Pin 13,15, V_{OL} = 0.95V
Transmitter O/P/Rise Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to +5.0 =V, C_L = 15 =pF
Transmitter O/P/Fall Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to +5.0V, C_L = 15pF

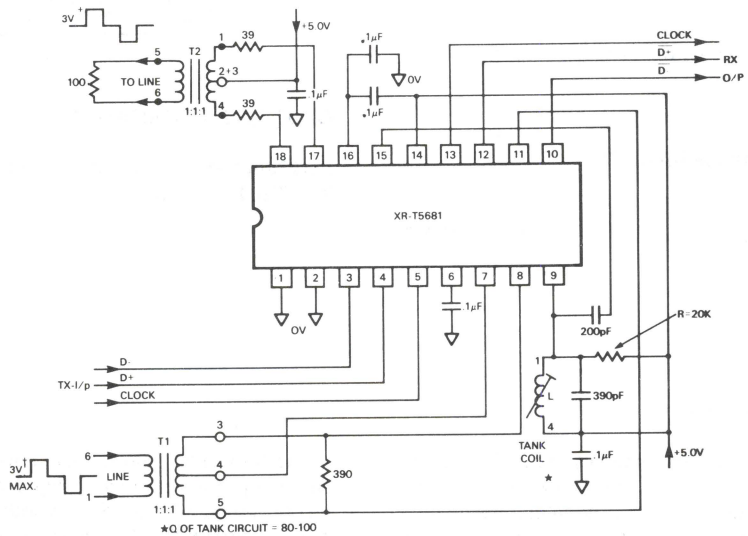


Figure 2. Circuit Connection Diagram for 2.048MBPS operating

PCM Line Interface Chip

GENERAL DESCRIPTION

The XR-T5683 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 8.448 M Bits/s and the signal level to the receiver can be attenuated by –10dB cable loss at half the bit rate. At nominal supply voltage operation the typical current consumption is 40mA.

FEATURES

Single +5.0V Supply
Receiver Input Can Be Either Balanced or Unbalanced
Up to 8.448 M Bits/s Operation in Both T_X and R_X Directions
TTL Compatible Interface

APPLICATIONS

T1, T148C, T2, 2048 & 8448 KBits/s
PCM Line Interface
CPI
DMI

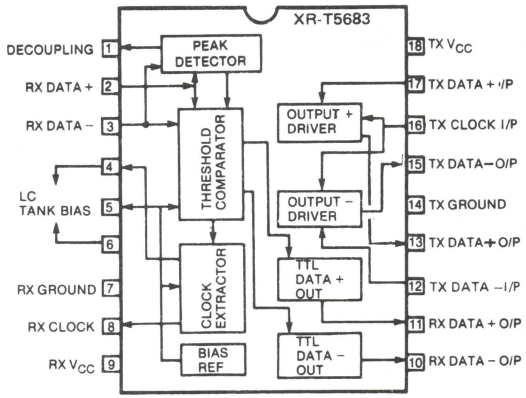
ABSOULTE MAXIMUM RATINGS

Supply Voltage	+20V
Storage Temperature	–65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5683	Ceramic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the threshold comparator and the peak detector. The peak detector generates a DC reference for the threshold comparator for data and clock extraction. A tank circuit tuned to the appropriate frequency is added to the later operation. The clock signal, data (+) data (–) all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 40 mA. With full width data applied to the inputs together with a synchronized clock. The output will generate a bipolar signal when driving a centre-tapped transformer. A typical circuit diagram to XR-T5683 is shown in Figure 1.

DC ELECTRICAL CHARACTERISTICS

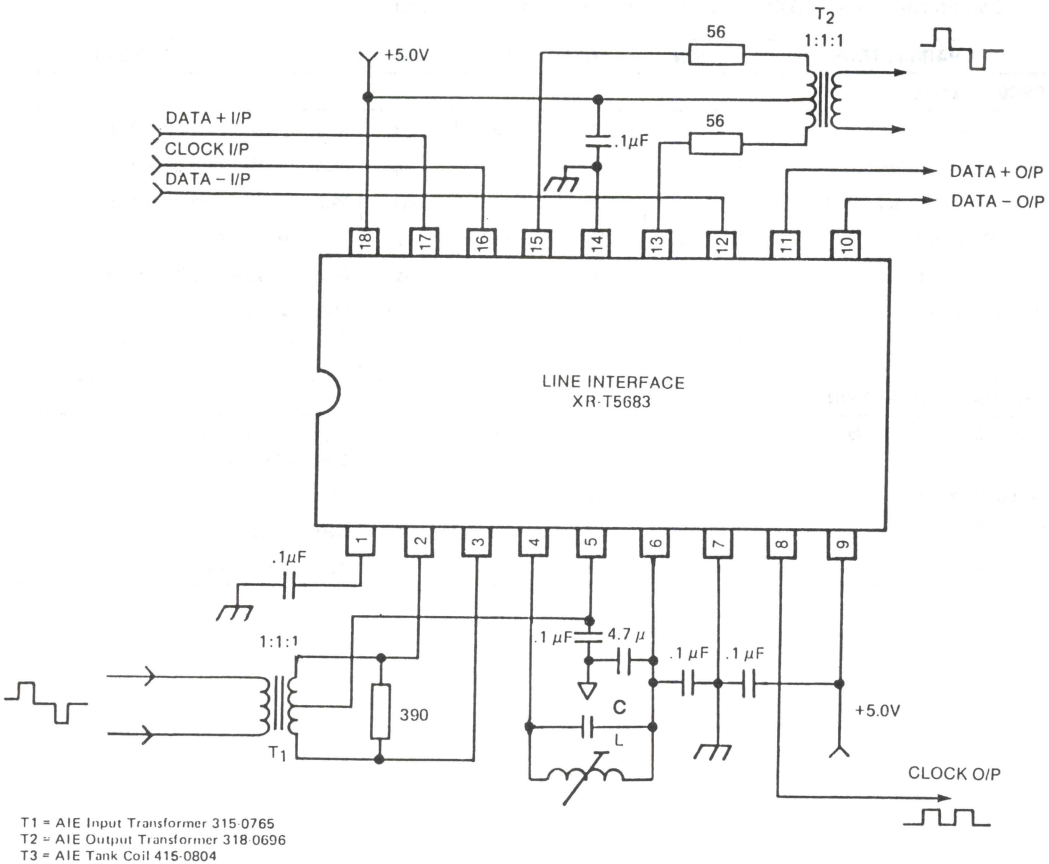
Test Conditions: V_{CC} = 5.0V ± 5%, T_A = 0°–70°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75	5	5.25	V	
Supply Current		40	55	mA	Total Current to Pin 9 & Pin 18 Transmitter Outputs Open
RECEIVER SECTION					
Tank Drive Current	300	500	700	µA	Measured at Pin 4, V_{CC} = 5V
Clock Output Low		0.3	0.6	V	Measured at Pin 8 I_{OL} = 1.6mA
Clock Output High	3.0	3.6		V	Measured at Pin 8
Data Output Low		0.3	0.6	V	Measured at Pin 10 & 11 I_{OL} = 1.6mA
Data Output High	3.0	3.6		V	Measured at Pin 10 & 11 I_{OH} = 400µA
TRANSMITTER SECTION					
Driver Output Low	0.6	0.8	1.0	V	Measured at Pin 13 & 15 I_{OL} = 40mA
Output Leakage Current		0	100	µA	Measured in Off State Output Pull-up to + 20V
Input High Voltage	2.2			V	Measured at Pin 12, 16 & 17 I_{OL} = 40mA, V_{OL} = 1.0V
Input Low Voltage			0.8	V	Measured at Pin 12, 16 & 17
Input Low Current			–1.6	mA	Measured at Pin 12, 16 & 17 Input Low Voltage = 0. 4V
Input High Current			40	µA	Measured at Pin 12, 16 & 17
Output Low Current			40	mA	Measured at Pin 13 & 15 V_{OL}= 1.0V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V, T_A = 25°C, unless otherwise specified.

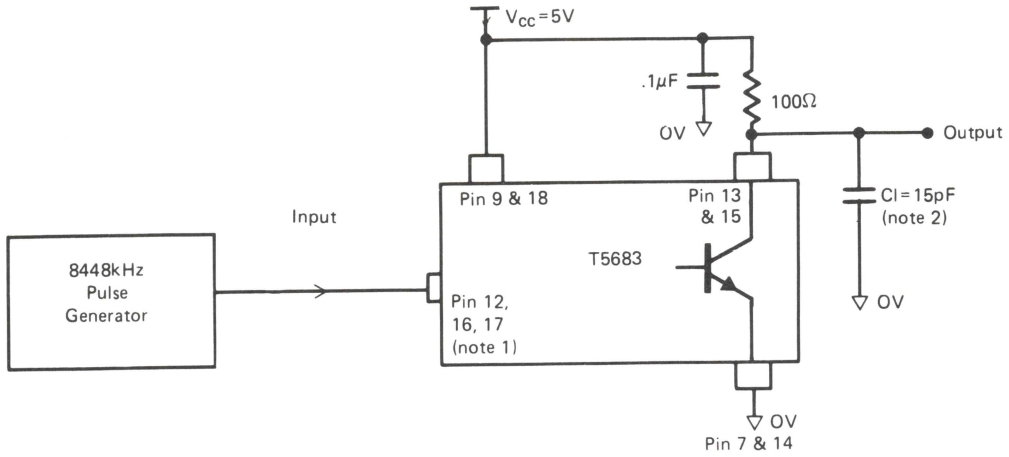
PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
RECEIVER SECTION					
Input Level		6	6.6	Vpp	Measured Between Pin 2 & 3
Loss Input Signal Alarm Level		0.8		Vpp	Measured Between Pin 2 & 3
Input Impedance at 2048KHz		2.5		kΩ	Measured Between Pin 2 & 3
Clock Duty Cycle	35	50	65	%	Measured at Pin 8 at 2.0V
Clock Rise & Fall Time		20		ns	Measured at Pin 8, C_L = 15pF
Data Pulse Width	35	50	75	% of clock period	Measured at Pin 10 & 11 At 1V DC Level, Cable Loss = 0
TRANSMITTER SECTION					
Pulse Width at 8448KHz	53		65	ns	Measured at Pin 13 & 15 See Test Circuit 1
Output Rise Time		12	25	ns	See Test Circuit 1
Output Fall Time		12	25	ns	See Test Circuit 1
Output Pulse Imbalance		2.5		ns	At 50% Output Level



T1 = AIE Input Transformer 315-0765
T2 = AIE Output Transformer 318-0696
L = AIE Tank Coil 415-0804 (1.5 & 2MBPS)
AIE Tank Coil 15-0111 (8MBPS)

Device	1.544 MBPS	2.048 MBPS	8.048MBPS
L	~60μH	~60μH	~5μH
C	175pF	100pF	70pF

Figure 1. Application Circuit for XRT5683



Note 1. Inputs that are not connected to pulse generator will be tied to $+V_{CC}$ via 1K resistor.
Note 2. Cl includes probe and jig capacitance.

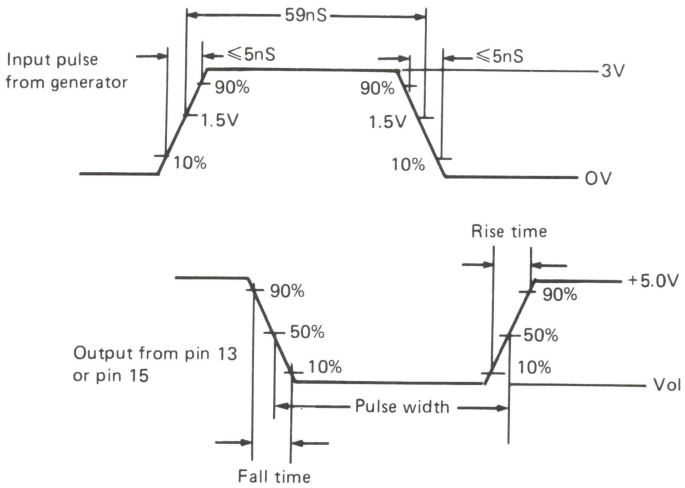


Figure 2. T5683 Transmitter test circuit and switching waveforms (measured @ 8.448 MBPS).



NOTES



Low Power T1 Analog Interface

GENERAL DESCRIPTION

The XR-T5684 is a fully integrated PCM line transceiver intended for DSX-1 digital cross-connect applications. It combines both transmit and receive circuitry in a 28 pin PLCC or PDIP package .The receiver extracts data from AMI coded input signal, and outputs synchronized clock and unipolar RPOS and RNEG data by means of an external 8X or 16X oversampling clock. The oversampling clock is necessary only for application where the clock recovery feature is required. The transmitter of the device pre-shapes the transmit pulse internally, providing the appropriate pulse shape at the cross-connect for line lengths ranging from 0 to 655 feet.The XR-T5684 is manufactured using advanced CMOS technology and requires only a single +5V power supply.

FEATURES

Fully Integrated T1 Transceiver
Low Power Consumption (normally 225 mW)
Recovered Data and Clock Outputs
Driver Performance Monitor
Internal Transmit LBO for Line Lengths Between 0 to 655 Feet
Compliance with TR-TSY-000499, 43802 and 43801
Input Jitter Tolerance Specifications

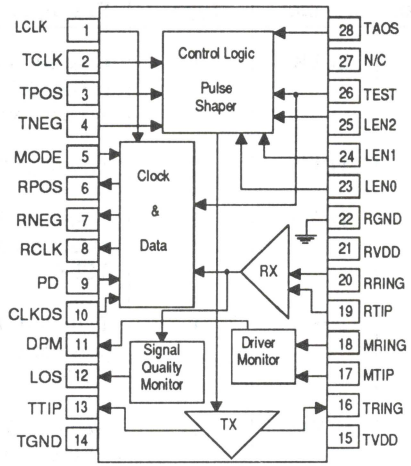
APPLICATIONS

Interfacing T1 Network Equipment such as Multiplexors, Channel Banks and DSX-1 Switching Systems.
Interfacing Customer Premises Equipment such as CSUs, PBX's, T1 Measurement and Test Equipment.

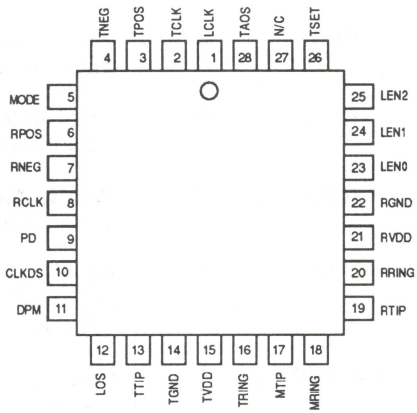
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (continuous)	-0.5 to +7V
Supply Current (continuous)	20mA to -20mA
Storage Temperature	-65°C to +150°C

PIN ASSIGNMENT



PDIP Package



PLCC Package

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5684IJ	28 pin PLCC	-40 to + 85°C
XR-T5684IP	28 pin PDIP	-40 to + 85°C

PIN DESCRIPTION

Pin No.	Symbol	Type	Description
1	LCLK	I	**Oversampling Clock.** 8X or 16X input clock for receive clock recovery circuit. 8X=12.352MHz+/-200ppm with pin 9 set to low. 16X=24.704MHz+/-200ppm with pin 9 set to high.
2	TCLK	I	**Transmit Clock.** T1=1.544MHz+/-50ppm.
3	TPOS	I	**Transmit Positive Data.** A positive NRZ data on this pin causes a positive pulse to be transmitted on TTIP. TPOS is sampled on the falling edge of TCLK.
4	TNEG	I	**Transmit Negative Data.** A positive NRZ data on this pin causes a negative pulse to be transmitted on TRING. TNEG is sampled on the falling edge of TCLK.
5	MODE	I	**Receive Output Data Select.** With this pin set to high, the extracted data at RPOS and RNEG are re-timed using the recovered clock RCLK. With this pin set to low, the received data have no relation to RCLK and are typically stretched by 80nS before being sent to the output. This pin is pulled down internally.
6	RPOS	O	**Receive Positive Data Output.** A positive pulse on this pin corresponds to a positive pulse on RTIP.
7	RNEG	O	**Receive Negative Data Output.** A positive pulse on this pin corresponds to a positive pulse on RRING.
8	RCLK	O	**Receive Clock Output.** Recovered clock using oversampling clock applied to pin 1.(see MODE select of pin 5 and PD of pin 9).
9	PD	I	**Programmable Divider.** The state of this pin determines the oversampling clock applied to pin 1. When LCLK=16X1.544MHz, set PD to high. When LCLK=8X1.544MHz, set PD to low.This pin is pulled down internally.
10	CLKDS	I	**Clock Disable.** With this pin set to high, the recovered clock at pin 8 is disabled. This function is provided for applications where upon input data loss, the output clock can be inhibited by connecting LOS to CLKDS externally. This pin is pulled down internally.
11	DPM	O	**Driver Performance Monitor.** Used as an early warning signal on non-functioning T1 links. If no signal is present on MTIP and MRING for 63 clock cycles. DPM goes high until a next pulse is detected.

PIN DESCRIPTIONS ***(continued)***

Pin No.	Symbol	Type	Description
12	LOS	O	**Loss of Signal.** This pin goes high either when the input signal at RTIP and RRING drops to below 0.4V peak or after 175 zeros are detected. The 175 zeros detection is active only when LCLK is applied.
13	TTIP	O	**Transmit Positive Data.** Transmit AMI signal is driven to the line via a step-up transformer from this pin.
14	TGND	—	**Transmitter Supply Ground.** This pin can be connected to RGND externally.
15	TVDD	—	**5 V +/-5%** Transmitter Supply.
16	TRING	O	**Transmit Negative Data.** Transmit AMI signal is driven to the line via a step-up transformer from this pin.
17	MTIP	I	**Driver Performance Monitor Input.** This pin is normally connected to TTIP for monitoring the driver's activity. It is pulled high internally.
18	MRING	I	**Driver Performance Monitor Input.** This pin is normally connected to TRING for monitoring the driver's activity. It is pulled high internally.
19	RTIP	I	**Receive Tip Input.** The AMI receive signal is input to this pin via a centre-tapped transformer.
20	RRING	I	**Receive Ring Input.** The AMI receive signal is input to this pin via a centre-tapped transformer.
21	RVDD	—	**5 V +/-5% Receive Supply.** This pin can be connected to TVDD externally.
22	RGND	—	**Receive Supply Ground.** This pin is also connected to the substrate of the device.
23	LEN0	I	**Pulse Shaper Select Pin.** Least significant bit.
24	LEN1	I	**Pulse Shaper Select Pin.** Second significant bit.
25	LEN2	I	**Pulse Shaper Select Pin.** Most significant bit.
26	TEST	I	**Factory Test Pin.** This pin must be grounded for normal operation.
27	N/C	—	**No Connection Pin.** This pin can be grounded or left floating.
28	TAOS	I	**Transmit All Ones Select.** Setting TAOS high causes a continuous AMI ones to be transmitted to the line at the frequency set by TCLK.

SYSTEM DESCRIPTION

The device consists of receiver and transmitter circuitry with separated power supplies to reduce crosstalk between the two sections.

RECEIVER

The receiver is sensitive to the entire cable length from the cross-connect and requires no external equalization networks. The receive AMI input signal is applied to RTIP and RRING through a center-grounded transformer. The positive pulse is input to RTIP and the negative pulse is input to RRING.

Comparators are used to slice the data on RTIP and RRING. The slicing level of the comparators are dynamically set at around 70% of peak level of the input signal to ensure optimum signal-to-noise ratio. With Mode Select (pin 5) set to low, the clock recovery feature is bypassed and the output data from the comparators are typically stretched by 80nS before output to RPOS and RNEG respectively.

A positive data at RPOS corresponds to a positive pulse received at RTIP and a positive data at RNEG corresponds to a positive pulse received at RRING.

With Mode Select (pin 5) set to high and an oversampling clock applied to pin 1, the recovered data can be synchronized with RCLK at pin 8. The clock recovery circuit extracts the timing contents from the incoming data transitions by means of an 8X or 16X divider. If there is no data on the input, the divider operates in its free running mode, generating a equal mark-and-space ratio output clock. This free running mode will be interrupted if a positive pulse is detected; the resultant mark-and-space ratio of the output clock is then determined by the position of the occurrence of the positive data relative to its free running position. See timing diagram in Figure 1 and Figure 2.

In all cases, the output data RPOS and RNEG remains stable on the falling edge of RCLK so as to be sampled correctly. The input jitter tolerance with an 8X oversampling clock is shown in Figure 3 and that with a 16X oversampling clock is shown in Figure 4.

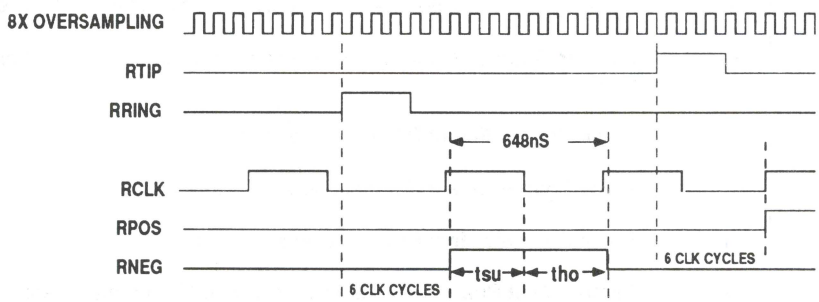


Figure 1. Typical Receive Timing Diagram Using 8X Oversampling Clock.

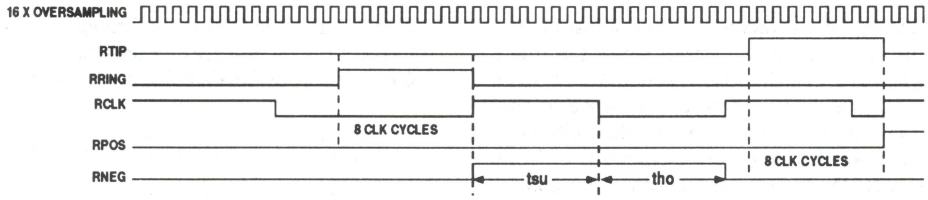


Figure 2. Typical Receive Timing Diagram Using 16X Oversampling Clock.

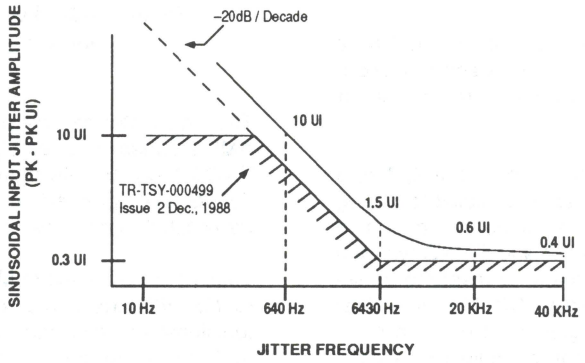


Figure 3. XR-T5684 Input Jitter Tolerance Using 8X Oversampling Clock.

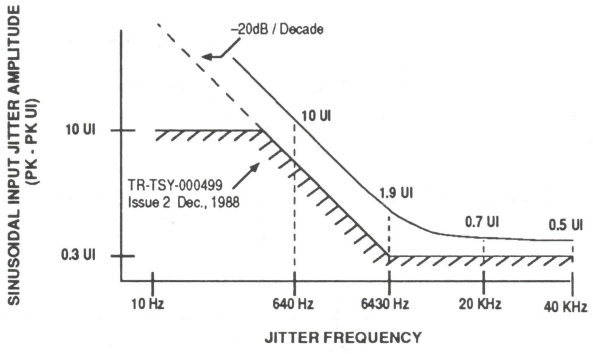


Figure 4. XR-T5684 Input Jitter Tolerance Using 16X Oversampling Clock.

Another function of the receiver is the signal quality monitor that reports loss of signal when the input level on RTIP and RRING falls below 0.4V or upon detection of 175+/-15 consecutive zeros in the incoming data stream. The zero detection circuit is active only when LCLK clock is applied. In both cases, the receiver reports loss of signal by setting LOS high, and at the same time, RPOS and RNEG are forced to low. Under the loss of signal conditions, the receiver will continue to recover data and will return to its normal operation if a valid data is detected on RTIP and RRING.

TRANSMITTER

The transmitter is designed to take dual rail NRZ data, plus a synchronized input clock and produce a bipolar signal with the appropriate shape for transmission to the line.

After sampling by the falling edge of TCLK, TPOS and TNEG data are processed by a digital to analog converter together with a slew-control circuit to generate output pulses at TTIP and TRING with the appropriate amplitude and shape to meet the cross-connect template specified in CB 119. A typical output pulse is shown in Figure 5. In order to meet the amplitude requirement with a single +5V supply, the transmit signal is driven to the line differentially via a 1:1.36 step-up transformer.

Pulse shaping is selectable through input control pins LEN2, LEN1 and LEN0 for line lengths ranging from 0 to 655 feet of ABAM cable as illustrated in Table 1.

LEN2	LEN1	LEN0	Line Length Selected (ft.)
0	1	1	0-133
1	0	0	133-266
1	0	1	266-399
1	1	0	399-533
1	1	1	533-655

Table 1. ABAM or ALVYN Cable Type Line Length Selection

The transmitter can be set to transmit a continuous AMI encoded all ones signal to the line by forcing TAOS high. In this mode, input data TPOS and TNEG are ignored and the frequency of the transmitted signal is determined by TCLK.

With TTIP connected to MTIP and TRING connected to MRING, the driver monitor can detect non-functional T1 transmitter by monitoring the activity at its input. If no signal is presented on MTIP and MRING for 63 TCLK clock cycles, DPM goes high until the next AMI signal is detected.

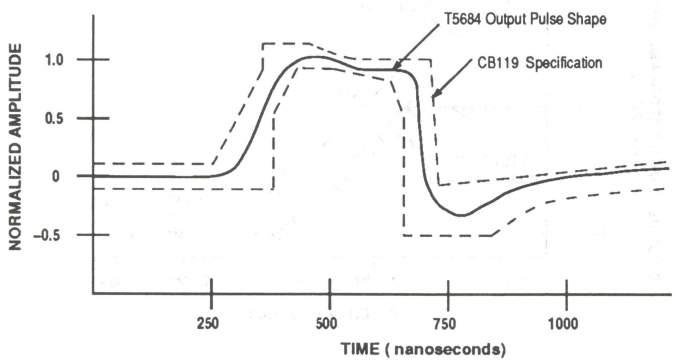


Figure 5. Typical Output Pulse at DSX-1 Cross-connect.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = -40 to + 85°C, RVDD and TVDD = 5V+/-5%, RGND and TGND = 0V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
RECOMMENDED OPERATING CONDITIONS						
VDD/TVDD	DC Supply Voltage	4.75	5	5.25	V	
PD	Total Power Dissipation			400	mW	100% ones density & max. line length @ 5.25V and with 16X oversampling clock running.
PD	Normal Power Dissipation		225		mW	50% ones density & 300ft. line length @5.0V and with over - sampling clock disabled.
INPUTS						
VIH	High Level Input (Note 1)	2.0			V	
VIL	Low Level Input (Note 1)			0.8	V	
IIL	Input Leakage Current			±10	µA	Pins = TCLK, TPOS, TNEG, LEN0/1/2.
OUTPUTS						
VOH	High Level Output (Note 2)	2.4			V	
VOL	Low Level Output (Note 2)			0.4	V	

Note 1: All input pins except RTIP, RRING, MTIP and MRING.

Note 2: All output pins except TTIP and TRING.

ANALOG SPECIFICATIONS

Test Conditions: TA= -40 to +85°C, RVDD and TVDD = 5V+/-5%, RGND and TGND = 0V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VPA	AMI Output Pulse Amplitudes	2.4	3.0	3.6	V	Measured at DSX-1 using a 1:1.36 step up transformer with all line length select as shown in Table1.
TXJA	Jitter added by the transmitter					
	10Hz - 40KHz (note 3)	—	0.025	—	UI	
	Broad Band (note 3)	—	0.05	—	UI	
RXS	Receiver Sensitivity Below DSX(0dB=2.4V)	6	—	—	dB	
RLOS	Receiver Loss of Signal Threshold	—	0.4	—	V	
	Number of consecutive zeros before LOS	160	175	190	—	
RTH	Receiver Data Slicing Threshold	—	70	—	% of peak	

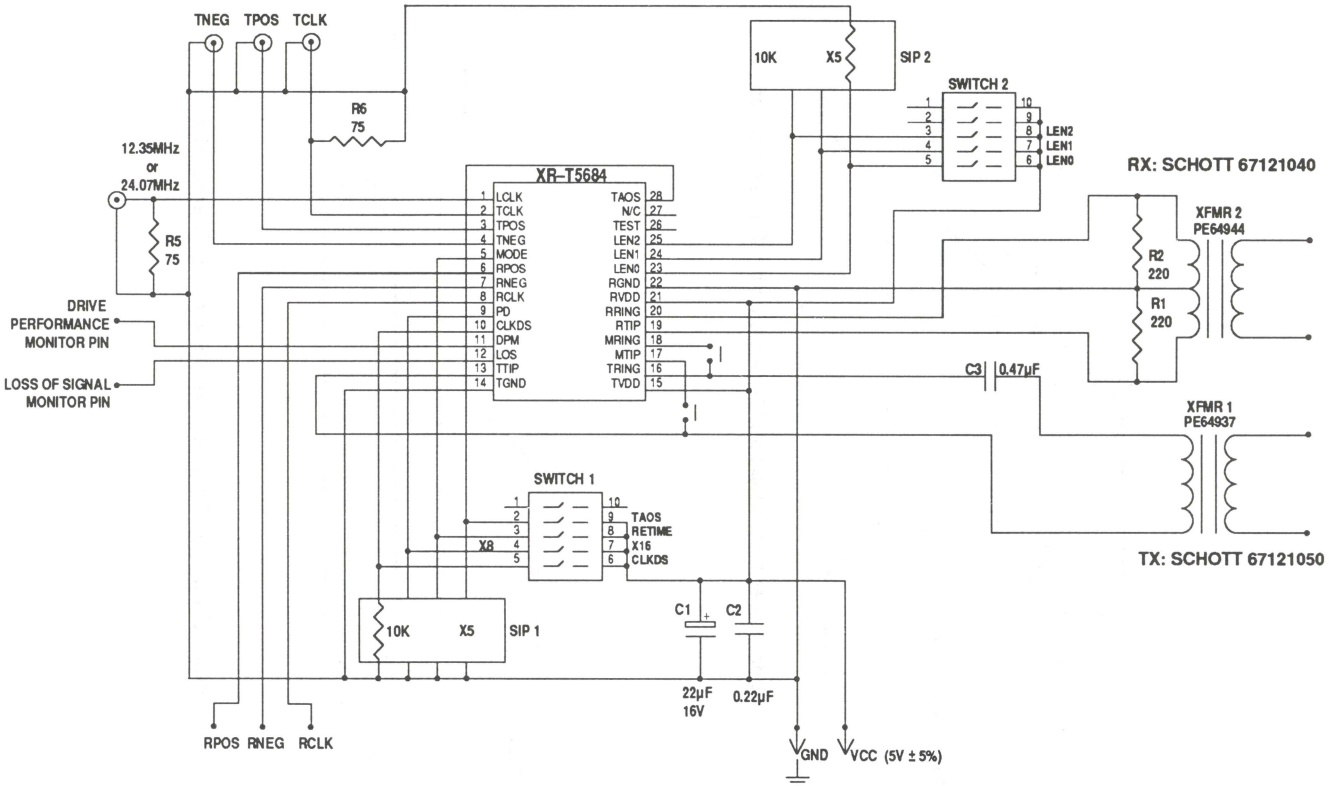
Note 3 : Input clock to TCLK is jitter free.

AC CHARACTERISTICS

Test Conditions: TA = -40 to + 85°C, RVDD and TVDD = 5V+/-5%, RGND and TGND = 0V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TCLKf	Clock Frequency		1.544		MHz	
	TCLK Clock Duty Cycle	40	50	60	%	
LCLKf	Frequency 8X		12.352		MHz	
LCLKf	16X		24.704		MHz	
	LCLK Clock Tolerance	—	—	+/-200	ppm	
	LCLK Clock Duty Cycle	35	50	65	%	
tsu	TPOS/TNEG to TCLK setup time	25	—	—	ns	
tho	TCLK to TPOS/TNEG hold time	25	—	—	ns	
tdr	RTIP/RRING Rising to RPOS/RNEG Rising (note 4)	15	30	120	ns	
tdf	RTIP/RRING Falling to RPOS/RNEG Falling (note 4)	60	120	250	ns	
	RCLK Duty Cycle	—	50	—	%	
tsu	RPOS/RNEG to RCLK Falling setup time	—	300	—	ns	
tho	RCLK Falling to RPOS/ RNEG hold time	—	324	—	ns	

Note 4. Pin 5 Set to Low .



Application Schematic Diagram

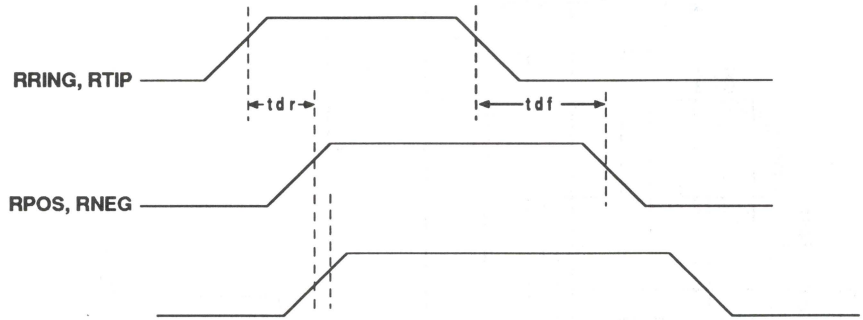


Figure 6. Receiver Clock and Data Switching Characteristics

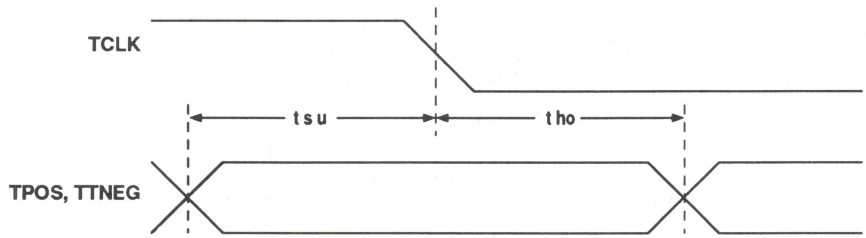


Figure 7. Transmit Clock and Data Switching Characteristics

T1/CEPT Jitter Attenuator

GENERAL DESCRIPTION

The function of the XR-T56188 is to attenuate the incomming jitter of clock and data. To do this, two buffer of 144 bits depth and a crystal oscillating at four times the receiver clock frequency are needed.This device is compliant to the latest specifications such as TR62411(Accunet [TM] T1.5 Service Description and Interface Specification December 1988),TR-TSY-000170 (Digital Cross Connect System Requirements and Objectives November, 1985), and CCITT Recommendations G.735 and G.742. The XR-T56188 is compatible to the XR-T5690 T1 Framer and the XR-T5684 DSX-1 Transceiver.

FEATURES

Reduces jitter present on clock and data for T1 and CEPT lines up to138Ulpp.
Meets jitter templates for TR62411, TR-TSY-000170, G.735, and G.742.
Minimum external components
Selectable buffer size: 144, 32, 16 and 8 bits
Disable pin option
Single 5V +/- 10% power supply
Pin to pin and functionally compatible to DS2188
Available in 16 pin DIP and SOIC

APPLICATIONS

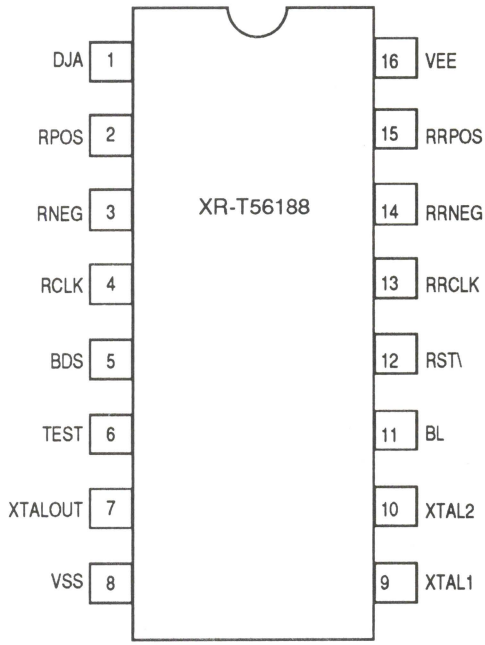
Carrier Systems
Switching Systems
Local Area Networks
Multiplexers
Cross Connects

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-1.0V to +7V
Storage Temperature	-65°C to 150°C
Soldering Temperature	260°C for 10sec

Note: Exceeding this ratings may affect reliability of this device.

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T56188CP	Plastic	0°C to 70° C
XR-T56188IP	Plastic	-40°C to 85°C
XR-T56188CD	SOIC	0°C to 70°C
XR-T56188ID	SOIC	-40°C to 85°C



NOTES



T1/CEPT High Speed Jitter Attenuator

GENERAL DESCRIPTION

The function of the XR-T56189 is to attenuate the incomming jitter of clock and data. To do this, two buffers of 128 bits depth and a crystal oscillating at the receiver clock frequency are needed.

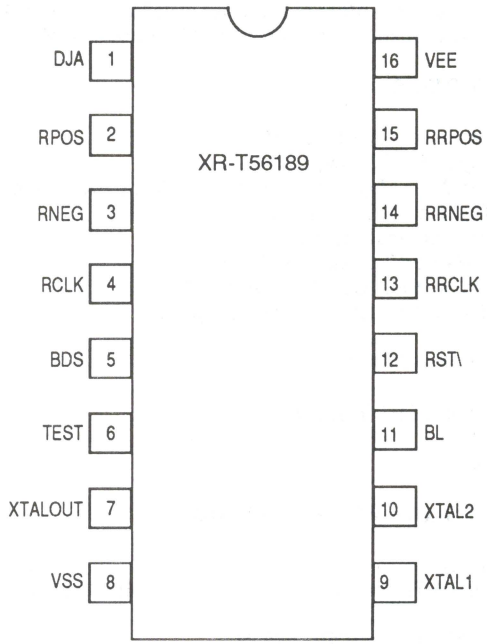
FEATURES

Reduces jitter present on clock and data for T1 and CEPT lines up to128 UIpp.
Minimum external components
Selectable buffer size: 144, 32, 16,and 8 bits
Disable pin option
Single 5V +/- 10% power supply
Pin to pin and functionallycompatible to DS2188
Maximum Data Rate (8.5MHz)
Available is 16 pin DIP and SOIC

APPLICATIONS

Carrier Systems
Switching Systems
Local Area Networks
Multiplexers
Cross Connects

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-1.0V to +7V
Storage Temperature	-65 C to 150 C
Soldering Temperature	260 C for 10sec

Note: Exceeding this ratings may affect reliability of this device.

ORDERING INFORMATION

Part Number	Package	Operating Temp
XR-T56188CP	Plastic	0°C to 70°C
XR-T56188IP	Plastic	-40°C to 85°C
XR-T56188CD	SOIC	0°C to 70°C
XR-T56188ID	SOIC	-40°C to 85°C

Low Power PCM Line Interface

GENERAL DESCRIPTION

The XR-T56L85 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 2.048 Mbps and the signal level to the receiver can be attenuated by –10dB of cable loss at half the bit rate. Total current consumption is between 12–16mA at +5V.

FEATURES

Low Power (Typical 14mA)
Single +5.0V Supply
Up to 2.048 Mbps Operation in Both TX and RX Directions
TTL Compatible Interface
Receiver Input can be:
  Balanced Transformer Coupled
  Capacitively Coupled (Twisted Pair)
  Single Coaxial Capacitive Coupling

APPLICATIONS

T1 and CEPT Interfaces
CPI
DMI

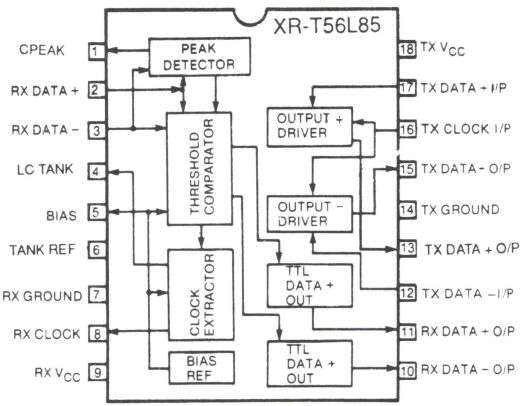
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20V
Storage Temperature	–65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T56L85N	Ceramic DIP	–40°C to +85°C
XR-T56L85D	S.O.I.C.	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the receiver input either through a balanced transformer or a single ended capacitive coupled terminal. A peak detector following the input generates a DC reference for the positive threshold comparator. This voltage in turn is mirrored around a reference voltage to establish the threshold voltage for the negative pulses. This way it is possible to extract the positive and negative data pulses as well as the recovered clock. A tank circuit tuned to the appropriate frequency is added externally to maintain the clock output. The clock signal, data + and data –, all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 80mA. With full width data applied to the inputs together with a synchronized clock the output will generate a bipolar signal when driving a centre-tapped transformer. A typical application diagram for the XR-T56L85 is shown in Figure 5.

DC ELECTRICAL CHARACTERISTICS

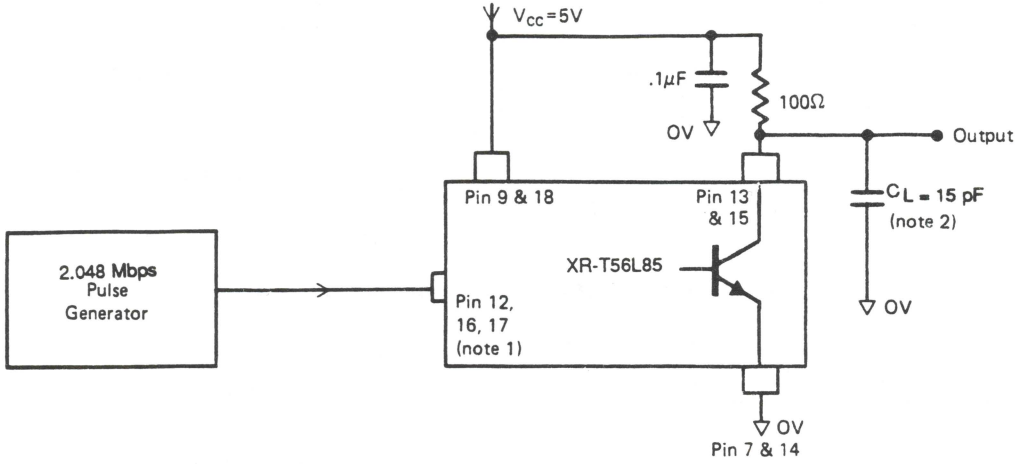
Test Conditions: V_{CC} = 5.0V ± 5%, T_A = –40°C to +85°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75	5	5.25	V	
Supply Current		14	16	mA	Total Current to Pin 9 & Pin 18 (Transmitter Outputs Open and All Ones Pattern)
Receiver Section					
Tank Drive Current	300	500	700	µA	Measured at Pin 4, V_{CC} = 5V
Clock Output Low		0.3	0.6	V	Measured at Pin 8 I_{OL} = –1.6mA
Clock Output High	3.0	3.6		V	Measured at Pin 8 I_{OH} = 400µA
Data Output Low		0.3	0.6	V	Measured at Pin 10 & 11 I_{OL} = –1.6mA
Data Output High	3.0	3.6		V	Measured at Pin 10 & 11 I_{OH} = 400µA
Transmitter Section					
Driver Output Low	0.6	0.9	1.2	V	Measured at Pin 13 & 15 I_{OL} = –40mA
Output Leakage Current			100	µA	Measured in Off State Output Pull-up to +20V
Input High Voltage	2.2			V	Measured at Pin 12, 16 & 17 I_{OL} = –40mA, V_{OL} = 1.0V
Input Low Voltage			0.8	V	Measured at Pin 12, 16 & 17 Output Off
Input Low Current			–1.6	mA	Measured at Pin 12, 16 & 17 Input Low Voltage = 0.4V
Input High Current			40	µA	Measured at Pin 12, 16 & 17 Input High Voltage = 2.7V
Output Low Current			–80	mA	Measured at Pin 13 & 15 V_{OL} = 1.0V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V ± 5%, T_A = –40°C to +85°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Receiver Section					
Input Level		6	6.6	Vpp	Measured Between Pin 2 & 3
Loss Input Signal Alarm Level		0.6		Vpp	Measured Between pin 2 & 3 Alarm On Pull Data/Clock Output High
Input Impedance at 2048 KHz		2.5		kΩ	Measured Between Pin 2 & 3 With Sinewave Input
Clock Duty Cycle	35	50	65	%	Measured at Pin 8 at 2.0V DC Level
Clock Rise & Fall Time		20	40	ns	Measured at Pin 8, C_L = 15pF
Data Pulse Width	35	50	75	% of clock period	Measured at Pin 10 & 11 At 1 V DC Level, Cable Loss = 0dB
Transmitter Section					
Pulse Width at 2048KHz	234	244	264	ns	Measured at Pin 13 & 15 Figure 1
Output Rise Time		12	25	ns	Figure 1
Output Fall Time		12	25	ns	Figure 1
Output Pulse Imbalance		2.5		ns	At 50% Output Level



Note 1. Inputs that are not connected to pulse generator will be tied to $+V_{CC}$ via 1k resistor.
Note 2. C_L includes probe and jig capacitance.

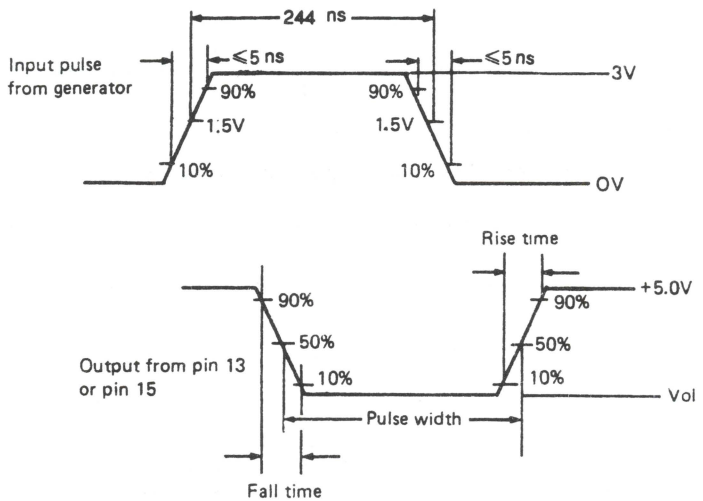


Figure 1. Transmitter Test Circuit and Switching Waveforms

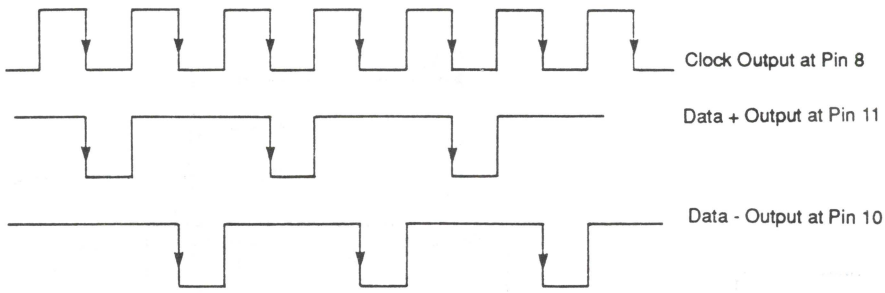


Figure 2. Receiver Output Timing Diagram With 1-1-1-1 Pattern

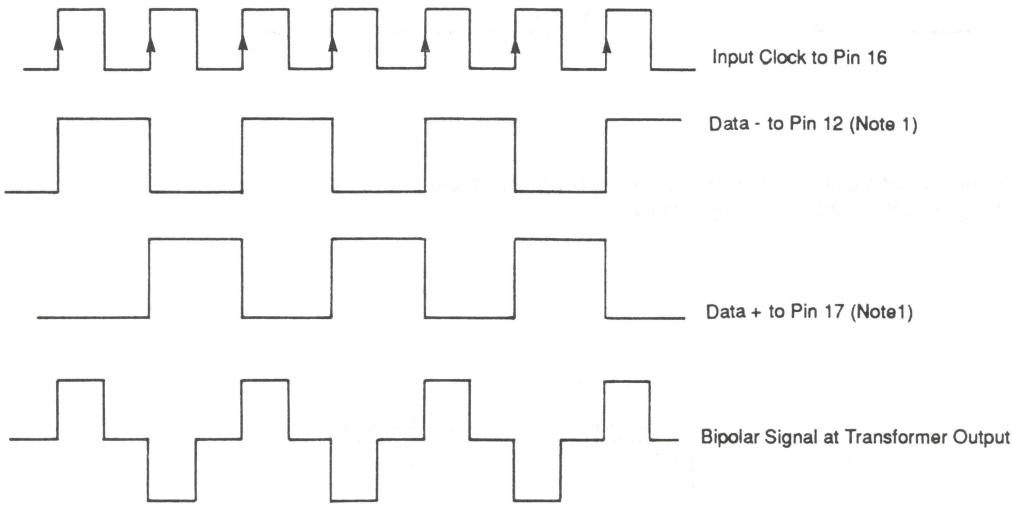


Figure 3. Transmitter Input Timing Diagram

Note 1: In the case where Data + and Data – are half-width data Pin 16 should be returned to $+V_{CC}$ via a 1k resistor.

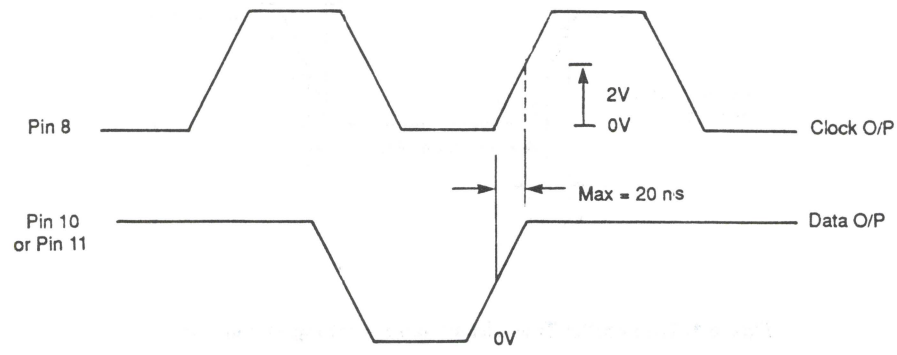
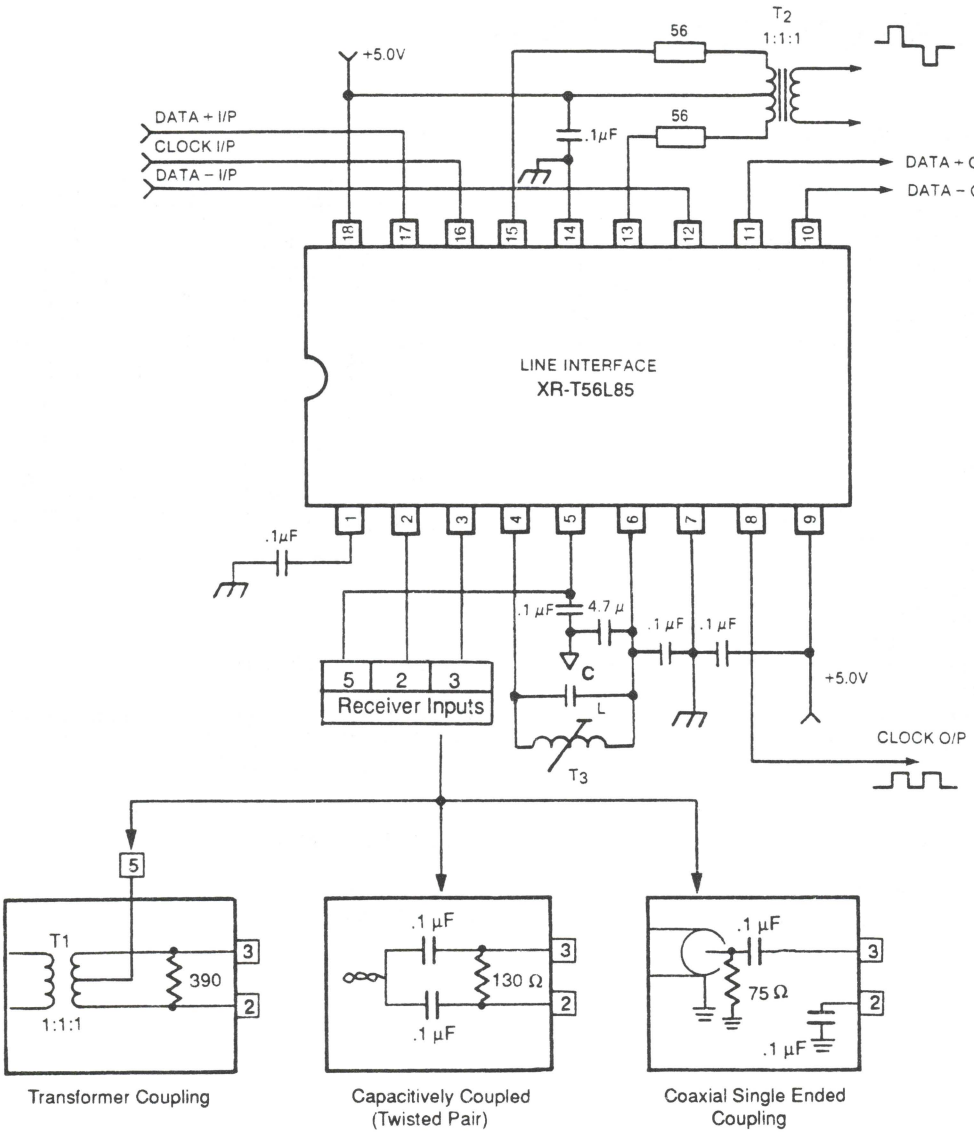


Figure 4. XR-T56L85 Data & Clock Timing Diagram with 1-1-1-1 Input Pattern and –3dB Cable Loss



T1 = AIE Input Transformer 315-0765
T2 = AIE Output Transformer 318-0696
T3 = AIE Tank Coil 415-0804

Device	1.544MBPS	2.048MBPS
L	60μH	60μH
C	175PF	100PF

Figure 5. Recommended Circuit for 1.544 & 2.048MBPS

64 Kbit/s Codirectional Interface

GENERAL DESCRIPTION

The XR-T6164 is a bipolar analog IC intended for general purpose line transceiver applications. The receiver is designed for short line applications (<10dB) at bit rates up to 1.544 Mbit/s (T1). When used in conjunction with either XR-T6165 or XR-T6166 the device conforms to CCITT G.703 specification requirements for a 64Kbit/s codirectional interface. Typical current consumption is 25mA.

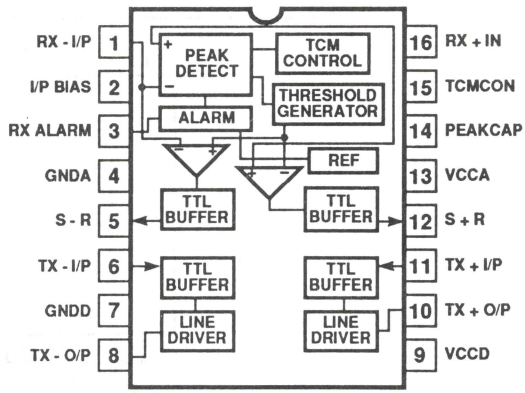
FEATURES

CCITT G.703 compatible when used with either XR-T6165 or XR-T6166
Low Power
TTL Compatible
Links Remote Equipment at Distances Up to 500M Without Equalization
Receive Input Gating Provides Ping Pong Operation Capability
Loss of Signal Alarm
Dual Matched Driver Outputs

APPLICATIONS

Data Adaption Unit (DAU).
General Purpose TTL Compatible Line Interface

PIN ASSIGNMENT



XR-T6164

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6164 CN	Ceramic DIP	0°C to 70°C
XR-T6164 CP	Plastic DIP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to 150°C
Supply Voltage	20V

PIN DESCRIPTIONS

Name	I/O	Pin	Description
RX – I/P	I	1	Receiver negative bipolar Input.
I/P BIAS	I	2	Internally generated bias voltage for receive inputs.
RX ALARM	O	3	Loss of signal alarm (<–15dB) (active low).
GNDA	I	4	Analog Ground
S – R	O	5	Receive negative output data (active low).
TX – I/P	I	6	Transmit negative input signal (active high).
GNDD	I	7	Digital Ground.
TX – O/P	O	8	Transmit negative output data, open collector.
VCCD	I	9	+5V ± 5% digital supply.
TX + O/P	O	10	Transmit positive output data, open collector.
TX + I/P	I	11	Transmit positive input signal — active high.
S + R	O	12	Receive positive output data (active low).
VCCA	I	13	+5V ± 5% analog supply.
PEAK CAP	O	14	Receiver peak detector storage capacitor.
TCM CON	I	15	Time compression multiplex control pin (active low). When active disables Rx inputs and stores peak voltage.
RX + I/P	I	16	Receiver positive bipolar input.

SYSTEM DESCRIPTION

The XR-T6164 is a general purpose line interface chip. It contains both receive and transmit circuitry necessary to interface TTL signals either to or from a twisted pair cable.

2

Receiver

In the receive direction XR-T6164 takes balanced bipolar input signals, having been attenuated and distorted by twisted pair cable, and outputs TTL compatible active low signals corresponding to received positive and negative input data (S+R, S–R). Received signals are fed to a peak detector and threshold generator circuit providing a slicing threshold proportional to the peak received input level. Dual stage data comparators slice the input signals at this threshold and pass signals to TTL compatible output buffers. An alarm comparator, with hysteresis to prevent output jitter, monitors input signal levels (threshold set at –15dB).

Transmitter

The XR-T6164 transmitter contains two matched open collector output drivers capable of driving line transformers directly with currents up to 40mA. The transmitter output circuits include diode clamps to ensure non-saturating operation. Transmitter inputs are TTL compatible.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, T_A = 25°C, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75		5.25	V	
Analog Supply Current	4		6.5	mA	
Digital Supply	13		20	mA	
RECEIVER					
Peak Input Signal		2	2.2	Vp	Pins 1, 16 with respect to pin 2 (See Note 1)
Dynamic Range			10	dB	Without Equalization
Input Impedance		20		kΩ	Pins 1, 16
Input Slicing Threshold		50		%	
Input Bias Voltage		1.45		V	Pin 2
Loss of Signal Alarm		–15		dB	
Alarm Level Hysteresis		1.5		dB	
Peak Detector Leakage		–80		µA	Pin 14; V_{IN} = 1V
Data Output Low			0.4	V	Pins 5, 12; I_{OUT} = –1.6mA
Data Output High	3.6			V	Pins 5, 12; I_{OUT} = +40µA
Alarm Output Low			0.4	V	Pin 3; I_{OUT} = –1.6mA
Alarm Output High	4.9			V	Pin 3; I_{OUT} = +40µA
TCM Input Low Voltage			0.8	V	Pin 15; I_{IN} min = –500µA Pin 15; I_{IN} max = +5µA
TRANSMITTER					
Input Low Voltage			0.8	V	Pins 6, 11; I_{IN} = –700µA
Input High Voltage	2.2			V	Pins 6, 11; I_{IN} = +5µA
Output Low Voltage		1		V	Pins 8, 10; I_{OUT} = –40mA
Output Low Current	–40		–40	mA	Pins 8, 10; V_{OUT} = 1V
Output Leakage	–100			µA	Pins 8, 10; V_{OUT} = 10V Outputs in off state.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} =5V ± 5%, T_A = 25°C, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
RECEIVER					
Input Level	1		2.2	Vp	Pin 1, 16 with Respect to Pin 2 (See Note 1)
Output Rise Time			50	ns	Pins 5, 12; C_L = 15pF 10% to 90%
Output Fall Time			50	ns	Pins 5, 12; C_L = 15pF
TRANSMITTER					
Output Rise Time			50	ns	Pins 8, 10; R_L = 130, C_L = 15pF 10% to 90%
Output Fall Time			50	ns	Pins 8, 10; R_L = 130, C_L = 15pF 90% to 10%
Rising Edge Delay			60	ns	Pins 8, 10; R_L = 130, C_L = 15pF 50% to 50% (i/p to o/p)
Falling Edge Delay			60	ns	Pins 8, 10; R_L = 130, C_L = 15pF 50% to 50% (i/p to o/p)

Note 1. Higher input voltages are possible if a resistive input attenuator is used.

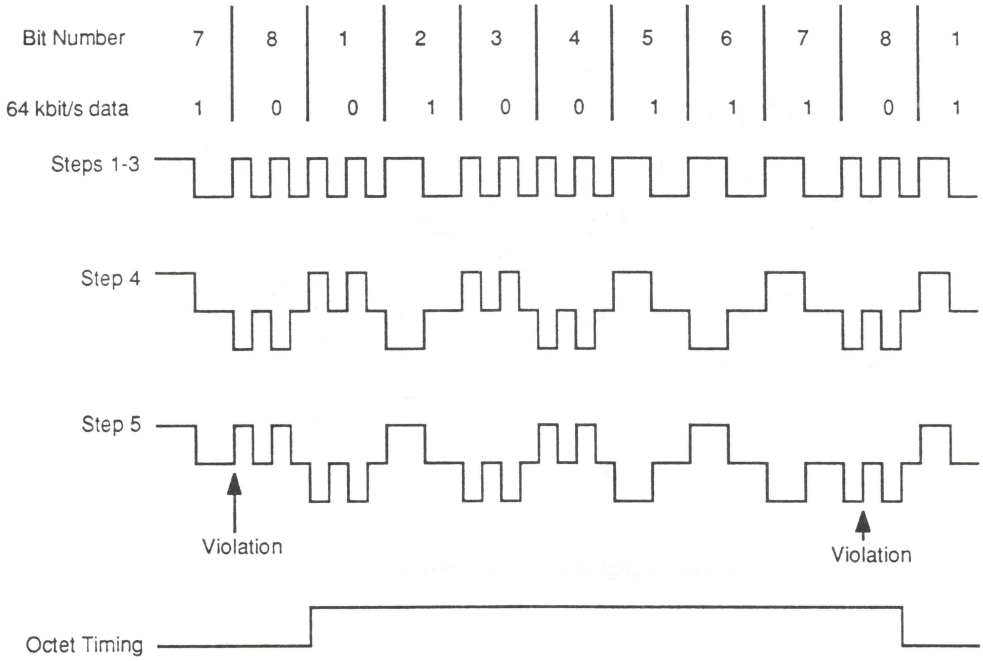


Figure 1. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

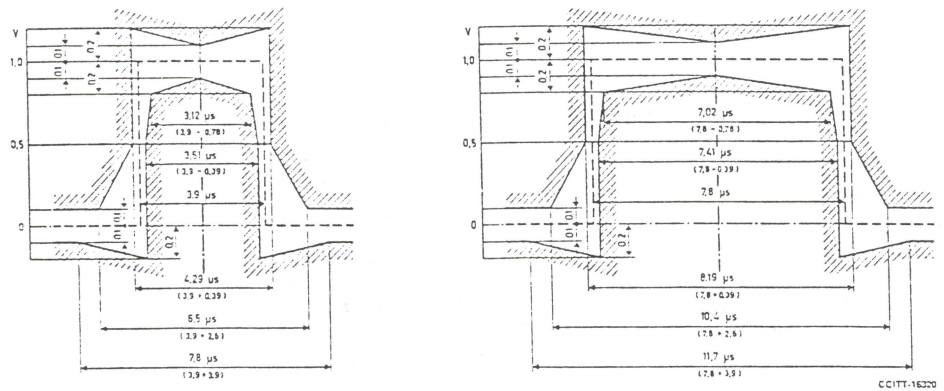


Figure 2. Pulse Masks of the 64 Kbit/s Codirectional Interface

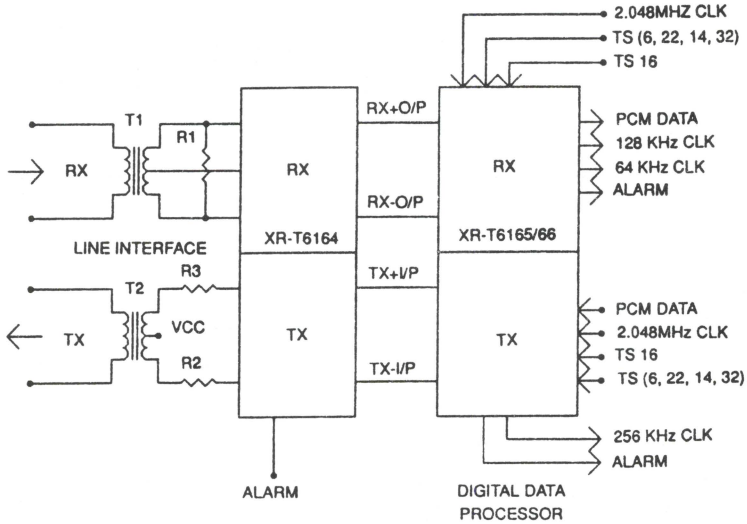


Figure 3. Digital Data Processor Application

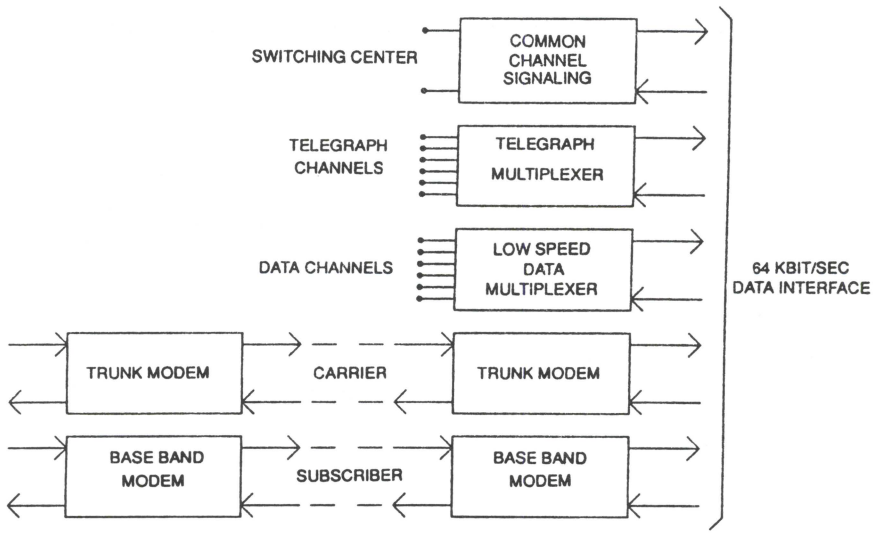


Figure 4. Typical 64 kbit/s Data Interface

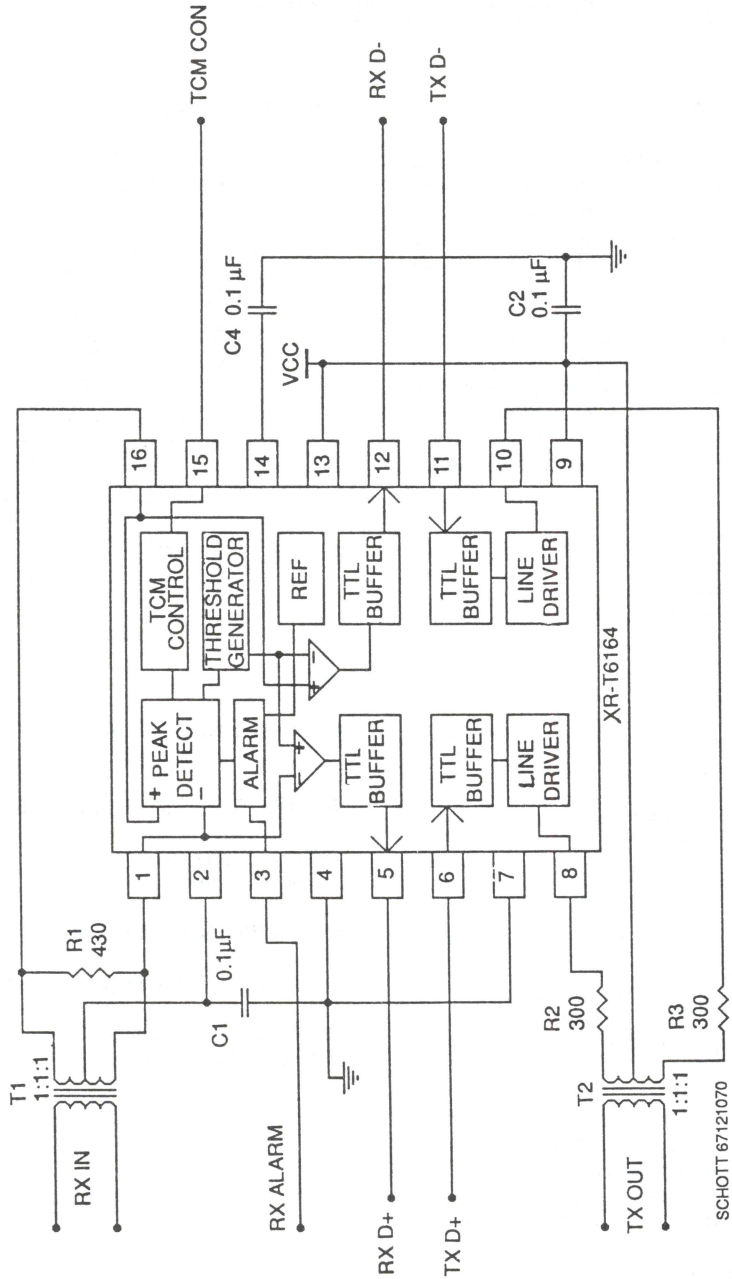


Figure 5. Typical Applications Schematic For XR-T6164

Codirectional Digital Data Processor

GENERAL DESCRIPTION

The XR-T6165 is a digital CMOS circuit which performs the interface function between a 64Kbit/s data stream and a 2048Kbit/s PCM timeslot data channel. When used in conjunction with the XR-T6164, the XR-T6165 conforms to CCITT G.703 specification requirements for a 64Kbit/s codirectional interface.

The XR-T6165 is composed of a transmitter which transforms 8 bit 2048Kbit/s timeslot data packets into a coded 64Kbit/s data stream, and a receiver which performs the reverse operation. Repetition or deletion of received or transmitted data when clock skews or transients occur is automatic, allowing continuous synchronized data transmission or reception.

FEATURES

Low Power CMOS Technology
All Receiver and Transmitter Inputs and Outputs are TTL Compatible

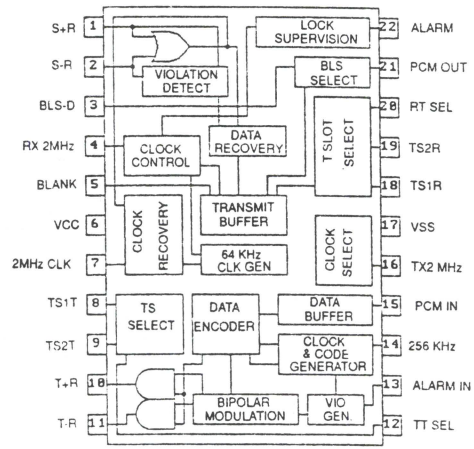
Receiver

Converts Received Encoded 64kbit/s Data to 2048Kbit/s Binary Data For Insertion Into a Timeslot of a PCM Frame
Recovers Both Clock and Octet Timing
Performs Byte Insertion or Deletion in Response to Local Clock Slips
Programmable Loss of Lock Alarm (Output Inhibit/ non-Inhibit)
Glitch Free Output Data Completely Available Within Supplied Timeslot Envelope
Up to 125µs Variance of Data Transfer Timing in Both Transmit and Receive Paths, Allowing Operation in Plesiochronous Networks

Transmitter

Extract 2048Kbit/s Data From a PCM Frame Timeslot and Encodes it as 64Kbit/s Data According to CCITT G.703 Requirements
Performs AMI Coding and Bipolar Violation Insertion for Octet Timing
Allows Inhibit of Bipolar Violation Insertion for Transmission of Alarm Conditions
Performs Byte Insertion or Deletion in Response to Local Clock Slips and Timeslot Changes

PIN ASSIGNMENT



APPLICATIONS

Data Adaptation Unit (DAU)
General 64Kbit/sec Interfaces

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to 150°C
Supply Voltage	4.5V to 5.5V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6165 CN	Ceramic DIP	0°C to 70°C
XR-T6165 CP	Plastic DIP	0°C to 70°C

PIN DESCRIPTIONS

Name	I/O	Pin	Description
S+R	I	1	Positive AMI data to receiver (Active Low).
S-R	I	2	Negative AMI data to receiver (Active Low).
BLS	I	3	Byte Locking Supervision (Active Low). When active causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	I	4	Receiver 2048kHz clock.
BLANK	I	5	PCMOUT data blanking (Active High), When active, forces PCMOUT data to all ones(AIS)
VCC	I	6	+5V ± 10% power supply.
RXCK2	I	7	2048kHz clock recovery MHz signal.
TS1T	I	8	Timeslot input 1 for transmitter.
TS2T	I	9	Timeslot input 2 for transmitter.
T+R	O	10	Transmit positive output AMI data (Active Low).
T-R	O	11	Transmit negative output AMI data (Active Low).
TTSEL	I	12	Transmit timeslot select. When high pin 8 selected. When low pin 9 selected.
ALARMIN	I	13	Alarm input (Active High). When active inhibits insertion of violation in transmitted data.
TX256KHZ	I	14	Transmitter 256kHz clock.
PCMIN	I	15	Transmitter PCM input.
TX2MHZ	I	16	Transmitter 2048kHz clock.
VSS	I	17	0V power supply.
TS1R	I	18	Timeslot input 1 for receiver.
TS2R	I	19	Timeslot input 2 for receiver.
RTSEL	I	20	Receive timeslot select. When high pin 18 selected; when low pin 19 selected.
PCMOUT	O	21	Received PCM output data.
ALARM	O	22	Alarm (Active High), When active, indicates loss of received bipolar violations.

SYSTEM DESCRIPTION

When used in conjunction with the XR-T6164, the XR-T6165 will form a CCITT G.703 compatible 64Kbit/s data adaption unit (DAU), interfacing between a 2048Kbit/s PCM highway and a variable length twisted pair cable.

Transmitter

Operation of the transmit circuit is to convert eight bit 2048Kbit/s PCM timeslot data packets into coded continuous 64Kbit/s data. PCM data is read into the transmitter using a 2048kHz local clock and timeslot signal. Transmission is controlled by a 256kHz local clock. Four periods are dedicated to each bit in order to code "0" (0101) and "1" (0011). Timeslot is an envelope derived externally from the 2048kHz clock. and covers eight clock pulses. A two input selector at the timeslot input allows the transmitter to be hard wired to two timeslot positions, selectable using TTSEL. Data is loaded to a storage buffer and transferred to an output shift register, controlled by the external 256kHz signal, only after complete transmission of previously received data. Circuitry is included to delete or repeat complete words of data should skew between the clock signals occur, or during an adjustment of the timing of the timeslot signal, for example when changing from one timeslot position to another. A byte repetition just occurs once; if no new PCM data is received, the transmitter outputs stay high. Octet timing is maintained during these operations. Coded data is alternately fed to two output pins to realize AMI coding, using an external transformer and two line drivers. Transmission of octet timing is performed by feeding the seventh and eighth data bits in each word to the same output. This function may be inhibited by setting ALARMIN active.

Receiver

Operation is to receive coded continuous 64kbit/s input and extract data in the form required for insertion into a 2048kbit/s PCM timeslot. A 128kHz clock is derived from the received data and used to perform decoding of the input signal. If lock is lost with received data the clock circuit enters a seek mode, increasing the speed of the internal clock and reducing the time required to regain lock. Bipolar violations, used to identify bit 1 in the input signal are used to synchronize circuit operation for octet timing. In the absence of violations, for example when receiving a transmitted alarm condition, the circuit will continue to operate in synchronization with respect to the last received violation, Under this condition the received signal PCMOUT (Received PCM output data) is held high indicating AIS. This function may be inhibited using BLS, and the output

set to all ones if required using the BLANK input. ALARM goes high after eight consecutive violations are missed. To accommodate differences between the remote (transmitting) and local clock rate, slip control logic is included in the receiver design. Under slow local clock conditions data will be deleted periodically, while under fast conditions the last output PCM data will be repeated. Octet timing is maintained during these operations. Data appearing at PCMOUT is arranged to be completely framed by the read timeslot signal and is glitch free. A two input selector at the timeslot input allows the receiver to be hard wired to two time slot positions, selectable using RTSEL.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Logic 1	2.4			V	
V_{IL}	Logic 0			0.4	V	
V_{DD}	Supply	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Supply Current		500		µA	
I_{IL}	Input Leakage			1	µA	
I_{OL}	O/P Low Current		2		mA	V_{OL} < 0.4V
I_{OH}	O/P High Current		2		mA	V_{OH} > 2.4V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
tr, tf	Output Rise/Fall Time		20		nS	
RECEIVER						
t_{RS}	TS Rising Edge to RX2MHZ Set up	0		TRXL −100	nS	Figure 1
t_{RH}	TS Falling Edge to RX2MHZ Hold	0		TRXL −100	nS	Figure 1
t_{DRS}	PCMOUT Edge to RX2MHz Set up		10		nS	Figure 1
t_{DRH}	PCMOUT Edge to RX2MHz Hold		10		nS	Figure 1
t_{PW}	PCMOUT Pulse Width		488		nS	Figure 1
t_{RXH}	RX2MHz High Time		244		nS	±100ppm
t_{RXL}	RX2MHz Low Time		244		nS	±100ppm
TRANSMITTER						
t_{TS}	TS Rising Edge to TX2MHZ Set Up	20		TTXL −100	nS	Figure 2
t_{TH}	TS Falling Edge to TX2MHz Hold	0		TTXL −100	nS	Figure 2
t_{DS}	PCMIN Edge to TX2MHz Set Up	100			nS	Figure 2
t_{DH}	PCMIN Edge to TX2MHz Hold	100			nS	Figure 2
t_{TXH}	TX2MHz High Time		244		nS	±100ppm Figure 2
t_{TXL}	TX2MHz Low Time		244		nS	±100ppm Figure 2
t_{KXH}	TX256kHz High Time		1.95		µS	±100ppm
t_{KXL}	TX256kHz Low Time		1.95		µS	±100ppm

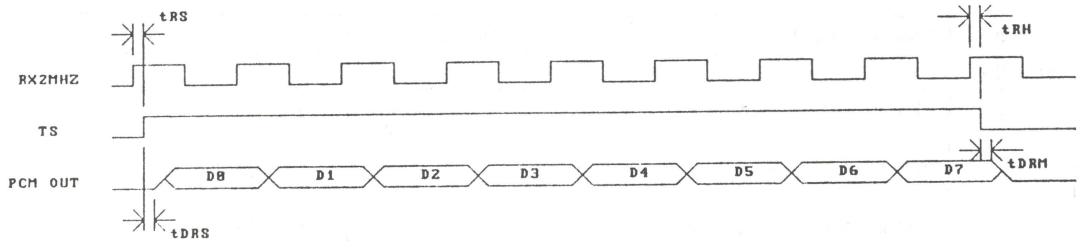


Figure 1. Receiver Time Slot Detail

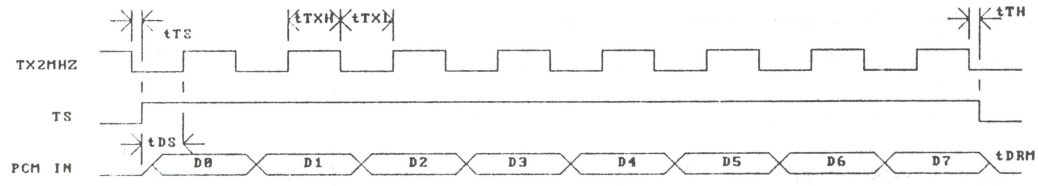


Figure 2. Transmit Time Slot

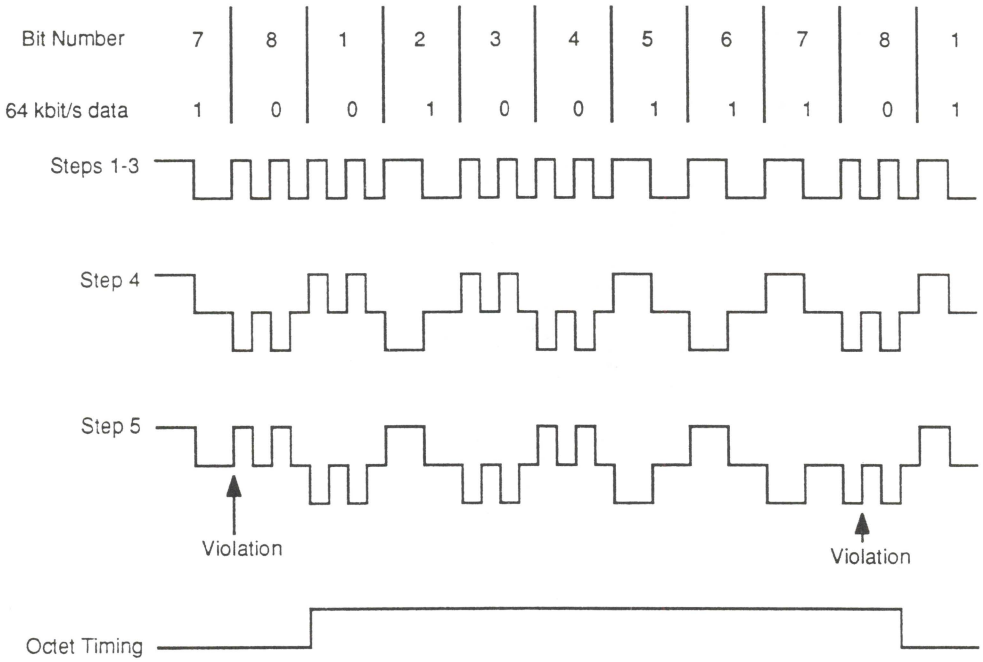


Figure 3. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

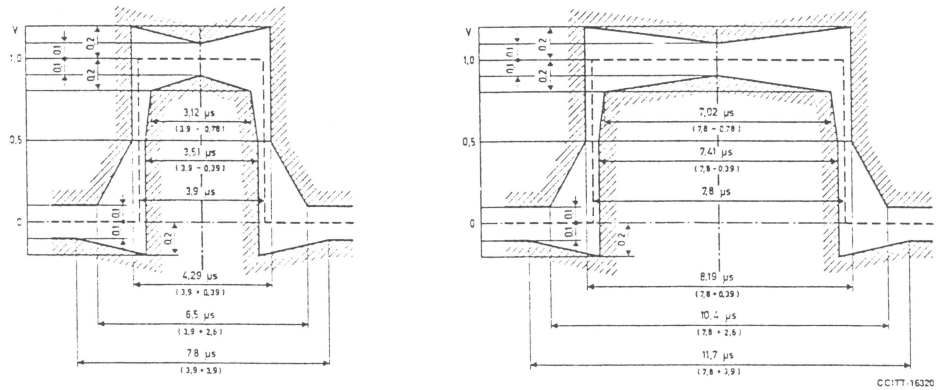


Figure 4. Pulse Masks of the 64kbit/s Codirectional Interface

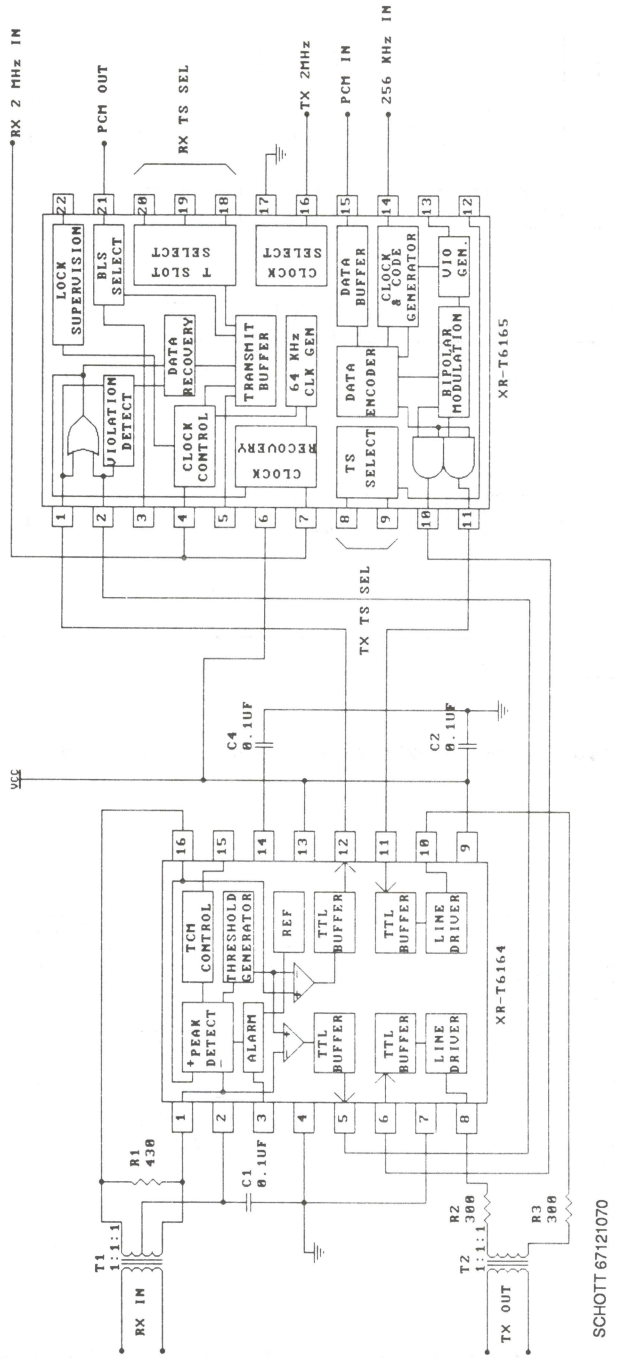


Figure 5. Typical Application Diagram For XR-T6164/65

Codirectional Digital Data Processor

GENERAL DESCRIPTION

The XR-T6166 is a digital CMOS circuit which performs the interface function between a 64Kbit/s data stream and a 2048Kbit/s PCM timeslot data channel. When used in conjunction with the XR-T6164, the XR-T6166 conforms to CCITT G.703 specification requirements for a 64Kbit/s co-directional interface.

The XR-T6166 is composed of a transmitter which transforms 8 bit 2048Kbit/s timeslot data packets into a 64Kbit/s data stream and a receiver which performs the reverse operation. The XR-T6166 provides additional features which allow the repetitions and deletions of both received and transmitted data as clock skews and transients occur. An extracted receive clock output is also provided together with a receive clock loss of lock flag.

FEATURES

Low Power CMOS Technology
All Receiver and Transmitter Inputs and Outputs are TTL Compatible
Up to 125µs Variance of Data Transfer Timing in Both Transmit and Receive Paths, Allowing Operation in Plesiochronous Networks

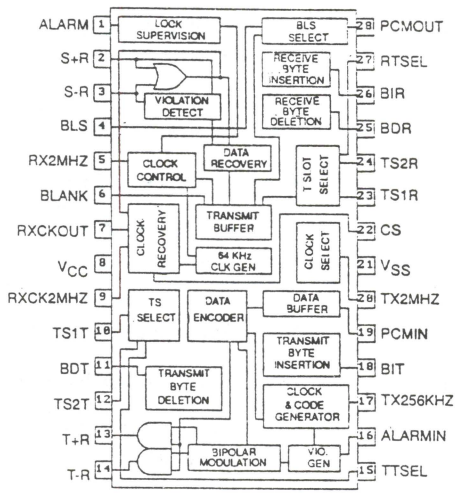
Receiver:

Converts Received Encoded 64Kbit/s Data to 2048Kbit/s Binary Data For Insertion into a Timeslot of a PCM Frame
Recovers Both Clock and Octet Timing. Outputs a Received Clock and Loss of Lock Signal
Performs Byte Insertion or Deletion in Response to Local Clock Slips. Provides Outputs Indicating Activity of Slip Logic
Programmable Loss of Lock Alarm (Output Inhibit/ Non-inhibit)
Glitch Free Output Data Completely Available within Supplied Timeslot Pulse

Transmitter:

Extracts 2048kbit/s Data from a PCM Frame Time-Slot and Encodes it as 64Kbit/s Data according to CCITT G.703 Requirements
Performs AMI Coding and Bipolar Violation Insertion for Octet Timing
Inhibits Bipolar Violation Insertion for Transmission of Alarm Conditions
Performs Byte Insertion or Deletion in Response to Local Clock Slips and Timeslot Changes. Provides Outputs Indicating Activity of Slip Logic

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS

When Used in Conjunction With the XR-T6164, it Forms a CCITT G.703 Compatible 64kbit/s Data Adaption Unit (DAU)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to 150°C
Operating Temperature	0°C to 70°C
Supply Voltage	4.5V to 5.5V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6166 CN	Ceramic DIP	0°C to 70°C
XR-T6166 CP	Plastic DIP	0°C to 70°C

PIN DESCRIPTIONS

Name	I/O	Pin	Description
ALARM	O	1	Alarm (active high) When active, indicates loss of received bipolar violations.
S + R	I	2	Positive AMI data to receiver (active low).
S - R	I	3	Negative AMI data to receiver (active low).
BLS	I	4	Byte Locking Supervision (active low). Causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	I	5	Receiver 2048kHz clock.
BLANK	I	6	PCMOUT data blanking (active high) When active, forces PCMOUT data to all ones. (AIS)
RXCKOUT	O	7	128kHz extracted clock.
VCC	I	8	+5V power supply.
RXCK2/ MHZ	I	9	2048kHz clock recovery signal.
TS1T	I	10	Timeslot input 1 for transmitter.
BDT	O	11	Transmitter data byte deletion flag (active high).
TS2T	I	12	Timeslot input 2 for transmitter.
T + R	O	13	Transmit positive output AMI data (active low).
T-R	O	14	Transmit negative output AMI data (active low).
TTSEL	I	15	Transmit timeslot select. When high, pin10; when low, pin 12.
ALARMIN	I	16	Alarm input (active high). When active inhibits insertion flag (active high).
TX256/KHZ	I	17	Transmitter 256kHz clock.
BIT	O	18	Transmitter data byte insertion flag (active high).
PCMIN	I	19	Transmitter PCM input.
TX2MHZ	I	20	Transmitter 2048kHz clock.
VSS	I	21	0V power supply.
CS	O	22	Clock seek (active high). Indicates loss of lock with received data.
TS1R	I	23	Timeslot input 1 for receiver.
TS2R	I	24	Timeslot input 2 for receiver.
BDR	O	25	Receive data byte deletion flag (active high).
BIR	O	26	Receive data byte insertion flag (active high).
RTSEL	I	27	Receive timeslot select. When high, pin 23; when low pin 24.
PCMOUT	O	28	Received PCM output data.

SYSTEM DESCRIPTION

Transmitter

Operation of the transmit circuit is to convert eight bit 2048Kbit/s PCM timeslot data packets into coded continuous 64Kbit/s data. PCM data is read into the transmitter using a 2048kHz local clock and timeslot signal. Transmission is controlled by 256kHz local clock. Four periods are dedicated to each bit in order to code "0" (0101) and "1"(0011). Timeslot is an envelope derived externally from the 2048kHz clock and covers eight clock pulses. A two input selector at the timeslot input allows the transmitter to be hard wired to two timeslot positions, selectable using TTSEL. Data is loaded to a storage buffer and transferred to an output shift register, controlled

by the external 256kHz signal, only after complete transmission of previously received data. Circuitry is included to delete or repeat complete words of data should skew between the clock signals occur, or during an adjustment of the timing of the timeslot signal, for example when changing from one timeslot position to another. Octet timing is maintained during these operations. Outputs are provided to indicate when a data byte is inserted or deleted. A byte repetition just occurs once; if no new PCM data is received, the transmitter outputs stay high. The BIT flag is active during the transmission of inserted data. The BDT flag is active when the transmitter receives extra data before transfer of the stored data byte to the output shift register. Under this condition, the stored data is overwritten. Coded data is alternately fed to two output pins to realize AMI coding, using an external transformer and two line drivers. Transmission of octet timing is performed by feeding the seventh and eighth data bits in each word to the same output. This function may be inhibited by setting ALARMIN active to transmit and alarm condition.

Receiver

Receiver operation is to take coded continuous 64Kbit/s input and extract data in the form required for insertion into a 2048Kbit/s PCM timeslot, under control of an external timeslot signal. A 128kHz clock is derived from the received data and used to perform decoding of the input signal. This signal is made available as the output RXCKOUT. If lock is lost with received data the clock recovery circuit enters a seek mode, increasing the speed of the internal clock to reduce the time required to regain lock. Hence, in clock seek mode the output CS is active. Bipolar violations, used to identify bit 1 in the input signal are used to synchronize circuit operation for octet timing. In the absence of violations, for example when receiving a transmitted alarm condition, the circuit will continue to operate in synchronization with respect to the last received violation. Under this condition the received signal PCMOUT (Received PCM output data) is held high indicating AIS. This function may be inhibited using BLS, and the output set to all ones if required using the BLANK input. ALARM goes high after eight consecutive violations are missed. To accommodate differences between the remote (transmitting) and local clock rate, slip control logic is included in the receiver design. Under slow local clock conditions data will be deleted periodically, while under fast conditions the last output PCM data will be repeated. Octet timing is maintained during these operations. Outputs are provided to indicate when a data byte is inserted or deleted. The BIR flag is active when PCMOUT data is a repetition of the previous data, The BDR flag is active when the receiver deletes a complete received data octet. Data appearing at PCMOUT is arranged to be completely framed by the read timeslot signal and is guaranteed glitch free. A two input multiplexer at the timeslot input allows the receiver to be hard wired at two timeslot positions, selectable using RTSEL.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Logic 1	V_{IH}	2.4			V	
Logic 0	V_{IL}			0.4	V	
Supply	V_{DD}	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = 5V \pm 5\%$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Supply Current	I_{DD}		500		µA	
Input Leakage	I_{IL}			1	µA	
O/P Low Current	I_{OL}		2		mA	$V_{OL} < 0.4V$
O/P High Current	I_{OH}		2		mA	$V_{OH} > 2.4V$

AC ELECTRICAL CHARACTERISTICS

PRELIMINARY Test Conditions: V_{CC} = 5V ± 10%, T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
GENERAL						
tr, tf	Output rise/fall time			20	nS	
RECEIVER						
tRS	TS rising edge to RX2MHz set up	0		TRXL −100	nS	Figure 5
tRH	TS falling edge to RX2MHz hold	0		TRXL −100	nS	Figure 5
tDRS	PCMOUT edge to RX2MHz set up			10	nS	Figure 5
tDRH	PCMOUT edge to RX2MHz			10	nS	Figure 5
tPW	PCMOUT pulse width		488		nS	Figure 5
tRXH	RX2MHz high time		244		nS	±100ppm
tRXL	RX2MHz low time		244		nS	±100ppm
tBDRH	BDR high time	488			nS	±100ppm
tBIRH	BIR high time		3.9		µS	
tRCKP	RXCKOUT period		7.8		µS	Figure 4
tRCKS	RXCKOUT active edge to received data edge		1.95		µS	Figure 4
TRANSMITTER						
tTS	TS rising edge to TX2MHz set up	20		TTXL −100	nS	Figure 6
tTH	TS falling edge to TX2MHz hold	0		TTXL −100	nS	Figure 6
tDS	PCMIN edge to TX2MHz set up	100			nS	Figure 6
tDH	PCMIN edge to TX2MHz hold	100			nS	Figure 6
tTXH	TX2MHz high time		244		nS	±100ppm Figure 6
tTXL	TX2MHz low time		244		nS	Figure 6
tKXH	TX256kHz high time		1.95		µS	±100ppm
tKXL	TX256kHz low time		1.95		µS	±100ppm
tBDTH	BDT high time	488			nS	Figure 3
tBITH	BIT high time	125			µS	Figure 3
tALH	ALARMIN high time	15.6			µS	Figure 3

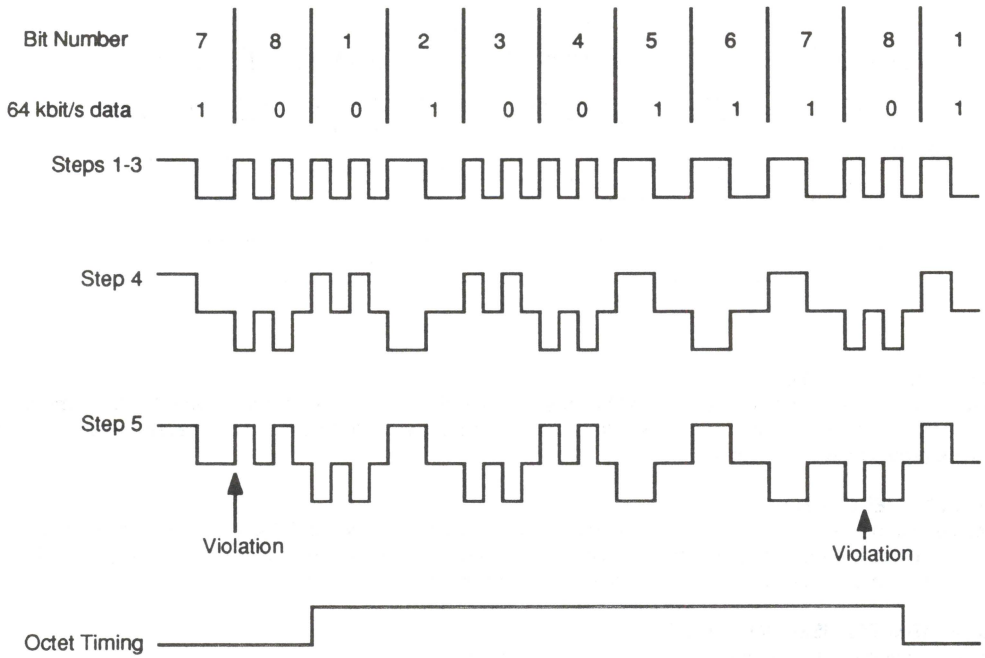


Figure 1. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

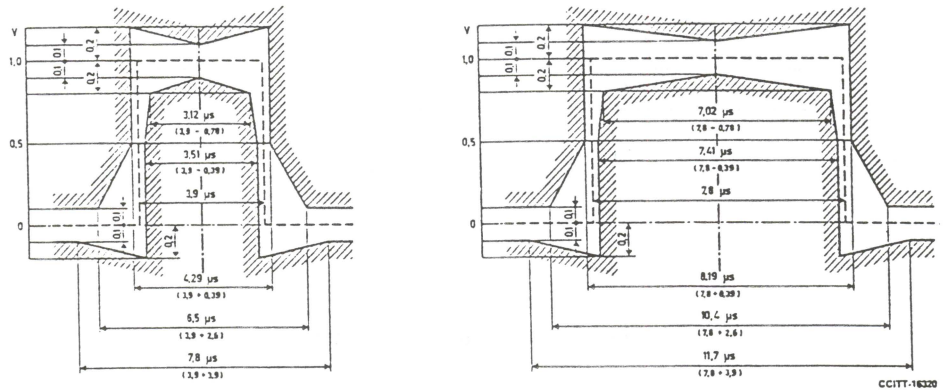
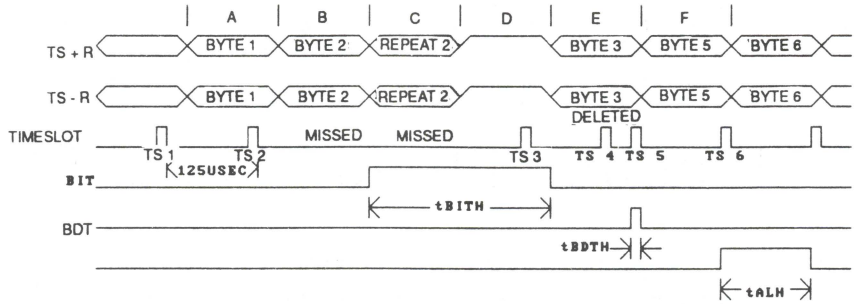


Figure 2. Pulse Masks of the 64 Kbit/s Codirectional Interface



NOTE 1: BYTE INSERTION
Transmitter word "B" is a repetition of word "A" because no new data was received during word "A" time frame. Output bit transitions high on the first edge of inserted data. Transmission in word "C" is inhibited because no new data was received in the previous two word time frame.

NOTE 2: BYTE DELETION
Data received during word "C" commences transmission at bit position 1 of word "D" with respect to the last transmitted frame "B". BDT flag is sent high during this word due to the occurence of two time slot pulses, BDT goes high immediately the second time slot pulse is received and remains high until the start bit of the next word.

NOTE 3: ALARM TRANSMISION (ALARM IN)
During active period of ALARMIN signal octet violation suppression occurs (word "F")

Figure 3. Transmitter Byte Insertion and Deletion

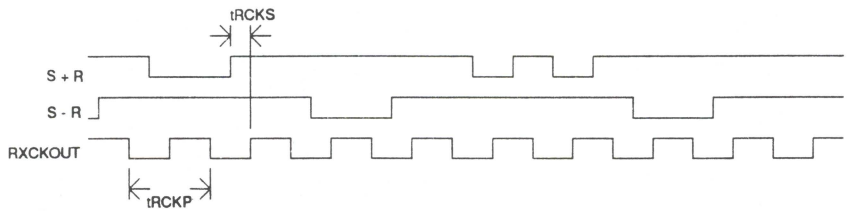


Figure 4. Extracted Clock Timing

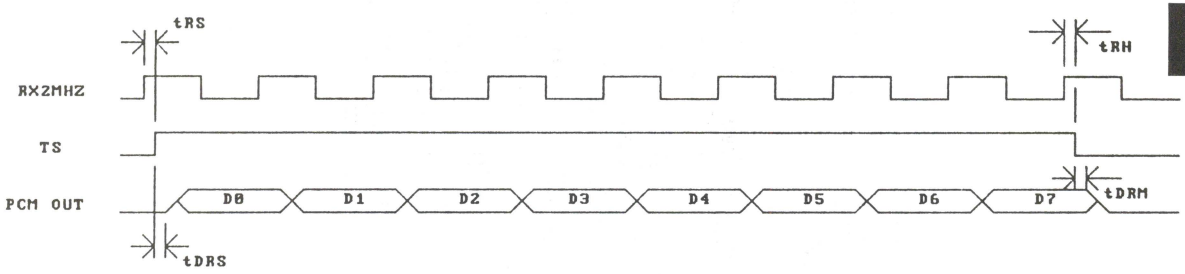


Figure 5. Receiver Time Slot Detail

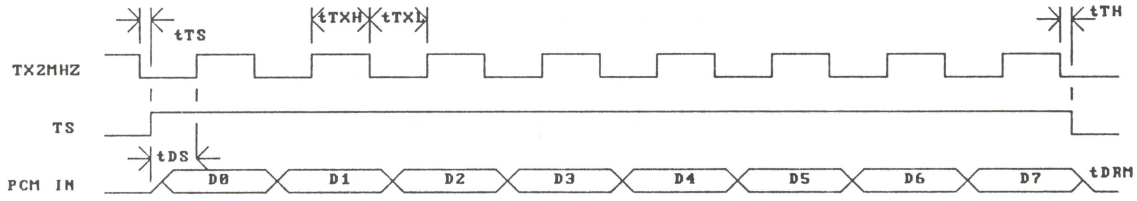


Figure 6. Transmit Time Slot

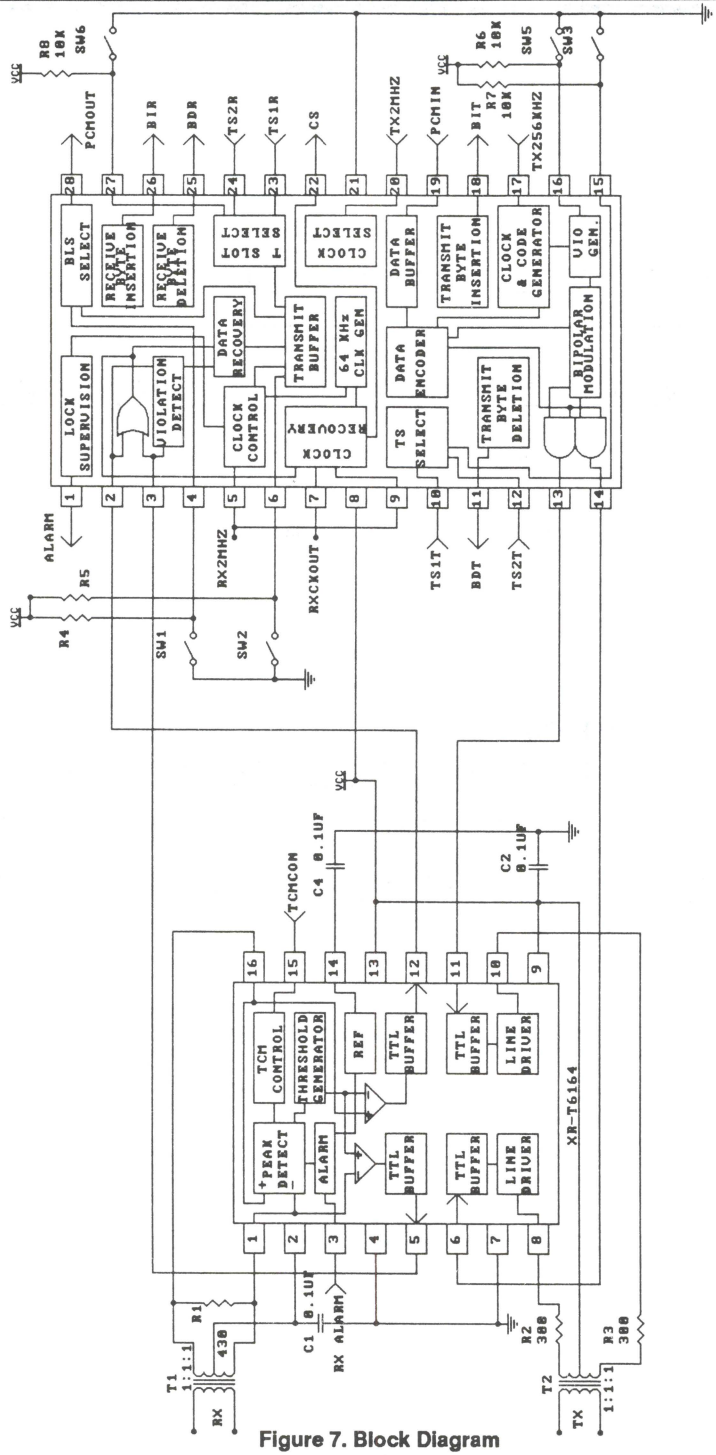


Figure 7. Block Diagram

DS3 / SONET STS-1 Integrated Line Receiver

GENERAL DESCRIPTION

The XR-T7295 DS3/SONET STS-1 Integrated Line Receiver is a fully integrated receive interface that terminates a bipolar DS3 (44.736 MBPS) or SONET (51.84 MBPS) signal transmitted over coaxial cable.

The device also provides the functions of receive equalization (optional), automatic-gain control (AGC), clock-recovery and data retiming, loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual-rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable distances of 0 to 450ft. from the cross-connect frame to the device. The receive input has a variable input sensitivity control, providing three different sensitivity settings. High input sensitivity allows for significant amounts of flat loss within the system. Figure 1 shows the block diagram of the device.

The XR-T7295 device is manufactured by using linear CMOS technology and is packaged in a 20-pin, plastic DIP or 20-pin, plastic SOJ package for surface mounting.

Two versions of the XR-T7295 are available, one for DS3 and one for STS-1 operation (see ordering information section) an input reference clock at 44.736MHz or 51.84MHz provides the frequency reference for the device.

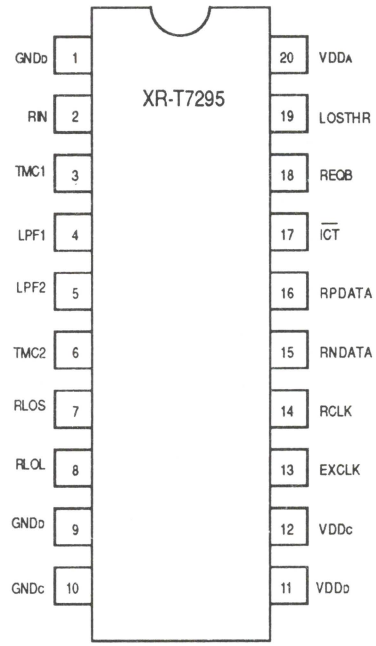
FEATURES

Fully Integrated Receive Interface for DS3 and STS-1 Rate Signals
Integrated Equalization (optional) and Timing Recovery
Loss-of-Signal and Loss-of-Lock Alarms
Variable Input Sensitivity Control
5V Power Supply

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.5V to +6.5V
Storage Temperature	-65°C to +150°

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Packages	Operating Temperature
XR-T7295TIP	Plastic DIP	-40°C to+85°C
XR-T7295TIW	SOJ	-40°C to+85°C
XR-T7295SIP	Plastic DIP	-40°C to+85°C
XR-T7295SOJ	SOJ	-40°C to+85°C

APPLICATIONS

Interface to DS-3 or E3 Networks
Digital Cross-Connect Systems
CSU/DSU Equipment
PCM Test Equipment
Fiber Optic Terminals

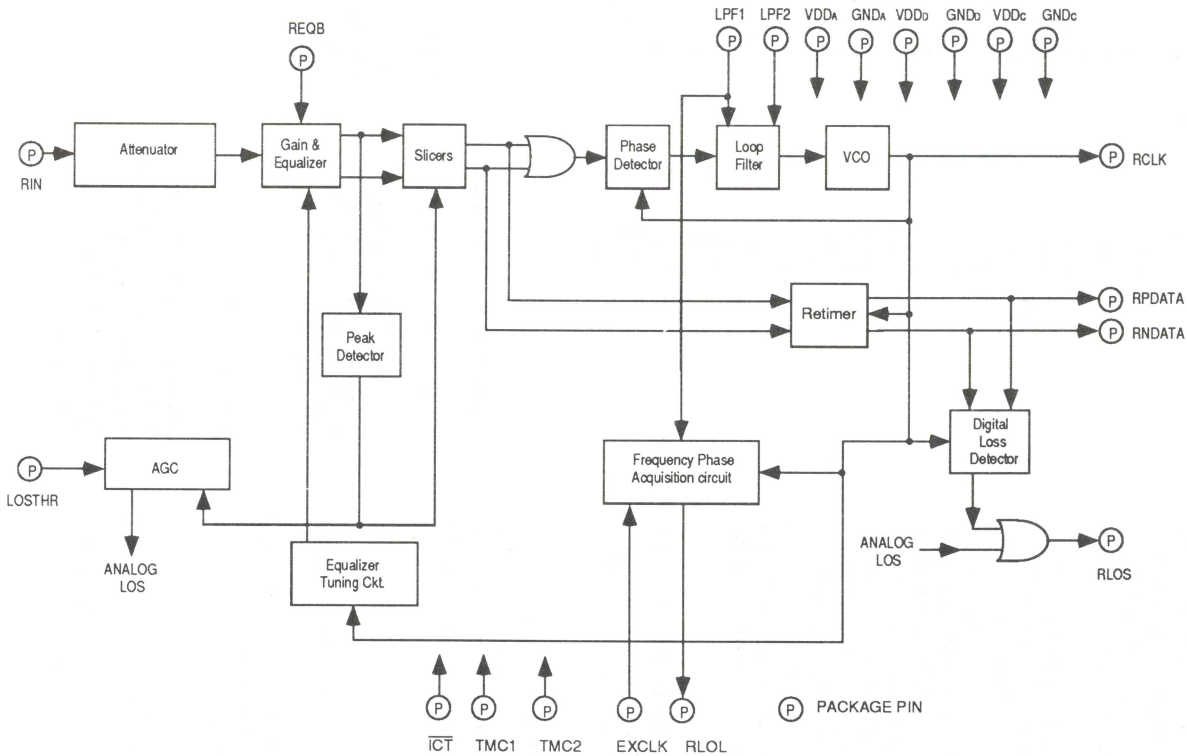


Figure 1. Block Diagram

PIN #	SYMBOL	TYPE	PIN DESCRIPTION
1	GND_A	—	**Analog Ground.**
2	RIN	I	**Receive Input.** Analog receive input. This pin is internally biased.
3,6	TMC1-TMC2	I	**Test Mode Control 1 and 2.** Internal test modes are enabled within the device by using TMC1 and TMC2. Users must tie these pins to the ground plane.
4,5	LPF1-LPF2	I	**PLL Filter 1 and 2.** An external capacitor (0.1µF ± 20%) is connected between these pins.
7	RLOS	O	**Receive Loss-of-Signal.** This pin is set high on loss of the data signal at the receive input.
8	RLOL	O	**Receive PLL Loss-of-Lock.** This pin is set high on loss of PLL frequency lock.
9	GND_D	—	**Digital Ground for PLL Clock.** Ground lead for all circuitry running synchronously with PLL clock.
10	GND_C	—	**Digital Ground for EXCLK.** Ground lead for all circuitry running synchronously with EXCLK.
11	VDD_D	—	**5V Digital Supply (±10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	VDD_C	—	**5V Digital Supply (±10%) for EXCLK.** Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock.** A valid DS3 (44.736MHz±100ppm) or STS-1 (51.84MHz ± 100ppm) clock must be provided at this input. The duty cycle of EXCLK, referenced to VDD /2 levels, must be 40%-60%. The EXCLK frequency determines the operation frequency of the device.
14	RCLK	O	**Receive Clock.** Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data.** Negative pulse data output to the terminal equipment.
16	RPDATA	O	**Receive Positive Data.** Positive pulse data output to the terminal equipment.
17	$\overline{ICT}$	I	**Output In-Circuit Test Control** (Active-Low). If $\overline{ICT}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-Impedance state to allow for in-circuit testing. There is an internal pull-up on this pin.
18	REQB	I	**Receive Equalization Bypass.** A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-Signal Threshold Control.** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD at LOSTHR.
20	VDD_A	—	**5 V Analog Supply (±10%).**

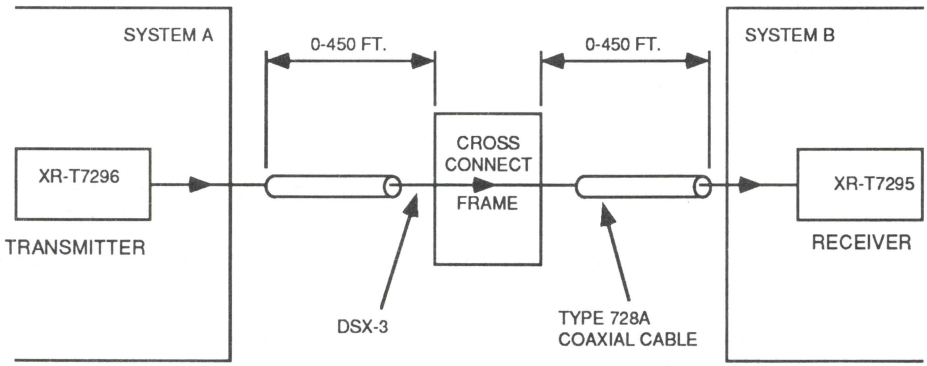


Figure 2. Application Diagram

SYSTEM DESCRIPTION

Receive Path Configurations

In the receive signal path (see Figure 1), the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB = 1. The equalizer bypass option allows easy interfacing of the XR-T7295 device into systems already containing external equalizers. Figure 3 illustrates the receive path options.

In Case 1, the signal from the DSX-3 cross-connect feeds directly into RIN. In this mode, the user should set REQB = 0, engaging the equalizer in the data path. Table 2 and the following sections describe the receive signal requirements.

In Case 2, external line build-out (LBO) and equalizer networks precede the XR-T7295 device. In this mode, the signal at RIN is already equalized, and the on-chip filters should be bypassed by setting REQB=1. The signal at RIN must meet the amplitude limits described in Table 2.

In applications where the XR-T7295 device is used to monitor DS3 transmitter outputs directly, the receive equalizer should be bypassed. Again, the signal at RIN must meet the amplitude limits described in Table 2.

Minimum signals are for SOJ devices. Due to increased package parasitics, add 5 dB to all table values for DIP devices.

Maximum input amplitude under all conditions is 850 mV pk.

Although system designers typically use power in dBm to describe input levels, the XR-T7295 responds to peak input signal amplitude, Therefore, the XR-T7295 input signal limits are given in mV pk. Conversion factors are as follows:

At DSX3: 390mV pk $\simeq$ 0dBm
At DSX3 + 450 ft. of cable 310 mV pk $\simeq$ 0 dBm.

DATA RATE	REQB	LOSTHR	MINIMUM SIGNAL	UNIT
DS3	0	0	80	mV pk
		$V_{DD}/2$	60	mV pk
		V_{DD}	40	mV pk
	1	0	80	mV pk
		$V_{DD}/2$	80	mV pk
		V_{DD}	80	mV pk
STS-1	0	0	110	mV pk
		$V_{DD}/2$	80	mV pk
		V_{DD}	60	mV pk
	1	0	110	mV pk
		$V_{DD}/2$	110	mV pK
		V_{DD}	110	mV pk

Table 2. Receive Input Signal Amplitude Requirements

DS3 SIGNAL REQUIREMENTS AT THE DSX

Pulse characteristics are specified at the DSX-3, which is an interconnection and test point referred to as the cross-connect (see Figure 2). The cross-connect exists at the point where the transmitted signal reaches the distribution frame jack. Table 3 lists the signal requirements. Currently, two isolated pulse template requirements exist: the ACCUNET T45 pulse template (see Table 4 and Figure 4) and the G.703 pulse template (see Table 5 and Figure 5) Tables 4 and 5 give the associated boundary equations for the templates. The XR-T7295 correctly transmitted signal that meets one of these templates at the cross-connect.

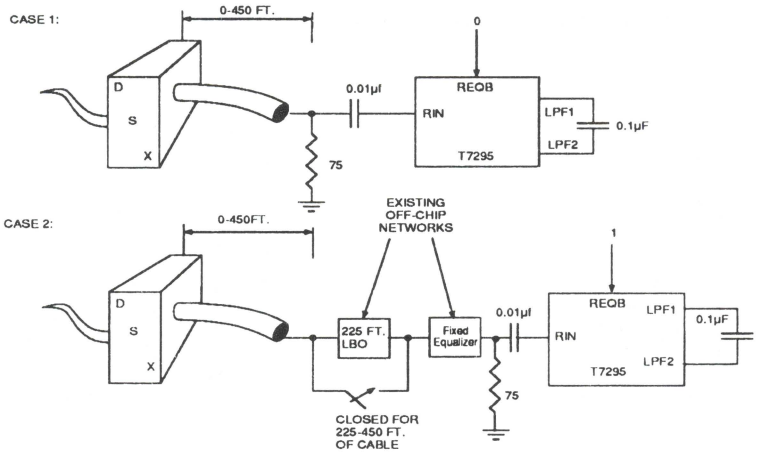


Figure 3. Receiver Configurations

PARAMETER	SPECIFICATION
Line Rate	44.736 MBPS ± 20 ppm
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω ± 5%
Pulse Shape	An isolated pulse must fit the template in Figure 4 or 5.* The pulse amplitude may be scaled by a constant factor to fit the template. The pulse amplitude must be between 0.36 Vpk and 0.85 Vpk , measured at the center of the pulse.
Power Levels	For and all 1s transmitted pattern, the power at 22.368 ± 0.002 MHz must be -1.8 to +5.7 dBm, and the power at 44.736 ± .002 MHz must be -21.8 dBm to -14.3 dBm.√ †

* *The pulse template proposed by G.703 standards is shown in Figure 5 and specified in Table 5. The proposed G.703 standards further state that the voltage in a time slot containing a 0 must not exceed ± 5% of the peak pulse amplitude, except for the residue of preceding pulses.*

√ *The power levels specified by the proposed G.703 standards are identical except that the power is to be measured in 3 kHz bands.*

† *The all-1s pattern must be a pure all-1s signal, without framing or other control bits.*

Table 3. DSX-3 Interconnection Specification

LOWER CURVE		UPPER CURVE	
Time	Equation	Time	Equation
$T \leq -0.36$	0	$T \leq -0.68$	0
$-0.36 \leq T \leq +0.28$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.18}\right]\right]$	$-0.68 \leq T \leq +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.34}\right]\right]$
$0.28 \leq T$	$0.11e^{-3.42(T-0.3)}$	$0.36 \leq T$	$0.05 + 0.407e^{-1.84(T-0.36)}$

Table 4. DSX-3 Pulse Template Boundaries for ACCUNET T45 Standards (See Figure 4.)

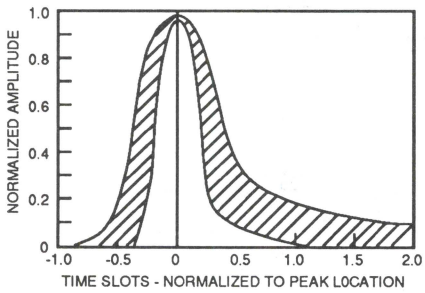


Figure 4. DSX-3 Isolated Pulse Template for ACCUNET T45 Standards

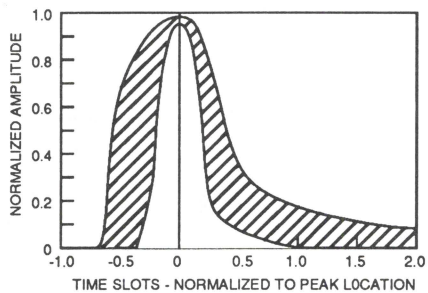


Figure 5. DSX-3 Isolated Pulse Template for G.703 Standards

LOWER CURVE		UPPER CURVE	
Time	Function	Time	Function
$T \leq -0.36$	0	$T \leq -0.65$	0
$-0.36 \leq T \leq +0.28$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.18}\right]\right]$	$-0.65 \leq T \leq +0$	$1.05\left[1 - e^{-4.6(T + 0.65)}\right]$
$0.28 \leq T$	$0.11e^{-3.42(T-0.3)}$	$0 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left[1 + \frac{T}{0.34}\right]\right]$
—	—	$0.36 \leq T$	$0.05 + 0.407e^{-1.84(T-0.36)}$

Table 5. DSX-3 Pulse Template Boundaries for G.703 Standards (See Figure 5.)

STS-1 SIGNAL REQUIREMENTS AT THE STSX

For STS-1 operation, the cross-connect is referred at the STSX-1. Table 6 lists the signal requirements at the STSX-1. Instead of the DS3 isolated pulse template, an eye diagram mask is specified for STS-1 operation (TA-TSY-000253). The XR-T7295 correctly decodes any transmitted signal that meets the mask shown in Figure 6 at the STSX-1.

PARAMETER	SPECIFICATION
Line Rate	51.84 MBPS
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω ± 5%
Power Levels	A wide-band power level measurement at the STSX-1 interface using a low-pass filter with a 3 dB cutoff frequency of at least 200 MHz is within -2.7 dBm and 4.7 dBm.

Table 6. STSX-1 Interconnection Specification

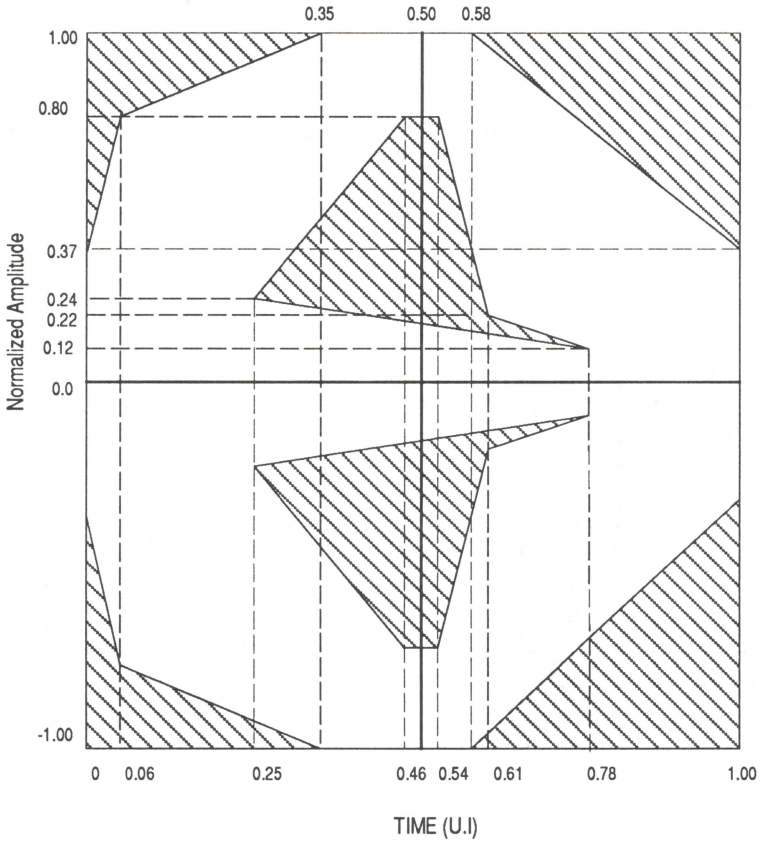


Figure 6. STSX-1 Eye Diagram Mask

LINE TERMINATION AND INPUT CAPACITANCE

The recommended receive termination is shown in Figure 3. The 75 Ω resistor terminates the coaxial cable with its characteristic Impedance. The 0.01 µF capacitor to RIN couples the signal into the receive input without disturbing the internally generated dc bias level present on RIN. The input capacitance at the RIN pin is 2.8 pF (SOJ package) and 3.6 pF (DIP package).

LOSS LIMITS FROM THE DSX-3 TO THE RECEIVE INPUT.

The signal at the cross-connect may travel through a distribution frame, coaxial cable, connectors, splitters, and backplanes before reaching the XR-T7295 device. This section defines the maximum distribution frame and cable loss from the cross-connect to the XR-T7295 input.

The distribution frame jack may introduce 0.6 ± 0.55 dB of loss. This loss may be any combination of flat or shaped (cable) loss.

The maximum cable distance between the point where the transmitted signal exits the distribution frame jack and the XR-T7295 device is 450 ft. (see Figure 2). The coaxial cable (Type 728A) used for specifying its distance limitation has the loss and phase characteristics shown in Figures 7 and 8. Other cable types also may be acceptable if distances are scaled to maintain cable loss equivalent to Type 728A cable loss.

TIMING RECOVERY

Figure 3 shows the connection to an external 0.1 µF capacitor at the LPF1/LPF2 pins. This capacitor is part of the PLL filter. A non-polarized, low-leakage capacitor should be used. A ceramic capacitor with the value 0.1 µF ± 20% is acceptable.

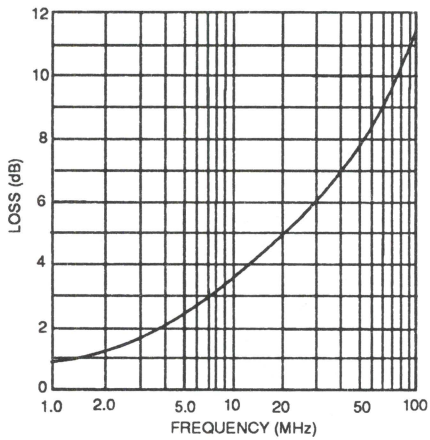


Figure 7. Loss Characteristic of 728A Coaxial Cable (450 ft.)

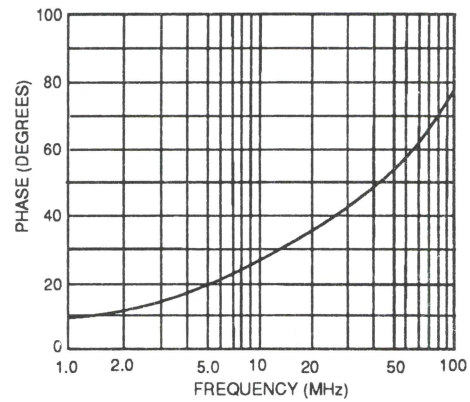


Figure 8. Phase Characteristic of 728A Coaxial Cable (450 ft.)

OUTPUT JITTER

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The next section discusses the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources within the XR-T7295 device or noise sources that are coupled into the device through the power supplies and data pattern dependent jitter due to misequalization of the input signal, all create jitter on RCLK. The magnitude of this internally generated jitter is a function of the PLL bandwidth, which in turn is a function of the input 1s density. For higher 1s densities, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. Figure 9 shows the suggested bypassing network, and Table 7 lists the typical generated jitter performance achievable with this network.

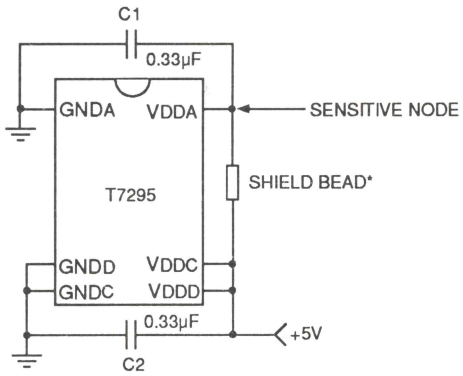
PARAMETER	TYP	MAX	UNIT
Generated Jitter*			
All-1s pattern	1.0	-	ns peak-to-peak
Repetitive 100 pattern	1.5	-	ns peak-to-peak
Jitter Transfer Characteristic••			
Peaking	0.05	0.1	dB
f 3dB	205	-	kHz

** Repetitive input data pattern at nominal DSX-3 level with VDD = 5V TA = 25°C.*
•• Repetitive 100 input at nominal DSX-3 level with VDD = 5V, TA = 25°C.

Table 7. Generated Jitter and Jitter Transfer Characteristics

JITTER TRANSFER CHARACTERISTIC

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. Table 7 shows Important jitter transfer characteristic parameters. Figure 10 also shows a typical characteristic, with the operating conditions as described in Table 7. Although standard documents do not specify jitter transfer characteristic requirements, the XR-T7295 information is provided here to assist in evaluation of the device.



**Recommended shield beads are the Fair-Rite 2643000101 or the Fair-Rite 2743019446 (surface mount).*

Figure 9. Recommended Power Supply Bypassing Network

JITTER ACCOMMODATION

Under all allowable operating conditions, the jitter accommodation of the XR-T7295 device exceeds all system requirements for error-free operation (BER<$1e^{-9}$). The typical (V_{DD} = 5V, T = 25°C, DSX-3 nominal signal level) jitter accommodation for the XR-T7295 is shown in Figure 11.

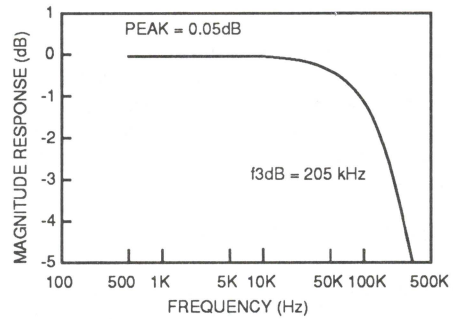
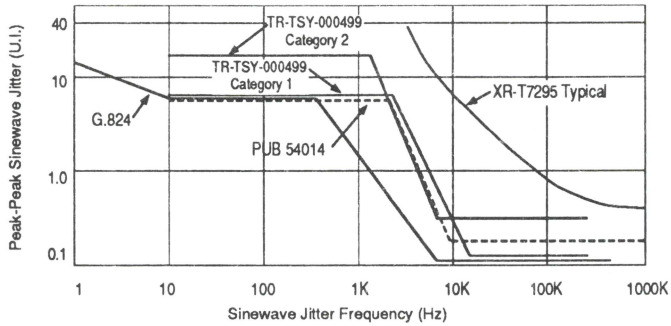


Figure 10. Typical PLL Jitter Transfer Characteristic



XR-T7295 Typical	
Jitter Frequency (Hz)	Jitter Amplitude (U.I.)
5k	10
10k	5
60k	1
300k	0.5
1M	0.4

Figure 11. Input Jitter Tolerance at DSX-3 Level

FALSE-LOCK IMMUNITY

False-lock is defined as the condition where a PLL recovered clock obtains stable phase-lock at a frequency not equal to the incoming data rate. The XR-T7295 device uses a combination frequency/phase-lock architecture to prevent false-lock. An on-chip frequency comparator continuously compares the EXCLK reference to the PLL clock. If the frequency difference between the EXCLK and PLL clock exceeds approximately ± 0.5%, correction circuitry forces re-acquisition of the proper frequency and phase.

ACQUISITION TIME

If a valid input signals is assumed to be already present at RIN, the maximum time between the application of device power and error-free operation is 20 ms. If power has already been applied, the interval between the application of valid data and error-free operation is 4 ms.

LOSS-OF-LOCK DETECTION

As stated above, the PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK frequency. The acquisition circuit also monitors the retimed data to detect possible phase-lock which is 180° out of a normal phase alignment. The RLOL alarm is activated if either or both of the following conditions exist:

- The difference between the PLL clock and the EXCLK frequency exceeds approximately ± 0.5%.
- Seven consecutive 0s are detected in the retimed data (indicates possible lock which is 180° out of normal alignment).

A high RLOL output indicates that the acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

LOSS-OF-SIGNAL DETECTION

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates LOS has occurred.

ANALOG DETECTION

The analog LOS detector monitors the peak input signal amplitude.RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of signal threshold defined in Table 8. The RLOS low-to-high transition (input signal loss) occurs at a level typically 1.0 dB below the high-to-low transition level. The hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allowing for system detection of a LOS condition without the use of an external alarm latch.

DATA RATE	REQB	LOSTHR	MIN. THRESHOLD	MAX. THRESHOLD	UNIT
DS3	0	0	60	220	mV pk
		$V_{DD/2}$	40	145	mV pk
		V_{DD}	25	90	mV pk
	1	0	45	175	mV pk
		$V_{DD/2}$	30	115	mV pk
		V_{DD}	20	70	mV pk
STS-1	0	0	75	275	mV pk
		$V_{DD/2}$	50	185	mV pk
		V_{DD}	30	115	mV pk
	1	0	55	220	mV pk
		$V_{DD/2}$	35	145	mV pk
		V_{DD}	25	90	mV pk

Lower threshold is 1.5 dB below upper threshold.

Table 8. Analog Loss-of-Signal Thresholds

Note: *The RLOS alarm is an indication of the presence of an input signal, not a bit error rate indication. Table 2 gives the minimum input amplitude needed for error free operation (BER < $1e^{-9}$) Independent of the RLOS state, the device will attempt to recover correct timing data. The RLOS low-to-high transition typically occurs 1dB below the high-tolow transition.*

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin. Setting LOSTHR = V_{DD} provides the lowest loss-of-signal threshold; LOSTHR = V_{DD} /2 (can be produced using between V_{DDD} and GND_D) provides an intermediate threshold; and LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at powerup and must not be changed during operation.

DIGITAL DETECTION

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 $\pm$ 32 or more consecutive 0s occur in the receive data stream. The alarm goes low when at least ten 1s occur in a string of 32 consecutive bits. This hysteresis prevents RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles.

RECOVERED CLOCK AND DATA TIMING

Table 10 and Figure 12 summarize the timing relationships between the high-speed logic signals RCLK, RPDATA, and RNDATA. All duty cycle and timing relationships are referenced to VDD/2 threshold level. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at RIN creates a high level on RPDATA and a low level on RNDATA. A negative pulse at the input creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

IN-CIRCUIT TEST CAPABILITY

When pulled low, the $\overline{ICT}$ pin forces all digital output buffers (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) to be placed in a high output impedance state. This feature allows in-circuit testing to be done on neighboring devices without concern for XR-T7295 device buffer damage. When forced high, the $\overline{ICT}$ pin does not affect device operation. An internal pull-up device (nominally 50 kΩ) is provided on this pin; therefore, users can leave this pin floating for normal operation. In-circuit test equipment can pull ICT low during in-circuit testing without damaging the device. This is the only pin for which Internal pull-up/pull-down is provided.

LOGIC INTERFACE CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $V_{DD} = 5V \pm 10\%$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Voltage					
Low	VIL	—	GNDD	0.5	V
High	VIH	—	VDDD-0.5	VDDD	V
Output Voltage					
Low	VOL	-5.0mA	GNDD	0.4	V
High	VOH	5.0mA	VDDD- 0.5	VDDD	V
Input Capacitance	CI	—	10	pF	
Load Capacitance	CL	—	10	pF	
Input Leakage	IL	-0.5 to VDD + 0.5V (all input pins except 2 and 17)	-10	+10	µA
		0 V (pin 17)	0.02	0.5	mA
		VDD (pin 2)	5	8	mA

Table 9. Logic Interface Characteristic

TIMING CHARACTERISTICS All timing characteristics are measured with 10pF loading

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tRCH1RCH2	Clock Rise Time (10% - 90%)	-	-	3.5	ns
tRCL2RCL1	Clock Fall Time (10% - 90%)	-	-	2.5	ns
tRDVRCL	Receive Data Set-up Time	5.5	-	-	ns
tRCLRDX	Receive Data Hold Time	8.5	-	-	ns
tRCHRDV	Receive Propagation Delay	0.6	-	3.0	ns
-	Clock Duty Cycle	45	50	55	%

Table 10. System Interface Timing Characteristics (See Figure 14.)

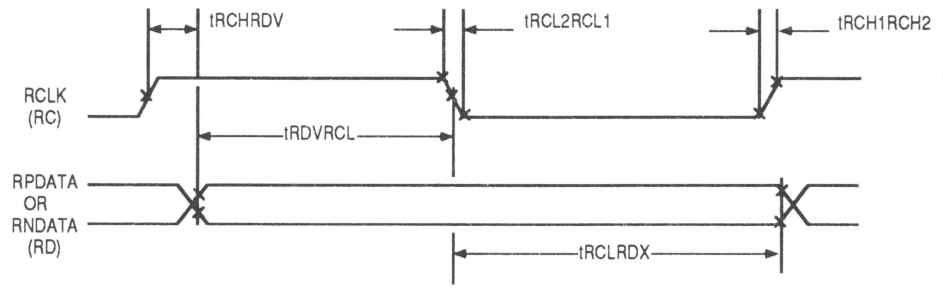


Figure 12. Timing Diagram for System Interface

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} = 5V ± 10%
Typical values are for V_{DD} = 5.0 V, 25°C, and random data. Maximum values are for V_{DD} = 5.5V all 1s data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Current	IDD				
DS3					
REQB = 0		-	82	106	mA
REQB = 1		-	79	103	mA
STS-1					
REQB = 0		-	87	111	mA
REQB = 1		-	83	108	mA

BOARD LAYOUT CONSIDERATIONS

Power Supply Bypassing

Figure 9 Illustrates the recommended power supply bypassing network. A 0.1 µF capacitor bypasses the digital supplies. The analog supply V_{DDA} is bypassed by using a 0.1 µF capacitor and a shield bead that removes significant amounts of that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good quality, high-frequency (low lead Inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.

Receive Input

The connections to the receive Input pin, RIN, must be carefully considered. Noise-coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the XR-T7295 input directly degrades the signal-to-noise ratio of the Input signal.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible. The LPF1 and LPF2 pins are adjacent, allowing for short lead lengths with no crossover's to the external capacitor. Noise-coupling into the LPF1 and LPF2 pins may degrade PLL performance.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting.

COMPLIANCE SPECIFICATIONS

• Compliance with *AT&T Publication54014, "ACCUNET* ® T45 Service Description and Interface Specifications," June 1987.

• Compliance with *ANSI Standard T1.102*-1989, " Digital Hierarchy - Electrical Interfaces, " 1989.

• Compliance with *Compatibility Bulletin 119,* "Interconnection Specification for Digital Cross-Connects," October 1979.

• Compliance with *CCITT Recommendations G.703 and G.824,* 1988.

• Compliance with *TR-TSY-000499,* "Transport Systems Generic Requirements (TSGR): Common Requirements, " December 1988.



NOTES



Advanced Information

DS3 / STS - 1 Integrated Line Transmitter

GENERAL DESCRIPTION

The XR-T7296 is a fully integrated PCM Line Driver IC intended for T3 (44.736MBPS) or E3 (34.368MBPS) applications. It can also be used for transmitting SONET STS-1(51.84 MBPS) signals over coaxial cable. The IC is designed to complement the XR-T7295 DS3/SONET STS-1 Integrated Line Receiver. It converts input clock, and unipolar POS and NEG data into AMI pulses according to AT&T Technical Advisory No.34 or CCITT G.703 recommendations.

The device provides B3ZS(T3) or HDB3(E3) encoding functions for data to be transmitted to the line. A complimentary decoder circuit is also included in the chip for decoding received signals from an external line receiver. Both encoder and decoder functions can be disabled independently through external control pins. In the receive direction, coding errors and bipolar violations will be detected and flagged at an output pin.

On-chip pulse shaper circuitry eliminates normally required external components for line equalization to meet the cross-connect template. For system level trouble-shooting and testing, both transmit and receive loop-backs are possible with the built-in loop-back circuit.

The XR-T7296 is manufactured using BiCMOS technology and is packaged in a 28-pin PDIP or SOJ packages. The device requires a single 5V power supply and dissipates a maximum power of 700mW.

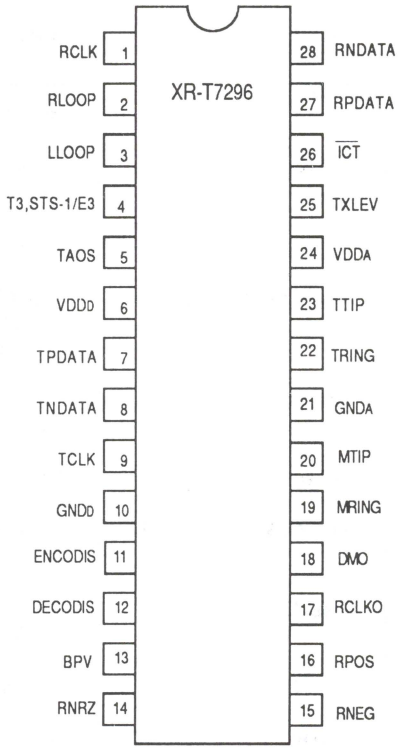
FEATURES

Fully Integrated Transmit Interface for T3/STS-1 or E3
Integrated Pulse Shaping Circuit
Compliance with Compatibility Bulletin 119
Compliance with CCITT Recommendations G.703 & G.824
Built-in B3ZS/HDB3 Encoder and Decoder
Remote and Local Loop-back Functions
Single 5 V Power Supply

APPLICATIONS

Interface for SONET, DS-3 and E3 Network Equipment
Digital Cross-Connect Systems
CSU/DSU Equipment
PCM Test Equipment
Fiber Optic Terminals

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T7296IP	Plastic DIP	-40°C to +85°C
XR-T7296IW	SOJ	-40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.5 to +6.5V
Storage Temperature	-65°C to 150°C
Voltage at any pin	-0.5V to VDD +0.5V
Power Dissipation	800mW
Input Voltage (any pin)	-0.5V to VDD + 0.5V
Input Current (any pin)	10mA

PIN DESCRIPTION

PIN	SYMBOL	TYPE	DESCRIPTION
1	RCLK	I	**Receive Clock Input.** Input sampling clock for RPDATA and RNDATA.
2	RLOOP	I	**Remote Loop-Back.** A high on this pin causes RPDATA and RNDATA to be transmitted to the line using RCLK.
3	LLOOP	I	**Local Loop-Back.** A high on this pin causes TPDATA and TNDATA to pass through the encoder and output at RPOS and RNEG respectively. Forcing LLOOP and RLOOP high simultaneously will set the device into test mode.
4	T3,STS-1/$\overline{E3}$	I	**T3,STS-1 or $\overline{E3}$ Select Pin.** A high on this pin selects T3 or STS-1 operation and sets the encoder and decoder in B3ZS mode. A low selects E3 and sets the encoder and decoder in HDB3 mode.
5	TAOS	I	**Transmit All Ones Select.** A high on this pin causes a continuous AMI all ones to be transmitted to the line.The frequency is determined by TCLK.
6	VDDD	—	**5 V Digital Supply(+/-5%)** for all logic circuitry.
7	TPDATA	I	**Transmit Positive Data.** TPDATA is sampled on the falling edge of TCLK. Pin 7 and pin 8 can be tied together for binary input signals.
8	TNDATA	I	**Transmit Negative Data.** TNDATA is sampled on the falling edge of TCLK. Pin 7 and pin 8 can be tied together for binary input signals.
9	TCLK	I	**Transmit Clock for TPDATA and TNDATA.** 50% +/- 5% duty cycle.
10	GNDD	—	**Digital Ground** for all logic circuitry.
11	ENCODIS	I	**Encoder Disable.** A high on this pin disables B3ZS or HDB3 encoding functions. This pin must be set high if TPDATA and TNDATA have already been encoded.
12	DECODIS	I	**Decoder Disable.** A high on this pin disables B3ZS or HDB3 decoding functions, unless overidden by TAOS request.
13	BPV	O	**Bipolar Violation Output.** This pin goes high for one bit period when a bipolar violation or coding error is detected in the received signal.
14	RNRZ	O	**Receive Binary Data.** Signal on this pin is the OR-output of RPOS and RNEG.
15	RNEG	O	**Receive Negative Data.** This signal is the decoded version of RNDATA.

PIN DESCRIPTION (*continued*)

PIN	SYMBOL	TYPE	DESCRIPTION
16	RPOS	O	**Receive Positive Data.** This signal is the decoded version of RPDATA.
17	RCLKO	O	**Receive Clock Output.** This signal is the inverted version of RCLK.
18	DMO	O	**Driver Monitor Output.** If no transmitted AMI signal is present on MTIP and MRING for 128 +/-32 TCLK clock periods. DMO goes high until the next AMI signal is detected.
19	MTIP	I	**Monitor Ring Input.** AMI signal from TRING can be connected to this pin for Line Driver failure detection. Internally pulled high.
20	MRING	I	**Monitor Tip Input.** AMI signal from TTIP can be connected to this pin for Line Driver failure detection. Internally pulled high.
21	GNDA	—	**Analog Ground** for analog circuitry.
22	TRING	O	**Transmit Ring Output.** Transmit AMI signal is driven to the line via a 1:1 transformer from this pin.
23	TTIP	O	**Transmit Tip Output.** Transmit AMI signal is driven to the line via a 1:1 transformer from this pin.
24	VDDA	—	**5 V Analog Supply(+/- 5%)** for analog circuitry.
25	TXLEV	I	**Transmit Level Select.** The output signal amplitude at TTIP and TRING can be varied by setting this pin high or low. When the cable length is greater than 225 ft. TXLEV should be set high. When it is below 225 ft, it should be set low.
26	$\overline{\text{ICT}}$	I	**In-Circuit Testing.** A low at this pin causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing.
27	RPDATA	I	**Receive Positive Data.** NRZ input data to the decoder block. Sampled on the falling edge of RCLK.
28	RNDATA	I	**Receive Negative Data.** NRZ input data of the decoder block. Sampled on falling edge of RCLK.

SYSTEM DESCRIPTION

B3ZS/HDB3 ENCODER

Data to be transmitted is input to the encoder block to be encoded either in B3ZS or HDB3 as determined by the state of the T3/E3 pin. Input data format can be unipolar or binary. For binary signals,TPDATA and TNDATA need to be connected together externally. The line code used for T3 is B3ZS . In this mode, each block of three consecutive zeros is removed and replaced by either of two codes which contain bipolar violations. These replacement codes are BOV and OOV; where B indicates a pulse conforming with the bipolar rule and V represents a pulse violating the rule. The choice of these codes is made such that an odd number of B pulses will be transmitted between consecutive bipolar violation(V) pulses. For E3 format, the line code is HDB3. The encoding rule of HDB3 is similar to B3ZS except the number of consecutive zeros is increased to four before a code replacement can take place. The replacement codes in this case are OOOV and BOOV.

TRANSMIT ALL ONE SELECT

Setting TAOS high causes continuous AMI encoded 1s to be transmitted to the line. In this mode, input TPDATA and TNDATA are ignored. If remote loopback (RLOOP) is set high, any TAOS request will be ignored.

REMOTE LOOP-BACK

Setting RLOOP high causes receive RPDATA and RNDATA to be transmitted to the line through TTIP and TRING. The data rate is determined by RCLK. In this mode, TPDATA and TNDATA are ignored.

LOCAL LOOP-BACK

Setting LLOOP high causes TPDATA and TNDATA to go through both the encoder and the decoder. In this mode, the transmit signal RCLKO, RPOS and RNEG corresponds to TCLK, TPDATA and TNDATA respectively. Unless overriden by TAOS request, TPDATA and TNDATA will still be transmitted to the line. Forcing RLOOP and LLOOP high simultaneously will set the device into test mode.

B3ZS/HDB3 DECODER

The decoder block is included to perform B3ZS or HDB3 decoding as determined by the state of the T3/$\overline{E3}$ pin. In the B3ZS format, the decoder detects both BOV and 00V pulses and replaces them with 000 data. If HDB3 decoding is selected by setting the T3/$\overline{E3}$ pin low, B00V and 000V pulses will be detected and replaced with 0000 code. In both cases, Bipolar Violation and coding errors which do not conform to the coding scheme will be detected and flagged at the BPV output pin.

DECODER DISABLE

For testing purpose and in applications where the decoder need to be bypassed, the decoder can be disabled by setting DECODIS high.

BIPOLAR VIOLATION

The BPV pin will go high for one bit period when a violation not corresponding to the appropriate coding rule is detected on the receive signal. The occurrence of the BPV pulse is coincident with the accused bit on RPOS or RNEG.

PULSE SHAPER

The pulse shaper circuit uses a combination of filters and slew rate control techniques to pre-shape the pulse going out to the line. The amplitude of the transmit pulse can be adjusted using the TXLEV (Transmit Level) pin. When the distance to the cross-connect exceeds 225 ft, TXLEV should be set high. When the distance is less than 225 ft. TXLEV should be set low. Setting TXLEV high enables the transmitter to send out a nominal voltage of 0.9V peak, and 750mV peak when low. Figure 1 shows a typical transmitted pulse shape at the DSX-3 cross-connect and Figure 2 shows a typical eye-diagram at the STSX-1.

DRIVER MONITOR

Using TTIP and TRING as input, the driver monitor detects driver failure by monitoring the activities at MTIP and MRING. If no signal is detected on these pins for 128 TCLK cycles ±32 cycles, TMO will be set high until the next AMI signal is detected.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V ± 5% TA=-40°C to +85°C, Unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DC Supply Voltage	VDDD,VDDA	4.75	5	5.25	V
Supply Current ***(Note1)***	—	—	—	133	mA
Input Low Voltage	VIL	0	—	0.5	V
Input High Voltage	VIH	VDDD-0.5	—	VDDD	V
Output Low Voltage IOut=-4.0mA	VOL	GNDD	—	0.4	V
Output High Voltage IOut=4.0mA	VOH	VDDD-0.5	—	VDDD	V
Input Leakage Current ***(Note 2)***	IL	—	—	±10	µA
Pin 19/20 (Input = 0V)		-70	—	-130	µA
Input Capacitance	CI	—	—	10	PF
Load Capacitance	CL	—	—	10	PF

Note 1: *Supply current is measured with transmitter sending all ones AMI signal and with Transmit Level(TXLEV) set to high.*
Note 2: *All inputs except pin 19 and pin 20.*

ANALOG SPECIFICATIONS

Test Conditions: VCC = 5V ± 5% TA=-40°C to +85°C, Unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TTIP/TRINGPulse Amplitude measured at DSX-3 after 450 ft. of 728A cable and with TXLEVset to high.	—		0.45		V
TTIP/TRING Pulse Amplitude measured at STSX-1 after 450 ft. of 728A cable and with TXLEV set to high.	—		0.42		V
TTIP/TRING Pulse Amplitude measured at the output of a 1:1 transformer at E3 rate (34.368 Mbit/s).	—		1.0		V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC=5V±5%, TA= 25°C unless otherwise specified. All timing characteristics are measured with 10pF loading.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Clock Duty Cycle	—	47.5	50	52.5	%
TPDATA/TNDATA to TCLK Falling Set Up Time	Ttsu	5.5		—	ns
TPDATA/TNDATA to TCLK Falling Hold Time	Ttho	8.5	—	—	ns
TTIP/TRING to TCLK Rising Propagation Delay ***(Note 3)***	Ttdy	2.0	—	18	ns
RCLK Clock Duty Cycle	—	45	50	55	%
RPDATA/RNDATA to RCLK Falling Set Up Time	Trsu	5.5	—	—	ns
RPDATA/RNDATA to RCLK Falling Hold Time	Trho	8.5	—	—	ns
RCLKO Clock Rise Time (10% to 90%)	Trise	—	—	4.0	ns
RCLKO Clock Fall Time (10% to 90%)	Tfall	—	—	4.0	ns
RPOS/RNEG/RNRZ to RCLKO Rising Propagation Delay ***(Note 4)***	Trdy	1.0	—	5.0	ns

Note 3 :*When the encoder is enabled, a handling delay of four and a half TCLK clock cycles for B3ZS and five and half clock cycles for HDB3 will always exist between TPDATA/TNDATA and TTIP/TRING. The handling delay is reduced to one and a half clock cycles when the encoder is disabled.*

Note 4: *When the decoder is enabled, a handling delay of six and a half RCLK clock cycles will always exist between RPDATA/RNDATA and RPOS/RNEG/RNRZ. The handling delay is reduced to one and half RCLK clock cycles when the decoder is disabled.*

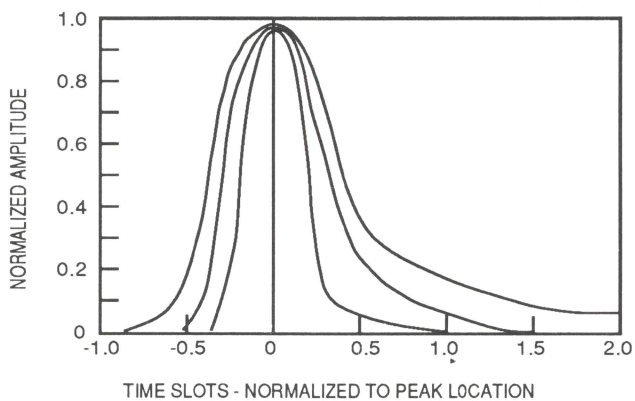


Figure 1. A Typical T7296 Pulse Shape at the DSX-3 Cross-connect

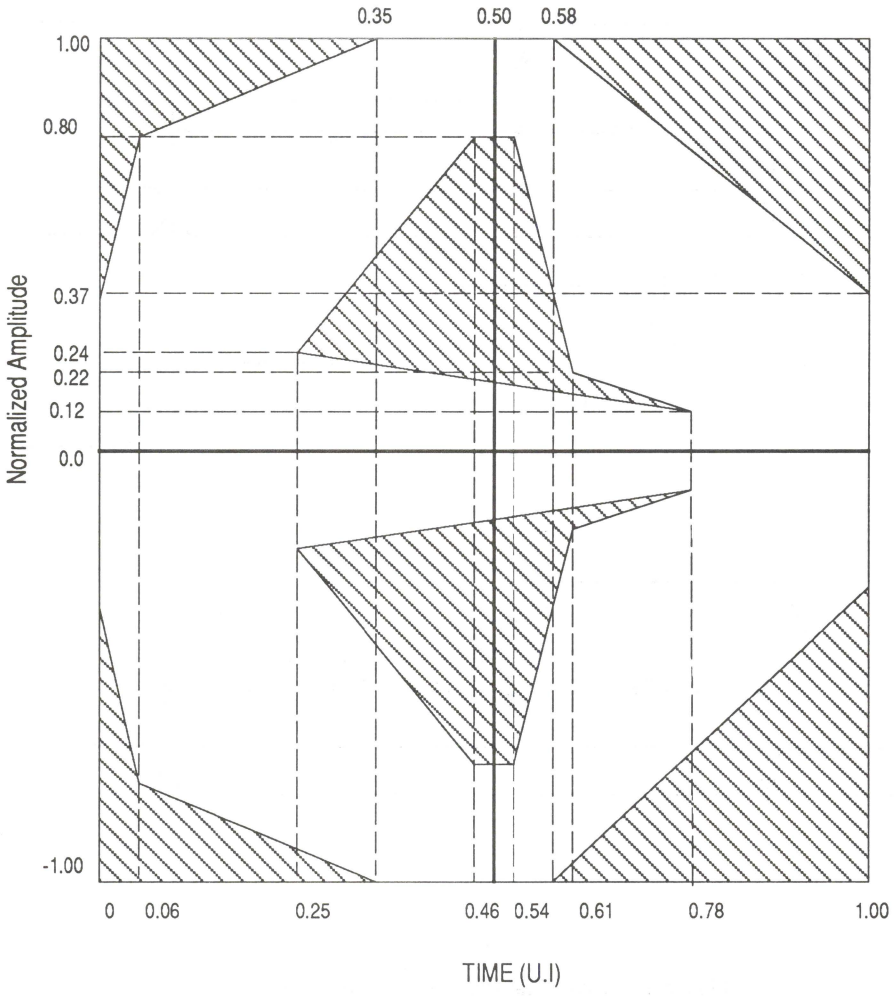


Figure 2. A Typical T7296 Transmitted Eye Diagram at the STSX-1

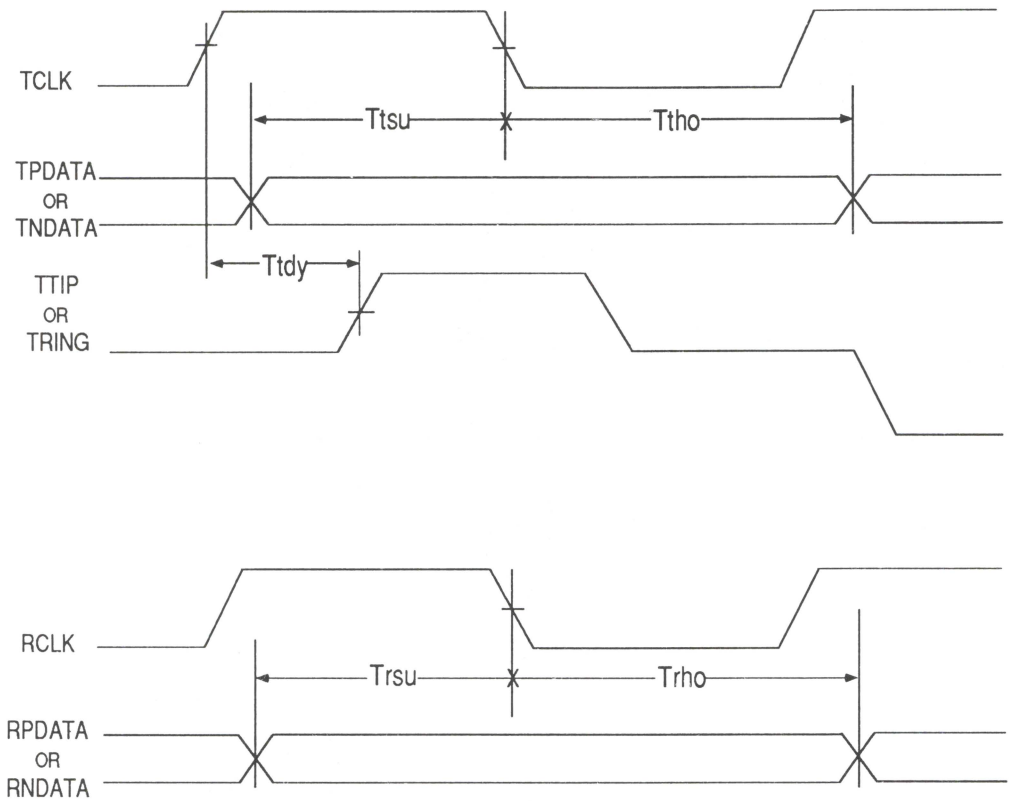


Figure 3. Timing Diagram for System Interface

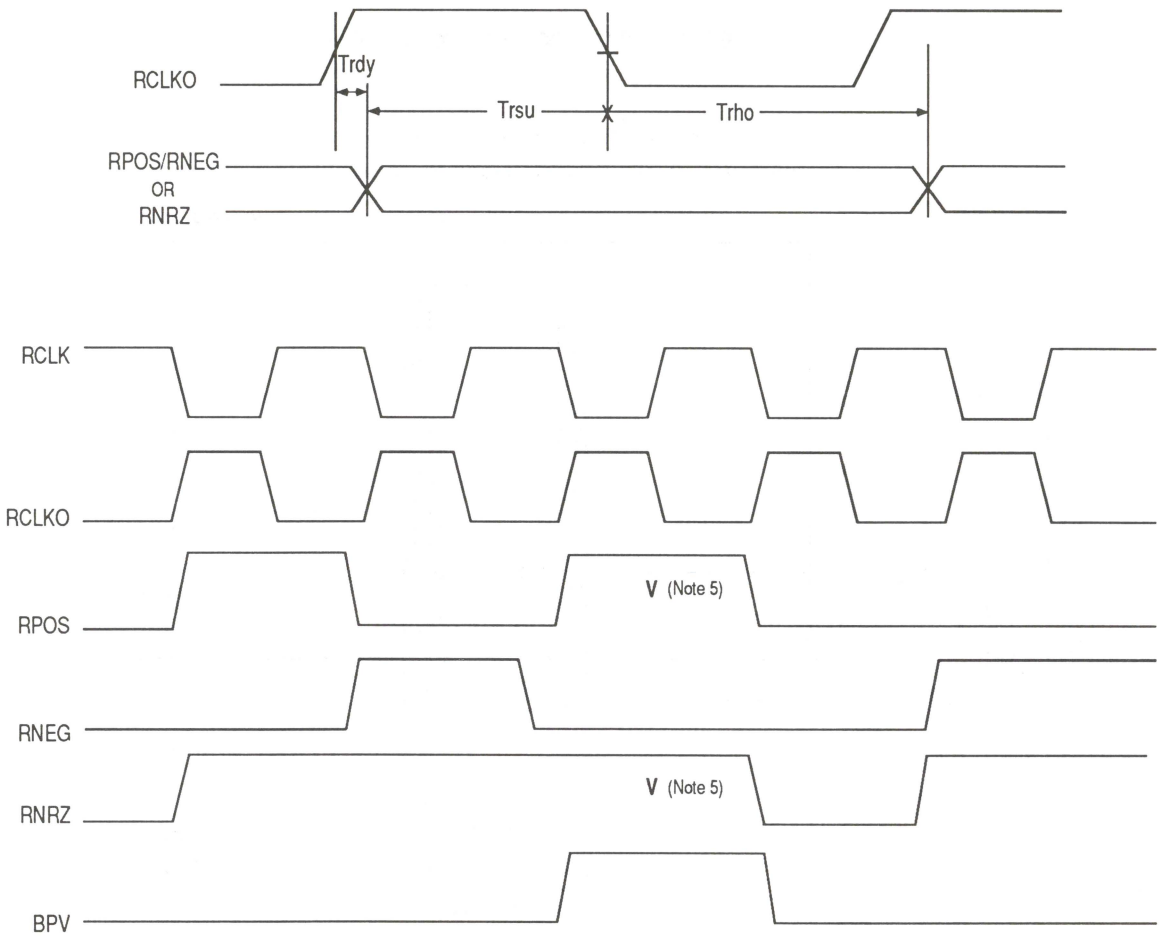
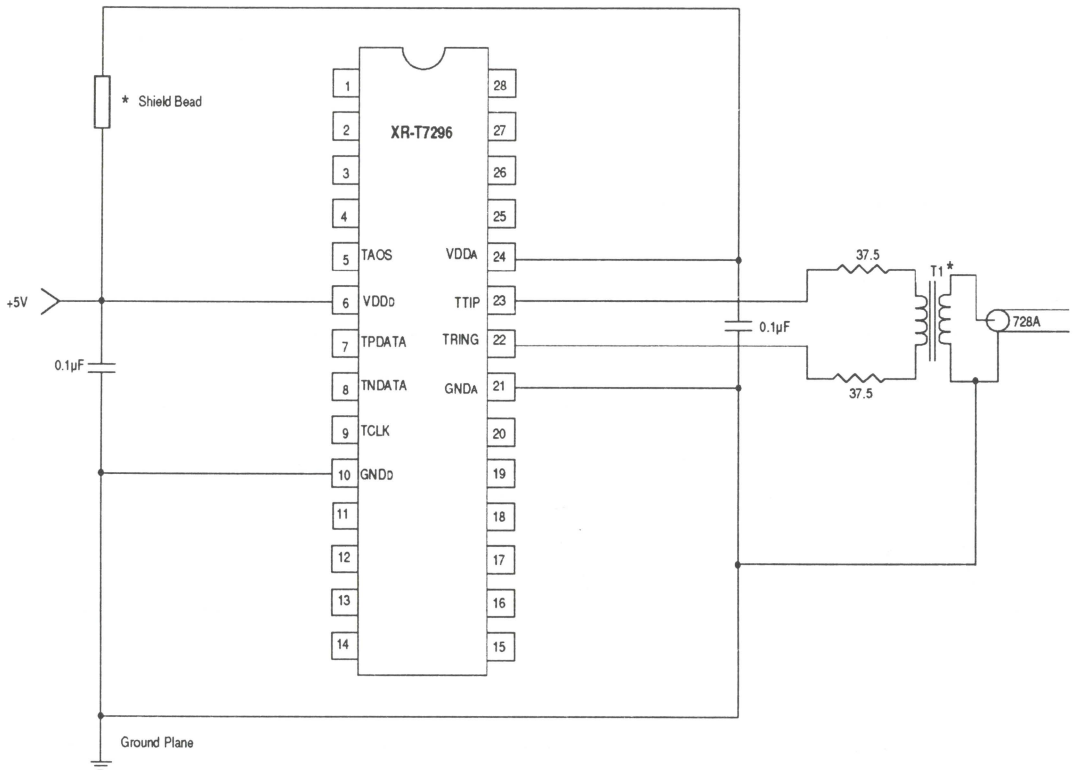


Figure 4. Decoder Output Timing Diagram

***Note 5** : The V pulse is a bipolar violation detected at the input data and reinserted at RPOS or RNEG.*



* Recommended shield bead is the Fair-Rite 2643000101 or equivalent

Output transformer T1= Minicircuits T1-1 or equivalent

Figure 5. XR-T7296 Application Circuit

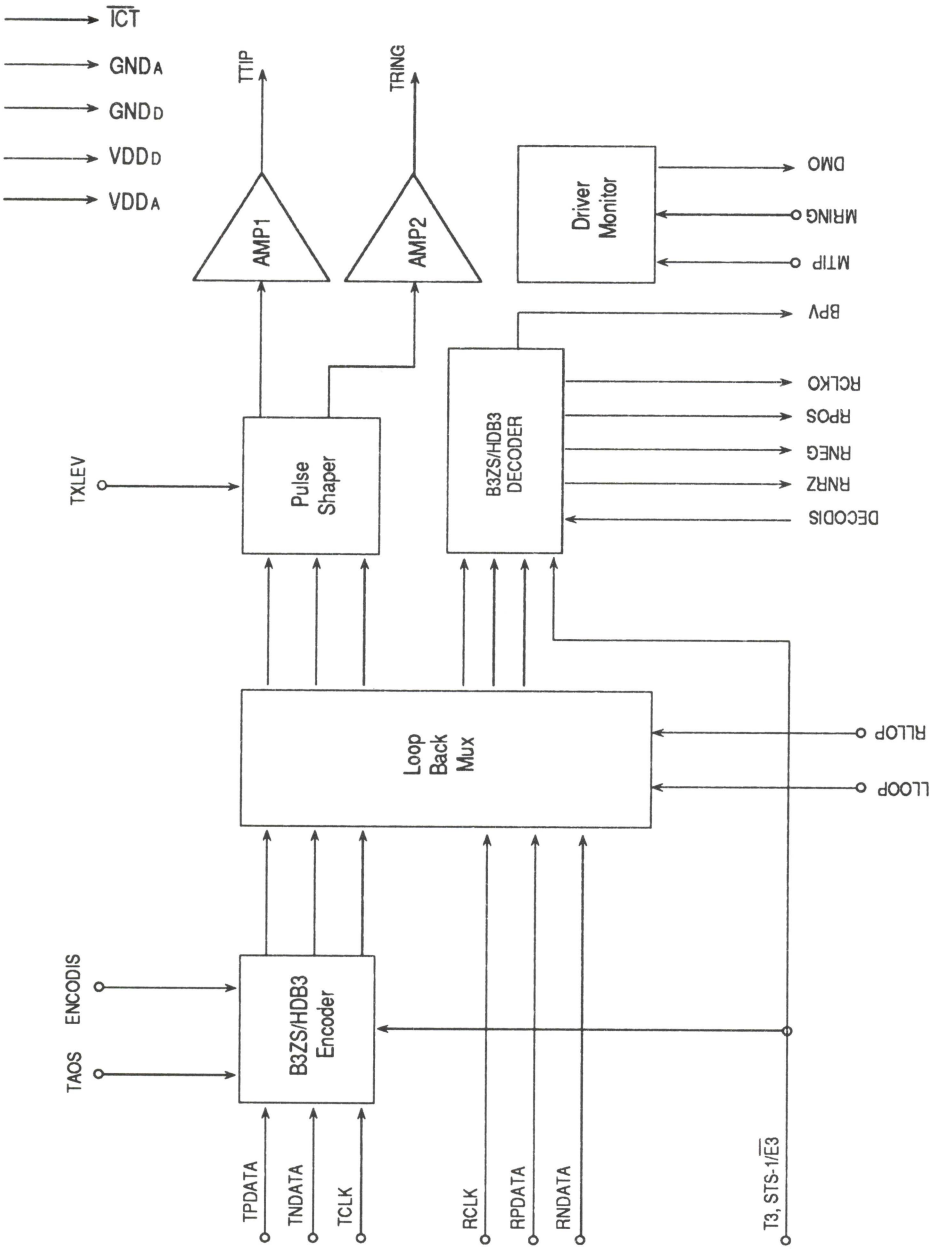


Figure 6. XR-T7296 Block Diagram



NOTES



B8ZS/AMI Line Transcoder

GENERAL DESCRIPTION

The XR-T5670 is an LSI CMOS integrated circuit which performs the B8ZS or AMI transmission coding and receiving decoding functions with error detection. It is intended for DS1 (1.544MBPS) PCM transmission applications, but can operate at clock frequencies up to 6MHz.

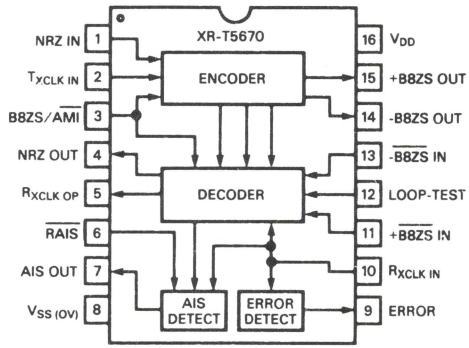
FEATURES

B8ZS Coding and Decoding for Data Rates up to 6MBPS to AT&T Technical Advisory 69
B8ZS/AMI Transmission Coding/Reception Decoding with Code Error Detection
All Transmitter and Receiver Inputs/Outputs are TTL Compatible
Internal Loop Test Capability
Single 5V ± 10% Supply Rail

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD})	-0.3 to 7.0V
Input Voltage Range (V_{IN})	–0.3 to V_{DD} + 0.3V
Input Protection Current (I_D)	±10mA
Storage Temperature Range	–55°C to 150°C,

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5670CP	Plastic	0°C to 70°C
XR-T5670CN	Ceramic	–40°C to +85°C

APPLICATIONS

AMI Encoding/Decoding
B8ZS Encoding/Decoding

SYSTEM DESCRIPTION

Coder

Binary data in "NRZIN" is clocked into the coder by a synchronous transmission clock "T_{XCLKIN}" on the failing edge. The "+B8ZS" and "–B8ZS" output signals appear 8.5 clock cycles later to allow for the insertion of extra pulses due to sequences of eight consecutive zeros. These two signals are full width data and will be mixed with the "T_{XCLKIN}" at the input of an external line driver to produce bipolar B8ZS signals for transmission.

Decoder

Received half width data on "+$\overline{\text{B8ZSIN}}$" and "–$\overline{\text{B8ZSIN}}$" are locked into the decoder on the rising edge of the received clock "R_{XCLKIN}". The "NRZOUT" binary data output occurs on eight clock cycles later. Received signals not consistant with B8ZS coding rules are detected as errors. The error output "ERROR" is active high during one "R_{XCLKIN}" clock period. The error output is not an accurate measure of error count; it is intended for alarm indication only.

AIS (Alarm Indication Signal)

If the decoder inputs received a continuous of ones (all marks) over two consecutive periods of the external reset signal "$\overline{\text{RAIS}}$", the "AISOUT" output will be set high and latched in that state until one or more zeros are received when the next reset signal "$\overline{\text{RAIS}}$" occurs.

The number of received zeros required to reset "AISOUT" over two consectuive periods of "$\overline{\text{RAIS}}$" can be mask programmed to two or three.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = –40°C to +85°C, V_{DD} = 4.5 to 5.5V, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX	UNIT	CONDITIONS
DYNAMIC CHARACTERISTICS						
T_{XCLKIN}	Clock Input Frequency			6	MHz	
R_{XCLKIN}	Clock Input Frequency			6	MHz	
t_{s1}	Data Set-Up Time	55			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{h1}	Data Hold Time	25			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{pd1}	Data Propagation Delay Time			65	ns	T_{XCLKIN} to B8ZS OUT See Figure, 3 and 6. Note 1
t_{s2}	Data Set-Up Time	55			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{h2}	Data Hold Time	0			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{pd2}	Data Propagation Delay Time			90	ns	R_{XCLKIN} to NRZOUT See Figures 4 and 7, Note 2 Loop Test = 0
t_{pd3}	Clock Delay Time			50	ns	R_{XCLK} IN to $R_{XCLKOUT}$ See Figure 8, Loop Test = 0
t_{s3}	RAIS = 0 Set-Up Time	30			ns	RAIS to R_{XCLKIN} See Figure 7
t_{h3}	RAIS= 0 Hold Time	30			ns	RAIS to R_{XCLKIN}
STATIC CHARACTERISTICS, V_{DD} = 5.0V						
I_{DD}	Quiescent Device Current			100	µA	
	Operating Current			4	mA	Input Clock Frequency = 2.0MHz
V_{DD}	Supply Voltage	4.5	5	5.5	V	
V_{IN}	Input Voltage 0	0		5.0	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.1	V	I_{OL} = 0
V_{OH}	Output High Voltage	4.9			V	I_{OH} = 0
I_{OL}	Output Lo, Current	1.6			mA	V_{OL} = 0.4V
I_{OH}	Output High Current	–1			mA	V_{OH} = 4.6V
I_{IL}	Input Low Current			–10	µA	V_{IL} = 0V
I_{IH}	Input High Current			10	µA	V_{IH} = 5V

Note 1: The encoded B8ZS OUT are delayed by 8 1/2 clock periods from NRZIN.
Note 2: The decoded NRZOUT are delayed by 7 = clock periods from B8ZS IN.

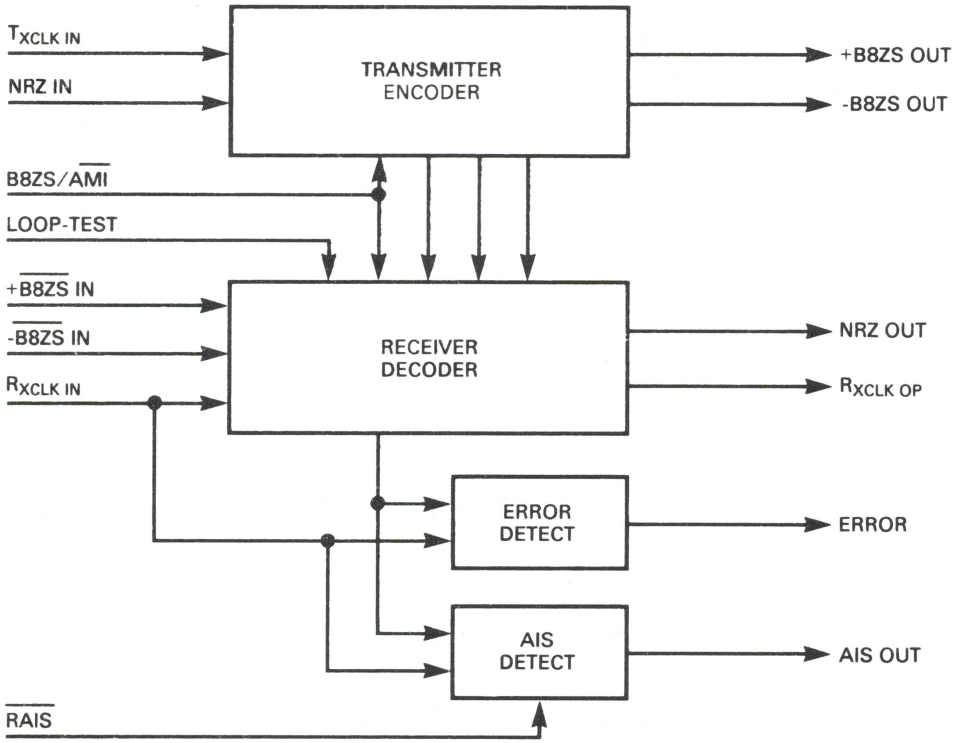


Figure 1. XR-T5670 Block Diagram

Loop Test

When the Loop Test control input is set high, a test mode is made in which the "+B8ZSOUT" and "–B8ZSOUT" are internally connected to the decoder inputs. The external B8ZS inputs and the "R_{XCLKIN}" are disabled, and the "T_{XCLKIN}" is used to control the decoder timing. The "NRZOUT" signals correspond to the "NRZIN" input, but delayed by 16 clock periods.

B8ZS/AMI

To operate the XR-T5670 in AMI mode, the B8ZS/AMI control input is driven low. In this mode, two consecutive pulses of the same polarity at the decoder inputs will be detected and flagged as an error at the "ERROR" output.

Definition of B8ZS Code Used in XR-T5670 Transcoder

With B8ZS coding, each block of eight consecutive zeros is removed and the B8ZS code is inserted. If the pulse preceding the inserted code is transmitted as a positive pulse (+), the inserted code is 000+–0–+. Bipolar violations occur in the fourth and seventh bit position of the inserted code. If the pulse preceeding the inserted code is a negative pulse (–), the inserted code is 000–+0+–. Bipolar violations again occur in the fourth and seventh bit positions as illustrated in Figure 2.

Binary Signal	1	0	0	0	0	0	0	0	0
B8ZS Signal	+1	0	0	0	+1	–1	0	–1	+1
or	–1	0	0	0	–1	+1	0	+1	–1

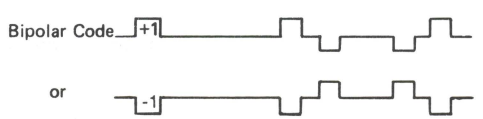


Figure 2. B8ZS Code

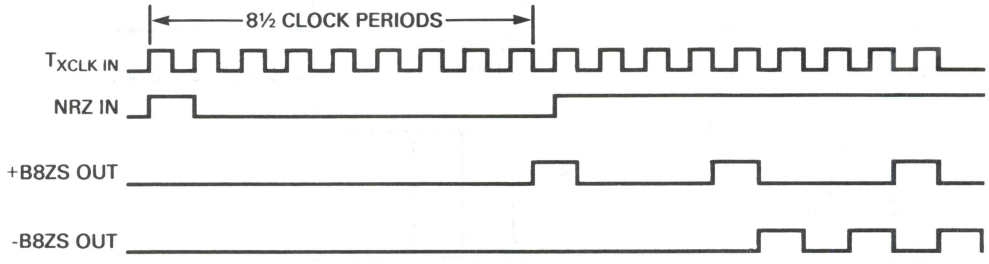


Figure 3. Encoder Waveforms

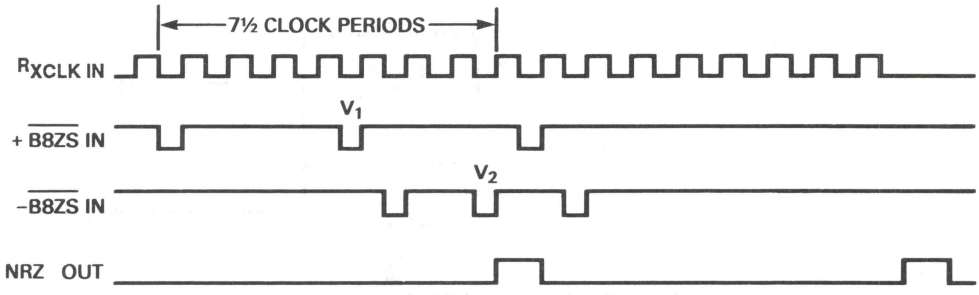


Figure 4. Decoder Waveforms

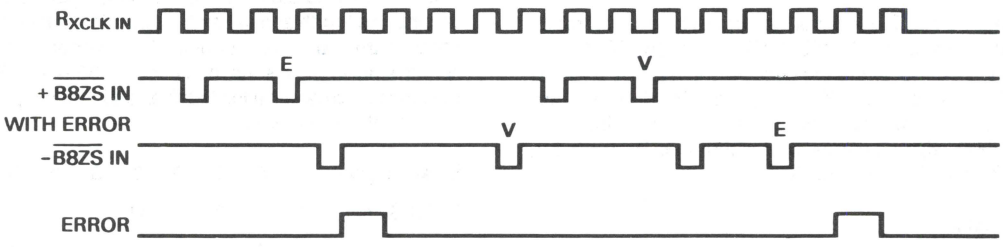


Figure 5. B8ZS Error Output Waveforms

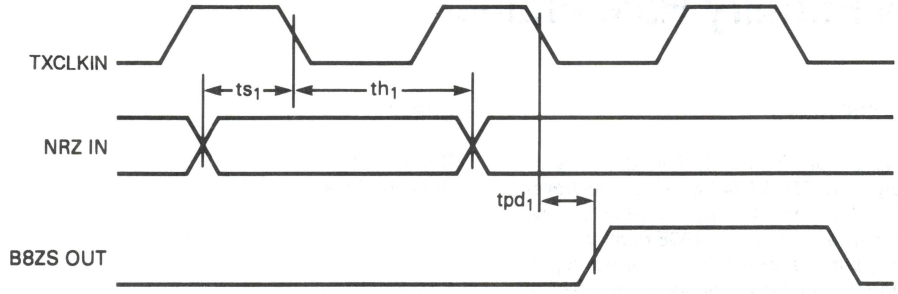


Figure 6. Encoder Timing Relationship

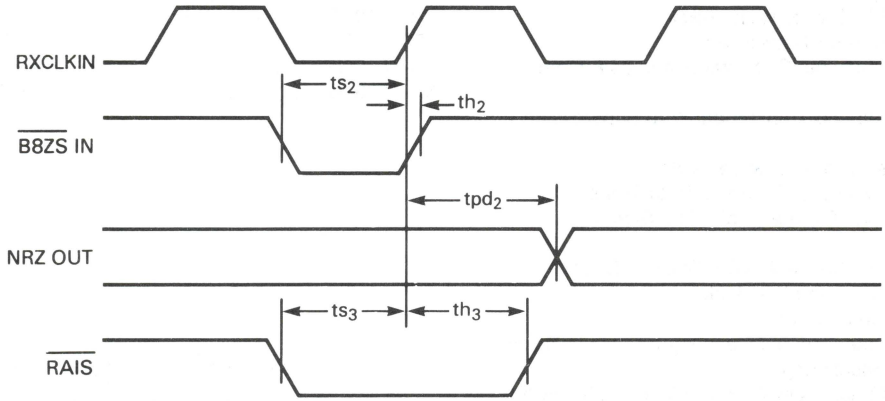


Figure 7. Decoder Timing Relationship

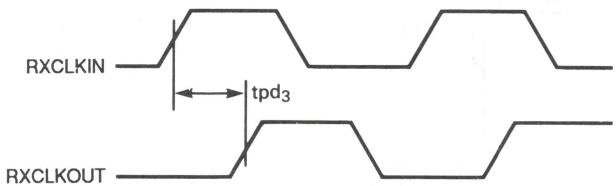


Figure 8. RXCLKIN To R XCLKOUT Relationship

T1/ISDN Primary Rate Framer

GENERAL DESCRIPTION

The XR-T5690 is a monolithic CMOS IC designed to implement primary rate PCM (1.544 MHz) T-Carrier transmitter and receiver functions. It supports 193S framing (12 frames per superframe) and also 193E framing which is the extended superframe format (24 frames per superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

FEATURES

Single +5V Supply
Low Power CMOS Digital Technology
Single Chip DS1 Rate Transceiver
Supports 12 Frames per Superframe and 24 Frames per Superframe
B8ZS, B7 Stuffing and Transparent Zero Suppression Modes
No Host Processor for Hardware Mode
Supports Host Processor for Serial Data Transmission
Selectable 0, 2, 4, 16 State Robbed Bit Signaling Mode
Allows Mix of "CLEAR" and "NON CLEAR" DSO Channels on the same DS1 Link
Alarm Generation and Detection
Receive Error Detection and Counting for Transmission Performance Monitoring
Pin to Pin and Functionally Compatible with DS2180A

APPLICATIONS

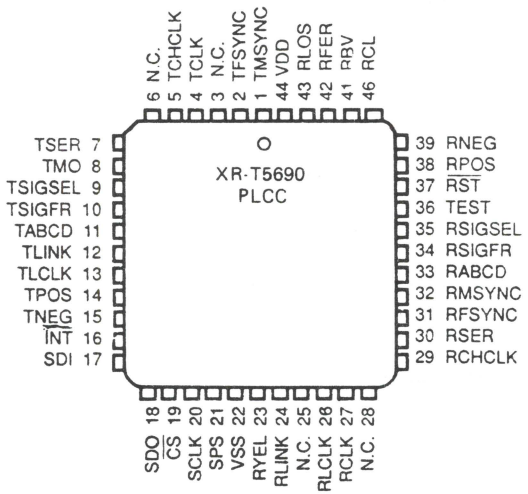
Digital Multiplexers
Channel Banks

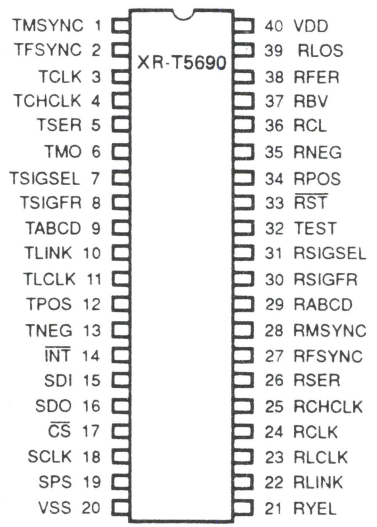
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V
Storage Temperature	–65°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5690CP	Plastic DIP	0°C to 70°C
XR-T5690CJ	PLCC	0°C to 70°C
XR-T5690IP	Plastic DIP	–40°C to 85°C
XR-T5690IJ	PLCC	–40°C to 85°C





SYSTEM DESCRIPTION

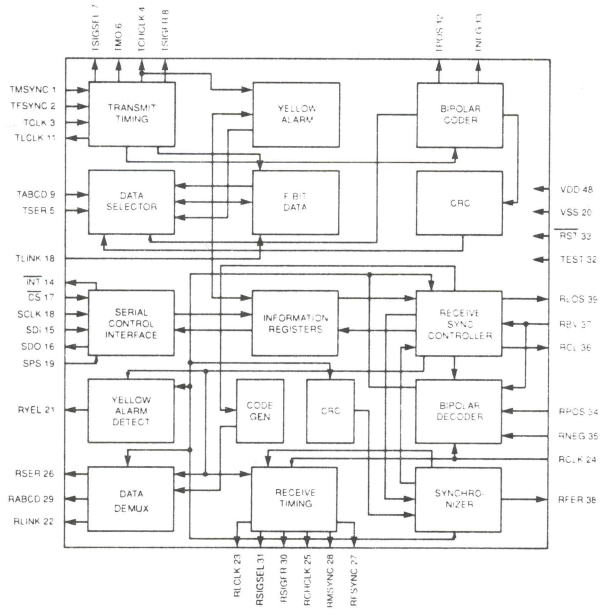
Transmitter Section

The XR-T5690 is compatible with the existing BELL system D4 (193S) framing standard described in ATT PUB 43801 and new extended superframe format (193E) as described in ATT C.B. #142. Programmable features of the XR-T5690 allows support of other framing standards which are derivatives of 193S and 193E. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe as opposed to 24 frames in 193E mode. Each frame consists of 24 channels of 8 bit data transmitted and received MSB first and preceded by an F-bit.

The transmit side of the XR-T5690 is made up of 6 major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC block. The timing and clock generation circuit develops all on board and output system clocks from its inputs TCLK (Transmit Clock), TFSYNC (Transmit Frame Sync) and TMSYNC (Transmit Multiframe Sync). The yellow alarm circuitry generates mode dependent yellow alarms which is a repeating pattern of FF(hex) and 00(hex) on the 4KHz Facility Data Link (FDL). The CRC block generates checksum results utilized in 193E framing and the F-bit data provides mode dependent framing patterns which allow insertion of link or S-bit data externally. All of these blocks feed into the data selector, where it is possible to modify the outgoing data stream by bit selection and insertion of the transmit registers (CCR, TCR, TIR and TTR). The bipolar coder formats the output of the data selector, supports on board loopback features and inserts zero suppression codes to make it compatible with bipolar transmission techniques.

Receiver Section

The heart of the receiver is the synchronizer and sync monitor. This circuit serves two purposes: (A) that of monitoring the incoming data stream for loss of frame or multiframe alignment, and (B) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off line search for the new alignment. Whenever this occurs, all output timing signals remain at the old alignment with the exception of RSIGFR (Receive Signaling Frame), which is forced low during resync. At the instant a valid sequence is detected, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS (Receive Loss of Sync) will transition low, indicating valid sync and the resumption to the normal sync monitoring mode. Several bits in the RCR (Receive Control Register) allow tailoring of the resync algorithm by the user.



FUNCTIONAL BLOCK DIAGRAM

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, unless otherwise specified.

MODEL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Supply Current		3	10	mA	Note 1,2
I_L	Input Leakage			1	µA	
I_{LO}	Output Leakage			1	µA	Note 3
I_{OH}	Output Current @2.4V	-1		+1	mA	Note 4
I_{OL}	Output Current @0.4V	-4			mA	Note 5
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		7		pF	
V_{IH}	Logic 1	2		V_{DD} +0.3	V	
V_{IL}	Logic 0	–0.3		+0.8	V	

Notes:
1. TCLK = RCLK = 1.544MHz
2. Outputs Open
3. Applies to SDO when tristated
4. All outputs except INT, which is open collector
5. All outputs

AC ELECTRICAL CHARACTERISTICS -Serial Port

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, unless otherwise specified.
Measured at $V_{IH} = 2.0V$ or $V_{IL} = 0.8V$ and 10ns maximum rise and fall time.

MODEL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DC}	SDI to SCLK Set-up	50			ns	
t_{CDH}	SCLK to SDI Hold	50			ns	
t_{CD}	SDI to SCLK	50			ns	
t_{CL}	SCLK Low Time	250			ns	
t_{CH}	SCLK High Time	250			ns	
t_R, t_F	SCLK Rise & Fall			500	ns	
t_{CC}	$\overline{CS}$ to SCLK Set Up	50			ns	
t_{CCH}	SCLK to $\overline{CS}$ Hold	50			ns	
t_{CWH}	$\overline{CS}$ Inactive Time	250			ns	
t_{CDV}	SCLK to SDO Valid			200	ns	Note 1
t_{CDZ}	$\overline{CS}$ to SDO High Z			75	ns	

Notes: 1. Output load capacitance = 100pF

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V ± 5%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER						
t_P	TLCK		648		ns	
t_{WL}, t_{WH}	TCLK Pulse Width		324		ns	
t_F, t_R	TCLK, RCLK Rise/Fall		20		ns	
t_{STD}	TSER, TABCD Set Up to TCLK Falling	50			ns	
t_{HTD}	TSER, TABCD Hold to TCLK Rising	50			ns	
t_{STL}	TLINK Set Up to TCLK Rising	50			ns	
t_{HTL}	TLINK Hold to TCLK Rising	50			ns	
t_{STS}	TFSYNC,TMSYNC Set Up to TCLK Rising	125			ns	
t_{FTS}	Propagation Delay TFSYNC to TMO, TSIGSEL,TSIGFR,TLCLK			75	ns	
t_{PTCH}	Propagation Delay TCLK to TCHCLK			75	ns	
t_{SP}	TFSYNC,TMSYNC Pulse Width	100			ns	
RECEIVER						
t_{PRS}	Propagation Delay RCLK to RMSYNC, RFSYNC, RLCLK RSIGSEL, RSIGFR, RCHCLK			75	ns	
t_{PRD}	Propagation Delay RCLK to RSER, RABCD, RLINK			75	ns	
t_{TTR}	Transition Time All Outputs			20	ns	
t_P	RCLK Period		648		ns	
t_{WL}, t_{WH}	RCLK Pulse Width		324		ns	
t_F, t_R	RCLK Rise and Fall		20		ns	
t_{PRA}	Propagation Delay RCLK to RYEL, $\overline{RCL}$, RFER, RLOS, RBV			75	ns	
t_{RST}	$\overline{RESET}$ Pulse Width	1			µs	

PIN DESCRIPTION

Pin	Symbol	Description
1	TMSYNC	**Transmit Multiframe Sync:** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	TFSYNC	**Transmit Frame Sync:** Rising edge indentifies frame boundary, may be pulsed every frame to reinforce internal frame counter, or tied low (allowing TMSYNC to establish frame and multi-frame alignment).
3	TCLK	**Transmit Clock:** 1.544MHz primary clock.
4	TCHCLK	**Transmit Channel Clock:** 192KHz clock which identifies time slot boundaries. For parallel to serial conversion of channel data.
5	TSER	**Transmit Serial Data:** NRZ data input, sampled on falling edge of TCLK.
6	TMO	**Transmit Multiframe Out:** Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	TSIGSEL	**Transmit Signaling Select:** 667Hz clock which identifies signaling frames A and C in 193E framing. 1.33KHz clock in 193S.
8	TSIGFR	**Transmit Signaling Frame:** High during signaling frames, low otherwise.
9	TABCD	**Transmit ABCD Signaling:** When enabled via TCR (bit-4), sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	TLINK	**Transmit Link Data:** Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-bit insertion).
11	TLCLK	**Transmit Link Clock:** 4KHz demand clock for TLINK input.
12	TPOS	**Transmit Bipolar +D Data Output.** Updated on rising edge or TCLK.
13	TNEG	**Transmit Bipolar -D Data Output.** Updated on rising edge of TCLK
14	$\overline{INT}$	**Receive Alarm Interrupt:** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI	**Serial Data In:** Data for on-board registers. Sampled on the rising edge of SCLK.
16	SDO	**Serial Data Out:** Control and status information from on-board registers. Updated on falling edge of SCLK, and tristated duringserial port write or when $\overline{CS}$ is high.
17	$\overline{CS}$	**Chip Select:** Active low during read or write operation from or to serial port.
18	SCLK	**Serial Data Clock:** Used to read or write the serial port registers.
19	SPS	**Serial Port Select:** Tie to V_{DD} to select serial port. Tie to Vss to select hardware mode.
20	V_{SS}	**Ground.**

Pin	Symbol	Description
21	RYEL	**Receive Yellow Alarm:** Transitions high when yellow alarm is detected; goes low when alarm clears.
22	RLINK	**Receiver Link Data:**Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	RLCLK	**Receive Link Clock:** 4KHz demand clock for RLINK.
24	RCLK	**Receive Clock:** 1.544MHzprimary clock.
25	RCHCLK	**Receive Channel Clock:** 192KHz clock, identifies time slot (channel) boundaries.
26	RSER	**Receive Serial Data:** Received NRZ serial data, updated on rising edges of RCLK.
27	RFSYNC	**Receive Frame Sync:** Extracted 8KHz clock, one RCLK wide, indicates F-bit position in each frame.
28	RMSYNC	**Receive Multiframe Sync:** Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	RABCD	**Receive ABCD Signaling:** Extracted signaling data output valid for each channel time in signaling frames, In non-signaling frames. RABCD outputs the LSB of each channel word.
30	SIGFR	**Receive Signaling Frames:** High during signaling frames, low during resync and non-signaling frames.
31	RSIGSEL	**Receive Signaling Select:** In 193E framing a 667Hz clock which identifies signaling frames A and C. A 1.33KHz clock in 193S.
32	TEST	**Test Mode:** Tie to V_{SS} for normal operation.
33	$\overline{RST}$	**Reset:** A high to low transition clears all internal registers and resets receive side counters. A high to low to high transition will initiate a receive resync.
34	RPOS	**Receive Bipolar +D Data Input:** Sampled on falling edge of RCLK.
35	RNEG	**Receive Bipolar –D Data Input:** Sampled on falling edge of RCLK. Tie RPOS and RNEG together to receive NRZ data and disable bipolar violation monitoring circuitry.
36	RCL	**Receive Carrier Loss:** High if 32 consecutive "0's" appear at RPOS and RNEG, goes low after next "1".
37	RBV	**Receive Bipolar Violation:** High during accused bit time at RSER if bipolar violation is detected, low otherwise.
38	RFER	**Receive Frame Error:** High during F bit time when F_T, or Fs errors occur (193S), or when FPS or CRC errors occur (193E), low during resync.
39	RLOS	**Receive Loss Sync:** Indicates sync status; high when internal resync is in progress, low otherwise.
40	V_{DD}	**+5 -0V Power Supply.**

REGISTER ADDRESS SUMMARY

Register	Address	T/R[1]	Function
RSR	0000	R*	**Receive Status Register.** Reports all receive alarm conditions.
RIMR	0001	R	**Receive Interrupt Mask Register.** Allows masking of individual alarm generated interrupts.
BVCR	0010	R	**Bipolar Violation Count Register.** 8 bit preset table counter which records individual bipolar violation.
ECR	0011	R	**Error Count Register.** 2 independent 4-bit counters which record OOF occurrences, and individual bipolar violation.
CCR	0100	T/R	**Common Control Register.** Selects device operating characteristics common to receive and transmit sides.
RCR	0101	R	**Receive Control Register.** Programs device operating characteristics unique to the receive side.
TCR	0110	T	**Transmit Control Register.** Selects additional transmit side modes.
TIR1	0111	T	**Transmit Idle Register 1.** Designate which outgoing channels are to be substituted with idle code.
TIR2	1000	T	
TIR3	1001	T	
TTR1	1010	T	**Transmit Transparent Register 1.** Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
TTR2	1011	T	
TTR3	1100	T	
RMR1	1101	R	**Receive Mark Register 1**. Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control or RCR.)
RMR2	1110	R	
RMR3	1111	R	

NOTES:

1. Transmit or receive side register

2. RSR is Read only register, all other registers are read/write

3. Reserved bit locations in the control registers should be programmed to 0, to maintain compatibility with fuure transceiver products.

REGISTER DESCRIPTION

Receive Status Register (RSR)
Reports all receive alarm conditions

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Bit #	Description
BVCS	RSR.7	**Bipolar Violation Count Saturation:** Set when the 8 bit counter at BVCR saturates.
ECS	RSR.6	**Error Count Saturation:** Set when either of the 4 bit counters at ECR satu rates.
RYEL	RSR.5	**Receive Yellow Alarm:** Set when yellow alarm is detected. (Detected yellow alarm format determined by CCR bit-4 and CCR bit-3).
RCL	RSR.4	**Receive Carrier Loss:** Set when 32 consecutive "0's" appears at RPOS and RNEG.
FERR	RSR.3	**Frame Bit Error:** Set when Ft (193S) or FPs (193E) bit error occurs.
B8ZSD	RSR.2	**Change of Frame Alignment Set via CCR.6:** When CCR.6=0; detected B8ZS code word is reported at RSR.2. When CCR.6=1; COFA (Change of frame alignment) is reported when last resync resulted in change of frame or multiframe alignment.
RBL	RSR.1	**Receive Blue Alarm:** Set when 2 consecutive frames have less than 3 zeros in the data stream.
RLOS	RSR.0	**Receive Loss Sync:** Set when resync is in process; if RCR bit-1=0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

Receive Interrupt Mask Register (RIMR)
Allows masking of individual alarm generated interupts

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

BVCS RIMR.7 **Bipolar Violation Count Saturation Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

ECS RIMR.6 **Error Count Saturation Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RYEL RIMR.5 **Receive Yellow Alarm Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RCL RIMR.4 **Receive Carrier Loss Mask:**
1 =interrupt enabled
0=interrupt disabled (masked)

FERR RIMR.3 **Frame Bit Error Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

B8ZSD RIMR.2 **B8ZS Detect Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RBL RIMR.1 **Receive Blue Alarm Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RLOS RIMR.0 **Receive Loss of Sync Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

Bipolar Violation Count Register (BVCR)
This is an 8 bit presetable counter which records individual bipolar violations.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

BVD7 BVCR.7 **MSB of Bipolar Violation Count**

BVD0 BVCR.0 **LSB of Blpolar Violation**

Error Count Register (ECR)

There are 2 independent 4 bit counters which record out-of frame occurences and CRC (Cyclic Redundancy Check) errors.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00F3	00F2	00F1	00F0	ESF3	ESF2	ESF1	ESF0

OOFD3	ECR.7	**MSB of OOF Event Count**
OOFD0	ECR.4	**LSB of OOF Event Count**
ESFD3	ECR.3	**MSB of Extended Superframe Error Count**
ESFDO	ECR.0	**LSB of Extended Superframe Error Count**

Common Control Register (CCR)

Selects device operating characteristics common to receive and transmit sides.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	B8ZSC	EFYA	FM	YELMD	B8ZS	B7	LPBK

0 CCR.7 This bit must be zero for proper operation.

B8ZSC CCR.6 **B8ZS/Change of Frame Report:**
0= detected B8ZS code word is reported at RSR.2
1 = detected change of frame or multiframe alignment after last resync is reported at RSR.2

EFYA CCR.5 **193E Yellow Alarm ModeSelect:**
0= Yellow alarm is a repeating pattern set of 00 hex and FFhex.
1= Yellow alarm is a "0" in the bit 2 position of all channels.

FM CCR.4 **Frame Mode Select:**
0=193S, 12 frame/superframe
1=193E, 24 frame/superframe

YELMD CCR.3 **193S Yellow Alarm Mode Select:**
Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12; if cleared, yellow alarm is a "0" in bit-2 of all channels. Does not affect 193E yellow alarm operation.

B8ZS CCR.2 **Bipolar Eight Zero Substitution:**
0=Disable B8ZS
1=Enable B8ZS

B7 CCR.1 **Bit Seven Zero Suppression:**
If CCR bit-1=1, channels with an all zero content will be transmitted with bit-7 forced to "1". If CCR bit-1=0, no bit-7 stuffing occurs.

LPBK CCR.0 **Loop Back:**
When enabled, the device internally loops output transmit data into the incomming receive data buffers and TCLK is internally substituted for RCLK.

Receive Control Register (RCR)
Programs device operating characteristics unique to the receive side.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ARC	00FC	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

ARC RCR.7

Auto Resync Criteria:
0=Resync on 00F or RCL event
1=Resync on 00F only

00FC RCR.6

Out-of-Frame Condition Detected:
0=2 of 4 framing bits in error
1=2 of 5 framing bits in error

RCI RCR.5

Receive Code Insert:
When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.

RCS RCR.4

Receive Code Selection:
0=idle code (7F HEX)
1=digital milliwatt

SYNCC RCR.3

Sync Criteria:
Determines the type of algorithm utilized by the receiver synchronizer and differs for each frame mode.

193S Framing (CCR.4=0)
0=Synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S.
1=Cross couple F_T and F_S patterns in sync algorithm.

193E Framing (CCR.4=1)
0=Normal sync. (Fps only)
1=Validate new alignment with CRC before declaring sync.

SYNCT RCR.2

Sync Time:
If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.

SYNCE RCR.1

Sync Enable:
If clear, the transceiver will automatically begin a resync if 2 of the previous 4 framing bits were in error, or if carrier loss is detected. If set, no auto resynic occurs.

RESYNC RCR.0

Resync:
When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

Transmit Control Register (TCR)
selects additional transmit side modes.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ODF	FTPT	TCP	RBSE	TIS	193SI	TBL	TYEL

0DF TCR.7 **Output Data Format:**
0= Bipolar data at TPOS & TNEG
1= NRZ data at TPOS; TNEG= 0

FTPT TCR.6 **FT/FPS Pass Through:**
0= FT/FPS sourced internally
1= FT/FPS sampled at TSER during F-bit time

TCP TCR.5 **Transmit CRC Pass-Through:**
0= transmit CRC code internally generated.
1= TSER sampled at CRC F-bit time for external CRC insertion.

RBSE TCR.4 **Robbed Bit Signaling Enable:**
1= Signaling inserted in all channels during signaling frames.
0= No signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DSO channels.)

TIS TCR.3 **Transmit Idle Code Selection:**
Determines idle code format to be inserted into channels marked by the TIR registers.
0=insert 7F (hex) into marked channels.
1=insert FF (hex) into marked channels.

193S1 TCR.2 **193S S-Bit Insertion:**
Determines source of transmitted S-bit.
0=internal S-bit generator
1 =external

TBL TCR.1 **Transmit Blue Alarm:**
0=disabled
1 =enabled

TYEL TCR.0 **Transmit Yellow Alarm:**
0=disabled
1 =enabled

Transmit Idle Registers (TIR1-TIR3)

Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR bit-3.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24 TIR3.7 **Channel 24 Transmit Idle Register**

CH1 TIR1.0 **Channel 1 Transmit Idle Register**

Transmit Transparency Register (TTR1-TTR3)

Each of these bit positions represents a DS0 channel in the outgoing frame. When set the corresponding channel is transparent.

TTR1	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

TTR2	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

TTR3	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24 TTR.3.7 **Channel 24 Transmit Transparent Register**

CH1 TTR1.0 **Channel 1 Transmit Transparent Register**

Receive Mark Registers (RMR)

Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set the corresponding channel will output codes determined by RCR bit-4 and RCR bit-5.

RMR1	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

RMR2	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

RMR3	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24 RMR3.7 **Channel 24 Receive Mark Register**

CH1 RMR1.0 **Channel 1 Receive Mark Register**

GLOSSARY

GENERAL FUNCTIONS

Line Coding

T1 line data is transmitted in a bipolar alternative mark inverted line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit-7 of any channel consisting of all 0's to 1. The use of bipolar eight zero substitution (B8ZS) satisfies the one's density requirement, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "1" transmitted was positive, the inserted code is 0 0 0 + – 0 – +; if negative, the code word inserted is 0 0 0 – + 0 + –. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the XR-T5690 error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all "0's" if B8ZS is enabled. Also, the receiver status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR bit-7.

F-BITS

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F^T bits) which provides frame alignment information, and the signaling framing pattern (known as F^S bits) which provides multiframe alignment information (See Table 2). In 193E framing, the F bit position is shared by the framing patten sequence (FPS), which provides frame and multiframe alignment information, a 4 KHz data link known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance. (See Table 1)

SIGNALING

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted (Table 2). In 193E, A and B data is inserted into frames 6 and 12, and C and D data is inserted into Frames 18 AND 24. This allows a maximum of 4 signaling states to be transmitted per superframe in 193S and 16 states in 193E (Table 1).

B8ZS

The XR-T5690 supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system "l's" density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces 8 consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

BIT SEVEN STUFFING

Existing systems meet one's density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is "globally" enabled by asserting CCR bit-1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1-TTR3.

LOOP BACK

Enabling loop back will typically induce an out of frame "OOF" condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all "1's". All operating modes are available in loop back.

ALARMS

The XR-T5690 supports all alarm pattern generation and detection required in typical BELL system applications. These alarm modes are explained in ATT PUB 43801, ATT C.B.#142

TABLE 1
193E FRAMING FORMAT

Frame No.	F-Bit Use			Bit Use per Channel		Signaling Bit Use		
	FPS[1]	FDL[2]	CRC[3]	Data Bits	Signaling Bits[4,5]	2 State	4 State	16 State
1	-	M	-	Bits 1-8				
2	-	-	C1	Bits 1-8				
3	-	M	-	Bits 1-8				
4	0	-	-	Bits 1-8				
5	-	M	-	Bits 1-8				
6	-	-	C2	Bits 1-7	Bit 8	A	A	A
7	-	M	-	Bits 1-8				
8	0	-	-	Bits 1-8				
9	-	M	-	Bits 1-8				
10	-	-	C3	Bits 1-8				
11	-	M	-	Bits 1-8				
12	1	-	-	Bits 1-7	Bit 8	A	B	B
13	-	M	-	Bits 1-8				
14	-	-	C4	Bits 1-8				
15	-	M	-	Bits 1-8				
16	0	-	-	Bits 1-8				
17	-	M	-	Bits 1-8				
18	-	-	C5	Bits 1-7	Bit 8	A	A	C
19	-	M	-	Bits 1-8				
20	1	-	-	Bits 1-8				
21	-	M	-	Bits 1-8				
22	-	-	C6	Bits 1-8				
23	-	M	-	Bits 1-8				
24	1	-	-	Bits 1-7	Bit 8	A	B	D

Notes:
1. FPS - Framing Pattern Sequence
2. FDL - Facility Data Link (4 KHz M = Message Bits)
3. CRC - Cyclic Redundancy Check Bits
4. In case of clear channel, bit 8 will be used for data and not signaling.
5. Users can support 2 state, 4 state or 16 state signaling with the following outputs (TMO, TSIGFR, TSIGSEL, RMSYNC, RSIGFR, RSIGSEL).

TABLE 2
193S FRAMING FORMAT

Frame No.	F-Bit Use		Bit Use per Channel		Signaling
	FT[1]	FS[2]	Data Bits	Signaling Bits[4]	Bit Use
1	1	-	Bits 1-8		
2	-	0	Bits 1-8		
3	0	-	Bits 1-8		
4	-	0	Bits 1-8		
5	1	-	Bits 1-8		
6	-	1	Bits 1-7	Bit 8	A
7	0	-	Bits 1-8		
8	-	1	Bits 1-8		
9	1	-	Bits 1-8		
10	-	1	Bits 1-8		
11	0	-	Bits 1-8		
12	-	0[3]	Bits 1-7	Bit 8	B

Notes:
1. FT - Terminal Framing Bits provide frame alignment.
2. FS - Signaling Frame Bits provide multiframe alignment.
3. For clear channel, bit 8 is used for data and not signalining.
4. The S bit in frame 12 may be used for yellow alarm transmission and detection for some applications.

RECEIVER FUNCTIONS

RECEIVE CODE INSERTION

Incoming receiver channels can be replaced with idle (7F Hex) or digital milliwatt (u-LAW format) codes. The receiver mark registers indicate which channels are inserted. When set, RCR bit-5 serves as a "global" enable for marked channels, and RCR bit-4 selects inserted code format: 0=idle code, 1=digtal milliwatt.

RECEIVER SYNCHRONIZER

RCR bit-0 through RCA bit-3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate quality testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

SYNC TIME

The RCR bit-2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR bit-2 is set to "1", the algorithm will validate 24 bits; if RCA bit-2 is set to "0", 10 bits are validated. 24 bit testing results in superior false framing protection, while 10 bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

RESYNC

A zero to one transition of RCR bit-0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

SYNC ENABLE

When RCR bit-1 is cleared, the receiver will initiate automatic resync if any of the following events occur: A) an out of frame (OOF), or B) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR bit-1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR bit-0 to "1", or externally via a low to high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receiver output timing while $\overline{RST}$ is low; use of RCR bit-1 does not affect output timing until the new alignment is located.

RECEIVER LOSS OF SYNC OUTPUT

The RLOS output of XR-T5690 indicates the status of the receiver synchronizer circuitry: when high, an off line resynchronization is in progress and a high low transition indicates resync is completed. The RLOS bit (RSR bit-0) is a "latched" version of the RLOS output. If the auto resync mode is selected (RCR bit-1=0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RESET

A high to low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

TRANSMITTER FUNCTIONS

TRANSMIT BLUE ALARM

The blue alarm is an unframed, all 1's sequence enabled by asserting TCR bit-1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR bit-1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM

In 193E framing a yellow alarm is a repeating pattern set of FF (HEX) and 00 (HEX) on the 4 KHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of CCR bit- 3. In all modes, yellow alarm is enabled by asserting TCR bit-0 and disabled by clearing TCR bit-0.

TRANSMIT SIGNALING

When enabled (Via TCR bit-4) channel signaling is inserted in frames 6 and 12 (193S), or 6, 12, 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate serial links for A, B, or A, B, C, D signaling sources.

TRANSMIT CHANNEL TRANSPARENCY

Individual DS0 channels in the T1 frame may be programmed clear by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data only environments such as ISDN, where data integrity must be maintained.

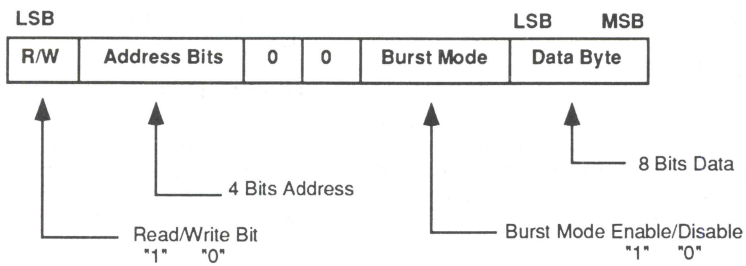


Figure 1 Serial Address /Command Format

Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. the following 4 bit nibble identifies register address. The next two bits are reserved and must be zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. Data is written to and read from the transceiver LSB first. (see Figure 1)

TRANSMIT IDLE CODE INSERTION

Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of the two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR bit-3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates extenal hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

SERIAL CONTROL INTERFACE

(See Figure 1 on previous page)

SERIAL PORT

Pin 14 through 18 of the XR-T5690 serve as a microprocessor or microcontroller compatible serial port. Sixteen on board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous read and/or writes by the host.

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the fishing edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tristated when $\overline{CS}$ is high.

DATA I/O

Following the 8 SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edge of the next 8 SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edge of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all on board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power up or system reset. Burst mode is initiated when ACB bit-7 is set and the address nibble is "0000". Burst is terminated by low to high transition on $\overline{CS}$.

HARDWARE MODE

For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying this pin to Vss disables the serial port, clears all internal registers except CCR, TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROLS

In the hardware mode TCR bit-2, CCR bit-4, TCR bit-0, CCR bit-1 and CCR bit-2 map to pins 14 through 18. The loopback feature (CCR bit-0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched when both pins are taken high, preserving the current zero suppression mode). Robbed bit signaling (TCR bit-4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. CCR bit-3 is forced to 0, which selects yellow alarm bit- 2 in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in hardware mode. The $\overline{RST}$ input may be used to force immediate receiver resync, and has no effect on transmit.

ALARMS

ALARM OUTPUTS

The transceiver provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on board alarm logic.

YELLOW ALARM OUTPUT

The RYEL output of XR-T5690 will go high when a yellow alarm is detected. A high to low transition indicates the alarm condition has been cleared. The RYEL bit (RSR bit-5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 HEX and FF HEX received at RLINK or a "O" in the bit 2 position of all channels. In 193S framing the yellow alarm format is dependent on CCR bit-3: if CCR bit-3=0, the RYEL output transitions high if bit 2 of 156 or more consecutive channels is 0; if CCR bit-3=1, yellow alarm is detected when the S- bit received in frame 12 is 1.

BIPOLAR VIOLATION OUTPUT

The RBV output transitions high when accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

RECEIVE FRAME OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing F^T and F^S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low to high to low transition (one bit period wide) one half RCLK period before a low to high transition on RMSYNC.

RECEIVE ALARM REPORTING

Incoming serial data is monitored by the transceiver for alarm occurrence. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt. Interrupts may be direct, in which case the transceiver demands service for a real time alarm, or count overflow triggered, in which case an on board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register.

ALARM SERVICING

The host controller must service the transceiver in order to clear an interrupt condition. Clear appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupt will be cleared when the RSR is read, unless the alarm condition still exists. Count overflow interrupts will be conditionally cleared by reading the RSR; the next event will trigger interrupt unless the user presents the appropriate count register.

COUNTERS

ALARM COUNTERS

The three on board alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presentable by the user, establishing an event count interrupt threshold. As each counter saturates, it will set a bit in RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

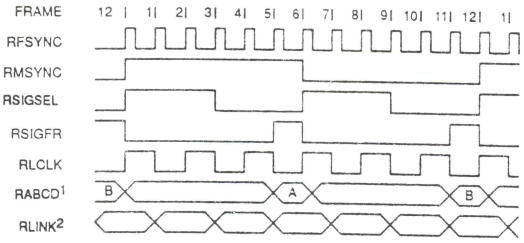
Out of frame is declared when two of four consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S; the FPS bits are tested in 193E. OOF events are recorded by the 4 bit OOF counter in the error count register. In the 193E framing mode, the OOF event is logically "OR'ed" with an on chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4 bit ESF error counter in the error count register. In the 193S framing mode, the 4 bit ESF error counter records individual F_T and F_S errors when RCR bit-3=1, or F_T errors only when RCR bit-3=0.

BIPOLAR VIOLATION COUNTER

This 8 bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation (RIMR bit-7=1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "UP" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

OOF AND ESF ERROR COUNTERS

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR bit-6=1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counter will count "UP" to saturation from the present value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously. The OOF counter records out of frame events in both 193S and 193E. The ESF error counter records errored superframes in 193E. In 193S the ESF counter records individual F_T and F_S errors when RCR bit-3=1; F_T errors only when RCR bit-3=0. ECR counter increments are disabled when resync is in progress (RLOS high).

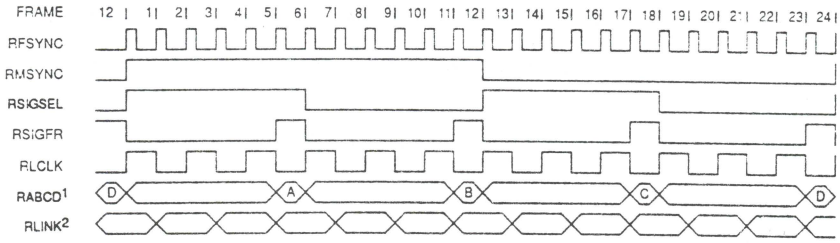


Note:

1. Signaling data is undated during signaling frames or channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.

2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193S Receive Multiframe Timing

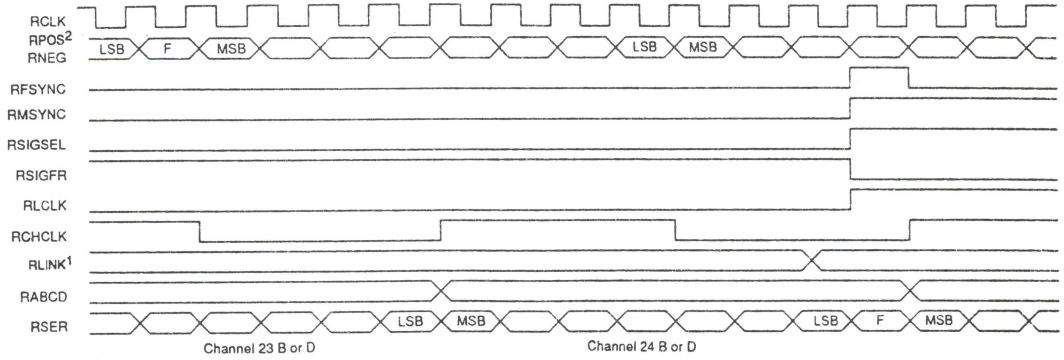


Note:

1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.

2. RLINK data (FDL-bit) is updated one bit-time prior to S-bit frames and held for two frames.

193E Receive Multiframe Timing

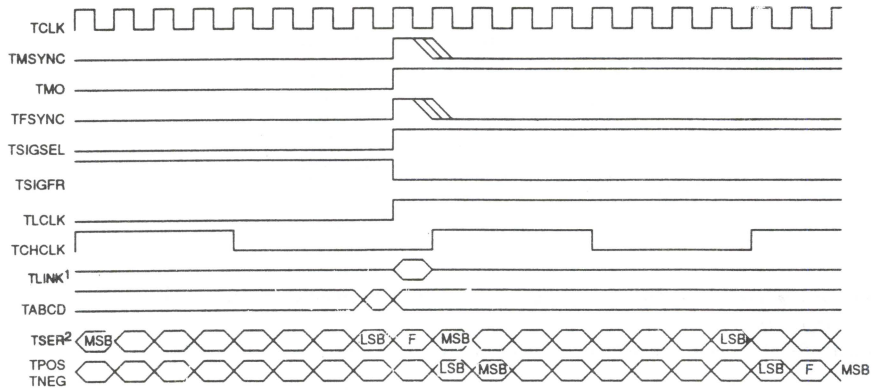


Note:

1. RLINK timing is shown for 193E; in 193S RLINK is updated on even frame boundaries and is held across multiframe edges.

2. Total delay from RPOS and RNEG output is 13 clock periods.

Receive Multiframe Boundary Timing

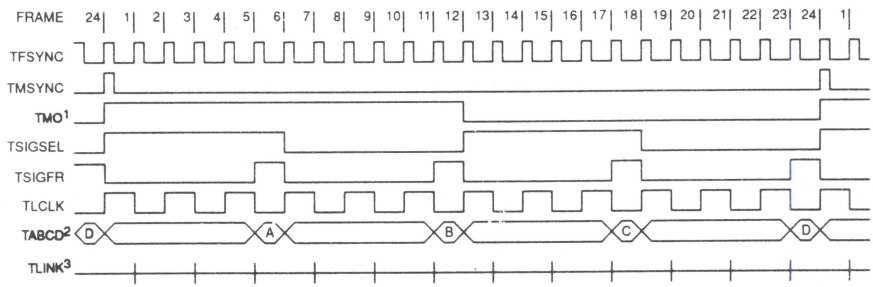


Note:

1. TLINK timing shown is for 193 E framing; where TLINK is a sampled as shown for insertion into F bit position of cold frames. When S-bit insertion is enabled in 193S. TLINK is sampled during even frames.

2. If TCR bit S=1; TSER is sampled during the F-bit time of CRC frames for insertion into the ougoing data stream (193E Framing only).

Transmit Multiframe Boundry Timing



Notes:

1. Establishing frame and multiframe:

a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries.

b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.

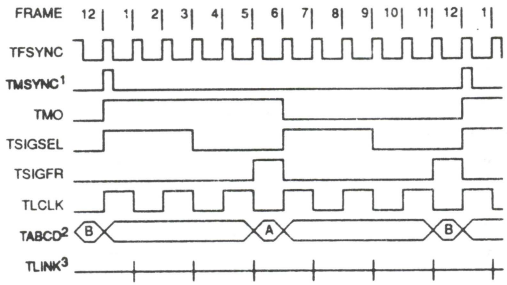
c) TMSYNC and TFSYNC may be continously pulsed to establish and reinforce frame and superframe timing.

d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitary multiframe boundary as indicated by TMO.

2. Channels with Robbed Bit Signaling enabled will sample TABCD during the LSB bit time in the frames indicated

3. TLINK is sampled during the F-Bit time of odd frames and inserted into the outgoing data stream (FDL data).

103E Transmit Multiframe Timing



Notes:

1. Establishing frame and multiframe:

a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries.

b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNBC once establishes multiframe boundaries.

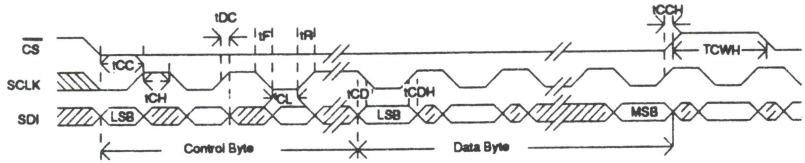
c) TMSYNC and TFSYNC may be continously pulsed to establish and reinforce frame and superframe timing.

d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.

2. Channels with Robbed Bit Signaling enabled will sample TABCD during the LSB bit time in the frames indicated.

3. When external S-bit insection is enabled. TLINK will be sampled during the F-Bit time of even frames and inserted into the outgoing data stream.

193S Transmit Multiframe Timing

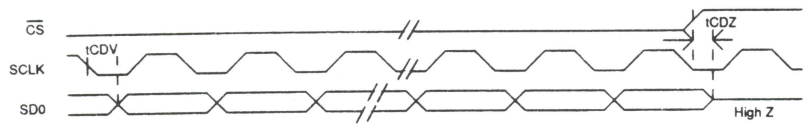


Notes:

1. Data byte must be valid across low clock periods to prevent transients in operating modes.

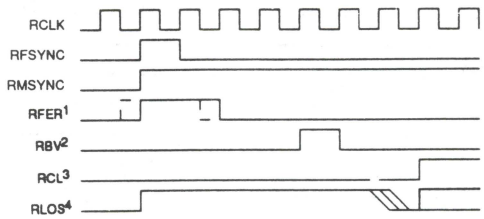
2. The shaded regions are don't care states of input data.

Serial Port Write AC Timing



Notes: 1. Serial port write must precede a port read to provide address information.

Serial Port Read[1] AC Timing



Note:

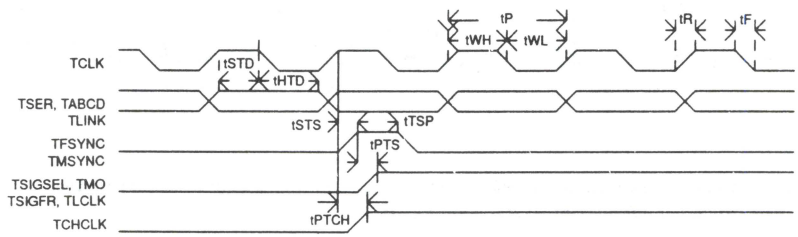
1. *RFER goes high during F-Bit if framing pattern is in error (Figure 12 F-bits are ignored if CCR bit 3=1). Also, in 193E Format, RFER transitions half a bit period before the rising edge of RMSYNC to indicate a CRC error.*

2. *RBV indicates received bipolar violations and transitions high together with the accused bit on RSER. If B8Zs is enabled RBV does not report the zero replacement code.*

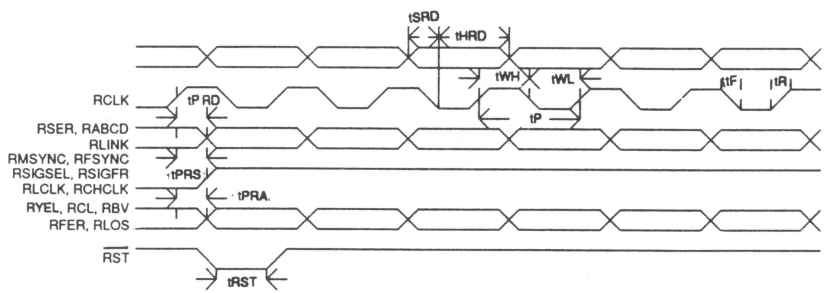
3. *RCL transitions high after 32 consecutive "0" bits are received. It goes low when the next "1" is received.*

4. *RLOS transitions high during the F-bit time that caused the OOF event if autoresync mode is selected (RCR-1 = 0)(2 out of 4 consecutive F-T or FPS bits are in error). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR 1=1 RLOS remains low until resync occurs, regardless of OOF carrier loss flags. In this situation, resync is initiated only when RCR-0 transitions low to high or RST pin transitions, high to low to high.*

Alarm Output Timing



Transmit AC Timing



Receive AC Timing

T1 Receive Buffer

GENERAL INFORMATION

The XR-T5691 is designed to synchronize receive loop-timed T-carrier data streams to systems side timing. It is very flexible and allows interfacing of incoming data to parallel or serial TDM backplanes. It is implemented using low power CMOS technology and is available in a "skinny" 24 lead plastic DIP & 24 pin PLCC packages. This device operates in conjunction with the XR-T5690 Framer and is capable of extracting, buffering and integrating ABCD Signaling.

FEATURES

Synchronizes T1 Data Streams to System Clocks
Two Frame Buffer Depth
Frame Slip Output at Frame Boundaries
Buffer Recentering Capability
Ideal for T1 (1.544MHz) to cept (2.048MHz) rate conversion
Interfaces to Parallel and Serial Backplanes
Robbed-bit Signaling Updates During Alarm or Slip Conditions
Integration Feature "Debounces" Signaling
Pin to Pin and Functionally Compatible to DS2176

APPLICATIONS

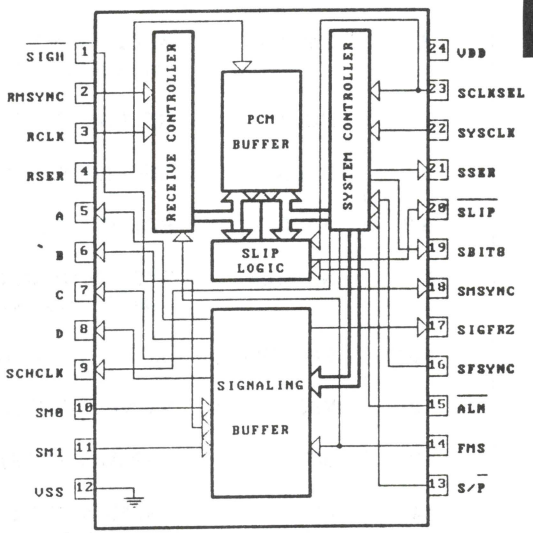
Digital Trunks
Drop and Insert Equipment
Transcoders
Digital Cross Connects
Private Network Equipment
PABX's
DMI's
CPI's

ABSOLUTE MAXIMUM RATINGS

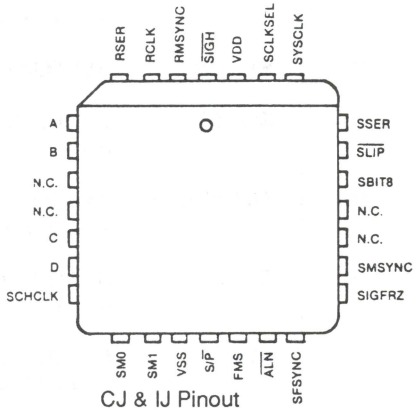
Input Voltage	-1.0V to 7.0V
Storage Temperature	-65°C to +150°C
Soldering Temperature	260°C for 10sec

NOTE: Stresses exceeding those specified above may cause permanent damage to the device or reduce normal operating life.

PIN ASSIGNMENT



CP & 1P Pinout



CJ & IJ Pinout

ORDERING INFORMATION

Part Number	Package	Operating Temp.
T5691 IP	Plastic	-40°C to +85°C
T5691 IJ	PLCC	-40°C to +85°C
XR-T5691CP	Plastic	0°C to 70°C
XR-T5691CJ	PLCC	0°C to 70°C

PIN DESCRIPTION

Pin #	Symbol	Description
1	SIGH	**SIGNALING INHIBIT.** When low it disables ABCD signaling updates for a period determined by SM0 and SM1 or until returned to high.
2	RMSYNC	**RECEIVE MULTIFRAMES SYNC.** When high during multiframe boundaries it establishes frame and multiframe alignment.
3	RCLK	**RECEIVE CLOCK.** Extracted 1.544 MHz clock.
4	RSER	**RECEIVE SERIAL DATA.** Sampled during the falling edge of RCLK.
5-8	A/B/C/D	**ROBBED-BIT SIGNALING OUTPUT A-D.**
9	SCHCLK	**SYSTEM CHANNEL CLOCK.** Needed for serial to parallel conversion of channel data. Transitions occur during channel boundaries.
10/11	SM0/SM1	**SIGNALING MODES** 0 AND 1. Select signaling logic.
12	VSS	**SIGNAL GROUND.**
13	S/P	**SERIAL TO PARALLEL SELECT.** Parallel (tie to VSS). Serial (tie to VDD).
14	FMS	**FRAME MODE SELECT.** For 193S Framing (tie to VSS) for 193E Framing (tie to VDD).
15	$\overline{\text{ALN}}$	**ALIGN.** When forced low, it recenters the buffer on the next system side frame boundary.
16	SFSYNC	**SYSTEM FRAME SYNC.** Rising edge establishes the start of the frame.
17	SIGFRZ	**SIGNALING FREEZE.** Indicates signaling updates when high. These can be caused internally via a slip or externally by forcing SIGH low.
18	SMSYNC	**SYSTEM MULTIFRAME SYNC.** Slip-compensated multiframe output; indicates when signaling updates are made.
19	SBIT8	**SYSTEM BIT 8.** Intended to reinsert the extracted signaling into the outgoing data stream. It is high during the LSB time of each channel.
20	$\overline{\text{SLIP}}$	**FRAME SLIP.** (Active low). Indicates a slip and held low for 64 SYSCLK cycles. Open collector output.
21	SSER	**SYSTEM SERIAL OUT.** Output data updated on the rising edge of SYSCLK.
22	SYSCLK	**SYSTEM CLOCK.** 1.544 MHz or 2.046 MHz clock.
23	SCLKSEL	**SYSTEM CLOCK SELECT. 1.544 MHz** (tie to VSS); 2.048 MHz (tie to VDD).
24	VCC	**POSITIVE SUPPLY VOLTAGE.** 5.0V +/- 10%.

SYSTEM DESCRIPTION

The XR-T5691 is designed to synchronize the received T1 PCM data (loop timed) to the host backplane, and also to supervise the robbed-bit signaling information embedded in the data stream. This device is intended to operate in conjunction with the XR-T5690 "T1 Framer" and the XR-T56L22 "T1 Line Receiver" to offer a complete system solution.

Synchronization

The XR-T5691 buffers the incoming PCM data from RSER into a 2-frame buffer (386 bits long). This data is sampled on the falling edge of RCLK and appears back at SSER where it is updated on the rising edge of SYSCLK. The frame and multiframe alignment on the receive side is established with the rising edge of RMSYNC. On the system side, a rising edge of SFSYNC establishes frame alignment. Buffer depth monitoring is done by an on board contention logic which signals a "slip" whenever the buffer is completely emptied or filled. After the occurence of a "slip", the SLIP output (open collector) is held low for 64 clock cycles and the buffer recenters automatically to a one-frame boundary. This configuration is adequate for most T-carrier applications which need to synchronize under short term jitter conditions. The XR-T5691 offers a good compromise between total delay and slip correction capability.

Buffer depth monitoring is achieved by sensing the distance between the rising edge of RMSYNC and SMSYNC real time. The output pulse SMSYNC which indicates the system side multiframe boundaries, is held high for 65 SYSCLK cycles.

This device is compatible with the two most common backplane frequencies (1.544 and 2.048MHz) which can be selected by strapping SCLKSEL to VCC for 2.048MHz and to VSS for 1.544MHz operation. In 1.544MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. For 2.048MHz applications the F-bit is dropped, and the MSB of channel 1 appears at SSER after a one bit period delay following the rising edge of SFSYNC. For the excess channels (greater than 24), the SSER pin is forced high. Also the slip criteria for 2.048MHz applications is different because of the faster system side read frequency.

The XR-T5691 is capable of interfacing to serial and/or parallel backplanes. For serial applications (S/P = 1), the data from channel 1 appears at SSER after a rising edge at SFSYNC as illustrated in Figure 8. For parallel applications a look-ahead mechanism is used whereby data is made available 8 clock cycles prior to SCHCLK in order to convert parallel data externally.

Signaling

Robbed-bit signaling data is inserted into the LSB portion of each channel during signaling frames. Depending on the type of frame format used (193S or 193E), the signaling information is first extracted from the incoming frames and then presented at the corresponding outputs (A, B, C or D). In 193S framing (FMS=0), the "A" signaling bits is inserted into frame 6 and the "B" signaling data into frame 12. In 193E framing (FMS=1), four signaling bits are available, in which case the two additional bits "C and D" are inserted into frames 18 and 24 correspondingly. The outputs A, B, C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframes. In 193S applications, the two extra outputs "C and D" contain the previous "A and B" data. Signaling updates occur once per multiframe at the rising edge of SMSYNC unless otherwise prohibited by the freeze function.

This "freeze function", which occurs during a slip condition or by forcing SIGH low, inhibits any signaling updates during alarm or slip conditions. The duration of the freeze is dependent on SM0 and SM1. During this period "old" data is recirculated in the output registers, and SIGFRZ is held high until the next signaling update. The input to output delay of the signaling data is equal to 1 multiframe plus the current depth of the PCM buffer (1 multiframe + 1 frame +/-1 frame).

Integration is another feature of the XR-T5691 which minimizes the impact of random noise and possible robbed-bit signaling corruption. This requires that the per channel signaling data be in the same state for 2 or more multiframes before appearing at A, B, C or D. As to what degree of integration is required can be selected by toggling SM0 and SM1. In order to minimize update delay, integration is limited to 1 multiframe during slip or alarm conditions. This is shown in Table 1.

Concerning ISDN applications and per channel capability, in order to assure integrity of data, the XR-T5691 will not merge processed signaling information back into the outgoing PCM frame. SBIT8 indicates the LSB position of each channel which can be combined with off chip logic to selectively reinsert robbed-bit signaling data into the outgoing data stream.

			TABLE 1. SIGNALING SUPERVISION MODES
SM0	**SM1**	**FMS**	**SELECTED MODE**
0	0	0	193S framing, no integration, 1 multiframe freeze
0	0	1	193E framing, no integration, 1 multiframe freeze
0	1	0	193S framing, 2 multiframes integration & freeze
0	1	1	193E framing, 2 multiframes integration & freeze
1	0	0	193S framing, 5 multiframes integration & 2 multiframes freeze. (1)
1	0	1	193E framing, 3 multiframes integration & 2 multiframes freeze. (1)
1	1	0	Test mode.
1	1	1	Test mode.

Notes: 1) During a slip or alarm condition, integration is limited to 2 multiframes to minimize signaling delay.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V+/-10%, Ta = -40°C to +85°C unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Logic 1	2.0		V_{DD}+0.3	V	
V_{IL}	Logic 0	-0.3		+0.8	V	
V_{CC}	Positive Supply	4.5		5.5	V	
I_{CC}	Current Input		6	10	mA	Note 1, 2
I_{IL}	Leakage In Current	-1.0		+1.0	µA	
I_{OH}	Current Output High	-1.0			mA	Note 3
I_{OL}	Current Output Low	+4.0			mA	Note 4
I_{LO}	Leakage Output	-1.0		+1.0	µA	Note 5
C_{IN}	Input Capacitance			5	pF	
C_{OUT}	Output Capacitance			7	pF	

Notes: 1) TCLK = RCLK = 1.544 MHz
2) Outputs open
3) Measured @ 2.4V; all outputs except SLIP which is collector
4) All outputs
5) Applies to SLIP when tri-stated.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V+/-10%, Ta = -40°C to +85°C unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t RCLK	RCLK Period	250	648		ns	Figure 1
tR, tF	RCLK, SYSCLK Rise/Fall Time			20	ns	Figure 1
tRWH tRWL	RCLK Pulse Width	125	324		ns	Figure 1
tSWH tSWL	SYSCLK Pulse Width	100	244		ns	Figure 2
tSYSCLK	SYSCLK Period	200	488		ns	Figure 2
tSC	RMSYNC Setup to RCLK Rising	-tRWH/2		+tRWL/2	ns	Figure 1
tSC	SFSYNC Setup to SYSCLK Rising	-tSWL/2		-tSWL/2	ns	Figure 1 & 2
tPW	SFSYNC, SFSYNC $\overline{\text{SIGH}}$, $\overline{\text{ALN}}$ Pulse Width	100			ns	Figure 1 & 2
tHD	RSER Hold from RCLK Falling	50			ns	Figure 1
tSD	RSER Setup to RCLK Falling	50			ns	
tPVD	Propagation delay SYSCLK to SSER A,B,C,D			100	ns	Figure2
tPSS	Propagation delay SYSCLK to SMSYNC High			75	ns	Figure 2
tPS	Propagation delay SYSCLK or RCLK to SLIP low			100	ns	Figure 1 & 2
tPSF	Propagation delay SYSCLK to SIGFRZ			75	ns	Figure 2
tSR	ALN, SIGH Setup to SFSYNC Rising	500			ns	Figure 2

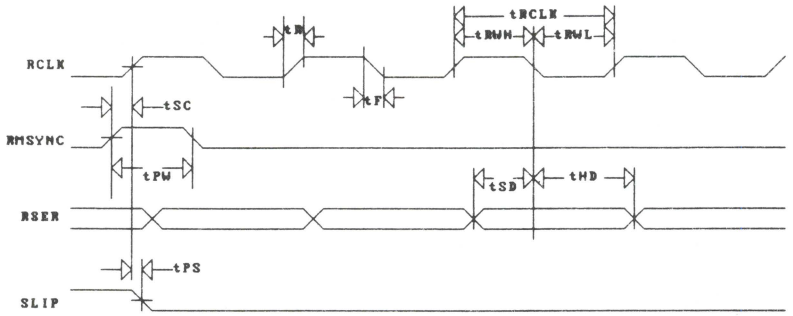


Figure 1. Receive A.C. Diagram

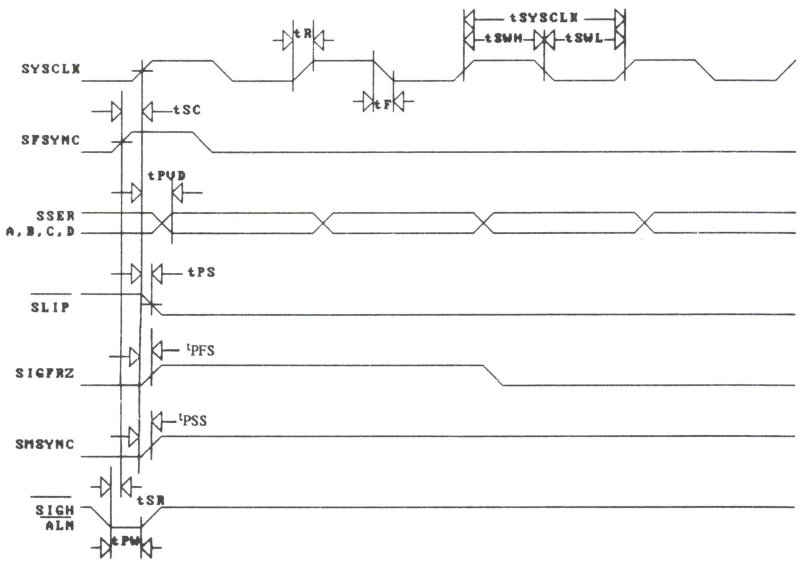


Figure 2. System AC Timing Diagram

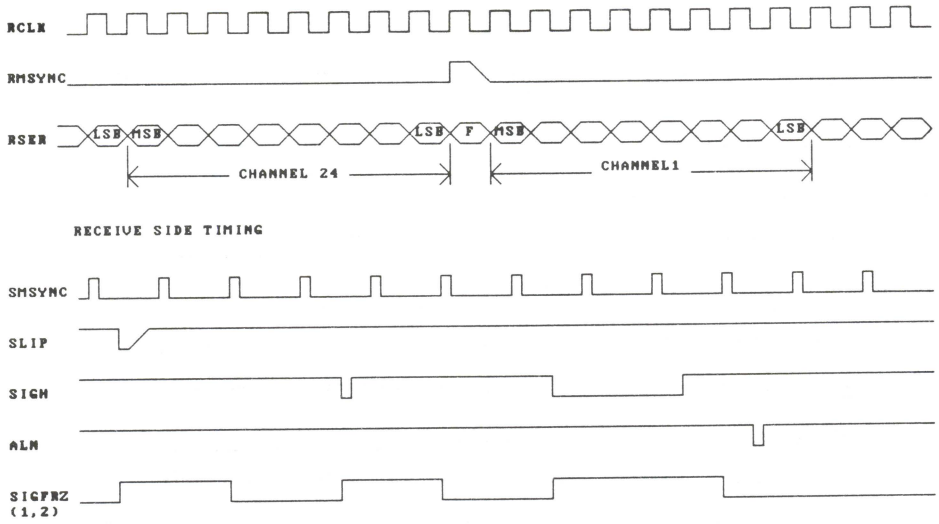


Figure 3. Slip and Signaling Supervision Logic Timing

Notes: 1) Integration feature disabled (SM0=SM1=0) in timing set shown.
2) Depending on present buffer depth, forcing ALN low may or may not cause a slip condition

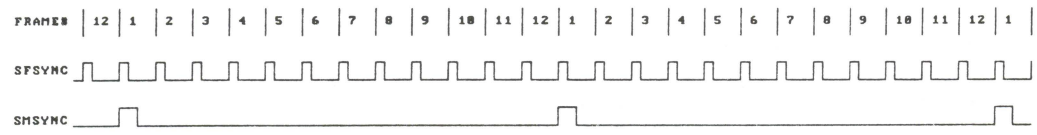


Figure 4. 193S System Multiframe Timing

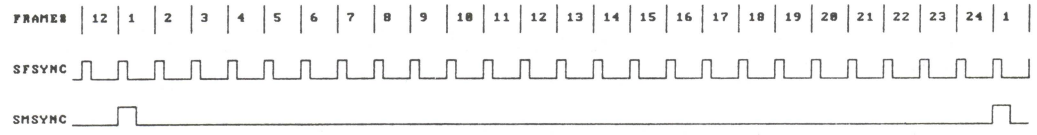


Figure 5. 193E System Multiframe Timing

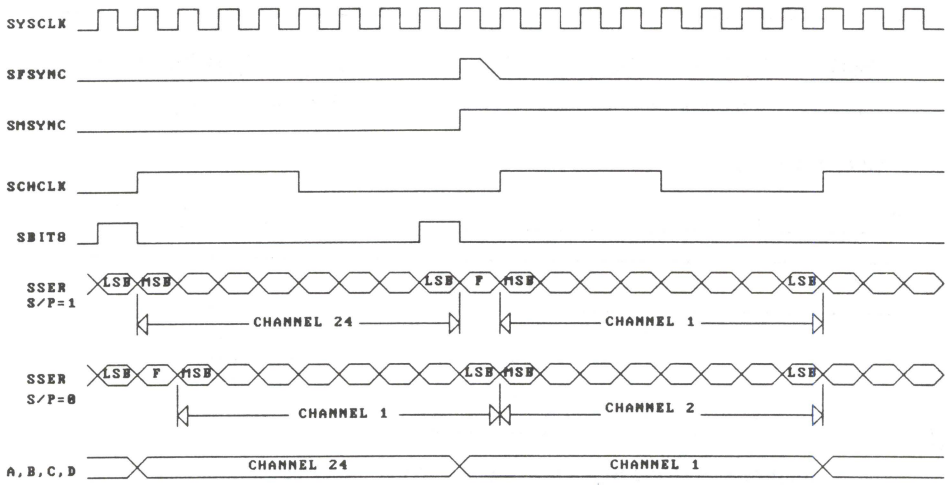


Figure 6. System Multiframe Boundry Timing (SYSCLM = 1.54 MHz)

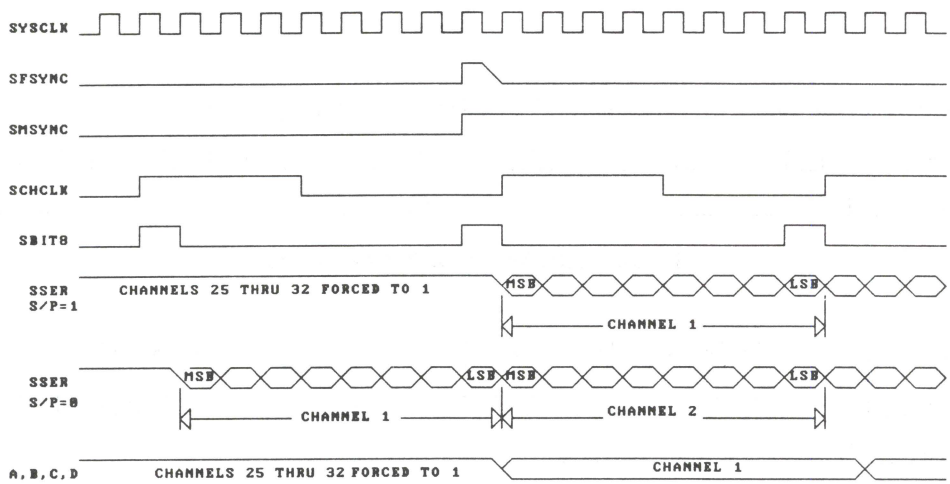


Figure 7. System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)

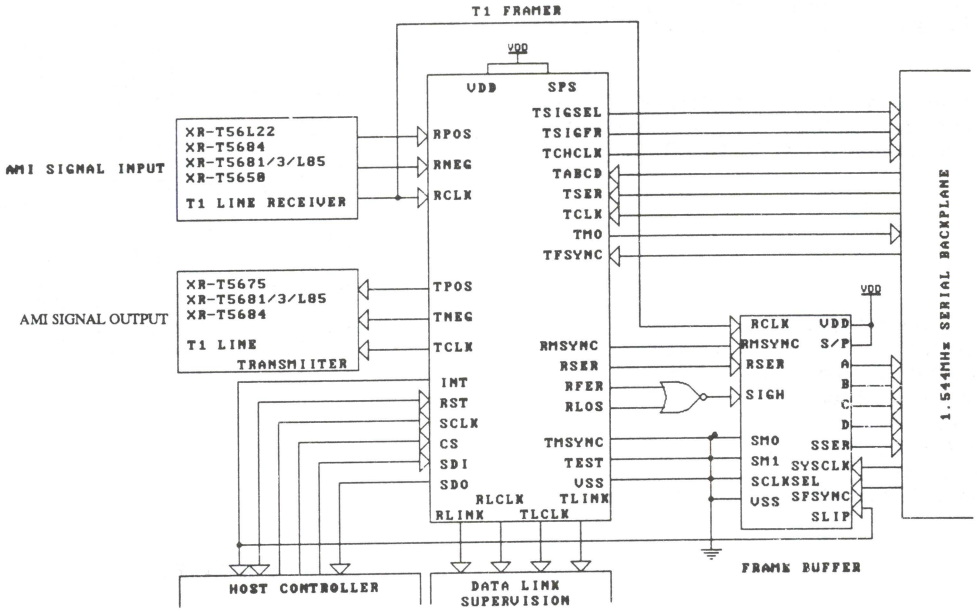


Figure 8. Typical Application using the XR-T5690 Framer and XR-T5691 Frame Buffer

Loopback Detector

GENERAL DESCRIPTION

The XR-T2713 is designed to be used with 4 wire maintenance terminating units in conjunction with manual or automatic testing systems in loopback mode to verify networK performance.

Utilizing switch capacitor technology, the IC detects the 2713 or 2813Hz signal and performs a loopback function in accordance with BELL PUB 43004.

FEATURES

Bell Pub 43004 Compliant
Uses standard color TV crystal (3.58MHz)
Detection band 2713 or 2813 +/- 15Hz
Detection level -32 dbm
Complementary output signals
Low power (4 mA @ 12 Volts)
CMOS process
Pin Selectable 4/20 Minutes Time-out

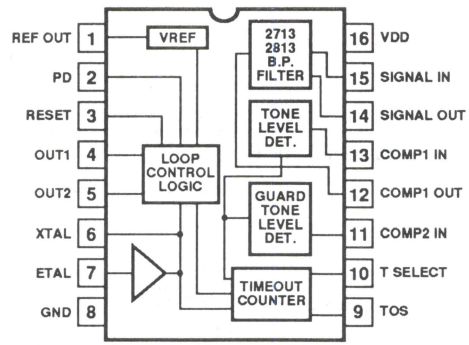
APPLICATION

4 wire maintenance terminating units

ABSOLUTE MAXIMUM RATINGS

DC Supply voltage	16 V
Voltage at any pin	GND -0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to 150°C
Operating temperature range	0°C to 70°C
Power Dissipation	100 mW

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T2713CP	Plastic DIP	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T2713 contains the necessary band pass filters to meet the BELL PUB 43004 requirements on minimum and maximum detection levels and frequency rejection band. For the specified frequency detection band, a digital filter is used to maintain narrow band-width and decision making.

The tone detection output will be activated when a continuous tone of 2713/2813 +/- 15Hz is present for 1.8 seconds. Deactivation of the loopback signal will take place when a continuous tone of 2713/2813 +/- 15Hz is present for 0.45 seconds. If the deactivation tone is not received for 4 or 20 minutes (pin selectable), the XR-T2713 will reset automatically. The output signal is TTL compatible with a maximum output current capability of 1.5mA.

PIN DESCRIPTIONS

Pin #	Symbol	Description
1	REF OUT	Voltage reference output pin
2	PD	The T2713 will be in power down mode when this pin is held high.
3	RESET	External power-up reset or manual loop back.(Figure 3).
4	OUT-1	Upon detection of the 2713/2813 tone for a minimum of 1.8 seconds, pin 4 will go high to indicate that the system has entered the test mode. These outputs will be deactivated when a 2713/2813 tone is present for a minimum of 450 msec. If no deactivation tone is received within 4 or 20 minutes(depending on the time out selection), the outputs will reset automatically OUT-1(see pin 4).
5	OUT-2	Complimentary output of OUT-1 (see pin 4).
6	XTAL	Crystal output pin.
7	ETAL	Crystal or external clock input pin.(Uses a standard color TVcrystal at 3.58MHz).
8	GND	Most negative supply pin or ground.
9	TOS	Time Out selection pin. A low at this pin selects a 4 minute time out. A high level extends the time-out to 20 minutes.
10	T-SELECT	A high level at this pin selects the 2813Hz dectection band and a low level selects the 2713Hz band.
11	COMP2 IN	Guardtone input coupled frompin 12.
12	COMP1 OUT	Guardtone output.
13	COMP1 IN	2713/2813 AC coupled frequency to tone and level detect circuitry.
14	SIGNAL OUT	2713/2813 Band pass filter output.
15	SIGNAL IN	Input of analog band pass filter.
16	VDD	Most positive supply.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A=25°C, V_{DD} =12V ±5% unless specified otherwise.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Supply Voltage		12		V	
I_{DD}	Supply Current		2	3	mA	
I_P	Output Sink Current	1.5			mA	
T_{DD}	Tone DetectionTime (on)		1.8		sec	Figure 1
T_{DF}	Tone Deactivation Time		.45		sec	Figure 1
T_{DO}	Detection on Time	20			msec	Figure 1
	Detection off Time	20			msec	Figure 1
T_{AB}	Tone Break			4	msec	Figure1
T_F	Time Out		20		min	PIN 9 high, Figure 2
			4		min	PIN 9 low, Figure 2
V_T	Detection Level	-32		0	dBm	
T	Detection Frequency	2698	2713	2728	Hz	PIN 10 high
		2798	2813	2828	Hz	PIN 10 low
V_R	Tone Rejection Level	-38			dBm	
V_G	Signal to Guard Ratio	6	8	12	dB	

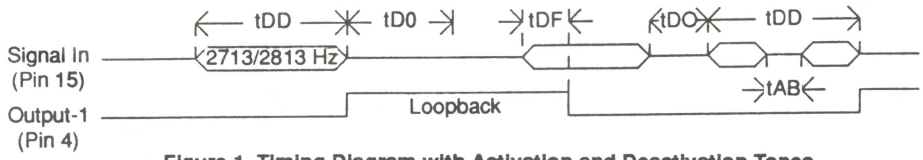


Figure 1. Timing Diagram with Activation and Deactivation Tones

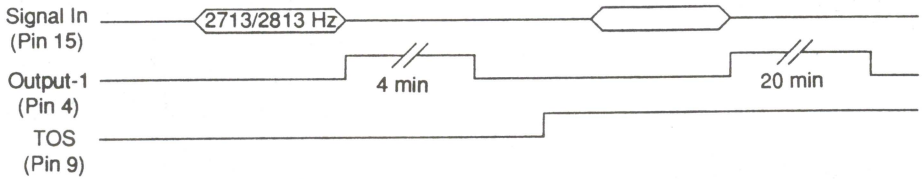


Figure 2. Timing Diagram without Deactivation Tone

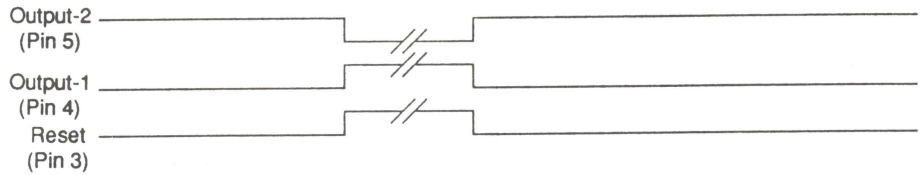
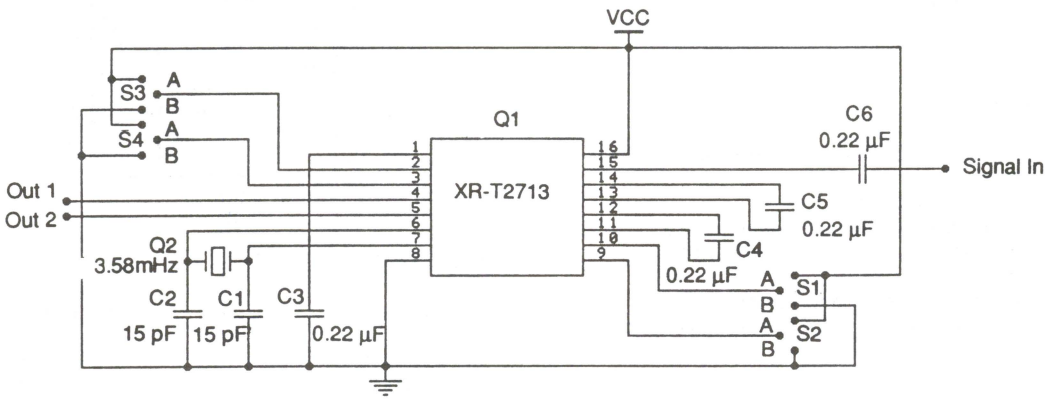


Figure 3. Manual Loopback Mode



	S4A	S4B
S3A	Factory Test	Power Down
S3B	Reset	Normal Op.

	A	B
S1	2813 Hz	2713 Hz
S2	20 min	4 min

Figure 4. Typical Application Circuitry

V.35 Interface Receiver/Transmitter

GENERAL DESCRIPTION

The V.35 chip set consists of two bipolar chips, one performing a receive function, the other a transmit function according to the specification requirements laid down in Appendix II of the V.35 CCITT Recommendation and Bell 306 modem interface specification.

Typical applications require three transmit and receive pairs to establish the link between distant DTE's at data rates ranging from 48Kbps to 10Mbps. To conserve power (especially in the case of the transmitter, which requires approximately 22mA for each output stage to meet CCITT specifications), power-down functions are included in both devices, allowing any of the three receive/transmit circuits to be disabled. All inputs and outputs are TTL compatible and designed to offer maximum versatility and performance.

Both the transmitter and receiver require termination resistors external to each device, to meet the V.35 specification tolerance.

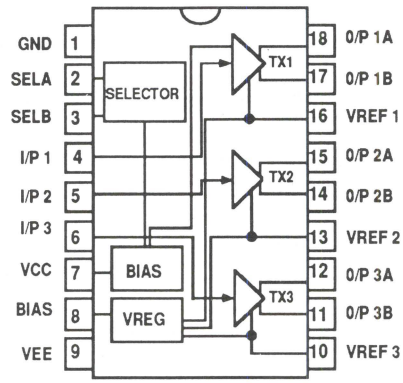
FEATURES

Compatible with CCITT V.35 and Bell 306 Interface Requirements
TTL Input Compatibility
High Common Mode Output Voltage Range
Excellent Stability over Supply and Temperature Range
High Speed Operation (up to 10Mbps)
Individual Receive/Transmit Power-down capability

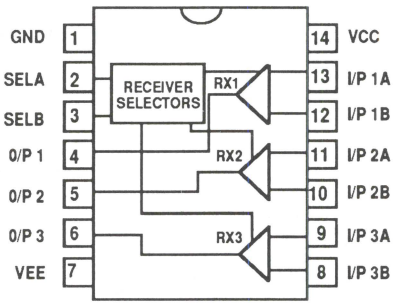
APPLICATIONS

High Speed Data Transmission Systems
Short Haul Modems
Signal Converters and Adapters
Network and Diagnostic Systems
Matrix Switches
Modem Emulators

PIN ASSIGNMENT



XR-T3588
TRANSMITTER



XR-T3589
RECEIVER

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T3588CN	Ceramic	0°C to 70°C
XR-T3589CN	Ceramic	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±7V
Storage Temperature	-65°C to +150°C
Power Dissipation	
XR-T3588CN	1000mW
XR-T3589CN	300mW

TRANSMITTER: XR-T3588
SYSTEM DESCRIPTION

The function of the transmitter is to take a TTL input signal at a maximum bit rate of 10Mbps and output a balanced differential signal with a peak amplitude of 0.55V and a maximum DC offset of 0.6V. An internal buffer provides the regulated output voltage to set the mean level of the transmitters to less than 0.6V.

To meet the pulse shape and offset requirements laid down in the V.35 specification, the transmitter employs an internal temperature compensated voltage generator to provide reference voltages for both offset control and output current generation. Load resistors for the output stage, which provide the required source impedance for the transmitter, are external to the IC and are required to meet the V.35 specified tolerance.

To generate well defined output pulses, device current is set using an external resistor, which should be of the same type as the transmitter load resistors. Each device contains three independent transmit circuits.

Individual transmitters may be shut down to achieve power savings for applications not requiring three channels. Two TTL compatible inputs provide four combinations of transmitter configurations, as defined in table 1. If either of the select pins is left open a high state is adopted, hence with no inputs applied, all channels are powered up.

TRANSMITTER	SEL A	SEL B
1-2-3	HIGH	HIGH
1-2	HIGH	LOW
1	LOW	HIGH
ALL OFF	LOW	LOW

TABLE 1. TRANSMITTER SELECTORS

XR-T3588 DC ELECTRICAL CHARACTERISTICS (TRANSMITTER)
Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 0°C to 70°C

SYMBOL	PARAMETER	PINS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC}	Positive Supply Voltage	7	4.75	5	5.25	V	
V_{EE}	Negative Supply Voltage	9	-4.75	-5	-5.25	V	
I_{CC}	Input Current	7		86	124	mA	
I_{EE}	Input Current	9		-92	-132	mA	
I_{PDL}	Power-down Input Current Low	2-6		-0.4		mA	Per Transmitter
I_{PDH}	Power Down Input Current High	2-6			50	mA	
I_{PCCO}	Power Down I_{CC} Current			9.2		mA	No Termination Resistors
I_{PEEO}	Power Down I_{EE} Current			11.6		mA	Mo Termination Resistors
I_{PCCT}	Power Down I_{CC} Current			51		mA	With Termination Resistor
I_{PEET}	Power Down I_{EE} Current			11.6		mA	With Termination Resistors
D_{IH}	High Level Input Voltage		2	2.5	V_{CC}	V	Data Inputs
D_{IL}	Low Level Input Voltage			0.4	0.8	V	Data Inputs
V_{SIH}	Selector High Level Voltage	2&3	2	2.5	V_{CC}	V	
V_{SIL}	Selector Low Level Voltage	2&3		0.4	0.6	V	
V_{OL}	Output Low Voltage			-0.275		V	*(NOTE 1)*
V_{OH}	Output High Voltage			0.275		V	*(NOTE 1)*
Z_S	Source Impedance		90	100	110	0hm	per CCITT V.35
R_{GND}	Resistance to GND		135	150	165	0hm	per CCITT V.35
I_{INH}	Input Current High			-10		µA	
I_{INL}	Input Current Low			1		mA	
I_{ODIFF}	Output Current Differential			22		mA	with 3.9K bias resistor *(NOTE 3)*

NOTE 1. *O/P Terminated with 100 Ohm Differential Load across external network pins 11, 12, 14, 15, 17, 18.*
NOTE 2. *O/P Terminated with External Network pins 11,12, 14, 15, 17, 18.*
NOTE 3. *O/P Terminated with External Network, common mode resistance between any pair of generator outputs and ground.*

AC CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{(PLH)}$	Input (I/P to O/P)		25	50	nsec	***(NOTE 1)***
$t_{(PHL)}$	Input 1, 2, 3		25	50	nsec	***(NOTE 1)***
t_R	TX Rise Time		10	20	nsec	***(NOTE 1)***
t_F	TX Fall Time		10	20	nsec	***(NOTE 1)***

NOTE 1. *O/P Terminated with External Network.*

RECEIVER: XR-T3589
SYSTEM DESCRIPTION

The XR-T3589 Line Receiver contains three identical receive circuits to complement the XR-T3588 Line Transmitter. Received differential signals are converted into a single TTL compatible output. The input stage is designed to meet the full V.35 noise and common mode input specification.

Individual receivers may be shut down to achieve power savings for applications not requiring three channels. Two TTL compatible inputs provide four combinations of transmitter configurations, as defined in table 2. If either of the select pins is left open a high state is adopted, hence with no inputs applied, all channels are powered up.

RECEIVER	SEL A	SEL B
1-2-3	HIGH	HIGH
1-2	HIGH	LOW
1	LOW	HIGH
ALL OFF	LOW	LOW

TABLE 2. RECEIVER SELECTORS

XR-T3589 DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 0°C to 70°C

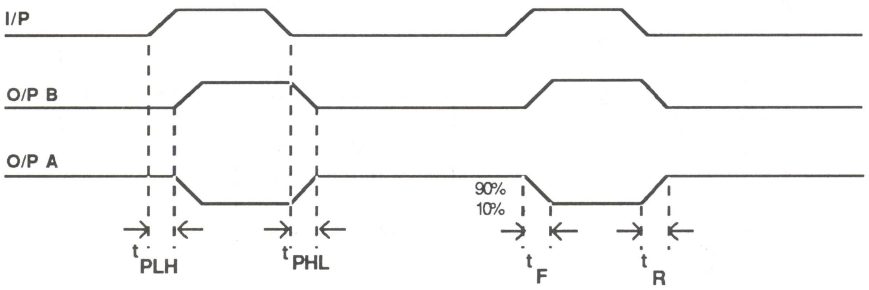
SYMBOL	PARAMETER	PINS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC}	Supply Voltage	14	4.75	5	5.25	V	
V_{EE}	Supply Voltage	7	-4.75	-5	-5.25	V	
I_{CC}	Input Current	14		40	60	mA	
I_{EE}	Input Current	7		7	9	mA	
I_{CCH}	High Level Current	4,5,6	40			µA	
V_{CCL}	Low Level Current	4,5,6			-1.6	mA	
V_{OH}	High Level Output	4,5,6	2.4			V	
V_{OL}	Low Level Output	4,5,6			0.4	V	
Z_{IN}	Input Impedance		8			KOhm	Differential ***(NOTE 2)***
Z_{IN}	Input Impedance		90	100	110	Ohm	per CCITT V.35 ***(NOTE 1,2)***
R_{GND}	Resistance to GND		135	150	165	Ohm	per CCITT V.35 ***(NOTE 1,2)***
V_{TH}	Power-down Threshold Voltage			2		V	
I_{PCC}	Power Down I_{CC} Current			1.1		mA	
I_{PEE}	Power Down I_{EE} Current		0.3		mA		

NOTE 1. *I/P Terminated with External Network*
NOTE 2. *Pins (8,9), (10,11), (12-13)*

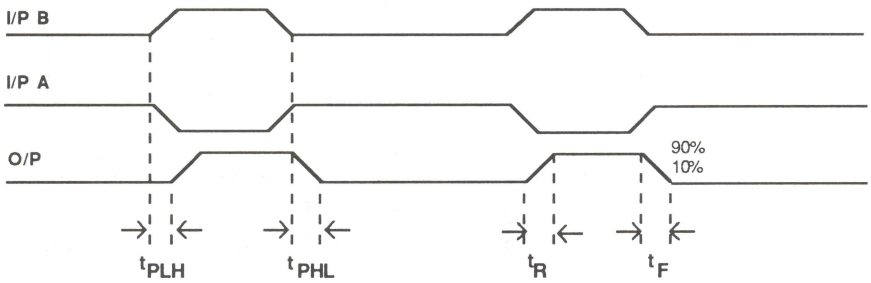
AC CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, V_{EE} = -5V ± 5%, T_A = 0°C to 70°C

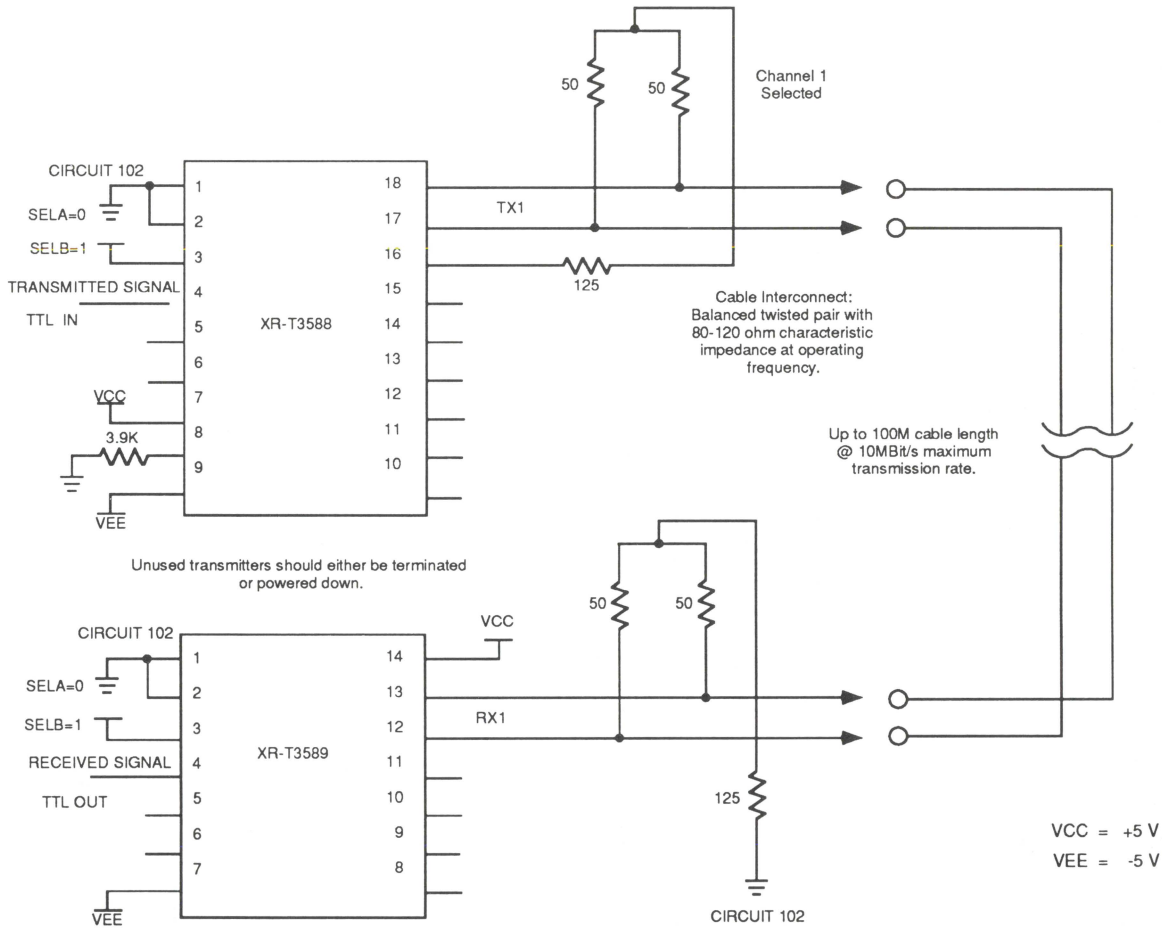
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{(PLH)}$	Input 1, 2, 3		50	70	nsec	
$t_{(PHL)}$	Input 1, 2, 3		50	70	nsec	
t_R	RX Rise Time		18	40	nsec	
t_F	RX Fall Time		12	30	nsec	



TRANSMITTER WAVEFORMS



RECEIVER WAVEFORMS



APPLICATION CIRCUIT XR-T3588, XR-T3589
(TERMINATION DIAGRAM)

PCM Line Receiver & Clock Recovery Circuit

GENERAL DESCRIPTION

The XR-T5650 is a monolithic bipolar IC designed for PCM type line receiver applications operating at T1. T148C, T1C and 2 MBPS data rates, It provides all the active circuitry required to perform Automatic Line Build Out (ALBO), threshold detection, positive and negative data and clock recovery.

Clock recovery using a crystal filter instead of an LC tank circuit is also available as XR-T5750.

FEATURES

On Chip Positive and Negative Data, Clock Recovery
Less than 10ns Sampling Pulse over the Operating Range
Double Matched ALBO Ports
Single 5.1V Power Supply
2 MBit/s Capability

APPLICATIONS

T1 PCM Line Receiver
T148C Line Receiver
T1C PCM Line Receiver (requires external amplifier)
General Purpose Bipolar Line Receiver
HDB3 Line Receiver
B8ZS Line Receiver

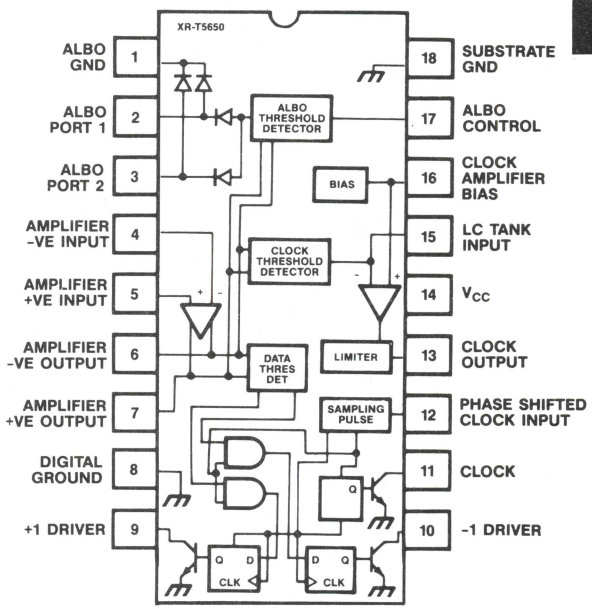
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	–40° to +85°C
Supply Voltage	–0.5 to +10V
Supply Voltage Surge (10ms)	+25V
Input Voltage (except Pins 2, 3, 4, 17)	–0.5 to 7V
Input Voltage (Pins 2, 3, 4, 17)	–0.5 to +0.5V
Data Output Voltage (Pins 10, 11)	20V
Voltage Surge (Pins 5, 6, 10, 11) (10msec only)	50V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5650	Ceramic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-T5650 is designed for interfacing T1, T148C and 2 MBPS PCM carrier lines on plastic or pulp insulated cables. It can also be used at T1C rate (3.152 MBPS) with external gain. Since it outputs plus and minus ones on a bipolar pulse stream together with the clock, it can be used to interface systems having different line codes like AMI, AMI-B8ZS or AMI-HDB3.

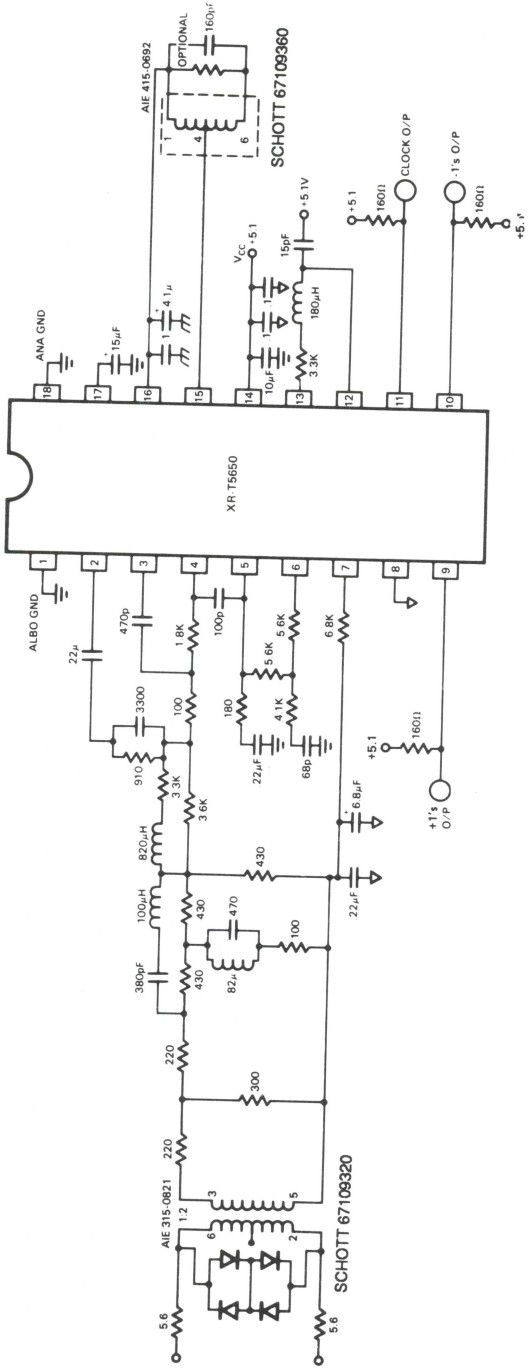
The XR-T5650 is a modified version of XR-T5620 PCM repeater IC. It contains all the active circuitry needed to build a PCM line receiver up to 6300 ft. cable length. The preamplifier, the clock amplifier, threshold detectors, data latches and output drivers are similar to the ones on XR-T5620. Clock extraction is done by means of an LC tank circuit.

In addition to plus and minus outputs, a synchronous clock signal is made available at Pin 11 by deleting one of the ALBO ports on XR-T5620 thus leaving two matched ALBO ports. All outputs have high current open collector transistors.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1V ± 5%, T_A = 25°C unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Supply Current		26	34	mA	ALBO Off
	Clock & Data					
	Output Leakeage Current		0	100	µA	$V_{pull\text{-}up}$ = 15V
	Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
	Amplifier Output Offset Voltage	–50	0	50	mV	R_S = 8.2kΩ
	Voltage Swing	2.2			V	Measured Differentially from Pin 7 to Pin 6
	Amplifier Input Bias Current			5	µA	
	ALBO on Current	3			mA	
	Drive Current		1		mA	
AC CHARACTERISTICS						
	Pre Amplifier AC Gain @ 1MHz		50		dB	
	Input Impedance	20			kΩ	
	Output Impedance			200	Ω	
	Clock Amplifier AC Gain		32		dB	
	–3dB Bandwidth	10			MHz	
	Delay		10		ns	
	Output impedance			200	Ω	
	ALBO					
	Off Impedance	20			kΩ	
	On Impedance			25	Ω	
CLOCK DATA OUTPUT BUFFERS						R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1V ± 5%
	Rise Time		30		ns	
	Fall Time		30		ns	
	Output Pulse Width		244		ns	
	Sample Pulse Width		10		ns	
	V_{OL}		0.7		V	
	I_L sink		35		mA	
THRESHOLDS						
	ALBO	1.4	1.5	1.6	V	
	Clock Drive Current Peak		1.0		mA	At V_O = V_{ALBO} Threshold
CLOCK THRESHOLD						
	% of ALBO	63	69	75	%	
DATA THRESHOLD						
	% of ALBO	40	46	52	%	



1.544 MBits/sec Universal PCM Line Receiver Application Circuit
Random Pattern — Max. Cable Loss 36dB

Dual Line Driver

GENERAL DESCRIPTION

The XR-T5675 is a bipolar monolithic dual line driver designed to drive PCM lines up to a 10 MBPS rate. The device is powered from a single 5V ± 5% source. Its current consumption is 14mA (typical) and the output can be pulled up to 20VDC.

FEATURES

50mA Output Drive Current Capability
Low Current Consumption (18mA Max.)
High Speed Switching
Dual Matched Driver Outputs
High Output Voltage
TTL or DTL Compatible Inputs

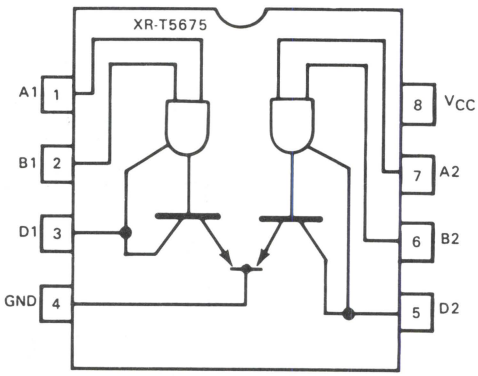
APPLICATIONS

T1, T1C, T2, 2.048MBPS and 8.448MBPS PCM Line Driver
LAN Line Driver
Relay Driver
LED/Lamp Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	+7.0V
Input Voltage (Pin 1,2,6,7)	–0.2V to +V_{CC}
Output Pull-up Voltages (Pin 3,5)	+35.0V
Power Dissipation	
Ceramic	700mW
Plastic	600mW
Storage Temperature	–65°C to 150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5675CP	Plastic	0°C to +70°C
XR-T5675CN	Ceramic	0°C to +70°C
XR-T5675 D	SOIC	0°C to +70°C

SYSTEM DESCRIPTION

Figure 1 contains the Functional Block Diagram of the XR-T5675. The circuit consists of two AND logic gates with their outputs internally connected to the bases of the output transistors. The low level outputs are clamped at 1 VBE to ground to insure non-saturating operation for fast switching.

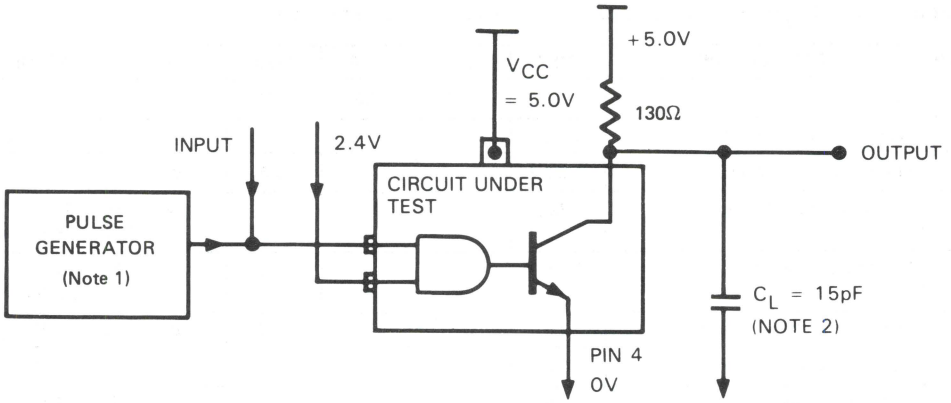
A	B	OUTPUT (D)
L	L	H (OFF)
L	H	H (OFF)
H	L	H (OFF)
H	H	L (ON)

Truth Table — XR-T5675
H = High Level, L = Low Level

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V, T_A = 0°C to +70°C, unless specified otherwise,

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CC}	Supply Voltage	8	4.75	5.0	5.25	V	
V_{IH}	High Level Input Voltage	1,2,6,7	2.2			V	I_{OL} = 50mA, V_{OL} = 0.95V
V_{IL}	Low Level Input Voltage	1,2,6,7			0.8	V	
I_{IH}	High Level Input Current	1,2,6,7			40	µA	V_{IH} = 2.7V, Pins 3 & 5 Open
I_{IL}	Low Level Input Current	1,2,6,7			−1.2	mA	V_{IL} = 0.4V, Pins 3 & 5 Open
V_{OL}	Low Level Output Voltage	3,5	0.6		0.95	V	V_{IH} = 2.2V, I_{OL} = 50mA
I_{OL}	Low Level Output Current	3,5			50	mA	V_{IH} = 2.2V, V_{OL} = 0.95V
I_{OH}	High Level Leakage Current	3,5			100	µA	Pins 3 & 5, Pull-up to +20V
I_{ccH}	Supply Current Output High	8			3.0	mA	Pins 3 & 5 Open
I_{ccL}	Supply Current Output Low	8		14.0	18.0	mA	Pins 3 & 5 Open
SWITCHING CHARACTERISTICS, V_{CC} = 5.0V ± 5%, T_A = +25°C							
t_{pLH}	Propagation Delay, Low to High	3,5		15		ns	See Figure 2
t_{pHL}	Propagation Delay, High to Low	3,5		15		ns	See Figure 2
t_{rise}	Rise Time	3,5		15	24	ns	See Figure 2
t_{fall}	Fall Time	3,5		10	24	ns	See Figure 2
	Output Pulse Imbalance			2.5		ns	At 50% Output Level



Note 1. Pulse Generator Frequency = 2.0MHz, Z_{OUT} = 50Ω.
Note 2. C_L Included — Probe and Jig Capacitance

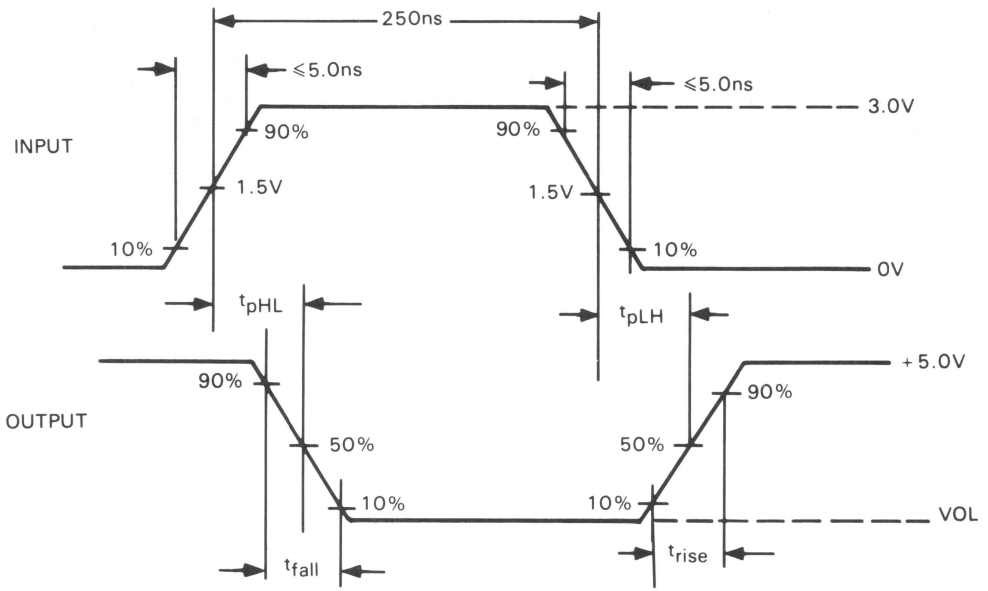
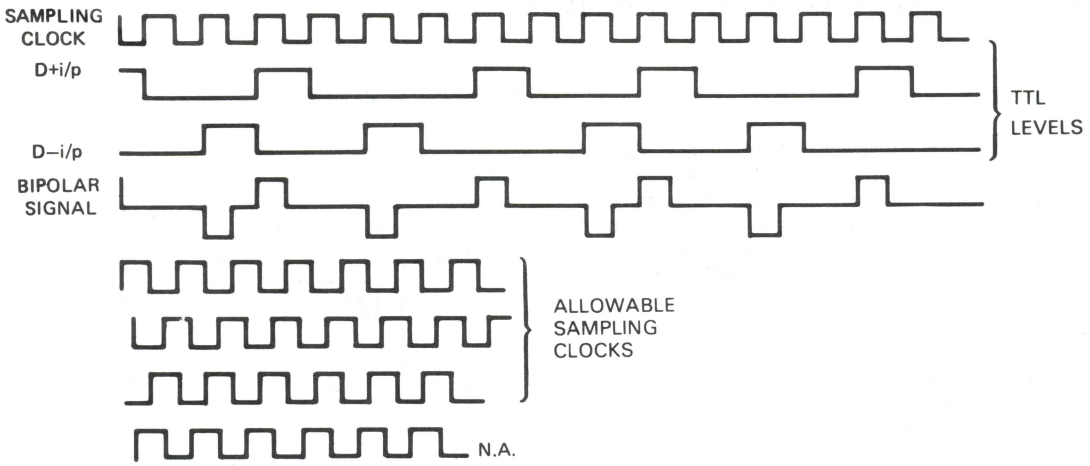
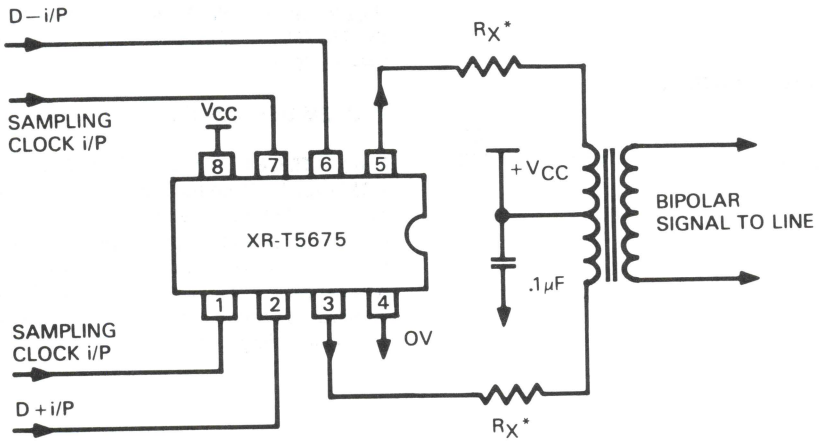


Figure 2. AC Test Circuit and Switching Waveforms



* R_X is intended for matching line impedance, but its final value may be determined by the output signal amplitude required.



In the case where D+ and D– are half width signals, Pin 1 and Pin 7 should be tied together and returned to +5.0V via a 1K resistor

Figure 3. XR-T5675 PCM Line Driver Application Circuit

Low Power PCM Line Receiver

GENERAL DESCRIPTION

The XR-T5676 is a low power PCM line receiver IC intended to operated up to 2.048 MBPS and a maximum signal level attenuation of –10dB (cable loss) at half the bit rate. Because of it's small outline and low power consumption, this device is very well suited for mux/demux applications interfacing to several T1/CEPT lines.

FEATURES

Low Power (Typ 6mA)
Single +5.0V Supply
Up to 2.048 MBPS Operation
TTL Compatible Interface
Inputs: Balanced Transformer Single Coaxial
Capacitive Coupled Twisted Pair

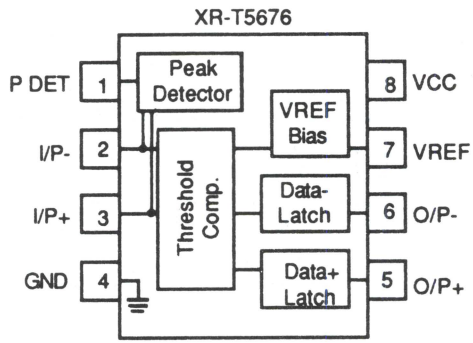
APPLICATIONS

Mux/Demux Equipment
T1 and CEPT Interfaces
CPI's
DMI's

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20V
Storage Temperature	–65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5676IN	Ceramic	–40°C to +85°C
XR-T5676IP	Plastic	–40°C to +85°C

SYSTEM DESCRIPTION

The XR-T5676 PCM line receiver IC accepts the incoming PCM signals which have been attenuated and distorted by the cable through a balanced transformer or a single capacitive coupled terminal. A peak detector which follows the input generates a DC reference voltage for the positive and negative threshold comparator. This voltage in turn is mirrored around a reference voltage to establish the threshold voltage for the negative pulses.

PIN DESCRIPTION

Pin	Name	Description
1	PDET	**Peak Detector Output.** Connects to a timing capacitor for signal peak detection.
2	I/P–	**Receiver Negative Input.**
3	I/P+	**Receiver Positive Input.**
4	GND	**Ground.** Most negative supply voltage (0V)
5	O/P+	**Data Positive Output.** (active low)
6	O/P–	**Data Negative Output.** (active low)
7	V_{REF}	**Reference Voltage.** Establishes reference voltage for transformer coupled applications.
8	V_{CC}	**Positive Supply Voltage.** (5.0V ± 5%)

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, T_A = 25°C unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	4.75		5.25	V	
Supply Current		6	10	mA	
Data Output Low		0.3	0.6	V	Pin 5 & 6 I_{OL} = 1.6mA
Data Output High	3.0	3.6		V	Pin 5 & 6 I_{OH} = 400µA

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 5%, T_A = 25°C unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Input Level		6	6.6	V_{p-p}	Pins 2 & 3
Loss Input Signal					
Alarm Level		0.6		V_{p-p}	Pins 2 & 3
Input Impedance		2.5		KΩ	@ 2.048 MBPS
Data Pulse Width	200	244	300	nS	Cable loss = 0dB

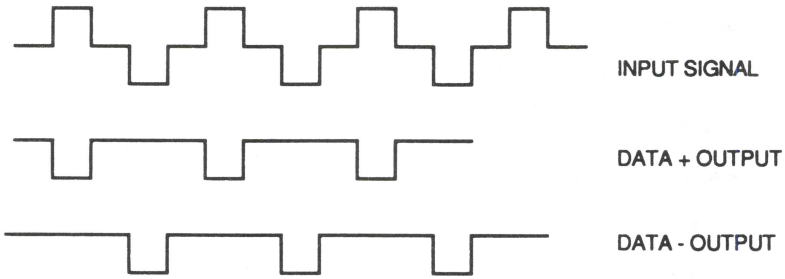


Figure 1. Reciever Output Timing Diagram with 1-1-1-1 Pattern

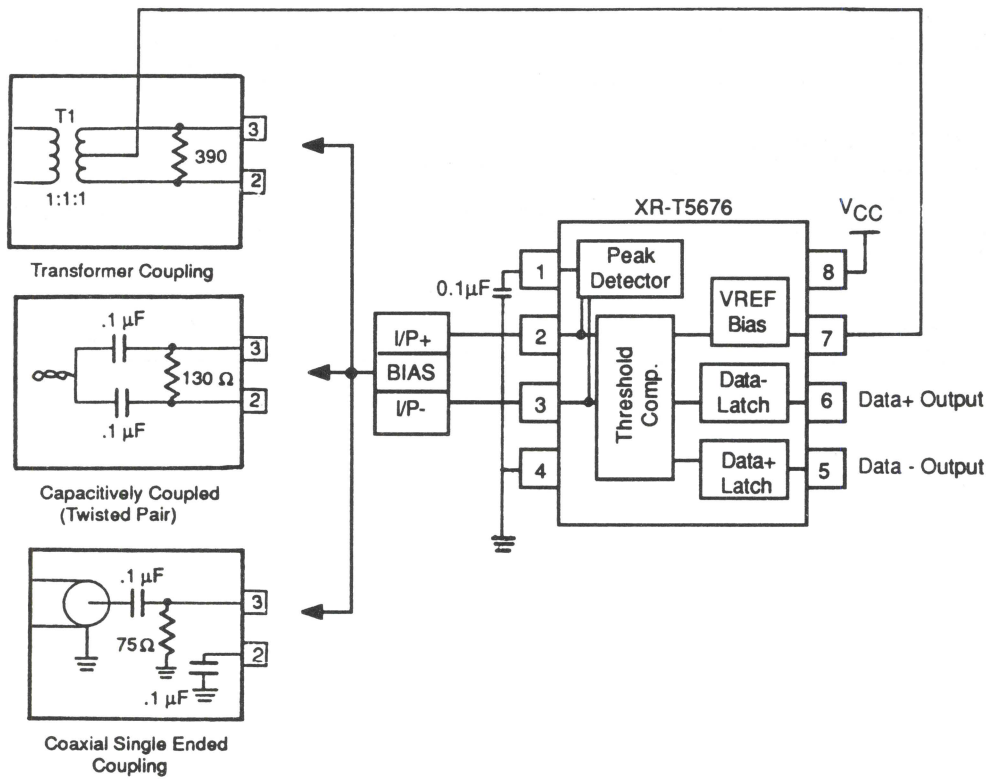


Figure 2. Typical Application Circuit

Preliminary Information

Caller I.D. Receiver IC

GENERAL DESCRIPTION

The XR-T66100 is a single-chip CMOS receiver IC designed to work in subscriber telephone equipment incorporating Calling Number Delivery (CND) capabilities. CND capabilities can be added to equipment such as telephones, adjunct units, answering machines, and facsimile machines, by using the XR-T66100 and any standard microcontroller IC. The XR-T66100 detects and qualifies the incoming ring signal, performs an energy detect qualification on the incoming FSK signal, and demodulates the 1200 Baud FSK data in accordance with Bell 202 standards. Integrating the above functions provides the equipment manufacturer a cost effective means of implementing CND capabilities into their products.

The device is fabricated on Exar's dual metal, dual poly process, and is housed in a 16 pin DIP and SOIC package.

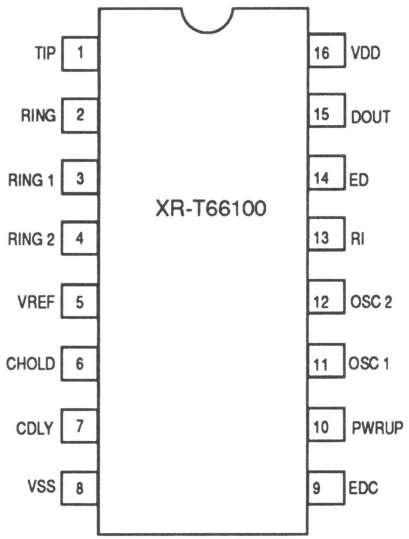
FEATURES

On-chip Ring Detector and Ring Qualifier
Power Down Operation
On-chip Band-Pass Filter (Bell 202 Compliant)
FSK Demodulator with Energy Detect
High Input Sensitivity (-35 dBm)
Low Current Consumption in Power Down Mode

APPLICATIONS

Answering Machines
Feature Phones
Fax Machines
Computer Interface Products

PIN ASSIGNMENT

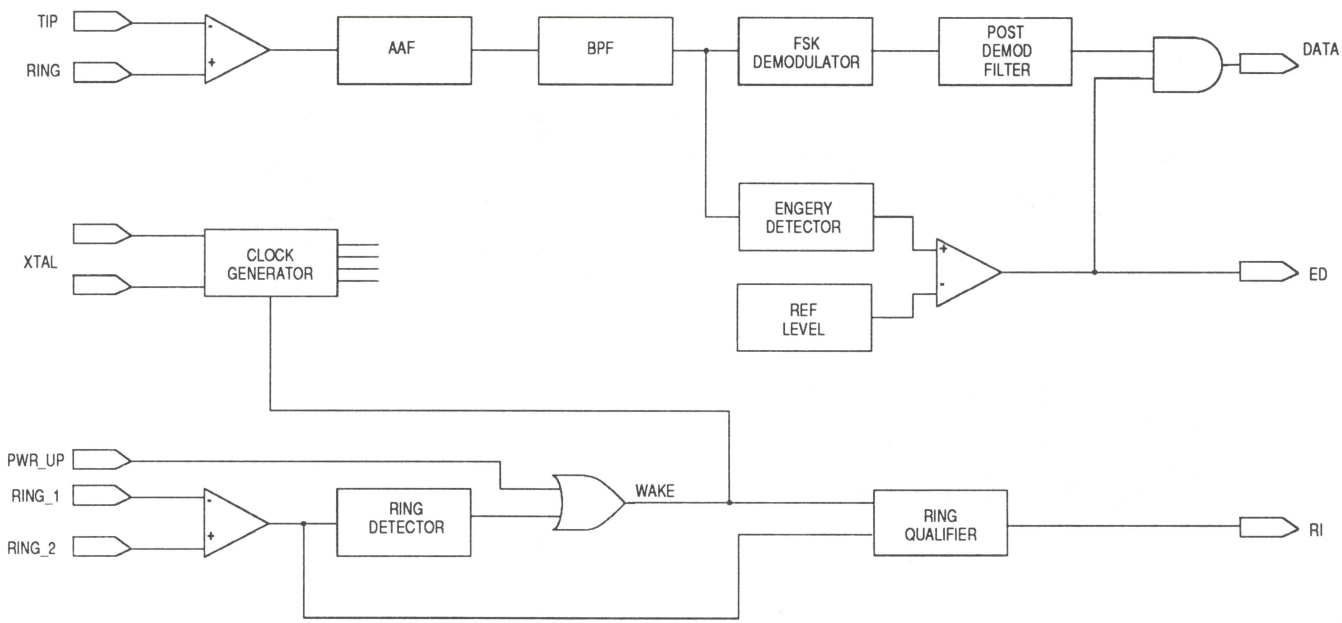


ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T66100CP	Plastic	0°C to 70°C
XR-T66100CD	SOIC	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5V to 7.0V
Input Voltage (All Pins)	-0.5V to VDD +0.5V
Storage Temperature	-65°C to +150°C



XR-T66100 Block Diagram

PIN DESCRIPTIONS

Pin #	Symbol	Type	Description
1	TIP	I	**Tip Input.** This input is connected to the tip line of the twisted pair.
2	RING	I	**Ring Input.** This input is connected to the ring line of the twisted pair.
3	RING1	I	**Ring Signal Input 1.** This input is coupled to one end of the line through an attenuation network. It is used to detect the occurrence of a valid ring signal *(refer to page 5).*
4	RING 2	I	**Ring Signal Input 2.** This input is coupled to the other end of the line through an attenuation network *(refer to page 5).*
5	VREF	O	**Voltage Reference.** This is used to establish the mid-point between Tip and Ring.
6	CHOLD	O	**Capacitor Hold.** Holding capacitor for the ring peak detect circuit.
7	CDLY	O	**C Delay.** A capacitor connected to this pin determines a valid ring period.
8	VSS	P	**Negative Power Supply.**
9	EDC	O	**Energy Detect Capacitor.** The capacitor connected to this pin determines whether the in-band energy is high enough.
10	PWRUP	I	**Power Up.** This active high input sets the chip into full power up. When low, the chip is put into a power down mode in the absence of a ring signal. In this mode, only the ring detect circuitry is active.
11	OSC1	I	**Oscillator Input 1.** This pin connects to a 3.58MHz crystal oscillator. It can also be used as an external clock input.
12	OSC2	O	**Oscillator Input 2.** This pin connects to the other side of the crystal oscillator.
13	RI	O	**Ring Indicator.** (Active high) This output detects the presence of a valid ring signal. The ring signal is qualified to have the proper frequency (16Hz-68Hz) as well as amplitude.
14	ED	O	**Energy Detect Output.** This active high output indicates the presence of in-band signals at the device input.
15	DOUT	O	**Data Output.** The demodulated FSK data is output to this pin.
16	VDD	P	**Positive Supply Voltage.** (4.5V-5.5V).

SYSTEM DESCRIPTION

The XR-T66100 is a CMOS device designed to support the Caller Number Delivery feature which is offered by the Regional Bell Operating Companies . With this service, the subscriber will have the ability to show the date, time and number of the calling party. This feature opens up several interesting applications such as phones with libraries that attach name to the number to be displayed, selective call blocking and redial of the last number that called. The information for CND originates from the Central Office and is transmitted to the customer while the telephone is on hook, during the silent period, between the first and the second power ring. The method of transmission complies to Bell 202 Standard Protocol which uses FSK (Frequency Shift Keying) carrier modulation and demodulation. Data transmission is one way (simplex), 1200 baud from the Central Office to the subscriber.

The XR-T66100 comprises two paths: the signal path and the ring indicator path (page 2). The signal path consist of an input differential buffer, an anti-aliasing filter, a four pole band pass filter, an FSK demodulator gated by an energy detect circuit. The ring indicator path includes a clock generator, a ring detector and qualifier with a special power up feature.

In a typical application, the ring detector maintains the line continuously while all other functions of the chip are inhibited. If a ring signal is sent, the ring detector wakes up the oscillator and the main bias generator. This in turn activates the rest of the IC. Once activated, a ring qualifier screens the input signal before toggling a valid RI (Ring Indicator) signal output. A PWRUP (active high) input pin is provided to activate the chip regardless of the presence of a power ring signal. If PWRUP is set low, the IC can still power itself up whenever it detects a valid ring signal, but will revert back to its normal power-down mode after a time period determined by the external capacitor connected to CDLY. The input buffer accepts a differential AC coupled input signal through the TIP and RING inputs and feeds this signal to an anti-aliasing filter followed by a four pole band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post demodulation filter. The output data is then made available at DOUT pin. This data, as sent by the central office, includes the header information (alternate "1" and "0") and the 150msec of marking which precedes the date, time and calling number. If no data is present, the DOUT pin is held in a high state. This is accomplished by an energy detect circuit which uses tthe output of the 4 pole band-pass filter. It rectifies this and uses an averaging circuit to determine if the in-band energy is high enough. If it is, this signifies that the incoming data is valid and thus the demodulated data is transfered to DOUT pin. If it is not, then the FSK demodulator is blocked. An external capacitor is used to determine the turn on and turn off times of this circuit. This device uses a 3.579545MHz crystal as a timing source for all the internal blocks.

DC ELECTRICAL CHARACTERISTICS

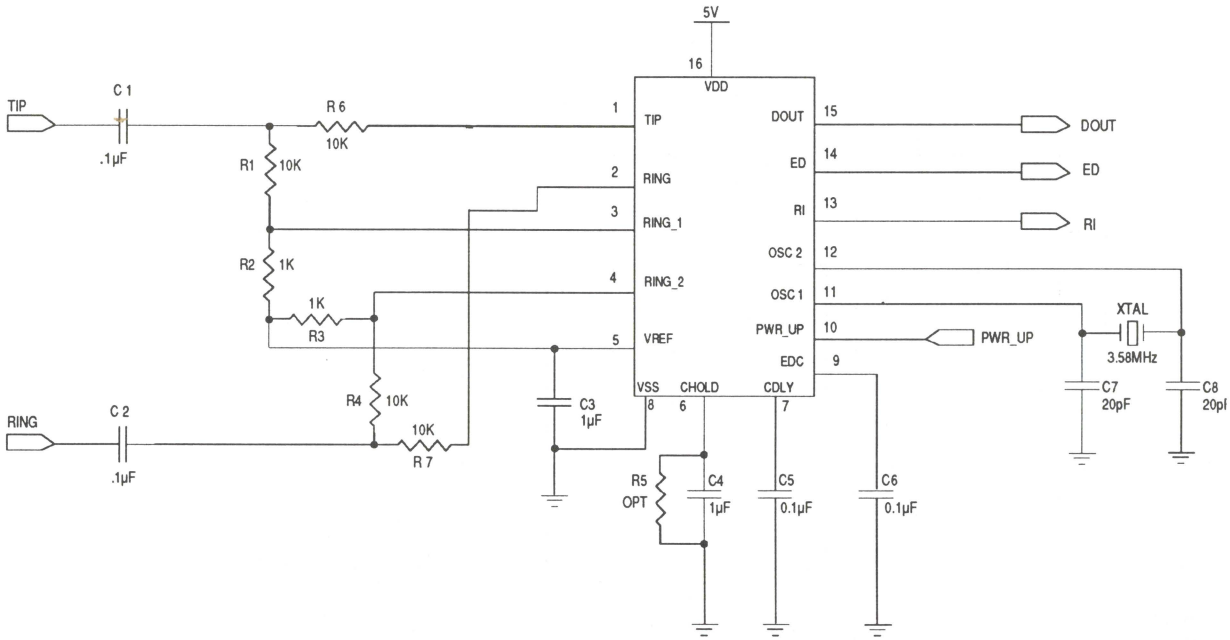
Test Conditions: VCC=5V+/-10%,TA=25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VCC	DC Voltage Range	3.5	5	6	V	
ICC-PU	Power Up Curent (Ring Det)		3.5		mA	
ICC-PD	Power Down Current			50	µA	
RXS	Input Sensitivity			-32	dBm	
VIL	Input Voltage 0 Level			0.7	V	
VIH	Input Voltage 1 Level	2.0			V	
VOL	Output Voltage Low Level			0.4	V	
VOH	Output Voltage High Level	2.5			V	
ILK	Input Leakage Current	-1		+1	µA	
ZRZ	Ring1\Ring2 Det. Input Imp.		100		kOhm	
VRV	Ring1/Ring2 Minimum Voltage	0.6			Vp-p	
VRT	Tip/Ring Minimum Voltage	0.4			Vp-p	
ZR	Tip/Ring Input Impedance		100		kOhm	
TRT	Ring Time Threshold			1	sec	
CCLK	Clock Load Capacitance			4	pF	
fXTAL	Crystal Frequency		3.58		MHz	

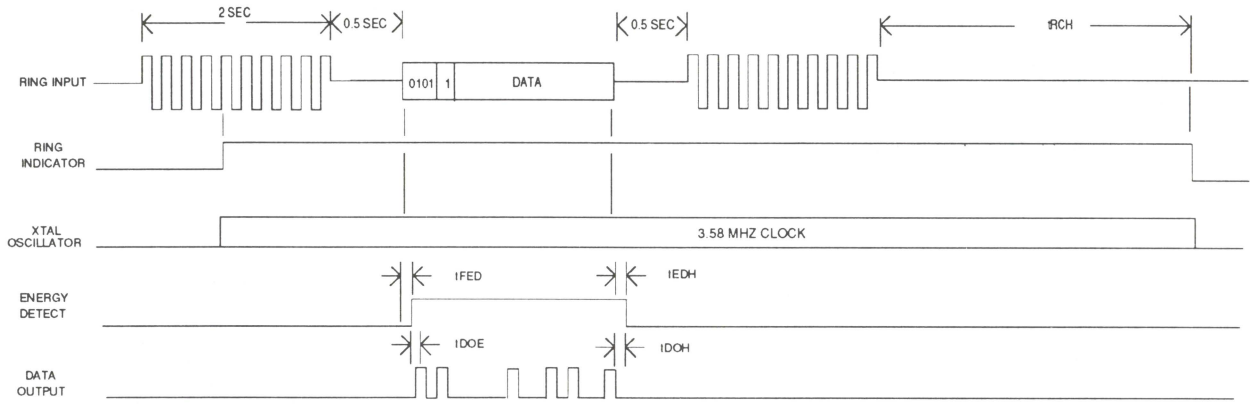
AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC=5V+/-10%,TA=25°C

tFED	FSK tp Energy Detect High		6		msec	@-32dBm
tEDH	FSK Low to Energy Detect Low		2		msec	@-32dBm
tRIH	Endof Ring to Power Down/Ri Low		4		sec	
tDOE	Data Out to Energy Detect High		10		nsec	
tDOH	Energy Detect Low to Data Out		350		nsec	



Caller I.D. Typical Application Circuit

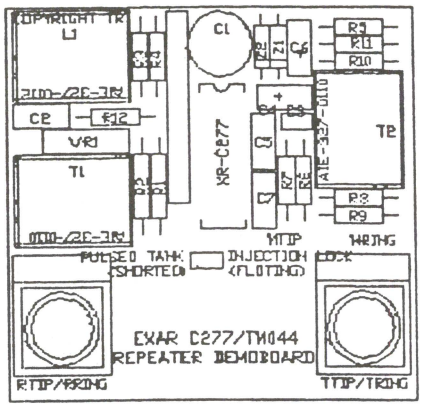


Timing Diagram for XR-T66100

XR-C277/TM044 Evaluation System

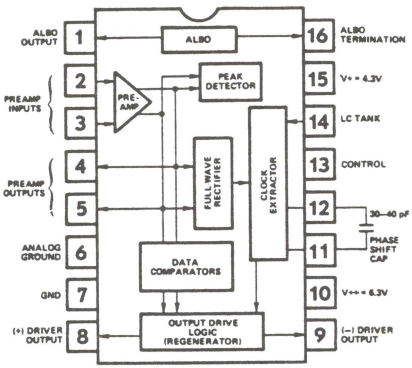
GENERAL DESCRIPTION

The XR-C277/TMO44 combination can be used as a T1/CEPT Receiver or Repeater capable of extracting, regenerating and retiming of AMI encoded data. With an additional comparator it is possible to extract the clock, which is generally required for receiver applications. Included in the XR-C277 monolithic repeater is a high performance preamplifier followed by a peak detector, a set of clock and data threshold detectors to extract the timing information, an ALBO (Automatic Line Build Out) circuit to insure that the preamplifier receives the correct amplitude and shape, a clock amplifier to generate a squarewave out of the sinusoidal tank waveform, and a set of latch circuits which sample and hold the received data. The outputs of the two data latches drive the two output driver stages which are designed to work with a nominal load of 100 ohm and be able to handle peak load currents of 30 mA.



FEATURES

1.544/2.048MBPS Repeater or Receiver
Space Saving Hybrid Equalizer
Complete ALBO and Smoothing Filter
Low Power Operation (13mA)
Improved Crosstalk and Noise Performance
Enhanced Performance (36DB Line Loss)
Operating Temperature Range (-40° to 85° C)
Available Packages (C277): Plastic, Ceramic and S.O.P.



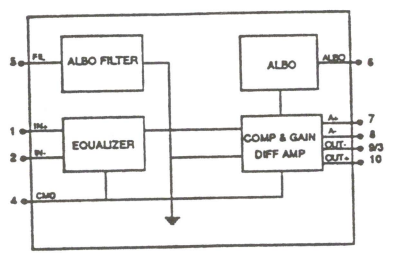
ASSEMBLY PROCEDURE

1) Attach four equal spacers to the corners of the Demoboard to ease the assembly procedure.

2) Insert and solder all capacitors as marked on the PC Board. Make sure you choose the correct component values, tolerances and polarity where applicable.

3) Insert and solder all resistors and diods in place and clip their leads.

4) Now insert the 16 pin integrated circuit socket. Notice the polarity to avoid damage to the IC when inserted.



SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF TM-044H

5) The magnetics used for the demoboard are manufactured by three qualified vendors which are:

a) AIE MAGNETICS	(813) 347-2181
b) SCHOTT	(612) 475-1173
c) PULSE ENGINEERING	(619) 268-2400

For further information and specs on these components please contact the selected magnetic manufacturers. Insert and solder these parts. Notice the polarity of the transformers and tank coil.

6) Carefully insert the XR-C277 IC into the socket without bending the leads and choose the desired input and output connectors. The board is intended to use BNC connectors but can vary depending on the type of test equipment used.

7) Lastly, insert the hybrid network into the corresponding socket.

TEST AND ADJUSTMENT PROCEDURE:

The XR-C277/TMO44 Demoboard is designed to operate as a repeater, but with the small addition of a comparator it is possible to extract the clock output as shown in the applications schematic. It is left to the customers choice to perform the testing and evaluation of this circuitry depending on the type of test instrument and application they may have. The testing of this board was done with the Sierra (415-11) which tests the board in a repeater configuration.

INITIAL ADJUSTMENT

1) Connect the AMI encoded input signal from the Sierra Test Set to the RTIP/RRING input connector of the demoboard. Similarly connect the TTIP/TRING or output signal back to the return line of the test set.

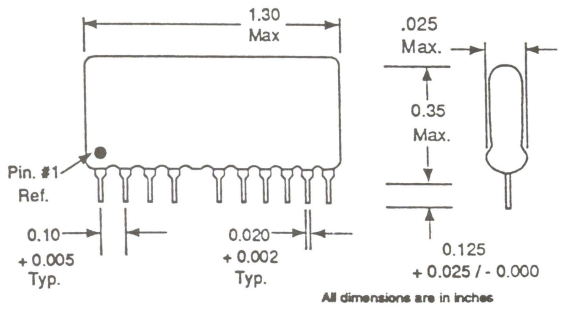
2) Apply power to the test set and check for a: the correct feed through current (supplied by the test set, approx. 50mA and adjustable) and b: the voltage drop (approx. 5V) on the loop which in this case is generated by the exterior zeners.

3) To be able to see the input and output waveforms with an oscilloscope, it is necessary to isolate the scope ground from the board ground with a small electrolytic capacitor. Connect this capacitor to the board ground and switch over to an all one's pattern on the test set. Check for a sign of life and look at the extracted data output (pin 8 or 9). Notice that it may look jittery since the board has not been adjusted so far.

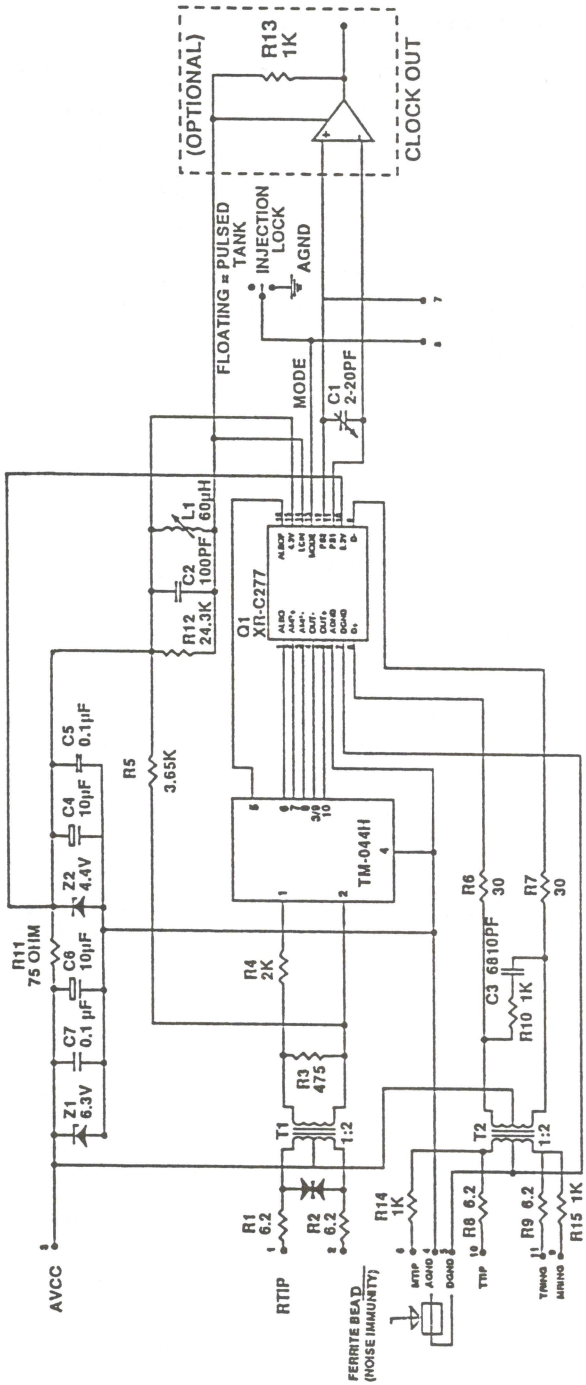
4) Place another scope probe on pin 14 (LC Input Pin) and adjust the variable inductor until the sinusoidal output waveform reaches it's maximum amplitude.

5) Switch the test instrument to generate a QRSS pattern sequence, and place a scope probe on one of the preamplifier output pins (4 or 5) and the other on the extracted data output (pin 8 or 9). Now adjust the phase shift capacitor (C1) until the falling or negative transition of the clock output waveform coinsides directly, or slightly less (30nses), with the top of the preamplifier output pulse (top of the eye.) At this point we should observe the least amount of errors under normal or noisy conditions. The board should be now operating satisfactorily from up to 36dB and approximately 11dB of noise.

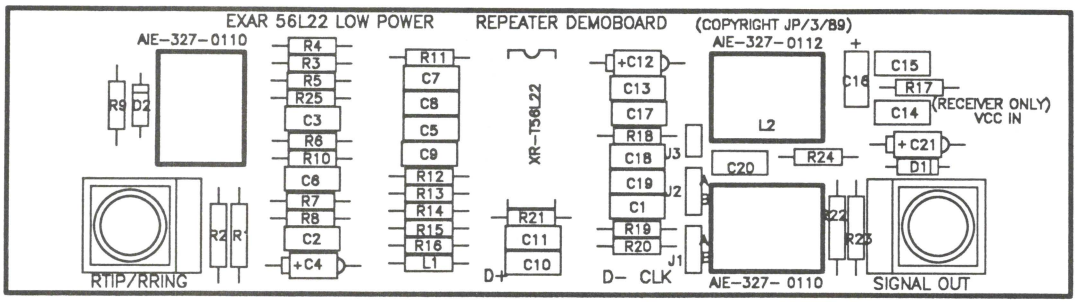
DIMENSIONS



7-FEB-1989 Bill of Material Print			
COMP NO.	**LABEL**	**PACKAGE**	**COMMENTS**
1	BNC1	BNC	
2	BNC2	BNC	
3	C1	VARCAP	2-20PF
4	C2	RAD0.2	100Pf
5	C3	RAD0.1	6.8NF
6	C4	RAD0.2	10UF TANT
7	C5	RAD0.2	0.1UF
8	C6	RAD0.2	10UF TANT
9	C7	RAD0.2	0.1UF
10	HYBRID1	HYB	XR-TM044
11	IND	TRANS	327-0112
12	J1	J2	JUMPER
13	R1	AXIAL0.6	6.2 OHM, 1/2W
14	R10	AXIAL0.5	1K, 1/4W
15	R11	AXIAL0.5	75, 1/4W
16	R12	AXIAL0.5	24K, 1/4W
17	R2	AXIAL0.6	6.2 OHM, 1/2W
18	R3	AXIAL0.5	475, I/4W
19	R4	AXIAL0.5	2K, 1/4W
20	R5	AXIAL0.5	3.65K, 1/4W
21	R6	AXIAL0.5	30.1, 1/4W
22	R7	AXIAL0.5	30.1, 1/4W
23	R8	AXIAL0.5	6.2, 1/2W
24	R9	AXIAL0.5	6.2, 1/2W
25	T1	TRANS	327-0110
26	T2	TRANS	327-0110
27	VAR1	RAD0.4	90V
28	XR-C277	DIP16	U1
29	Z1	DIODE0.4	ZENER 6.2V, 1/4W
30	Z2	DIODE0.4	ZENER 4.4V, 1/4W


(OPTIONAL)
R13
1K
CLOCK OUT
FLOATING = PULSED TANK
INJECTION LOCK
AGND
MODE
C1
2-20PF
L1
60µH
C2
100PF
R12
24.3K
Q1
XR-C277
R5
3.65K
C5
0.1µF
C4
10µF
Z2
4.4V
R11
75 OHM
C6
10µF
C7
0.1 µF
Z1
6.3V
R4
2K
R3
475
T1
1:2
TM-044H
R6
30
R7
30
C3 6810PF
R10 1K
T2
1:2
R1
6.2
R2
6.2
R14
1K
R8 6.2
R9 6.2
R15 1K
AVCC
RTIP
FERRITE BEAD
(NOISE IMMUNITY)
TTIP
TRING
RRING

XR-T56L22 Evaluation System



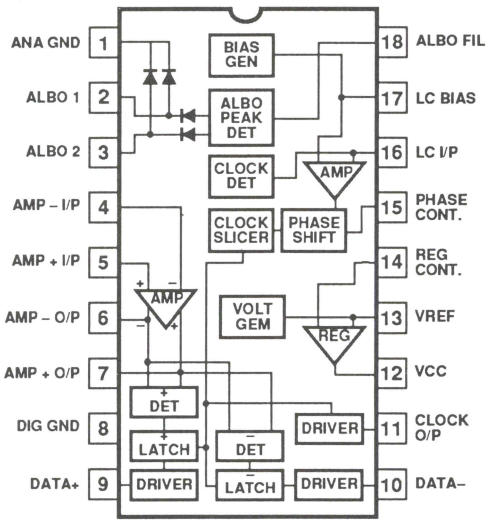
GENERAL DESCRIPTION

The XR-T56L22 is a T1/CEPT Receiver or Repeater capable of extracting, regenerating and retiming of AMI encoded data as well as providing the extracted clock output for applications where it is required. Included are a shunt regulator to generate +5V supply out of the phantom feed current, a high performance preamplifier followed by a set of clock and data threshold detectors to extract the timing information, an ALBO (Automatic Line Build Out) Circuit to insure that the preamplifier receives the correct amplitude and shape, a clock amplifier to generate a square-wave out of the sinusoidal tank waveform, a phase shift network which delays the extracted clock by 90 degrees, and a set of latch circuits which sample and hold the received data. The output stage is capable of driving up to 100mA and it's output is produced by ORing the latched preamplifier information with the inverse clock to insure the correct phase and output pulse shape.

FEATURES

Very Low Power Consumption (7 to 8.75mA)
Data and Clock Extraction up to 40dB
Dual Matched ALBO Ports
Internal Adjustable Phase Shift Network
Internal Shunt Regulator
Operating Temperature Range (–40° to +85°C)
Available Packages: Plastic, Ceramic and S.O.P.

FUNCTIONAL BLOCK DIAGRAM



ASSEMBLY PROCEDURE

1) Attach four equal spacers to the corners of the Demoboard to ease the assembly process.

2) Insert and solder all capacitors as marked on the PC Board. Make sure you choose the correct component values, tolerances and polarity where applicable.

   Included are the schematic and Bill of Material for 1.544MBPS and 2.048MBPS applications.

3) Insert and solder all resistors and diodes in place and clip their leads.

Note:
The magnetics used for the demo boards are manufactured by three qualified vendors which are:

a) AIE Magnetics 813-347-2181
b) Schott 612-475-1173
c) Pulse Engineering 619-268-2400

For further information and specifications please contact the selected magnetics manufacturers. Insert and solder these parts. Notice the polarity of the transformers and tank coil.

4) Solder in an 18 pin socket and carefully insert the XR-T56L22 IC into it without bending the leads. Use BNC or other type of connectors as input and output ports.

5) Jumpers: Notice the jumper configuration between receivers and repeaters.

	RECEIVER	REPEATER
J1	A SHORTED	B SHORTED
J2	B SHORTED	A SHORTED
J3	SHORTED	OPEN
J4	DIG GND SHORT	DIG GND SHORT
R21	1K OHM	47 OHM
R20	1K OHM	47 OHM

TEST AND ADJUSTMENT PROCEDURE

The XR-T56L22 Demoboard can be configured as a receiver or as a repeater. It is left to the customers choice to perform the testing and evaluation of this circuitry depending on the type of test instruments they feel is most appropriate.

Again, depending on the application, the Sierra (415-11) was used to test the board as a repeater, and an H.P. Pattern Generator/Error Detector (3780A) was used to test the demoboard as a receiver. In both cases the adjustment procedure is very similar.

Initial Adjustment

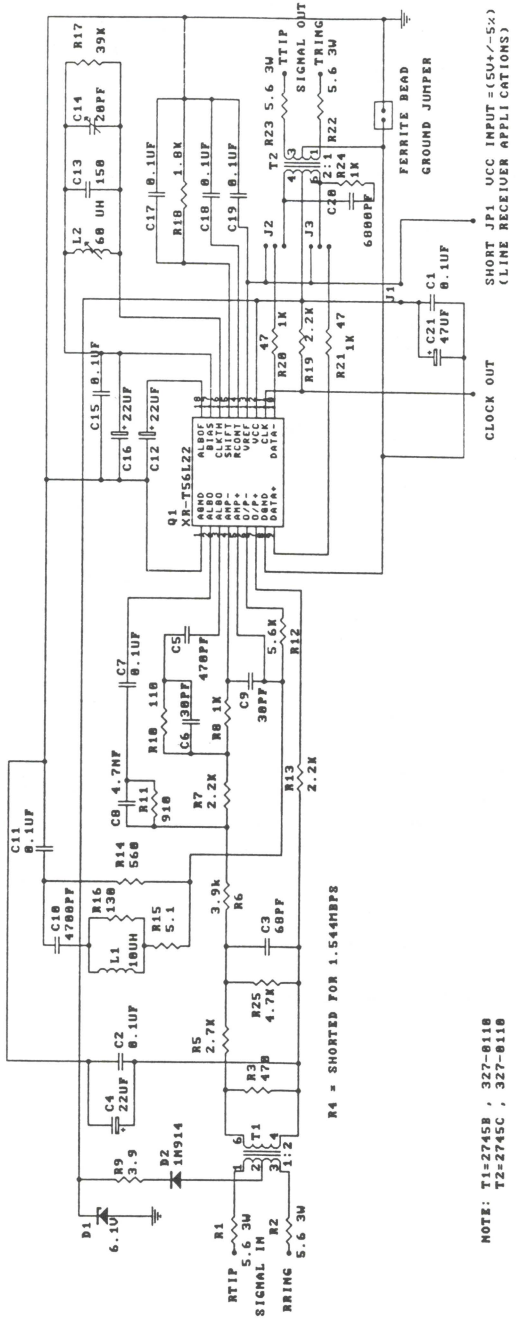
1) Connect the AMI encoded input signal from the Sierra Test Set to the RTIP/RRING input connector of the demoboard. Similarly connect the TTIP/TRING or output signal back to the return of the test set.

2) Apply power to it and check for a: the correct feed current supplied by the test set (approx. 50mA, adjustable) and b: the voltage drop (approx. 5V) on the loop which in this case is generated by the shunt regulator of the XR-T56L22.

3) To be able to see the input and output waveforms with an oscilloscope, it is necessary to isolate the scope ground from the board ground with a small electrolytic capacitor, Connect this capacitor to the board ground and switch over to an all one's pattern on the test set. Check the extracted clock output pin marked CLK. Notice that it may look jittery since the board has not been adjusted so far.

4) Place another scope on pin 16 (LC Input Pin) and adjust the variable inductor until the sinusoidal output waveform reaches it's maximum amplitude.

5) Switch the test instrument to generate a QRSS pattern sequence; place a scope probe on one of the preamplifier output pins (6 or 7) and the other on the extracted clock output (pin 11). Now adjust the phase shift resistor (R18) until the falling or negative transition of the clock output waveform coinsides directly, or slightly less (30ns), with the top of the preamplifier output pulse (top of the eye). At this point we should observe the least amount of errors under normal or noisy conditions. At this point the tank may need to be readjusted to operate error free from approximately 5 to 40dB of cable attenuation.



TYPICAL APPLICATION FOR THE XR-T56L22 AT 1.544 MBPS

Bill of Material for 1.544 MBPS Application Circuit

DESCRIPTION	QUANTITY		COMPONENT NAME (S)			
0.1µF	8	C1	C2	C7	C11	C13
		C17	C18	C19	C	
1.8K	1	R18				
1:2	1	T1				
1K	2	R8	R24			
1N914	1	D2				
2.2K	3	R7	R13	R19		
2.7K	1	R5				
2:1	1	T2				
3.9	1	R9				
3.9K	1	R6				
4.7K	1	R25				
4.7NF	1	C8	C10			
5.1	1	R15				
5.6 3W	4	R1	R2	R22	R23	
5.6K	1	R12				
6.1V	1	D1				
10UH	1	L1				
20pF	1	C14				
22UF	3	C4	C12	C16		
30pF	2	C6	C9			
39K	1	R17				
47	2	R20	R21			
47UF	1	C21				
60UH	1	L2				
68pF	1	C3				
110	1	R10				
130	1	R16				
150pF	1	C13				
470	1	R3				
560	1	R14				
910	1	R11				
4700pF	1	C10				
6800pF	1	C20				
XR-T56L22	1	Q1				
470pF	1	C5				

XR-T6164/65/66 Evaluation System

GENERAL DESCRIPTION

This application note describes the XR-T6164/65/66 evaluation kit. This two chip set performs the 64kBPS co-directional interface function as defined in CCITT G.703 recommendations. The newly developed adaptation unit (DAU 64) provide access to a time slot of the PCM frame.

Primary PCM CH-30 has been used originally for voice transmission. The increasing need for high-speed data transmission has lead to the development of equipment which allows the user to multiplex data and digitized voice information into a common 2048kBPS PCM channel. With the XR-T6164/65/66 chip set, a data adaptation unit (DAU) can be realized with minimal components. Various application areas using T6164/65/66 chip set are shown in figure 3 and 4. The main function of a DAU is to provide access to any time slot of a PCM frame in both transmit and receive directions.

BASIC OPERATION

The T6164 is a 16 pin analog device. It consists of both a line driver and a line receiver to interface to the twisted pair cable via external transformers. The T6165 or T6166 are digital CMOS ICs which perform the necessary data format and rate conversions between G.703 64kBPS and PCM 2048kBPS data.

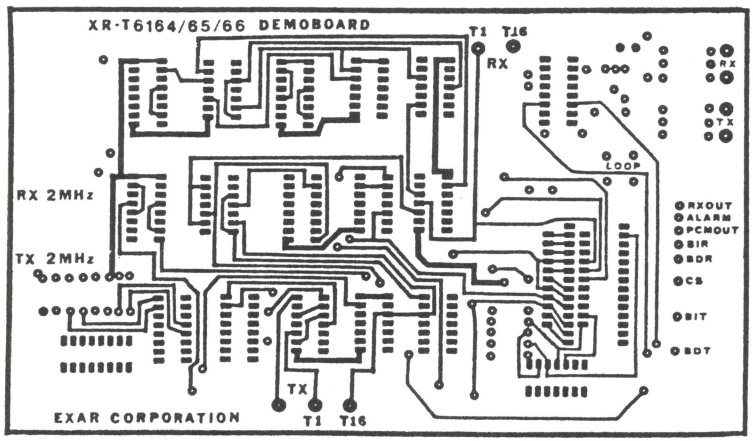
DATA EXTRACTION FROM THE FRAME

To extract 64kBPS data from a PCM CH-30 system, the 2048kBPS signal is applied to the input of the digital transmitter together with synchronous 2.048MHz and 256KHz clocks. When a time slot pulse goes high (8 clock pulses derived externally) the information present will be clocked into the transmitter. Four periods are dedicated to each bit of 64kbit/s data in order to code "0" as 0101 and "1" as 0011. The binary signal is then converted into a modified bipolar signal by alternating the polarity of the consecutive blocks, and output as "T+R" and "T-R" to the line driver portion of the T6164 for transmission. The final bit of each input word is coded with a bipolar violation producing the necessary octet timing information.

DATA INSERTION INTO THE PCM FRAME

Incoming bipolar signals at the secondary of the input transformer are fed to the receiver portion of the T6164, which consists of a peak detector and two data comparators for positive and negative data retrieval. The receiver has adequate sensitivity to accurately extract data which has been attenuated by cable losses of up to 10dB at 128KHz.

Receiving data is converted into LSTTL compatible signals and output as "S+R" and "S-R" to the T6165 or T6166 for timing extraction and formatting.



Before data can be inserted into the PCM frame, it is necessary to regenerate a 64KHz clock from the incoming signal for synchronization and data decoding. This is done with an octet locking circuit and a variable length counter which behaves like a digital phase lock-loop. Once in sync., data can be multiplexed into the PCM frame under the control of receive 2.048MHz read clock and a time slot pulse. When the time slot goes high, a burst of eight bits data at 2.048MHz rate is sent out at "PCM OUT".

TIMING AND BLOCK DIAGRAM

Figure 5 shows a typical application circuit for the T6164/6165 and their block diagrams. Pulse masks and coding for a codirectional G.703 interface are shown if figure 1 and 2.

DEMO KIT INSTRUCTIONS

The kit contains a printed circuit board which permits easy evaluation of the T6164/T6165 or T6166 parts. The board requires two external 2048KHz clocks, one for transmit and the other for receive. These clocks are TTL level clocks applied to the Rx 2MHz and Tx 2MHz BNC connectors. The rest of the timing signals are generated on-board using HCMOS logic. Power is applied to the red and black banana plugs. (red = +5V ±10%, black =0V)

OPERATION

After power up and with the two 2MHz clocks connected, check TS1 in both Tx and Rx for a stable time slot pulse. If any of these pulses cannot be synchronized by the scope, the external logic needs to be reset by disconnecting the +5V supply from the board and temporarily shorting its VCC line to ground.
The transmitter section generates two time slot pulses and an 8KHz frame clock. An 8 bit word is also generated on board whose output pattern can be selected by means of the 8 position DIP switch on the left. Depending on the position of S4, the 4th DIP switch on the right, the 8 bit word can be placed either in TS1 or TS16 of a frame. The transmit data is input to pin 15 of the XR-T6165 or pin 19 of the XR-T6166 and appears as positive and negative data at "T+R" and "T-R" respectively. This same data is then passed to the T6164 for transmission, the resulting bipolar signal can be observed at "TX O/P".

RECEIVER

The "TX O/P" data in this demo kit is looped back to the receive circuit via jumpers (Loop). With the loop broken, it is possible to evaluate the sensitivity of the receiver and other functions of the analog device by means of externally generated signals.

The XR-T6164 converts the incoming bipolar signals it receives into negative going LSTTL level data at "S+R" and "S-R". If sync. is achieved by the digital chip (this usually is not a problem as long as the Tx and Rx clock frequencies are within 2048KHz ±10KHz), the received data should appear at "PCM OUT". Figure 1 shows 8 bit data to be inserted into a PCM frame within an envelope of a time slot pulse.

The main difference between the XR-T6165 and the XR-T6166 is some added features which indicate repetitions and deletions of both received and transmitted data whenever clock skews or transients occur. An extracted receive clock output is also provided together with a receive clock loss of lock flag.

DIP 2 SWITCH SETTING

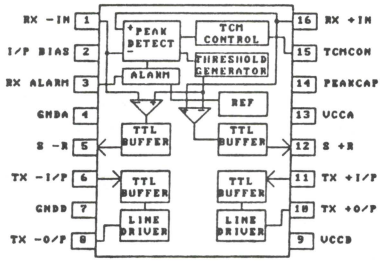
Switch 1 is intended to enable or disable the "Byte Locking" feature. When closed (active low) it causes blanking of PCMOUT under received alarm conditions.

Switch 2 forces the PCMOUT data stream to an all ones condition when closed (active low).

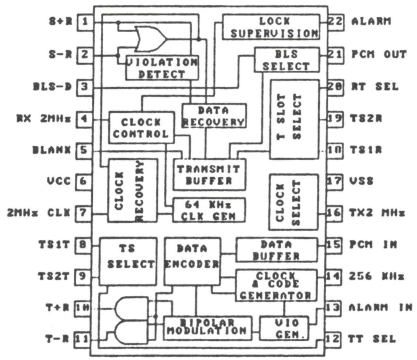
Switch 3 toggles the receiver time slot select of the XR-T6165 or 6166.

Switch 4 toggles the transmitter time slot select.

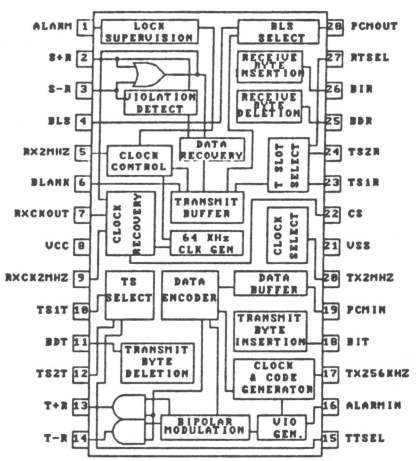
Switch 5 connects to the alarm input pin of the XR-T6165/66. When open (active high), the insertion of violations to the transmitted data is inhibited.



XR-T6164



XR-T6165



PIN DESCRIPTIONS - XR-T6164

Name	Pin	Description
RX-I/P	1	Receiver negative bipolar input.
I/P BIAS	2	Internally generated bias voltage for receive inputs.
RXALARM	3	Loss of signal alarm (<15dB) (Active Low)
GNDA	4	Analog Ground
S-R	5	Receive negative output data (Active Low)
TX-I/P	6	Transmit negative input signal (Active High)
GNDD	7	Digital Ground
TX-O/P	8	Transmit negative output data, open collector.
VCCD	9	+5V± 5% digital supply.
TX+O/P	10	Transmit positive output data, open collector.
TX+I/P	11	Transmit positive input signal (Active High).
S+R	12	Receive positive ouput data (Active Low).
VCCA	13	+5V ± 5% analog supply.
PEAKCAP	14	Receiver peak detector storage capacitor.
TCMCON	15	Time compression multiplex control pin (Active Low). When active disables Rx inputs and stores previous peak voltage.
RX+I/P	16	Receiver positive bipolar input.

PIN DESCRIPTIONS - XR-T6165

Name	Pin	Description
S+R	1	Positive AMI data to receiver (Active Low).
S-R	2	Negative AMI data to receiver (Active Low).
BLS	3	Byte locking supervision (Active Low). When active causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	4	Receiver 2048KHz clock.
BLANK	5	PCMOUT data blanking (Active High). When active, forces PCMOUT data to all ones (AIS).
VCC	6	+5V ±5% power supply.
RXCK2MHZ	7	2048KHz clock recovery signal.
TS1T	8	Time slot input 1 for transmitter.
TS2T	9	Time slot input 2 for transmitter.
T+R	10	Transmit positive output AMI data (Active Low).
T-R	11	Transmit negative output AMI data (Active Low).
TTSEL	12	Transmit time slot select. When high pin 8 selected, when low pin 9 selected.
ALARMIN	13	Alarm input (Active High). When active inhibits insertionof violation into transmitted data.
TX256KHZ	14	Transmitter 256KHz clock.
PCMIN	15	Transmitter PCM input.
TX2MHZ	16	Transmitter 2048KHz clock.
VSS	17	Ground.
TS1R	18	Time slot input 1 for receiver.
TS2R	19	Time slot input 2 for receiver.
RTSEL	20	Receive time slot select. When high pin 18 selected, when low pin 19 selected.
PCMOUT	21	Received PCM output data.
ALARM	22	Alarm (Active High). When active, indicates loss of received bipolar violations.

PIN DESCRIPTION - XR-T6166

Name	Pin	Description
ALARM	1	Alarm (Active High) When active, indicates loss of received bipolar violations.
S+R	2	Positive AMI data to receiver (Active Low).
S-R	3	Negative AMI data to receiver(Active Low).
BLS	4	Byte Locking Supervision (Active Low). Causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	5	Receiver 2048KHz clock.
BLANK	6	PCMOUT data blanking (Active High). When active,forces PCMOUT data to all ones (AIS).
RXCKOUT	7	128KHz extracted clock.
VCC	8	+5V power supply.
RXCK2MHZ	9	2048 KHz clock recovery signal.
TS1T	10	Time slot input 1 for transmitter
BDT	11	Transmitter data byte deletion flag (Active High).
TS2T	12	Time slot input 2 for transmitter
T+R	13	Transmit positive output AMI data (Active Low).
T-R	14	Transmit negative output AMI data (Active Low).
TTSEL	15	Transmit time slot select When high, pin 10; low pin 12
ALARMIN	16	Alarm input (Active High). When active inhibits insertion of violations into transmitted data.
TX256KHZ	17	Transmitter 256KHz clock.
BIT	18	Transmitter data byte insertionflag (Active High).
PCMIN	19	Transmitter PCM input.
TX2MHZ	20	Transmitter 2048KHz clock.
VSS	21	Ground.
CS	22	Clock seek (Active High). Indicates loss of lock with received data.

PIN DESCRIPTION - XR-T6166 *(continued)*

Name	Pin	Description
TS1R	23	Time slot input 1 for receiver.
TS2R	24	Time slot input 2 for receiver.
BDR	25	Receive data byte deletion flag (Active High).
BIR	26	Receive data byte insertion flag (Active High).
RTSEL	27	Receive time slot select. When high, pin 23; when low pin 24.
PCMOUT	28	Received PCM output data.64 kBPS data

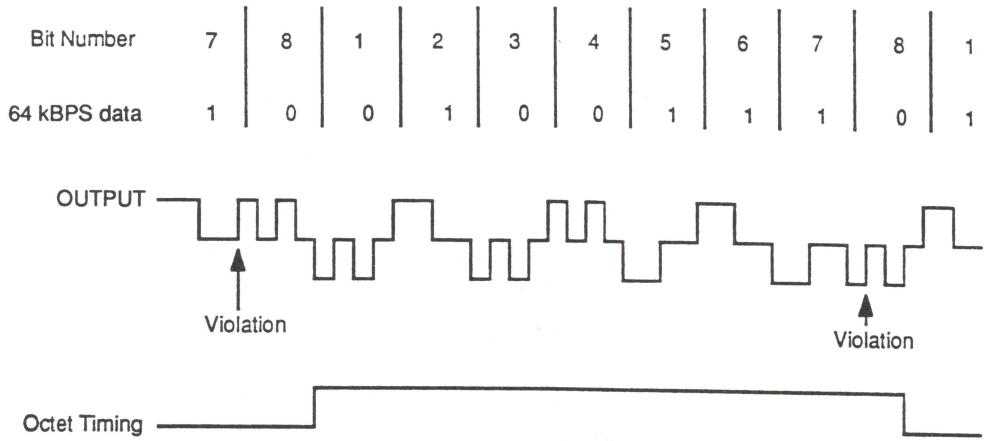


Figure 1. Transmitter Code Conversion for 64 kBPS Bipolar Line Signal.

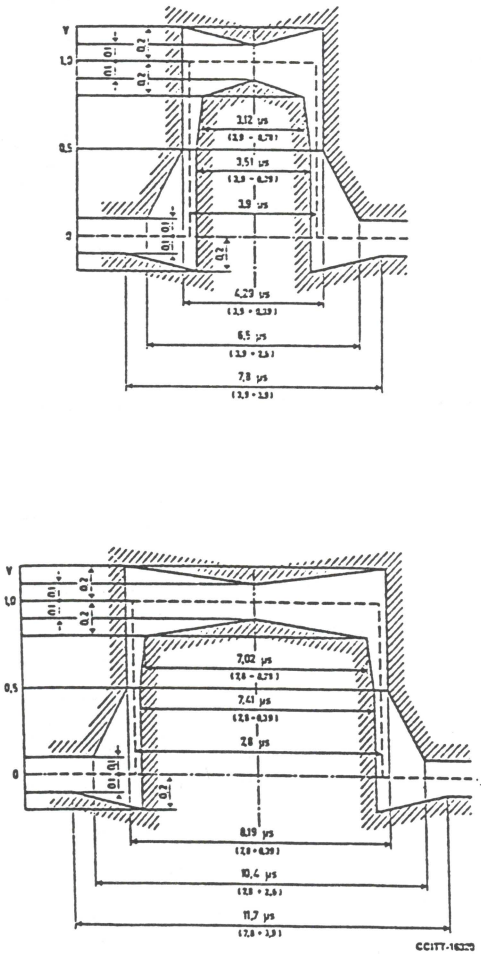


Figure 2. Pulse Masks of the 64 kBPS Codirectional Interface

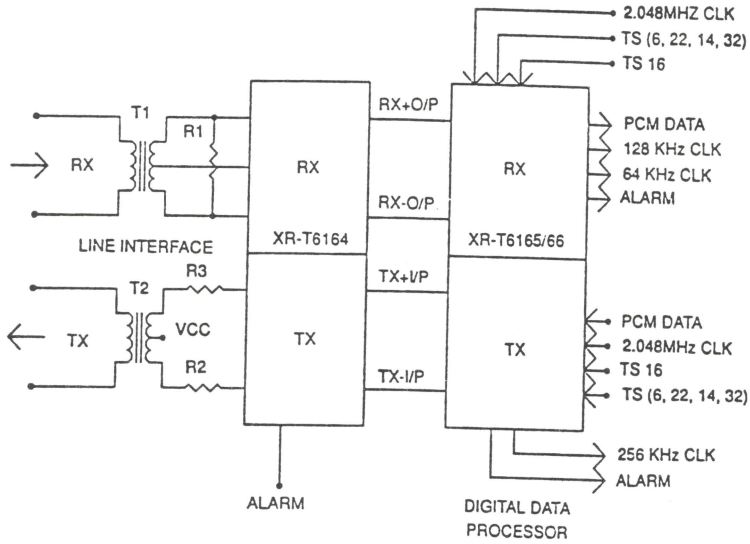


Figure 3. Digital Data Processor Application.

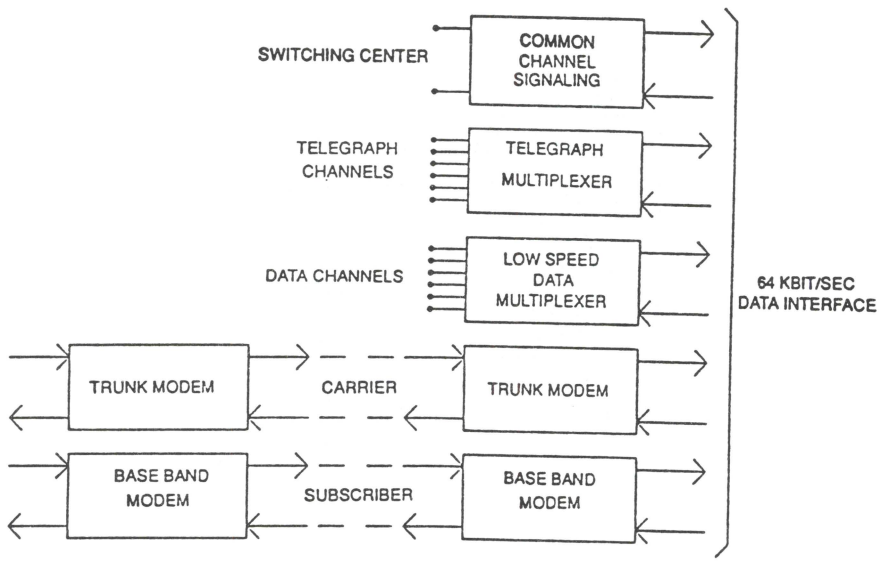


Figure 4. Digital Data Processor Application.

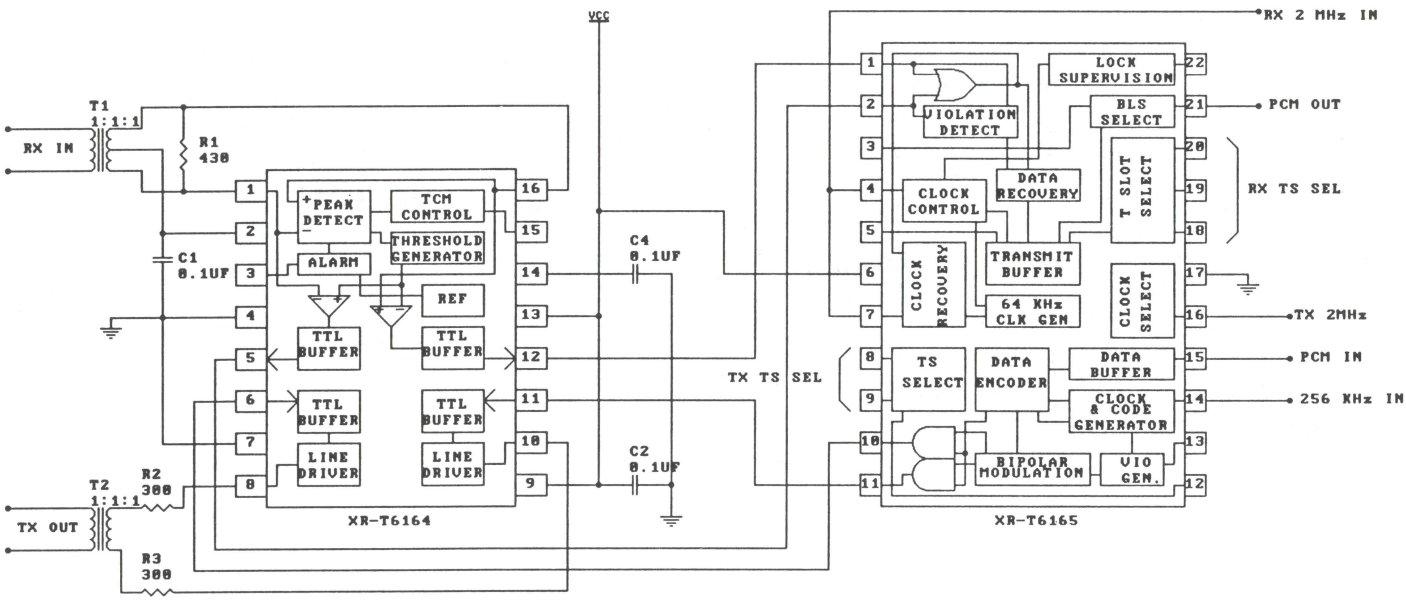


Figure 5. Typical 64 kbit/s Data Interface.

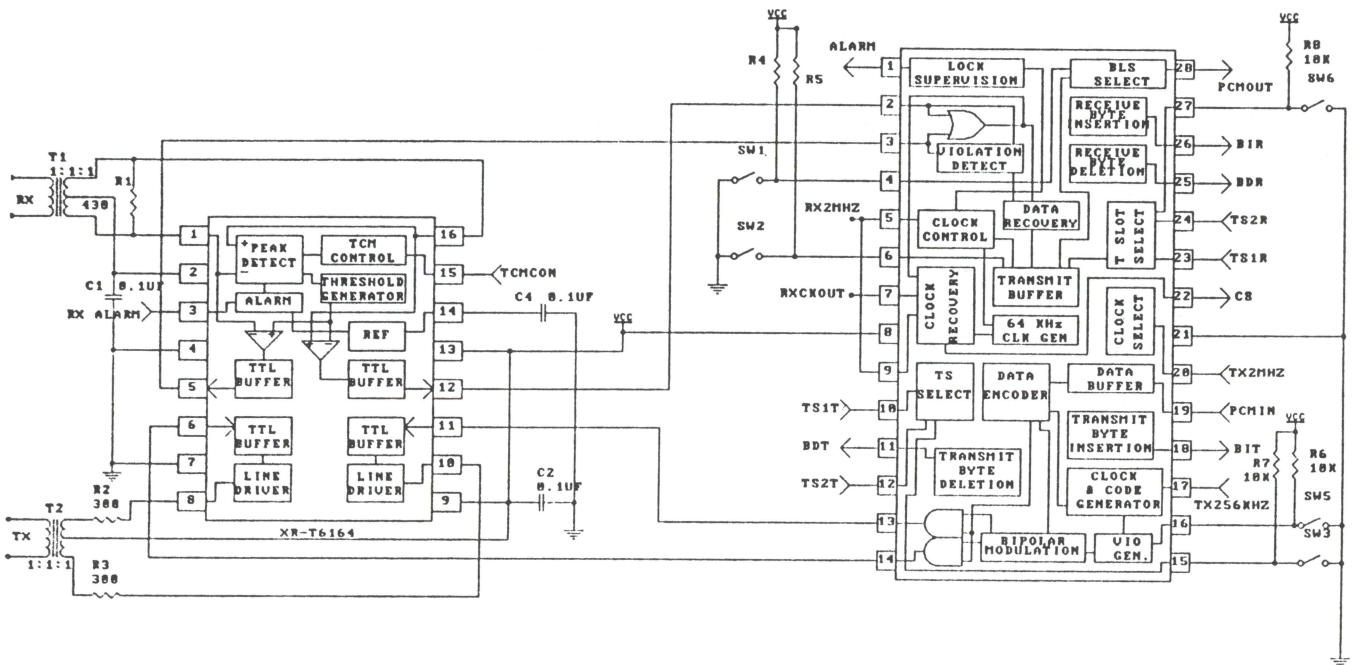


Figure 6. Typical Application Diagram for XR-T6166.

FSK Modulator/Demodulator

GENERAL DESCRIPTION

The XR-210 is a highly versatile monolithic phase-locked loop system, especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters, and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accommodate analog signals between 300μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range	0.5Hz to 20MHz
Wide Supply Voltage Range	5V to 26V
Digital Programming Capability	
RS-232C Compatible Demodulator Output	
DTL, TTL and ECL Logic Compatibility on Inputs	
Wide Dynamic Range	300μV to 3V
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	±1% to ±50%
Good Temperature Stability	200 ppm/°C
High-Current Logic Output	50mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

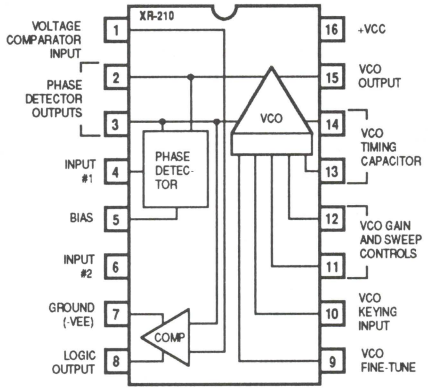
APPLICATIONS

Data Synchronization
Signal Conditioning
FSK Generation
Tone Decoding
Frequency Synthesis
FSK Demodulation
Tracking Filter
FM Detection
FM and Sweep Generation
Wideband Discrimination

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750mW
Derate Above + 25°C	6.0mW/°C
Storage Temperature	65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-210M	Ceramic	–55°C to +125°C
XR-210CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-210 is made up of a stable wide-range voltage- controlled oscillator (VCO), exclusive OR gate type phase detector, and an analog voltage comparator. The VCO, which produces a square wave as an output, is either used in conjunction with the phase detector to form a phase-locked loop (PLL) for FSK demodulation and tone detection or as a generator in FSK modulation schemes. The phase detector when used in the PLL configuration produces a differential output voltage with a 6 KΩ output impedance, which when capacitively loaded forms a single pole loop filter. The voltage comparator is used to sense the phase detector output and produces the output in the FSK demodulation connection.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 12V$ (single supply), $T_A = +25°C$, Test circuit of Figure 1 with $C_O = 0.02\mu F$, S_1, S_2, S_5 closed, S_3, S_4, S_6, S_7 open, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{CC}	Supply Voltage					
	Single Supply	5		26	V dc	See Figure 1
	Split Supply	±2.5		113	V dc	See Figure 2
I_{CC}	Supply Current	9	12	16	mA	See Figure 1, S_2 open
f_{UL}	Upper Frequency Limit	15	20		MHz	See Figure 1, S_1 open, S_4 closed
f_{LL}	Lowest Practical Operating Frequency		0.5		Hz	$C_O = 500\mu F$ non polarized
VCO SECTION						
	Stability					
T_C	Temperature		200	500	ppm/°C	f = 10 kHz, $V^+ \geq 10V$, $0 < T_T < 70°C$*
PSR	Power Supply		0.05	0.5	%/V	$10V < V^+ < 24V$
f_{SW}	Sweep Range	5:1	8:1			S_3 closed, S_4 Open, $0 < V_S < 6V$ See Figure 5, $V^+ = 12V$
V_O	Output Voltage Swing	1.5	2.5		V p-p	S_5 open
DC	Duty Cycle Asymmetry		±1	±3	%	S_5 open
T_R	Rise Time		20		ns	10 pF to ground at Pin 15, S_5 open
T_F	Fall Time		40		ns	10 pF to ground at Pin 15, S_5 open
PHASE DETECTOR SECTION						
K_D	Conversion Gain		2		V/rad	$V_{IN} > 50mV$ rms, see Figure 8
Z_O	Output Impedance		6		kΩ	Measured looking into Pin 2 or 3
V_{OOS}	Output Offset Voltage		35	150	mV	Measured across Pin 1 and 3, $V_{IN} = 0$, S_5 open
VOLTAGE COMPARATOR SECTION						
A_{VOL}	Open Loop Voltage Gain	66	80		dB	f = 20Hz
Z_{IN}	Input Impedance	0.5	2		MΩ	Measured looking into Pin 1
V_{OS}	Input Offset Voltage		1		mV	
I_B	Input Bias Current		80		nA	
CMRR	Common Mode Rejection		90		dB	
LOGIC OUTPUT SECTION						
SR	Slew Rate		15		V/μsec	$R_L = 3k\Omega$, $C_L = 10pF$, S_2 closed
I_{OL}	"1" Output Leakage Current		0.02	10	μA	$V_O = +24V$
V_{OL}	"0" Output Voltage		0.2	0.4	V	$I_L = 10mA$
I_{SINK}	Current Sink Capability	30	50		mA	$V_O \leq 1V$

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

PRINCIPLES OF OPERATION

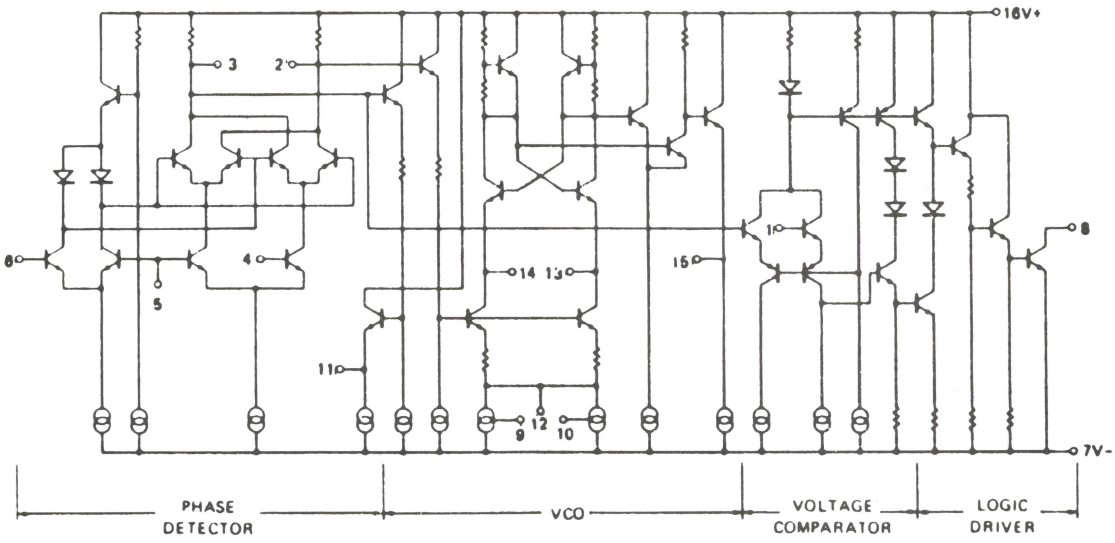
Description of Controls

Phase-Detector Inputs (Pin 4 and 6):
One input to the phase detector is used as the signal input; the remaining input should be ac coupled to the VCO output (Pin 15), to complete the PLL (see Figure 1). For split supply operation, these inputs are biased from ground as shown in Figure 2.

Phase-Detector Bias (Pin 5):
This terminal should be dc biased as shown in Figures 1 and 2, and ac grounded with a bypass capacitor. The bias resistor in series with this pin should be half the value as those in series with Pin 4 and 6.

Phase-Detector Outputs (Pin 2 and 3):
The low-frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase-detector inputs (Pin 4 and 6).

EQUIVALENT SCHEMATIC DIAGRAM



These differential phase-detector outputs are internally connected to the VCO control terminals. Pin 3 is also internally connected to the reference input of the voltage comparator section.

In normal use, the low-pass loop-filter capacitor, C_1, is connected between Pin 2 and 3. The 6 kΩ impedances of the two outputs add to 12 kΩ in the single-pole RC low-pass loop filter. Pin 2 is externally connected to the voltage comparator input (Pin 1) through an RC low-pass filter.

Frequency-Keying Input (Pin 10):
The VCO frequency can be varied between two discrete frequencies, f_1 and f_2, by connecting an external resistor, R_X, to this terminal, Referring to Figure 6, the VCO frequency is proportional to the sum of currents, I_1 and I_2, through the transistors, T_1 and T_2, on the monolithic chip. These transistors are biased from a fixed internal reference. The current, I_1, is set internally, and is partially controllable by the fine-tune adjustment, R_T. The current, I_2, is set by the external resistor, R_X, connected between Pin 10 and Pin 7. For any C_O setting, the VCO frequency, f_2, with R_X connected to Pin 10, can be expressed as:

$$f_2 = f_1 \left(1 + \frac{0.3}{R_X} \right) \text{Hz}$$

where f_1 is the frequency with Pin 10 open-circuited, and R_X is in kΩ. Note that f_2 can be fine-tuned to a desired value by the proper choice of R_X.

VCO Sweep input (Pin 12):
The VCO frequency can be swept over a broad range by applying an analog sweep voltage, V_S to Pin 12 (see Figure 5). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 5. The VCO temperature dependence is minimal when the sweep input is not used, and should be left open-circuited.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5mA or less, under all operating conditions.

VCO Conversion Gain (Pin 11):
The VCO voltage-to-frequency conversion gain, K_O, is inversely proportional to the value of the external gain-control resistor, R_O, connected across Pin 11 and 12.

Fine Tune Control (Pin 9):
For a given choice of timing capacitor, C_O, the VCO frequency can be further fine-adjusted to a desired frequency, f_1, by means of a trimmer resistor, R_T, connected from Pin 9 to Pin 7, as shown in Figure 6. The fine tuned VCO frequency, f_1, is related to R_T as:

$$f_1 \approx \frac{220}{C_O}\left(1 + \frac{0.1}{R_T}\right) \text{Hz}$$

where C_O is in µF, and R_T is in kΩ.

VCO Timing Capacitor (Pin 13 and 14):
The VCO free-running frequency, f_0, is inversely proportional to the timing capacitor, C_O, connected between Pin 13 and 14. With Pin 9 and 10 open-circuited, the VCO frequency is related to C_O as:

$$f_0 \approx \frac{220}{C_O} \text{ Hz}$$

where C_O is in µF.

VCO Output (Pin 15):
The VCO produces approximately a 2.5V p-p square wave output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to Pin 7 through a 10kΩ resistor to increase the output current drive capability. For high-voltage operation (V_{CC} > 20V), a 20kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output, for short-circuit protection. This output can drive a 10kΩ or larger load.

Using the frequency-keying control, the VCO frequency can also be stepped in a binary manner by applying a logic signal to Pin 10, as shown in Figure 6. For high-level logic inputs, the transistor, T_2, is turned off, R_X is effectively switched out of the circuit, and the VCO frequency is shifted from f_2 to f_1.

Voltage Comparator Input (Pin 1):
This pin provides the signal input to the voltage comparator section. The comparator section is normally used for post-demodulation slicing and pulse shaping. Normally, Pin 1 is connected to Pin 2 through a 15K external resistor, as shown in Figures 1 and 2. The input impedance level at this pin is approximately 2 MΩ.

Logic Driver Output (Pin 8):
This pin provides a binary logic output corresponding to the polarity of the input signal, at the voltage comparator inputs. It is an open-collector type stage with high-current sinking capability.

Definition of Terms

Phase-Detector Gain, K_d:
K_d is the output voltage from the phase detector per radian of phase difference at the phase-detector inputs (Pin 4 and 6). K_d is proportional to the input signal for low-level inputs (≤25mV rms), and is constant at high-input levels (see Figure 8).

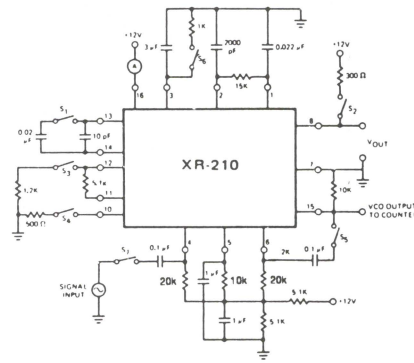


Figure 1. Test Circuits for Single Supply Operation

VCO Conversion Gain, K_O:

$$K_O \approx \frac{700}{C_O R_O} \text{ (radians/sec)/volt}$$

where C_O is in µF and R_O is in kΩ. For most applications, recommended values for R_O range from 1 kΩ to 10 kΩ.

When the XR-210 is connected as a PLL, its lock range can be controlled by varying the VCO gain control resistor, R_O, across Pin 11 and 12. For input signals greater than 30 mV rms, the PLL loop-gain is independent of signal amplitude, but is inversely proportional to R_O. Figure 7 shows the dependence of lock range, $\pm\Delta f_L$, on R_O.

Lock Range ($\Delta\omega_L$):
The range of frequencies in the vicinity of f_0 over which the PLL can maintain lock with an input signal. If saturation or limiting does not occur, the lock range is equal to the loop gain; i.e., $\Delta\omega L = K_T = K_d K_O$.

Capture Range ($\Delta\omega_C$):
The band of frequencies in the vicinity of fo where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range, and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L \, |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C)|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

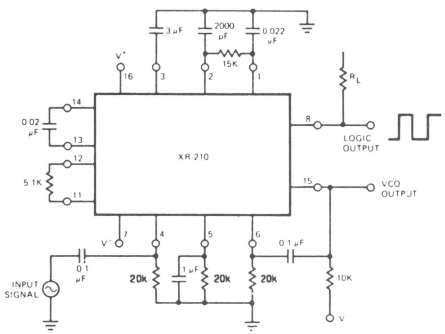


Figure 2. Test Circuit for Split Supplt Operation

APPLICATIONS INFORMATION

FSK Demodulation

Figure 3 shows a generalized circuit connection for FSK demodulation. The circuit is connected as a PLL system, by ac coupling the VCO output (Pin 15) to Pin 6. The FSK input is applied to Pin 4. When the input frequency is shifted, corresponding to a data bit, the polarity of the dc voltage across the phase-detector outputs (Pin 2 and 3) is reversed. The voltage comparator and the logic driver section convert this dc level shift to a binary pulse. The capacitor, C_1, serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. The timing capacitor, C_O, and fine-tune adjustments are used to set the VCO frequency, f_0, midway between the mark and space frequencies of the input signal. Typical component values for 300 baud (103-type) and 1200 baud (202-type) MODEM applications are listed below:

OPERATING CONDITIONS		TYPICAL COMPONENT VALUES
300 Baud		
Low Band:	f_1 = 1070Hz	R_0 = 5.1kΩ, C_0 = 0.22μF
	f_2 = 1270Hz	$C_1 = C_2$ = 0.047μF, C_3 = 0.033μF
High Band:	f_1 = 2025Hz	R_0 = 8.2kΩ, C_0 = 0.1μF
	f_2 = 2225Hz	$C_1 = C_2 = C_3$ = 0.033μF
1200 Baud		
	f_1 = 1200Hz	C_1 = 0.033μF, C_3 = 0.02μF
	f_2 = 2200Hz	C_2 = 0.01μF

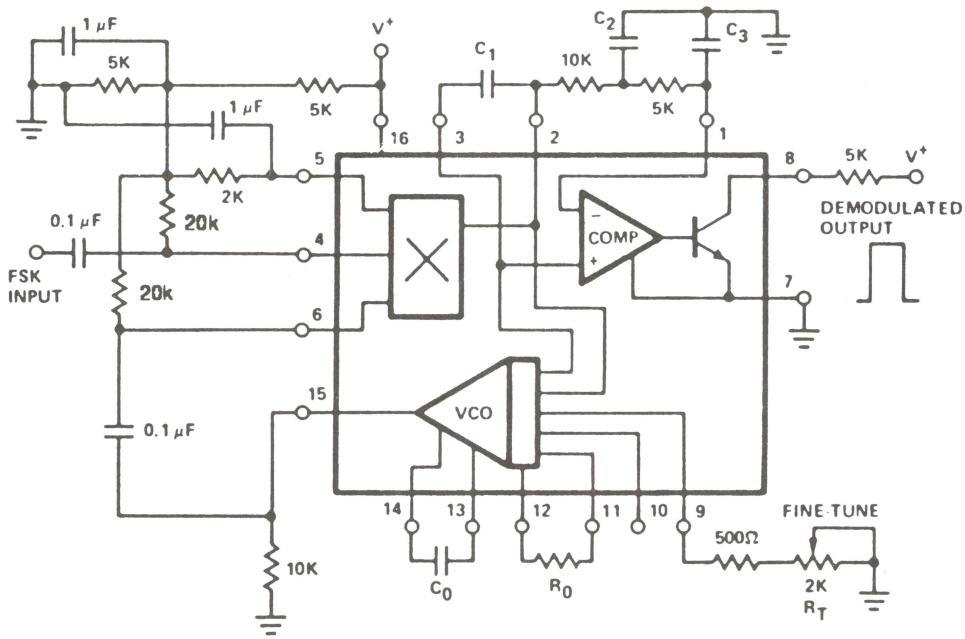


Figure 3. Circuit Connection for FSK Demodulation (Single Supply)

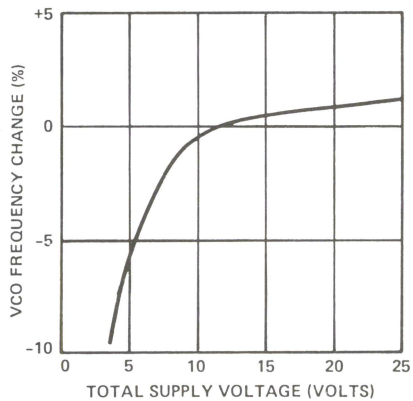
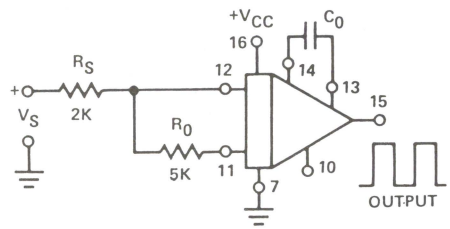


Figure 4. VCO Frequency Variation as a Function of Supply Voltage



(NOTE: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

Figure 5. Frequency Sweep Characteristics as a Function of Net Applied Sweep Voltage (Pin 10 Open)

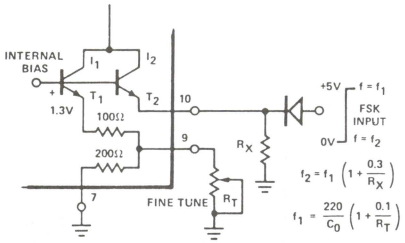


Figure 6. VCO Fine-Tune (Pin 9) and Frequency-Keying (Pin 10) Controls

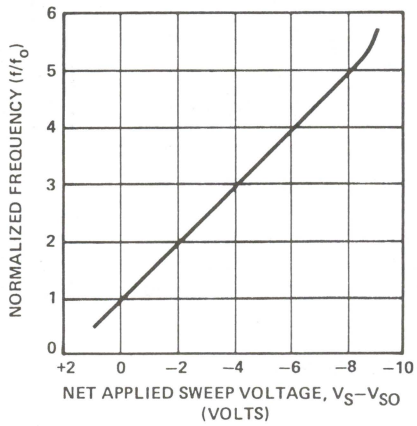


Figure 7.

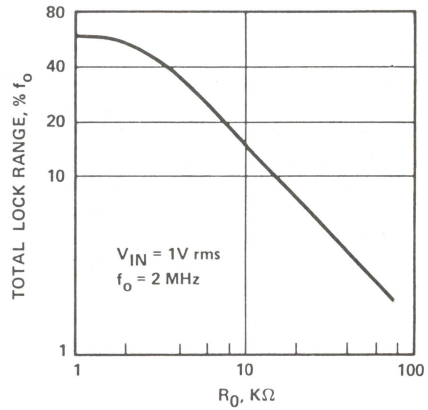


Figure 8. Total Lock Range, $\pm\Delta f_L$, versus VCO Gain Control Resistor, R_0

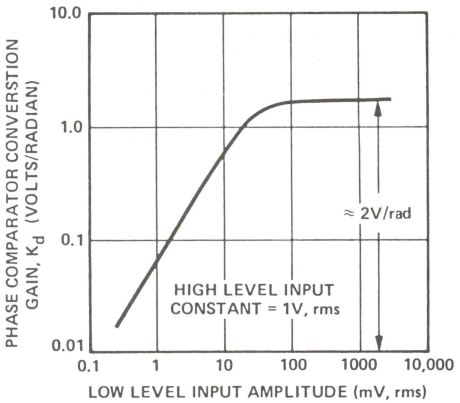


Figure 9. Phase Detector Conversion Gain, K_d, versus Input Amplitude

Monolithic Phase-Locked Loop

The XR-215 is a highly versatile monolithic phase-locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5V to 26V and a wide frequency band of 0.5Hz to 35MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range: 0.5Hz to 35MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL and ECL Logic Compatibility on Inputs
Wide Dynamic Range: 300μV to 3V, nominally
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to 50%
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65dB

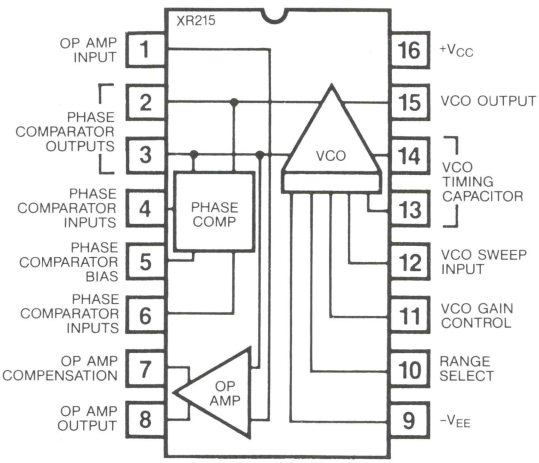
APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
Tone Decoding
Data Synchronization
Telemetry Coding/Decoding
FM, FSK and Sweep Generation
Crystal-Controlled Clock Recovery
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (Package Limitation)	
Ceramic	750mW
Derate above 25°C	5mW/°C
SO-16	500mW
Derate above + 25°C	4mW/°C
Temperature	
Storage	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-215CN	Ceramic	0°C to 70°C
XR-215MD	Japanese Dimension SO-16	0°C to 70°C

SYSTEM DESCRIPTION

The XR-215 monolithic PLL system consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the noninverting input of the operational amplifier A self-contained PLL System is formed by simply AC coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on-off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single external capacitor. The operational amplifier can be used for audio preamplification in FM detector applications or as a high speed sense amplifier (or comparator) in FSK demodulation.

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 12V (single supply), T_A = 25°C, Test Circuit of Figure 2 with C_0 = 100 pF, (silver-mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I — GENERAL CHARACTERISTICS					
SUPPLY VOLTAGE					
Single Supply	5		26	V dc	See Figure 2
Split Supply	±2.5		±13	V dc	See Figure 3
Supply Current	8	11	15	mA	See Figure 2
Upper Frequency Limit	20	35		MHz	See Figure 2, S^1 open, S^4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500µF (non-polarized)
VCO SECTION:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 6, 0°C ≤ T_T < 70°C*
Power Supply		0.1			V+ > 10V
Sweep Range	5:1	8:1			S_3 closed, S_4 open, 0 < V_S < 6V
					See Figure 9, C_0 = 2000pF
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Rise Time		20		ns	
Fall Time		30		ns	10pF to ground at Pin 15
PHASE COMPARATOR SECTION:					
Conversion Gain		2		V/rad	V_{IN} > 50mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	100	mV	Measured across Pins 2 and 3, V_{IN} = 0, S_5 open
OP AMP SECTION:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/µsec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		Vp-p	R_L = 30kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
II — SPECIAL APPLICATIONS					
A) FM Demodulation Test Conditions: Test circuit of Figure 4, V+, = 12V, input signal = 10.7MHz FM with Δf = 75kHz. f_{mod} = 1kHz.					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude		500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{IN} = 10mV rms, 30% AM
Output Signal/Noise		65		dB	
B) Tracking Filter Test Conditions: Test circuit of Figure 5, V+ = 12V, f_0 = 1 MHz, V_{IN} = 100mV rms, 50Ω source.					
Tracking Range (% of f_0)		±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{OUT}}{\Delta f/f_0}$		50		mV/%	Adjustable — See applications information

* Guaranteed, but not tested.

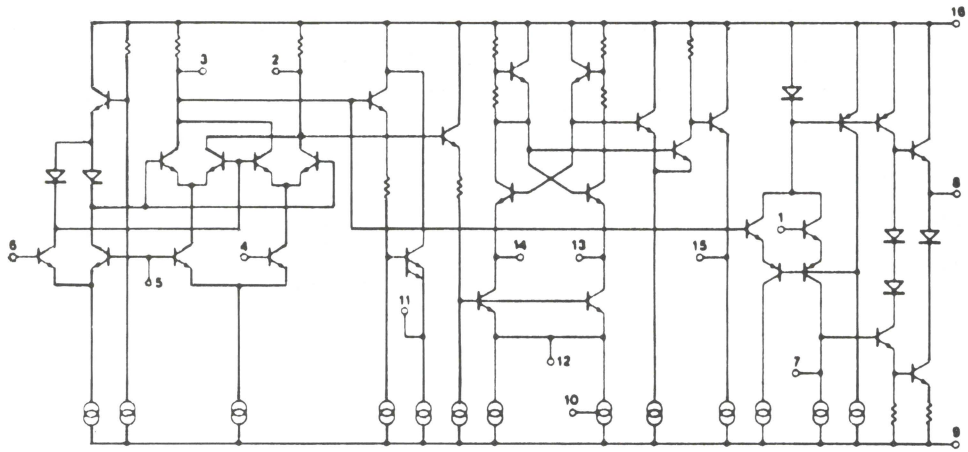


Figure 1. Equivalent Schematic Diagram

DESCRIPTION OF CIRCUIT CONTROLS

Phase Comparator Inputs (Pins 4 and 6)

One input to the phase comparator is used as the signal input. the remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see Figure 2). For split supply operation, these inputs are biased from ground as shown in Figure 3. For single supply operation, a resistive bias string similar to that shown in Figure 2 should be used to set the bias level at approximately $V_{CC}/2$. The dc bias current at these terminals is nominally 8μA.

Phase Comparator Bias (Pin 5)

This terminal should be dc biased as shown in Figures 2 and 3, and ac grounded with a bypass capacitor.

Phase Comparator Outputs (Pins 2 and 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase comparator inputs (pins 4 and 6). The phase comparator outputs are internally connected to the VCO control terminals (see Figure 1). One of the outputs (pin 3) is internally connected to the noninverting input of the operational amplifier. The low-pass filter is achieved by connecting an RC network to the phase comparator outputs as shown in Figure 14.

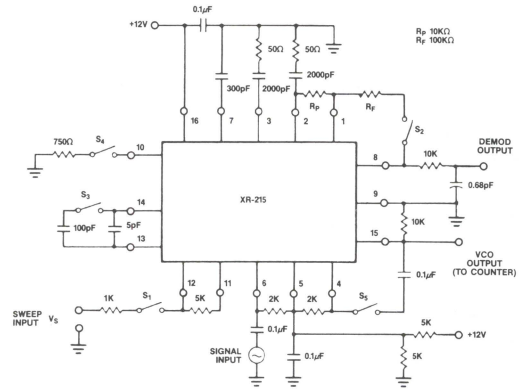


Figure 2. Test Circuit for Single Supply Operation

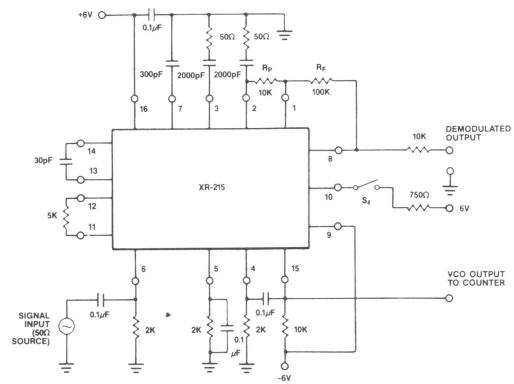


Figure 3. Test Circuit for Split-Supply Operation

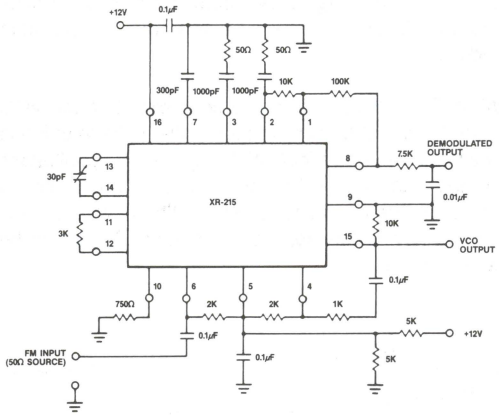


Figure 4. Test Circuit for FM Demodulation

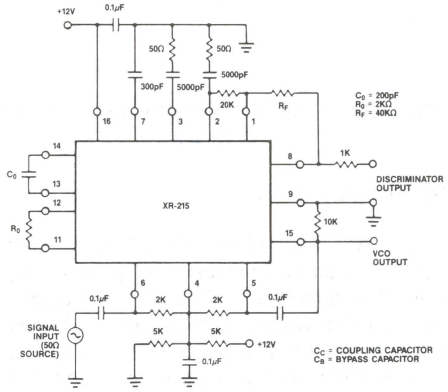


Figure 5. Test Circuit For Tracking Filter

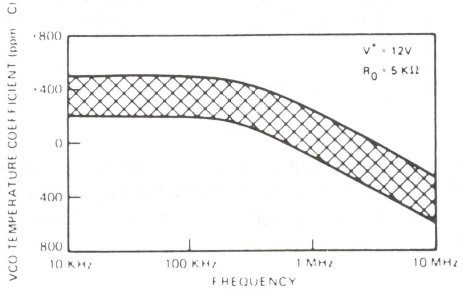


Figure 6. Typical VCO Temperature Coefficient Range as a Function of Operating Frequency (Pin 10 open)

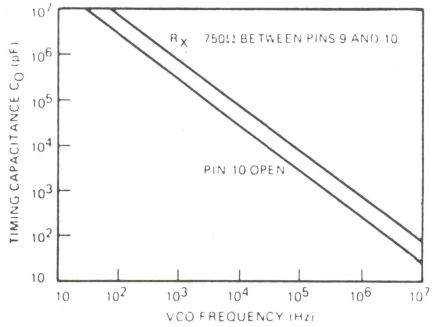


Figure 7. VCO Free Running Frequency vs Timing Capacitor

VCO Timing Capacitor (Pins 13 and 14)

The VCO free-running frequency, f_0, is inversely proportional to timing capacitor C_0 connected between pins 13 and 14. (See Figure 7).

VCO Output (Pin 15)

The VCO produces approximately a $2.5V_{p-p}$ output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 9 through a 10kΩ resistor to increase the output current drive capability. For high voltage operation (V_{CC} > 20V), a 20kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output tor short circuit protection.

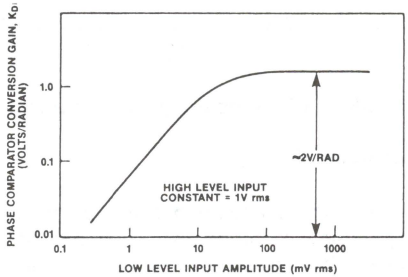


Figure 8. Phase Comparator Conversion Gain, K_d, versus Input Amplitude

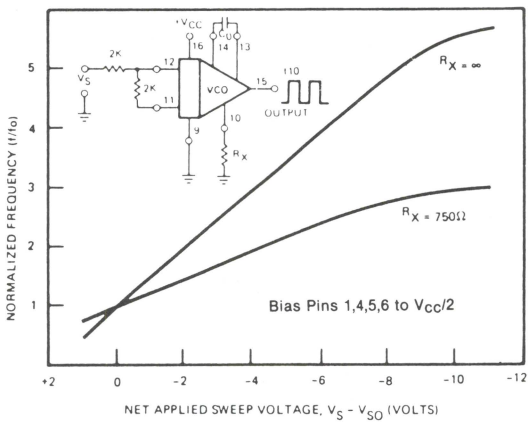


Figure 9. Typical Frequency Sweep Characteristics as a Funciton of Applied Sweep Voltage

(Note: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

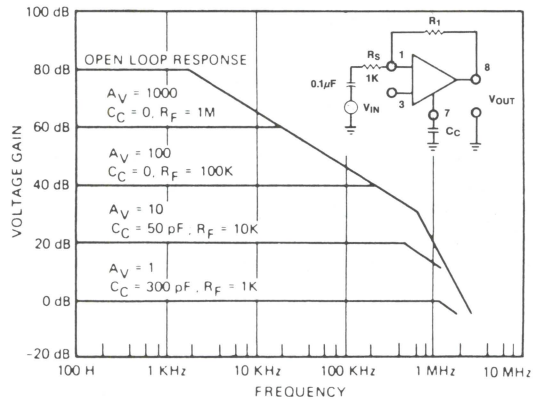


Figure 10. XR-215 Op Amp Frequency Response

VCO Sweep Input (Pin 12)

The VCO Frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see Figure 9). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 9. The VCO temperature dependence is minimum when the sweep input is not used.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5mA or less under all operating conditions.

ON-OFF KEYING: With pin 10 open circuited, the VCO can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 2 kΩ, oscillations will stop if the applied potential at pin 12 is raised 3 volts above its open-circuit value. When sweep, sync, or on-off keying functions are not used, R_S should be left open circuited.

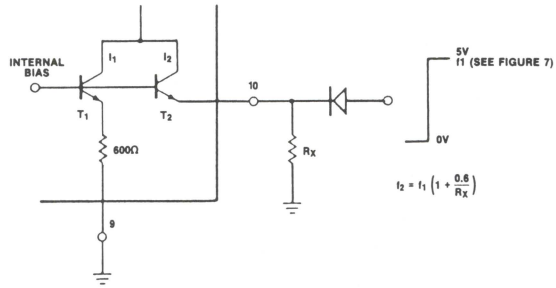


Figure 11. Explanation of VCO Range-Select Controls

Range-Select (Pin 10)

The frequency range of the XR-215 can be extended by connecting an external resistor, R_X, between pins 9 and 10. With reference to Figure 11, the operation of the range-select terminal can be explained as follows: The VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I_1 is set internally, whereas I_2 is set by the external resistor R_X. Thus, at any C_0 setting, the VCO frequency can be expressed as:

$$f_o = f_1 \left(1 + \frac{0.6}{R_X} \right)$$

where f_1 is the frequency with pin 10 open circuited and R_X is in kΩ. External resistor R_X (≈ 750Ω) is recommended for operation at frequencies in excess of 5MHz.

The range select terminal can also be used for fine tuning the VCO frequency, by varying the value of R_X. Similarly, the VCO frequency can be changed in discrete steps by switching in different values of R_X between pins 9 and 10.

Digital Programming

Using the range select control, the VCO frequency can be stepped in a binary manner, by applying a logic signal to pin 10, as shown in Figure 11. For high level logic inputs, transistor T_2 is turned off, and R_X is effectively switched out of the circuit. Using the digital programming capability, the XR-215 can be time-multiplexed between two separate input frequencies, as shown in Figures 18 and 19.

Amplifier Input (Pin 1)

This pin provides the inverting input for the operational amplifier section. Normally it is connected to pin 2 through a 10 kΩ external resistor (see Figure 2 or 3).

Amplifier Output (Pin 8)

This pin is used as the output terminal for FM or FSK demodulation. The amplifier gain is determined by the external feedback resistor, R_F, connected between pins 1 and 8. Frequency response characteristics of the amplifier section are shown in Figure 10.

Amplifier Compensation (Pin 7)

The operational amplitier can be compensated by a single 300 pF capacitor from pin 7 to ground. (See Figure 10).

BASIC PHASE-LOCKED LOOP OPERATION

Principle of Operation

The phase-locked loop (PLL) is a unique and versatile circuit technique which provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 12, the PLL is a feedback system comprised of three basic functional blocks: phase comparator, low-pass filter and voltage-controlled oscillator (VCO). The basic principle of operation of a PLL can be briefly explained as follows: with no input signal applied to the system, the error voltage V_d, is equal to zero. The VCO operates at a set frequency, f_0, which is known as the "free-running" frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_0, the feedback nature of the PLL causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

A Linearized Model for PLL

When the PLL is in lock, it can be approximated by the linear feedback system shown in Figure 13. ϕ_s and ϕ_o are the respective phase angles associated with the input signal and the VCO output, F(s) is the low-pass filter response in frequency domain, and K_d and K_o are the conversion gains associated with the phase comparator and VCO sections of the PLL.

DEFINITION OF XR-215 PARAMETERS FOR PLL APPLICATIONS

VCO Free-Running Frequency, f_o

The VCO frequency with no input signal. It is determined by selection of C_0 across pins 13 and 14 and can be increased by connecting an external resistor R_X between pins 9 and 10. It can be approximated as:

$$f_o \approx \frac{220}{C_O}\left(1 + \frac{0.6}{R_X}\right)$$

where C_0 is in µF and R_X is in kΩ. (See Figure 7).

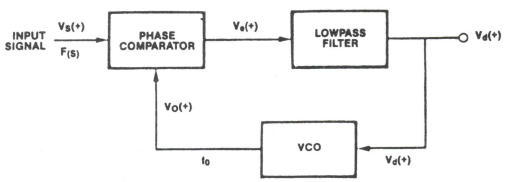


Figure 12. Block Diagram of a Phase-Locked Loop

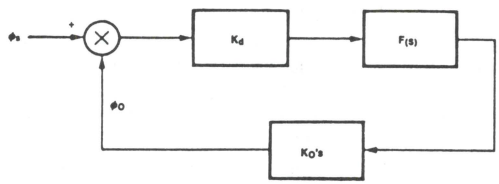


Figure 13. Linearized Model of a PLL as a Negative Feedback System

Phase Comparator Gain K_d

The output voltage from the phase comparator per radian of phase difference at the phase comparator inputs (pins 4 and 6). The units are volts/radians.

VCO Conversion Gain K_o

The VCO vollage-to-frequency conversion gain is determined by the choice of timing capacitor C_0 and gain control resistor, R_0 connected externally across pins 11 and 12. It can be expressed as

$$K_o \approx \frac{700}{C_0 R_0} \quad \text{(radians/sec)/volt}$$

where C_0 is in μF and R_0 is in kΩ. For most applications, recommended values for R_0 range from 1kΩ to 10kΩ.

Lock Range ($\Delta\omega_L$)

The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the "tracking" or "holding" range. If saturation or limiting does not occur, the lock range is equal to the loop gain, i.e. $\Delta\omega_L = K_T = K_d K_o$.

Capture Range ($\Delta\omega_C$)

The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L \, |F(j\Delta\omega_C|$$

where $|F(j\Delta\omega_C|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

where T_1 is the filter time constant.

Amplifier Gain A_V

The voltage gain of the amplifier section is determined by feedback resistors R_F and R_p between pins (8,1) and 2,1) respectively. (See Figures 2 and 3). It is given by:

$$A_V \approx \frac{-R_F}{R_1 + R_P}$$

where R_1 is the 6KΩ) internal impedance at pin 2, and R_p is the external resistor between pins 1 and 2.

Low-Pass Filter

The low-pass filter section is formed by connecting an external capacitor or RC network across terminals 2 and 3. The low-pass filter components can be connected either between pins 2 and 3 or, from each pin to ground. Typical filter configurations and corresponding filter transfer functions are shown in Figure 14 where R_1 (6kΩ) is the internal Impedance at pins 2 and 3. It should be noted that the rejection of the low pass filter decreases above 2MHz when the capacitor is tied from Pin 2 to 3.

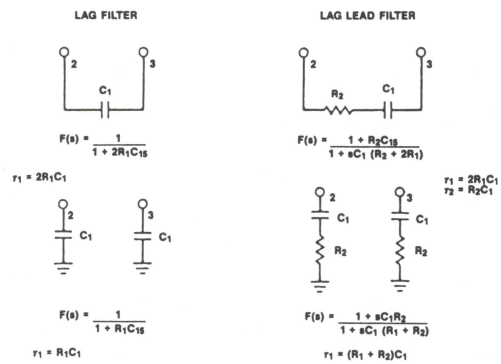


Figure 14.

APPLICATIONS INFORMATION

FM Demodulation

Figure 15 shows the external circuit connections to the XR-215 for frequency-selective FM demodulation. The choice of C_0 is determined by the FM carrier frequency (see Figure 7). The low-pass filter capacitor C_1 is determined by the selectivity requirements. For carrier frequencies of 1 to 10MHz, C_1 is in the range of 10 C_0 to 30 C_0. The feedback resistor R_F can be used as a "volume-control" adjustment to set the amplitude of the demodulated output. The demodulated output amplitude is proportional to the FM deviation and to resistors R_0 and R_F For ±1% FM deviation it can be approximated as:

$$V_{OUT} \approx R_0 R_F \left(1 + \frac{0.6}{R_X} \right) \text{ mV, rms}$$

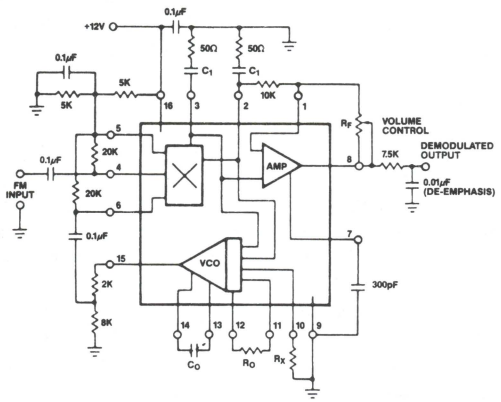


Figure 15. Circuit Connection for FM Demodulation

The damping factor can be calculated by using

$$\zeta = 1/2 \left(\frac{K_0 K_d}{\tau_1} \right)^{1/2} \cdot \tau_2 + \left(\frac{1}{K_0 K_d} \right)$$

where all resistors are in kΩ and R_X is the range extension resistor connected across pins 9 and 10. For circuit operation below 5MHz, R_X can be open circuited. For operation above 5MHz, $R_X \approx 750\Omega$ is recommended.

Typical output signal/noise ratio and harmonic distortion are shown in Figures 16 and 17 as a function of FM deviation, for the component values shown in Figure 4.

Multi-Channel Demodulation

The ac digital programming capability of the XR-215 allows a single circuit be time-shared or multiplexed between two information channels, and thereby selectively demodulate two separate carrier frequencies. Figure 18 shows a practical circuit configuration for time- multiplexing the XR-215 between two FM channels, at 1MHz and 1.1MHz respectively. The channel-select logic signal is applied to pin 10, as shown in Figure 18 with both input channels simultaneously present at the PLL input (pin 4). Figure 19 shows the demodulated output as a function of the channel-select pulse where the two inputs have sinusoidal and triangular FM modulation respectively.

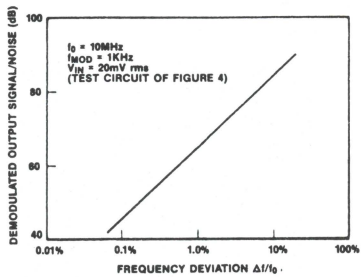


Figure 16. Output Signal/Noise Ratio as a Funciton of FM Deviation

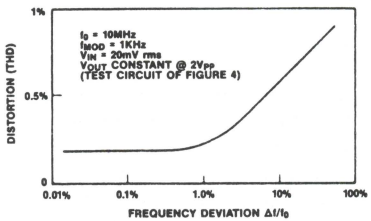


Figure 17. Output Distortion as a Function of FM Deviation

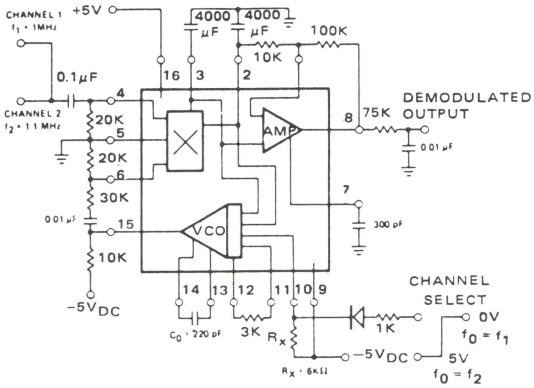


Figure 18. Time-Multiplexing XR-215 Between Two Simultaneous FM Channels

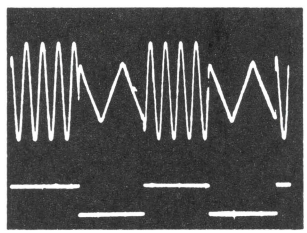


Figure 19. Demodulated Output Waveforms for Time-Multiplexed Operation

Top: Demodulated Output
Sinewave — Channel 1
Triangle Wave — Channel 2

Bottom: Channel Select Pulse

FSK Demodulation

Figure 20 contains a typical circuit connection for FSK demodulation. When the input frequency is shifted, corresponding to a data bit, the dc voltage at the phase comparator outputs (pins 2 and 3) also reverses polarity. The operational amplifier section is connected as a comparator, and converts the dc level shift to a binary output pulse. One of the phase comparator outputs (pin 3) is ac grounded and serves as the bias reference for the operational amplifier section. Capacitor C_1 serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. Range select resistor, R_X, can be used as a fine- tune adjustment to set the VCO frequency.

Typical component values for 300 baud and 1200 baud operation are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070Hz	R_0 = 5kΩ, C_0 = 0.17μF
f_2 = 1270Hz	$C_1 = C_2$ = 0.047μF, C_3 = 0.033μF
High Band: f_1 = 2025Hz	R_0 = 8kΩ, C_0 = 0.1μF
f_2 = 2225Hz	$C_1 = C_2 = C_3$ = 0.033μF
1200 Baud	R_0 = 2kΩ, C_0 = 0.12μF
f_1 = 1200Hz	$C_1 = C_3$ = 0.003μF
f_2 = 2200Hz	C_2 = 0.01μF

Note that for 300 Baud operation the circuit can be time-multiplexed between high and low bands by switching the external resistor R_X in and out of the circuit with a control signal, as shown in Figure 11.

FSK Generation

The digital programming capability of the XR-215 can be used for FSK generation. A typical circuit connection for this application is shown in Figure 21. The VCO frequency can be shifted between the mark (f_2) and space (f_1) frequencies by applying a logic pulse to pin 10. The circuit can provide two separate FSK outputs: a low level (2.5 V_{p-p}) output at pin 15 or a high amplitude (10 V_{p-p}) output at pin 8. The output at each of these termihals is a symmetrical squarewave with a typical second harmonic content of less than 0.3%.

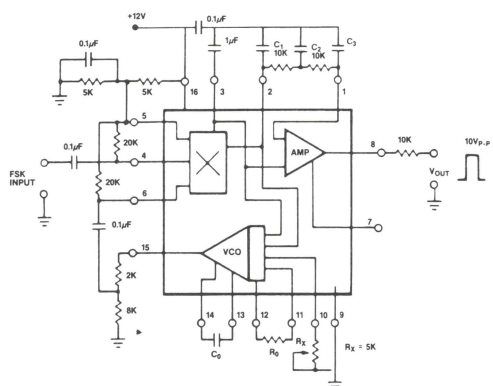


Figure 20. Circuit Connection for FSK

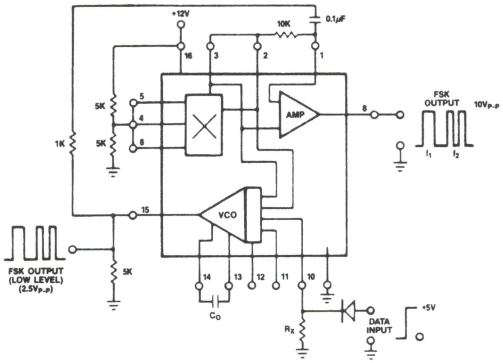


Figure 21. Circuit Connection For FSK Generation

Frequency Synthesis

In frequency synthesis applications, a programmable counter or divide-by-N circuit is connected between the VCO output (pin 15) and one of the phase detector inputs (pins 4 or 6), as shown in Figure 22. The principle of operation of the circuit can be briefly

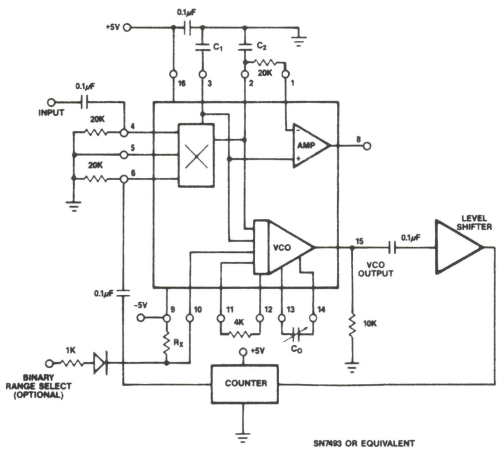


Figure 22. Circuit Connection For Frequency Synthesis

explained as follows: The counter divides down the oscillator frequency by the programmable divider modulus, N. Thus, when the entire system is phase-locked to an input signal at frequency, f_s, the oscillator output at pin 15 is at a frequency (Nf_s), where N is the divider modulus. By proper choice of the divider modulus, a large number of discrete frequencies can be synthesized from a given reference frequency. The low-pass filter capacitor C_1 is normally chosen to provide a cut-off frequency equal to 0.1% to 2% of the signal frequency, f_s.

The circuit was designed to operate with commercially available monolithic programmable counter circuits using TTL logic, such as MC4016, SN5493 or equivalent. The digital or analog tuning characteristics of the VCO can be used to extend the available range of frequencies of the system, for a given setting of the timing capacitor C_0.

Typical input and output waveforms for N = 16 opera. tion with f_s = 100kHz and f_o = 1.6MHz are shown in Figure 23.

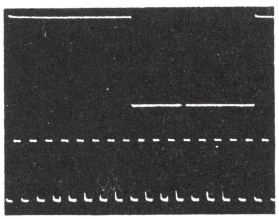


Figure 23. Typical Input/Output Waveforms for N=16
Top: Input (100kHz)
Bottom: VCO Output (1.6MHz)
Vertical Scale 1 V/cm

Tracking Filter/Discriminator

The wide tracking range of the XR-215 allows the system to track an input signal over a 3:1 frequency range, centered about the VCO free running frequency. The tracking range is maximum when the binary range-select (pin 10) is open circuited. The circuit connections for this application are shown in Figure 24. Typical tracking range for a given input signal amplitude is shown in Figure 25. Recommended

values of external components are: $1k\Omega < R_0 < 4k\Omega$ and $30\ C_0 < C_1 < 300\ C_0$ where the timing capacitor C_0 is determined by the center frequency requirements (see Figure 7).

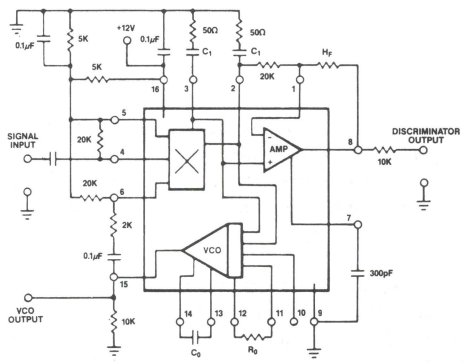


Figure 24. Circuit Connection For Tracking Filter Applications

The phase-comparator output voltage is a linear measure of the VCO frequency deviation from its free-running value. The amplifier section, therefore, can be used to provide a filtered and amplified version of the loop error voltage. In this case, the dc output level at pin 15 can be adjusted to be directly proportional to the difference between the VCO free-running frequency, f_o, and the input signal, f_s. The entire system can operate as a "linear discriminator" or analog "frequency-meter" over a 3:1 change of input frequency. The discriminator gain can be adjusted by proper choice of R_0 or R_F, For the test circuit of Figure 24, the discriminator output is approximately $(0.7\ R_0R_F)$ mV per % of frequency deviation where R_0 and R_F are in kΩ. Output non-linearity is typically less than 1% for frequency deviations up to ±15%. Figure 27 shows the normalized output characteristics as a function of input frequency, with $R_0 = 2k\Omega$ and $R_F = 36k\Omega$.

Crystal-Controlled PLL

The XR-215 can be operated as a crystal-controlled phase-locked loop by replacing the timing capacitor with a crystal. A circuit oonnection for this application is shown in Figure 27. Normally a small tuning capacitor (≈ 30 pF) is required in series with the crystal to set the crystal frequency. For this application the crystal should be operated in its fundamental mode. Typical pull-in range of the circuits is 11kHz at 10MHz. There is some distortion on the demodulated output.

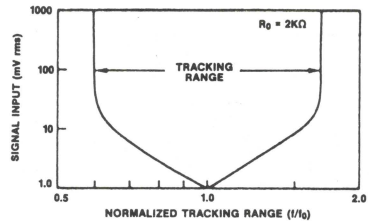


Figure 25. Tracking Range vs Input Amplitude (Pin 10 Open Circuited)

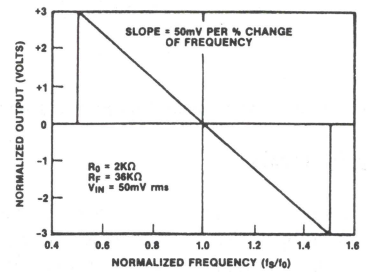


Figure 26. Typical Discriminator Output Characteristics for Tracking Filter Applications

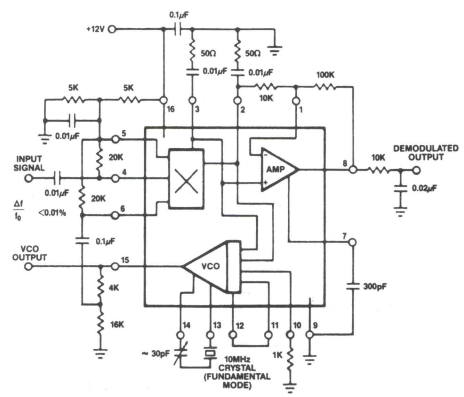


Figure 27. Typical Circuit Connection for Crystal-Controlled Clock Recovery.

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides rationometric operation for low system performance variations with power supply changes.

The XR-2211 is available in 14 pin DIP ceramic or plastic packages specified for commercial or military temperature ranges.

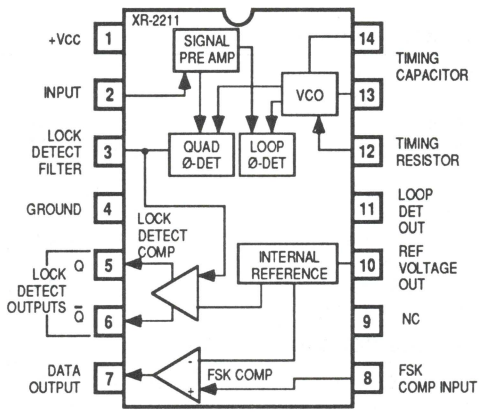
FEATURES

Wide Frequency Range	0.01Hz to 300kHz
Wide Supply Voltage Range	4.5V to 20V
HCMOS/TTL/Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2mV to 3V rms
Adjustable Tracking Range (±1% to 80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	900mW
Ceramic Package	750mW
Derate Above T_A = +25°C	8mW/°C
Plastic Package	800mW
Derate Above T_A = +25°C	60mW/°C
JEDEC SO	390mW
Derate Above T_A = +25°C	5mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	–55°C to +125°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C
XR-2211N	Ceramic	–40°C to +85°C
XR-2211P	Plastic	–40°C to +85°C
XR-2211D	JEDEC SO-14	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 12V$, $T_A = +25°C$, $R_O = 30K\Omega$, $C_O = 0.033\mu F$.

PARAMETER	2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Curreent		4	7		5	9	mA	$R_0 \geq 10k\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		11	13		11		%	Deviation from fo = 1/RoCo
Frequency Stability								$R_1 = 1/2$
Temperature		120	150		120		ppm/°C	* See Figure 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$. See Fig. 7.
		0.2			0.2		%/V	$V^+ 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2k\Omega$, $C_0 = 400pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2M\Omega$, $C_0 = 50\mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	kΩ	
Recommended Range 1	15			5		100	kΩ	See Figs. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	1150	1200	1300	1 100	±200	±300	µA	Measured at Pin 11.
Output Offset Current		1			±2		µA	
Output Impedance		1			1		MΩ	
Maximum Swing	14	±5		14	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		µA	
Output Imped		1			1		MΩ	
Maximum Swing		11			11		V pp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		kΩ	
Input Signal								
Voltage Required to								
Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTION								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70			55 70		dB	$R_L = 5.1k\Omega$
Output Voltage Low		300			300		mV	$I_C = 3mA$
Output Leakage Current		0.01			0.01		µA	$V_O = 20V$
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	AC Small Signal
Maximum Source Current		80			80		µA	

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

SYSTEM DESCRIPTION

The output of the phase detector produces sum and difference frequencies of the input and the VCO (internally connected). When in lock, these frequencies are $f_{IN} + f_{VCO}$ (2 times f_{IN} when in lock) and $f_{IN} - f_{VCO}$ (0HZ when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produced both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock detect outputs. It the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5mA of load current.

Lock Detect Complement, $\bar{Q}$ (Pin 6): The output at Pin 6 is the logic complement of the lock detect output at Pin 5. This output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate,

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by R_F and C_F of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

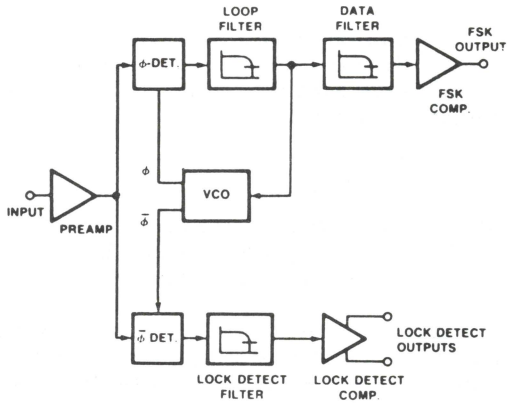


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V + /2 - 650mV$. The dc voltage level at this pin forms an internal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (see Figure 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

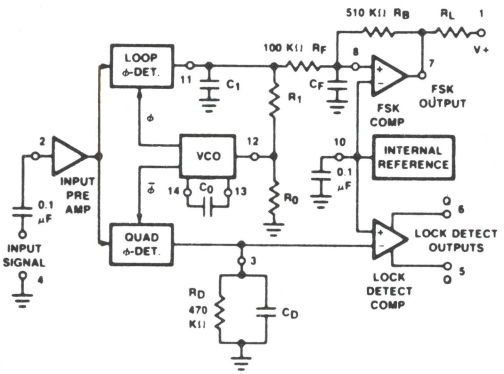


Figure 2. Generalized Circuit Connection for FSK and Tone Detection

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ see Figure 8).

This terminal is a low impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤ 3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200pF to 10μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in Figure 2, and applying an alternating bit pattern of O's and I's at known mark and space frequencies. By adjusting R_O, the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_o value is accurately referenced to the mark and space frequencies.

DESIGN EQUATIONS

(See Figure 2 for definition of components.)

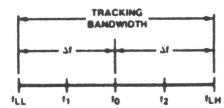
1. VCO Center Frequency, f_0:
   $f_0 = 1/R_oC_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 10):
   $V_R = V+/2 - 650mV$

3. Loop Low-Pass Filter Time Constant, τ:
   $\tau = R_1C_1$

4. Loop Damping, ζ:
   $\zeta = 1/4 \sqrt{\frac{C_0}{C_1}}$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τ_F:
   $\tau_F = R_FC_F$

7. Loop Phase Detector Conversion Gain, Kø: (Kø is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase detector input):
   Kø = $02V_R/\pi$ volts/radian

8. VCO Conversion gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):
   $K_0 = -1/V_RC_0R_1$ Hz/volt

9. Total Loop Gain, K_T:
   $K_T = 2\pi K\text{ø}K_0 = 4/C_0R_1$ rad/sec/volt

10. Peak Phase Detector Current I_A:
    $I_A = V_R$ (volts)/25mA

APPLICATIONS INFORMATION

FSK Decoding

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510KΩ) from Pin 7 to Pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states. Recommended component values for some of the most commonly used FSK bands are given in Table 1.

Design Instructions:

The circuit of Figure 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_0:

$$f_0 = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_0, to be in the range of 10KΩ to 100KΩ. This choice is arbitrary. The recommended value is R_0 = 20KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$C_0 = 1/R_0 f_0$

d) Calculate R_1 to give a Δf equal to the mark space deviation:

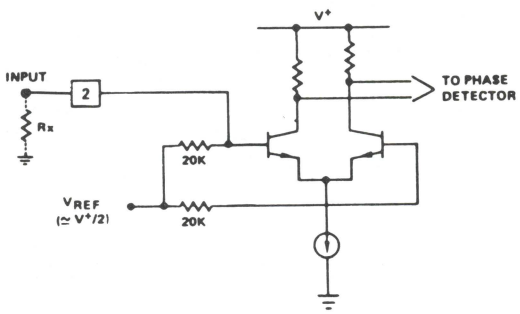
$R_1 = R_0[f_0/(f_1 - f_2)]$

e) Calculate C_1 to set loop damping. (See design equation No. 4.):

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

f) The input to the XR-2211 may sometimes be to sensitive to noise conditions on the input line. Figure 3 illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, R_X, connected from pin 2 to ground. The value of R_X is chosen by the equation and the desired minimum signal threshold level.



$$V_{IN\ MINIMUM\ (PEAK)} \approx V+ \left[\frac{10K}{R_X + 20K}\right] \pm 2.8\ mV$$

Figure 3. Desensitizing Input Stage

g) Calculate Data Filter Capacitance, C_F:

For R_F = 100KΩ, R_B = 510KΩ, the recommended value of C_F is:

$C_F \approx 3/(\text{Baud Rate})\ \mu F$

Note: All calculated component values except R_0 can be rounded to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 9.)

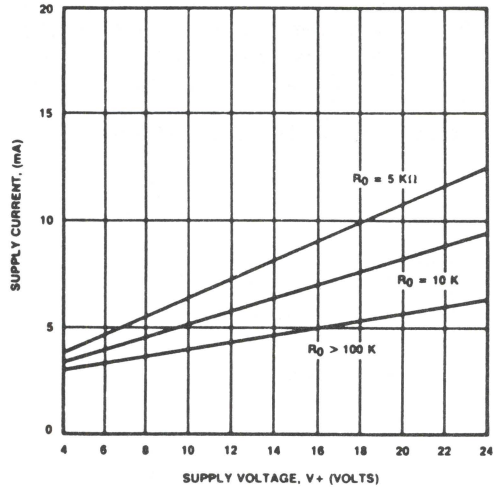


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

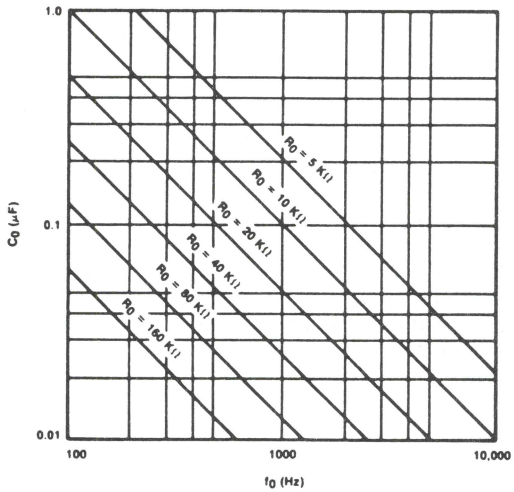


Figure 5. VCO Frequency vs Timing Resistor

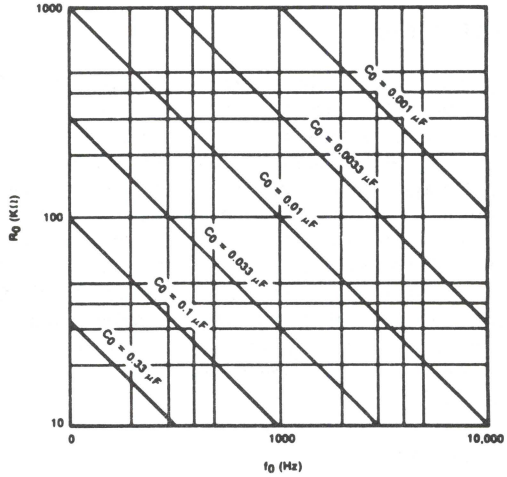


Figure 6. VCO Frequency vs Timing Capacitor

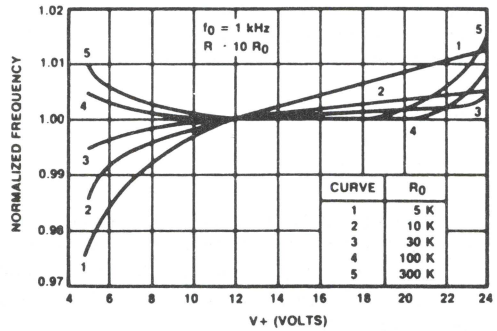


Figure 7. Typical f_0 vs Power Supply Characteristics

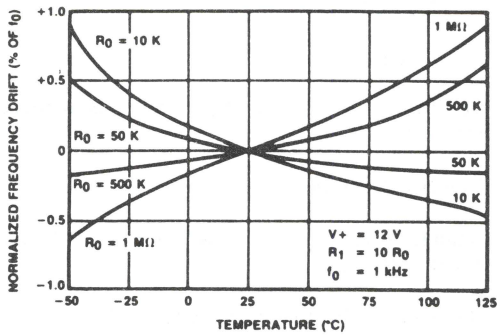


Figure 8. Typical Center Frequency Drift vs Temperature

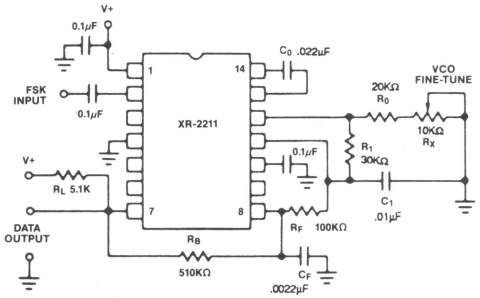


Figure 9. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

Design Example:

1200 Baud FSK demodulator with mark space frequencies of 1200/2200Hz:

Step 1: Calculate f_0: f_0 (1200 + 2200) (1/2) = 1700Hz

Step 2: Choose $R_0 \simeq 26.7K\Omega$ (20KΩ fixed resistor in series with 10KΩ potentiometer)

Step 3: Calculate C_0 from design equation 1: yielding $C_0 = 0.022\mu F$

Step 4: Calculate R_1: $R_1 = R_0$ (1700/1000) ≈ 45KΩ

Step 5: Calculate C_1: $C_1 = C_0/4 = 0.055\mu F \approx 0.01\mu f$

Note: All values except R_0 can be rounded to nearest standard value.

Table 1. Recommended Component Values for Commonly Used FSK Bands. (See Circuit of Figure 10.)

FSK BAND	COMPONENT VALUES	
300 Baud	$C_0 = 0.039\mu F$	$C_F = 0.005\mu F$
f_1 = 1070 Hz	$C_1 = 0.01\mu F$	$R_0 = 18K\Omega$
f_2 = 1270 Hz	$R_1 = 100K\Omega$	
300 Baud	$C_0 = 0.022\mu F$	$C_F = 0.005\mu F$
f_1 = 2025 Hz	$C_1 = 0\ 0047\mu F$	$R_0 = 18K\Omega$
f_2 = 2225 Hz	$R_1 = 200K\Omega$	
Caller I.D. Rec'v		
(1200 Baud)	$C_0 = 0.022\mu F$	$C_F = 0.0022\mu F$
f1 = 1200 Hz	C1 = 0.01μF	R0 = 26.7KΩ
f_2 = 2200 Hz	$R_1 = 45K\Omega$	$C_D = 0.1\mu F$
		$R_D = 470K\Omega$

FSK Decoding with Carrier Detect

The lock detect section of XR-2211 can be used as a carrier detect option, for FSK decoding. The recommended circuit connection for this application is shown in Figure 10. The open collector lock detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL and the Pin 6 output goes "high," to enable the data output.

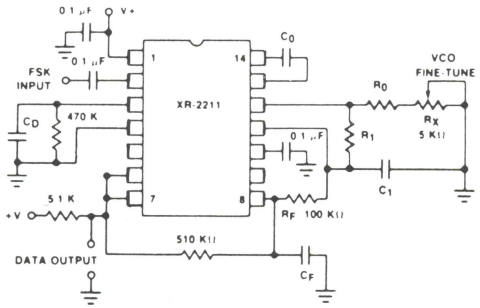


Figure 10. External Connectors for FSK Demodulation with Carrier Detect Capability

Note: Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_c > \Delta f/2$. For R_D = 470KΩ, the approximate minimum value of C_D can be determined by:

C_D (μF) ≥ 16/capture range in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output. For Caller I.D. applications choose $C_D = 0.1\mu F$.

Tone Detection

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs. Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these

outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

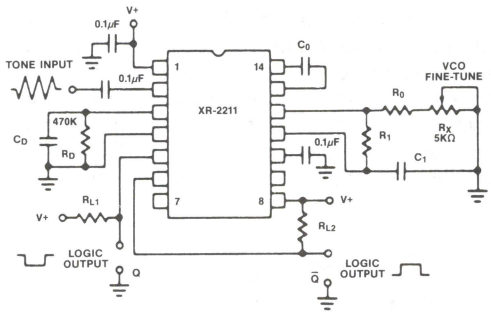


Figure 11. Circuit Connection for Tone Detection

Both logic outputs at Pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 11.

With reference to Figures 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\bar{Q}$ logic outputs.

Design Instructions:

The circuit of Figure 11 can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15KΩ to 100KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_S (see Figure 6): $C_0 = 1/R_0 f_S$

c) Calculate R_1 to set bandwidth ±Δf (see design equation No. 5):

$R_1 = R_0(f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor;

$C_1 = C_0/16\,\zeta\,2$

Normally $\zeta \approx 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\ C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470KΩ, C_D must be:

$C_D(\mu F) \geq (16/\text{capture range in Hz})$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1kHz ± 20Hz:

a) Choose R_0 = 20KΩ (18KΩ in series with 5KΩ potentiometer).

b) Choose C_0 for f_0 = 1kHz (from Figure 6): C_0 = 0.05μF.

c) Calculate R_1: $R_1 = (R_0)\,(1000/20)$ = 1MΩ.

d) Calculate C_1: for ζ = 1/2, C_1 = 0.25, C_0 = 0.013μF

e) Calculate C_D: $C_D = 16/38$ = 0.42μF.

f) Fine-tune center frequency with 5KΩ potentiometer, R_X.

Linear FM Detection

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 12.

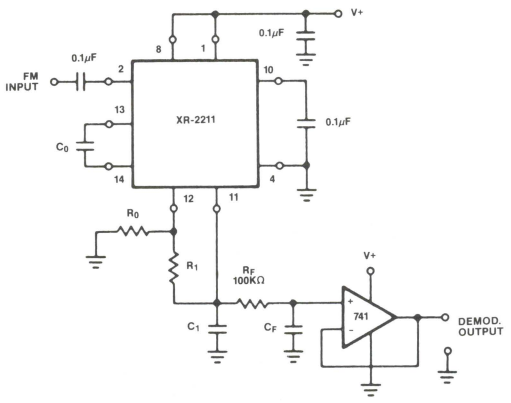


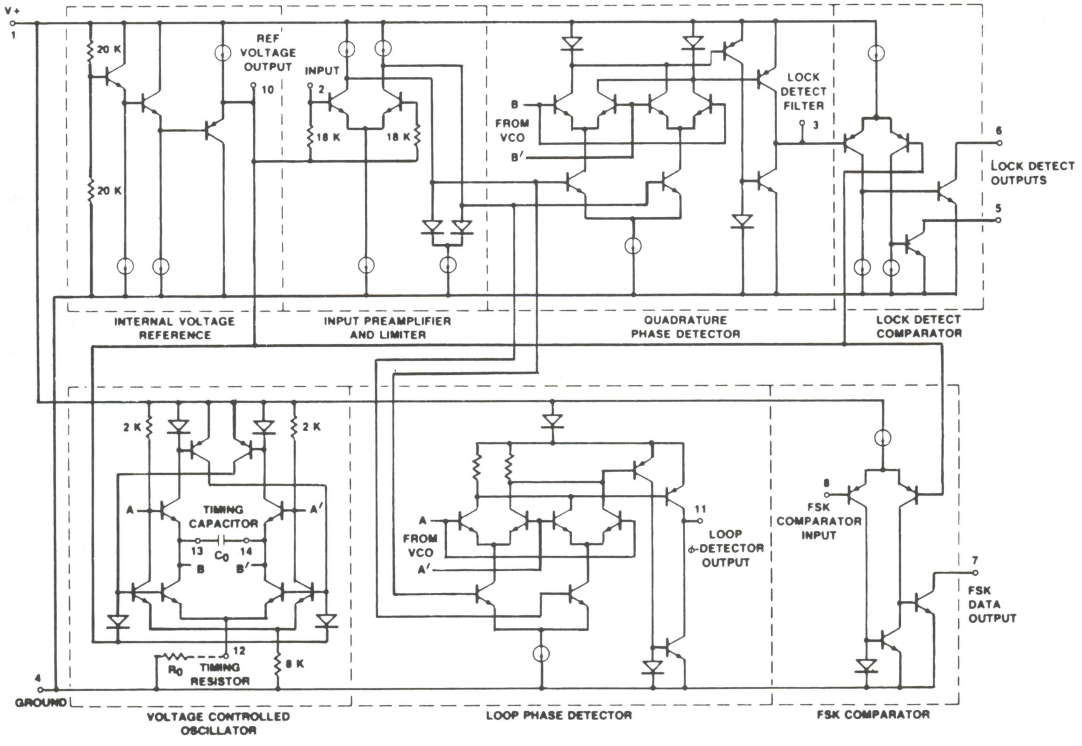
Figure 12. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section an Design Equation for Component Values.)

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = R_1 V_R/100 R_0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage ($V_R = V + /2 - 650mV$). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on design equations.

EQUIVALENT SCHEMATIC DIAGRAM



Precision Phase-Locked Loop

GENERAL DESCRIPTION

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communications and control system applications. Its on board reference and uncommitted operational amplifier, together with a typical temperature stability of better than 20 ppm/°C, make it ideally suited for frequency synthesis, FM detection, and tracking filter applications. The wide input dynamic range, large operating voltage range, large frequency range, and HCMOS and TTL compatibility contribute to the usefullness and wide applicability of this device.

FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01Hz to 300kHz
Wide Supply Voltage Range	4.5V to 20V
TTL/HCMOS Compatible	(V_{CC} = 5VDC)
Wide Dynamic Range	2mV to 3Vrms
Adjustable Tracking Range(±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, Typ.

APPLICATIONS

Frequency Synthesis
Data Synchronization
FM Detection
Tracking Filters
FSK Demodulation

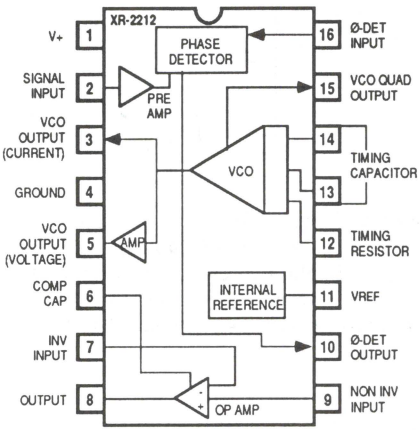
ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Input Signal Level	3Vrms
Power Dissipation	
Ceramic Package:	750mW
Derate Above T_A = + 25°C	6mW/°C
Plastic Package:	625mW
Derate Above T_A = + 25°C	5mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2212M	Ceramic	–55°C to +125°C
XR2212CN	Ceramic	0°C to +70°C
XR-2212CP	Plastic	0°C to +70°C
XR-2212N	Ceramic	–40°C to +85°C
XR-2212P	Plastic	–40°C to +85°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-2212 is a complete PLL system with buffered inputs and outputs, an internal reference, and an uncommited op amp. Two VCO outputs are pinned out; one sources current, the other sources voltage. This enables operation as a frequency synthesizer using an external programmable divider. The op amp section can be used as an audio preamplifier for FM detection or as a high speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth, and tracking range of the PLL are controlled independantly by external oomponents. The PLL output is directly by compatible with CMOS, HCMOS and TTL logic families as well as microprocessor peripheral systems.

The precision PLL system operates over a supply voltage range of 4.5V to 20V, a frequency range of 0.01Hz to 300kHz, and accepts input signals in the range of 2mV to 3Vrms. Temperature stability of the VCO is typically better than 20 ppm/°C with the optimum timing resistor value.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30k\Omega$, $C_0 = 0.033\mu F$, unless otherwise specified. See Figure 2 for component designation.

PARAMETER	XR-2212/2212M			XR-2212C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		15	4.5		15	V	
Supply Current		6	10		6	12	mA	$R_0 \geq 10K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.*
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$ See Fig. 7.
		.2			.2		%/V	$V^+ = 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2K\Omega$, $C_0 = 400pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2M\Omega$, $C_0 = 50\mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
OSCILLATOR OUTPUTS								
Voltage Output								Measured at Pin 5.
Positive Swing, V^OH		11			11		V	
Negative Swing, V^OL		.4	.8		.5		V	
Current Sink Capability		1			1		mA	
Current Output								Measured at Pin 3.
Peak Current Swing	100	150			150		µA	
Output Impedance		1			1		MΩ	
Quadrature Output								Measured at Pin 15.
Output Swing		0.6			0.6		V	
DC Level		0.3			0.3		V	Referenced to Pin 11.
Output Impedance		3			3		KΩ	
LOOP PHASE DETECTOR SECTION								Measured at Pin 10.
Peak Output Current	±150	±200	±300	±100	±200	±300	µA	
Output Offset Current		±1			±2		µA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 11.
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		KΩ	
Input Signal to Cause Limiting		2	10		2		mVrms	
OP AMP SECTION								
Voltage Gain	55	70		55	70		dB	$R_L = 5.1K\Omega$, $R_F = \infty$
Input Bias Current		0.1	1		0.1	1	µA	
Offset Voltage		±5	±20		±5	±20	mV	
Slew Rate		2			2		V/µsec	
INTERNAL REFERENCE								Measured at Pin 11.
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	
Output Impedance		100			100		Ω	AC Small Signal
Maximum Source Current		80			80		µA	

* For XR-2212P and XR-2212N, the parameters, although guaranteed over the recommended operating coniditions, are not 100% tested In production

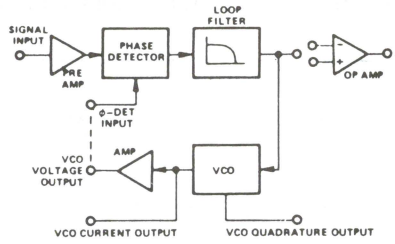


Figure 1. Functional Block Diagram of XR-2212 Precision PLL System

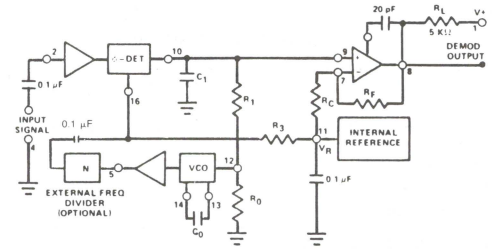


Figure 2. Generalized Circuit Connection for FM Detection, Signal Tracking or Frequency Synthesis

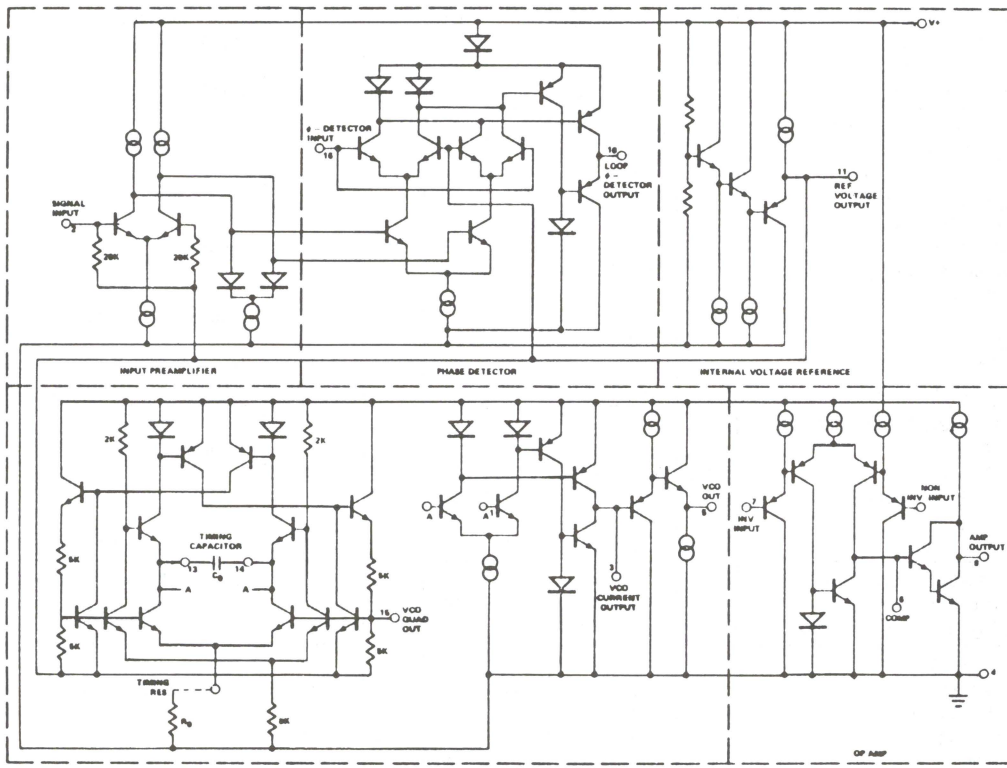


Figure 3. Simplified Circuit Schematic of XR-2212

TYPICAL CHARACTERISTICS

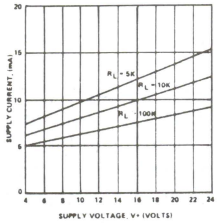


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

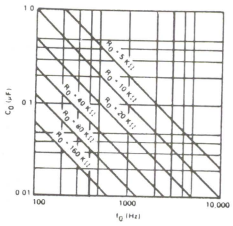


Figure 5. VCO Frequency vs Timing Resistor

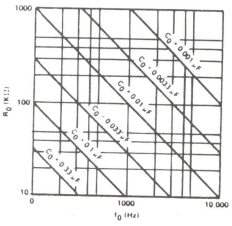


Figure 6. VCO Frequency vs Timing Capacitor

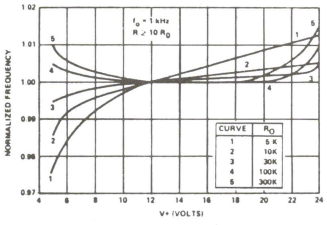


Figure 7. Typical f_0 vs Power Supply Characteristics

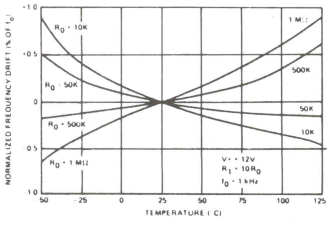


Figure 8. Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV to 5V peak-to-peak. If desired , the input can be de-sensitized by adding R_X to pin 2 to V_{EE} (pin 4). The formula is V_{IN} =

$$V+ \left[\frac{10K}{R_X + 20K}\right] \pm 2.8mV$$

VCO Current Output (Pin 3): This is a high impedance (MΩ) current output terminal which can provide ±100μA drive capability with a voltage swing equal to V+. This output can directly interface with CMOS or NMOS logic families.

VCO Voltage Output (Pin 5): This terminal provides a low- impedance (≈ 50Ω) buffered output for the VCO. It can directly interface with low-power Schottley TTL. For interfacing with standard TTL circuits, a 750Ω pull-down resistor from pin 5 to ground is required. For operation of the PLL without an external divider, pin 5 can be dc coupled to pin 16.

Op Amp Compensation (Pin 6): The op amp section is frequency compensated by connecting an external capacitor from pin 6 to the amplifier output (pin 8). For unity-gain compensation a 20pF capacitor is recommended.

Op Amp Inputs (Pins 7 and 9): These are the inverting and the non-inverting inputs for the op amp section. The common-mode range of the op amp inputs is from +1V to (V+ – 1.5) volts.

Op Amp Output (Pin 8): The op amp output is an open- collector type gain stage and requires a pull-up resistor, R_L, to V+ for proper operation. For most applications, the recommended value of R_L is in 5kΩ to 10kΩ range.

Phase Detector Output (Pin 10): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 10 (see Figure 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 10 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

Reference Voltage, V_R (Pin 11): This pin is internally biased at the reference voltage level. V_R:V_R = V+/2 – 650mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 10, 12 and 16. Pin 1 must be bypassed to ground with a 0.1µF capacitor, for proper operation of the circuit.

VCO Control Input (Pin 12): VCO free-running frequencies determined by external timing resistor, R_0, connected from this terminal to ground. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ (see Figure 8).

VCO Frequency Adjustment: VCO can be fine-tuned by connecting á potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 10).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200pF to 10µF.

VCO Quadrature Output (Pin 15): The low-level (≈ 0.6 V_{pp}) output at this pin is at quadrature phase (i.e. 90° phase-offset) with the other VCO outputs at pins 3 and 5. The dc level at pin 15 is approximately 300mV above V_R. The quadrature output can be used with an external multiplier as a "lock detect" circuit. In order not to degrade oscillator performance, the output at pin 15 must be buffered with an external high-impedance low-capacitance amplifier. When not in use, pin 15 should be left open-circuited.

Phase Detector Input (Pin 16): Voltage output of the VCO (pin 5) or the output of an external frequency divider is connected to this pin. The dc level of the sensing threshold for the phase detector is referenced to V_R. If the signal is capacitively coupled to pin 16, then this pin must be biased from pin 11, through an external resistor, R_B (R_B ≈ 10KΩ). The peak voltage swing applied to pin 16 *must not* exceed (V+ – 1.5) volts.

PHASE-LOCKED LOOP PARAMETERS

Transfer Characteristics:

Figure 9 shows the basic frequency to voltage characteristics of XR-2212. With no input signal present, filtered phase detector output voltage is approximately equal to the internal reference voltage, V_R, at pin 11. The PLL can track an input signal over its tracking bandwidth, shown in the figure. The frequencies f_{TL} and f_{TH} represent the lower and the upper edge of the tracking range, f_0 represents the VCO center frequency.

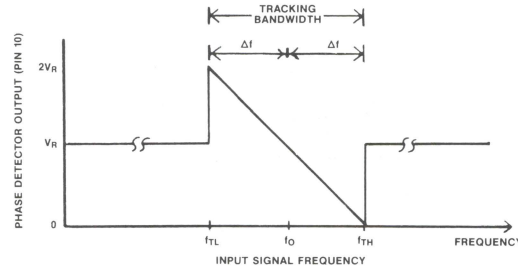


Figure 9. Phase Detector Output Voltage (Pin 10) as a Function of Input Signal Frequency.

Note: Output Voltage is Referenced to Internal Reference Voltage V_R at Pin 11

Design Equations:

(See Figure 2 and Figure 9 for definition of components.)

1. VCO Center Frequency, f_0: $f_0 = 1/R_0C_0$ Hz
2. Internal Reference Voltage, V_R (measured at Pin 11) V_R = V+/2 – 650mV
3. Loop Low-Pass Filter Time Constant, τ: $\tau = R_1C_1$
4. Loop Damping, ζ: $\zeta = 0.25\sqrt{\frac{NC_0}{C_1}}$

   where N is the external frequency divider modular (See 2). If no divider is used, N = 1.
5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$: $\Delta f/f_0 = R_0/R_1$
6. Phase Detector Conversion Gain, Kø: (Kø is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input) Kø = $-2V_R/\pi$ volts/radian

7. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 10. It is the reciprocal of the slope of conversion characteristics shown in Figure 9). $K_0 = -1/V_R C_0 R_1$ Hz/volt

8. Total Loop Gain, K_T.
   $K_T = 2\pi K \varnothing K_0 = 4/C_0 R_1$ rad/sec/volt

9. Peak Phase-Detector Current, I_A; available at pin 10.
   $I_A = V_R$ (volts)/25mA

APPLICATION INFORMATION

FM Demodulation

XR-2212 can be used as a linear FM demodulator for both narrow-band and wide-band FM signals, The generalized circuit connection for this application is shown in Figure 10, where the VCO output (pin 5) is directly connected to the phase detector input (pin 16). The demodulated signal is obtained at phase detector output (pin 10). In the circuit connection of Figure 10, the op amp section of XR-2212 is used as a buffer amplifier to provide both additional voltage amplification as well as current drive capability. Thus, the demodulated output signal available at the op amp output (pin 8) is fully buffered from the rest of the circuit.

In the circuit of Figure 10, R_0C_0 set the VCO center frequency, R_1 sets the tracking bandwidth, C_1 sets the low-pass filter time constant. Op amp feedback resistors R_F and R_C set the voltage gain of the amplifier section.

Design Instructions:

The circuit of Figure 10 can be tailored to any FM demodulation application by a choice of the external components R_0, R_1, R_C, R_F, C_0 and C_1. For a given FM center frequency and frequency deviation, the choice of these components can be calculated as follows, using the design equations and definitions given on page 1-34, 1-35 and 1-36.

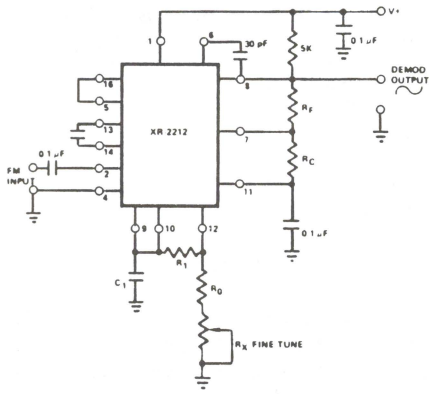


Figure 10. Circuit Connection for FM Demodulation

a) Choose VCO center frequency f_0 to be the same as FM carrier frequency.

b) Choose value of timing resistor R_0, to be in therange of 10KΩ to 100KΩ. This choice is arbitrary. The recommended value is $R_0 \cong$ 20KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$$C_0 = 1/R_0 f_0$$

d) Choose R_1 to determine the tracking bandwidth, if (see design equation 5). The tracking bandwidth, Δf, should be set significantly wider than the maximum input FM signal deviation, Δf_{SM}. Assuming the tracking bandwidth to be "N" times larger than Δf_{SM}, one can re-unite design equation 5 as:

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1} = N \frac{\Delta f_{SM}}{f_0}$$

Table 1 lists recommended values of N, for various values of the maximum deviation of the input FM signal.

% Deviation of FM Signal ($\Delta f_{SM}/f_0$)	Recommended Value of Bandwidth Ratio, N ($N = \Delta f/\Delta f_{SM}$)
1 % or less	10
1 to 3%	5
1 to 5%	4
5 to 10%	3
10 to 30%	2
30 to 50%	1.5

Table 1

Recommended values of bandwidth ratio, N, for various values of FM signal frequency deviation. (Note: N is the ratio of tracking bandwidth Δf to max. signal frequency deviation, Δf_{SM}).

e) Calculate C_1 to set loop damping (see design equation 4). Normally, $\zeta = 1/2$ is recommended. Then, $C_1 = C_0/4$ for $\zeta = 1/2$. Otherwise ζ is calculated by

$$\zeta = \frac{1}{2\sqrt{K_D K_O \cdot 2 \cdot \pi \cdot 1 \times 10^6 \cdot C}} \quad \frac{\text{sec}}{\text{sec}}$$

f) Calculate R_C and R_F to set peak output signal amplitude. Output signal amplitude, V_{OUT}, is given as:

$$V_{OUT} = \left(\frac{\Delta f_{SM}}{f_0}\right)\left(V_R\right)\left(\frac{R_1}{R_0}\right)\left[\frac{R_C + R_F}{R_C}\right]$$

In most applications, $R_F = 100K\Omega$ is recommended; then R_C, can be calculated from the above equation to give desired output swing. The output amplifier can also be used as a unity-gain voltage follower, by open circuiting R_C (i.e., $R_C = \infty$).

Note: All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X, (See Figure 10.)

Design Example:

Demodulator for FM signal with 67kHz carrier frequency with ±5kHz frequency deviation. Supply voltage is +12V and required peak output swing is ±4 volts.

Step a) f_0 is chosen as 67kHz.

Step b) Choose $R_0 = 20K\Omega$ (18KΩ fixed resistor in series with 5KΩ potentiometer).

Step c) Calculate C_0; from design Eq. (1).

$C_0 = 746pF$

Step d) Calculate R_1. For given FM deviation, $\Delta f_{SM}/f_0 = 0.0746$, and N = 3 from Table 1.
Then:
$R_0/R_1 = (3)(0.0746) = 0.224$
or:
$R_1 = 89.3K\Omega$.

Step e) Calculate $C_1 = (C_0/4) = 186pF$.

Step f) Calculate R_C and R_F to get ±4 volts peak output swing: Let $R_F = 100K\Omega$. Then,

$R_C = 80.6K\Omega$.

Note: All values except R_0 can be rounded-off to nearest standard value.

Frequency Synthesis

Figure 11 shows the generalized circuit connection for frequency synthesis, In this application an external frequency divider is connected between the VCO output (pin 5) and the phase-detector input (pin 16). When the circuit is in lock, the two signals going into the phase-detector are at the same frequency, or $f_S = f_1/N$ where N is the modulus of the external frequency divider, Conversely, the VCO output frequency, f_1 is equal to N_{fS}.

In the circuit configuration of Figure 11, the external timing components, R_0 and C_0, set the VCO free-running frequency; R_1 sets the tracking bandwidth and C_1 sets the loop damping, i.e., the low-pass filter time constant (see design equations).

The total tracking range of the PLL (see Figure 9), should be chosen to accommodate the lowest and the highest frequency, f_{max} and f_{min}, to be synthesized. A recommended choice for most applications is to choose a tracking half-bandwidth Δf, such that:

$$\Delta f \approx f_{max} - f_{min}$$

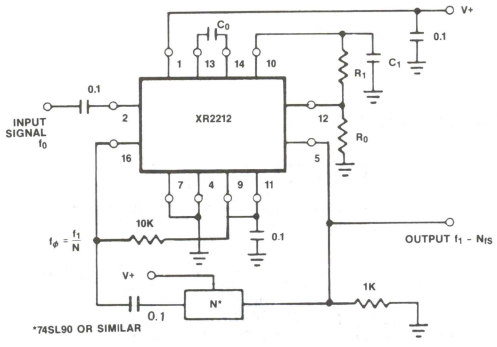


Figure 11. Circuit Connection for Frequency Synthesizer

If a fixed output frequency is desired, i.e. N and f_S are fixed, then a ±10% tracking bandwidth is recommended. Excessively large tracking bandwidth may cause the PLL to lock on the harmonics of the input signals; and the small tracking range increases the "lock- up" or acquisition time.

If a variable input frequency and a variable counter modulus N is used, then the maximum and the minimum values of output frequency wiil be:

$$f_{max} = N_{max} (f_S)_{max} \text{ and } f_{min} = N_{min} (f_S)_{min}$$

Design Instructions:

For a given performance requirement, the circuit of Figure 11 can be optimized as follows:

a) Choose center frequency, f_0, to be equal to the output frequency to be synthesized. If a range of output frequencies is desired, set f_0 to be at mid-point of the desired range,

b) Choose timing resistor R_0 to be in the range of 15KΩ to 100KΩ. This choice is arbitrary. R_0 can be fine tuned with a series potentiometer, R_X.

c) Choose timing capacitor, C_0 from Figure 6 or Equation 1.

d) Calculate R_1 to set tracking bandwidth (see Figure 9, and design equation 5). If a range of output frequencies are desired, set R_1 to get:

$$\Delta f = f_{max} - f_{min}$$

It a single fixed output frequency is desired, set R_1 to get:

$$\Delta f = 0.1\ f_0$$

e) Calculate C_1 to obtain desired loop damping. (See design equation 4). For most applications, $\zeta = 1/2$ is recommended, thus:

$$C_1 = NC_0/4$$

Note: All component values except R_0 can be rounded- off to nearest standard value.

Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01Hz to 500kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enables the system to distinguish between the presence or absence of an input signal at the center frequency.

FEATURES

Bandwidth adjustable from 0 to 14%
Logic compatible output with 100mA current sinking capability
High stable center frequency
Center frequency adjustable from 0.01Hz to 500kHz
Inherent immunity to false signals
High rejection of out-of-band signals and noise
Frequency range adjustable over 20:1 range by external resistor

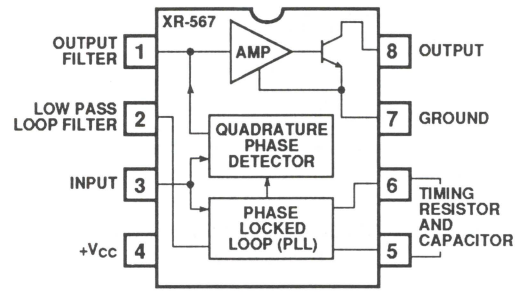
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385mW
Plastic Package	300mW
SO-8	220mW
Derate Above + 25°C	2.5 mW/°C
Temperature	
Storage	65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567M	Ceramic	–55°C to + 125°C
XR-567CN	Ceramic	0°C to + 70°C
XR-567CP	Plastic	0°C to + 70°C
XR-567MD	Japanese SOIC	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-567 monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100mA.

The input signal is applied to Pin 3 (20kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

In applications requiring two or more 567-type devices, consider the XR-2567 dual tone decoder. Where center frequency accuracy and drift are critical, compare the XR-567A. Investigate employing the XR-L567 in low power circuits.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test circuit of Figure 2.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		9.0	V dc	
Supply Current					
Quiescent XR-567M		6	8	mA	R_L = 20kΩ
XR-567C		7	10	mA	R_L = 20kΩ
Activated XR-567M		11	13	mA	R_L = 20kΩ
XR-567C		12	15	mA	R_L = 20kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 9
0°C < T_T < 70°C *		1 60		ppm/°C	See Figure 9
−55 < T_T < +125°C *		1140		ppm/°C	See Figure 9
Supply Voltage					
XR-567M		0.5	1.0	%/V	f_o = 100kHz
XR-567C		0.7	2.0	%/V	f_o = 100kHz
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567M	12	14	16	% of f_o	f_o = 100kHz
XR-567C	10	14	18	% of f_o	f_o = 100kHz
Largest Detection Bandwidth Skew					
XR-567M		1	2	% of f_o	
XR-567C		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		10.1		%/°C	V_{IN} = 300mV rms
Supply Voltage		12		%/V	V_{IN} = 300mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L = 30mA, V_{in} = 25mV rms
		0.6	1.0	V	I_L = 100mA, V_{in} = 25mV rms
Output Leakage Current		0.01	25	µA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

DEFINITION OF XR-567 PARAMETERS

Center Frequency f_0

f_o is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground f_o can be approximated by

$$f_0 \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

Detection Bandwidth (BW)

The detection bandwidth is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The band-width of the filter, as a percent of f_o, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_0 C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

Largest Detection Bandwidth

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

Detection Band Skew

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2 f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls).

DESCRIPTION OF CIRCUIT CONTROLS

Output Filter — C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass *post detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3 C_3$, where R_3 (4.7kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be ≥ 2 C_2. where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the tum-on or tum-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector (see Functional Block Diagram) may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

Loop Filter — C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-567. The filter time constant is given by $T_2 = R_2 C_2$, where R_2 (10kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 6. For additional information see section on "Definition of XR-567 Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20mV/% frequency deviation.

Input (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20kΩ.

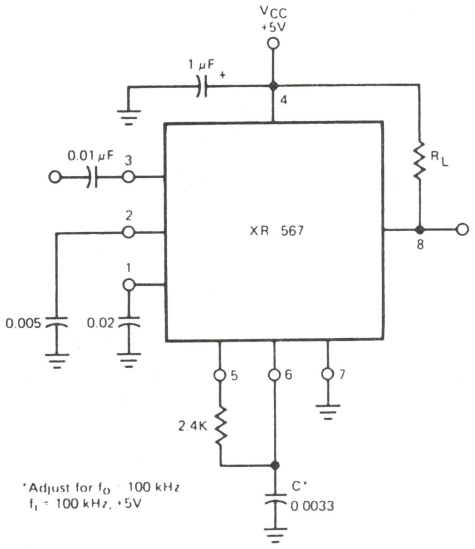


Figure 2. XR-567 Test Circuit

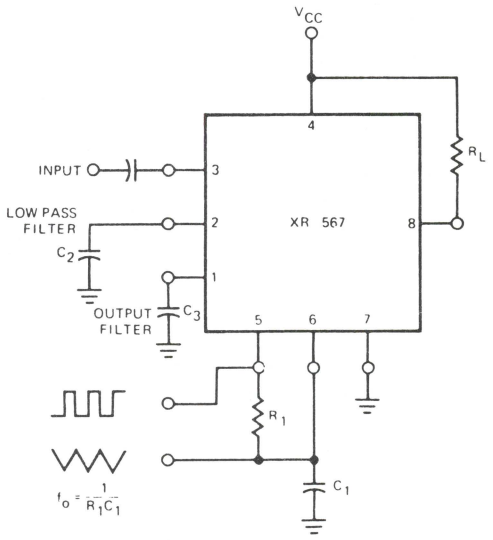


Figure 3. XR-567 Connection Diagram

Timing Resistor R_1 and Capacitor C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately $V_{CC} - 1.4V$ and an average dc level of $V_{CC}/2$. A 1kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

Logic Output (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤ 20 volts.

OPERATING INSTRUCTIONS

Selection of External Components

A typical connection diagram for the XR-567 is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that $2k\Omega \leq R_1 \leq 20k\Omega$, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

TYPICAL CHARACTERISTIC CURVES

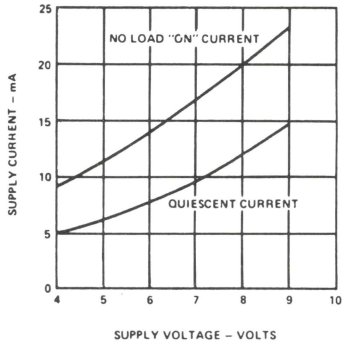


Figure 4. Supply Current vs Supply Voltage

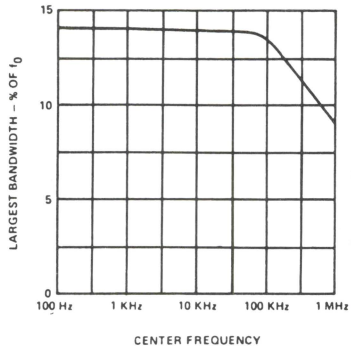


Figure 5. Largest Detection Bandwidth vs Operating Frequency

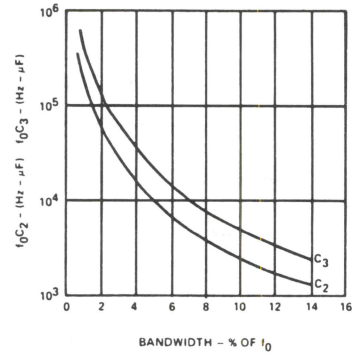


Figure 6. Detection Bandwidth as a Function of C_2 and C_3

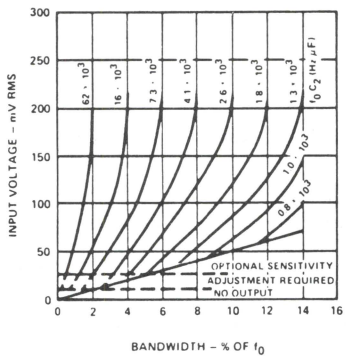


Figure 7. Bandwidth vs Input Signal Amplitude (C_2 in μF)

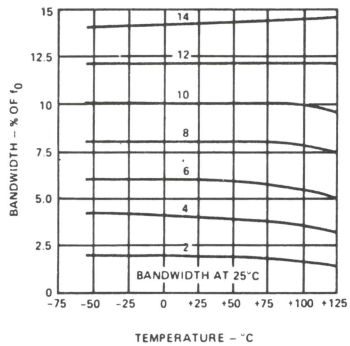


Figure 8. Bandwidth Variation with Temperature

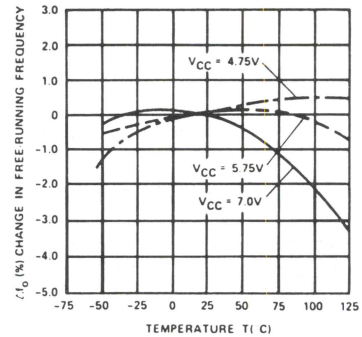


Figure 9. Frequency Drift with Temperature

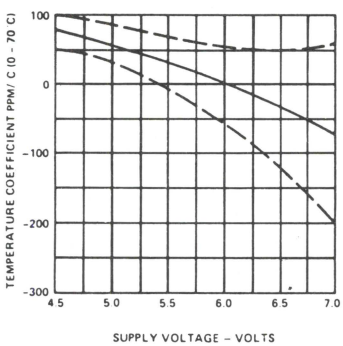


Figure 10. Temperature Coefficient of Center Frequency (Mean and S.D.)

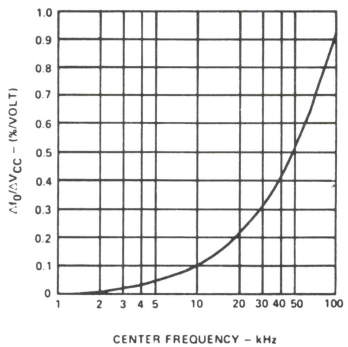


Figure 11. Power Supply Dependence of Center Frequency

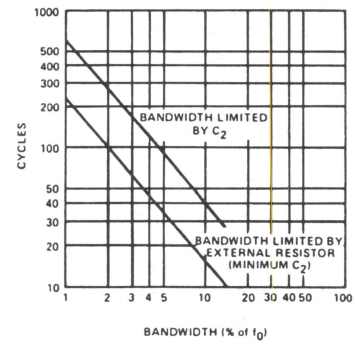
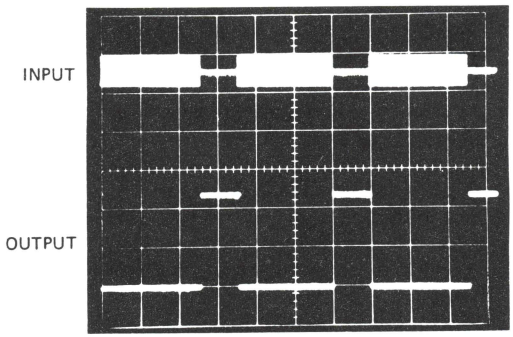
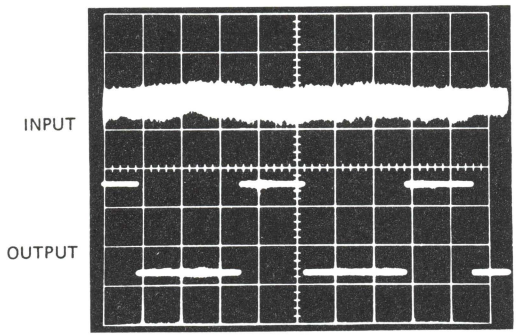


Figure 12. Greatest Number of Cycles Before Output



Response to 100 mV rms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = - 6 dB R_L = 100 ohms

Noise Bandwidth = 140 Hz

Figure 13. Typical Response

2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires V_i > 200mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.

3. Capacitor C_3 sets the end edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value of C_3 is 2 C_2.

   Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The XR-567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3.

OPTIONAL CONTROLS

Programming

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

Speed of Response

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}, C_3 = \frac{260}{f_o} \ \mu F$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 14 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

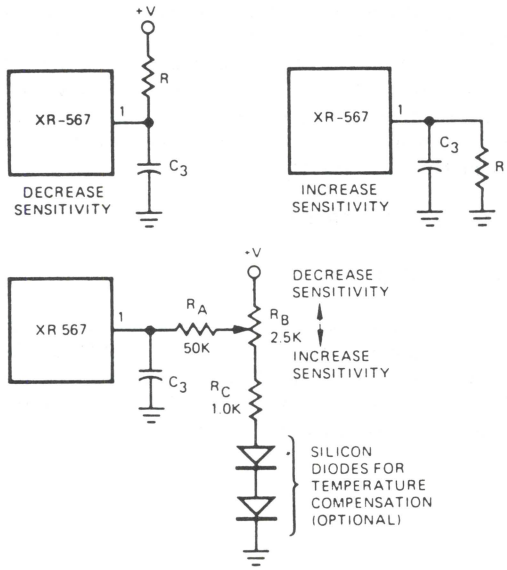


Figure 14. Optional Sensitivity Connections

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 15. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

Skew Adjustment

The circuits shown in Figure 16 can be used to change the position of the detection band (capture range) within the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

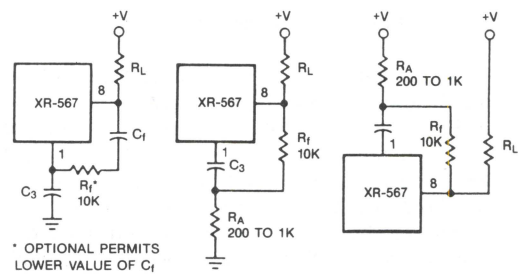


Figure 15. Methods of Reducing Chatter

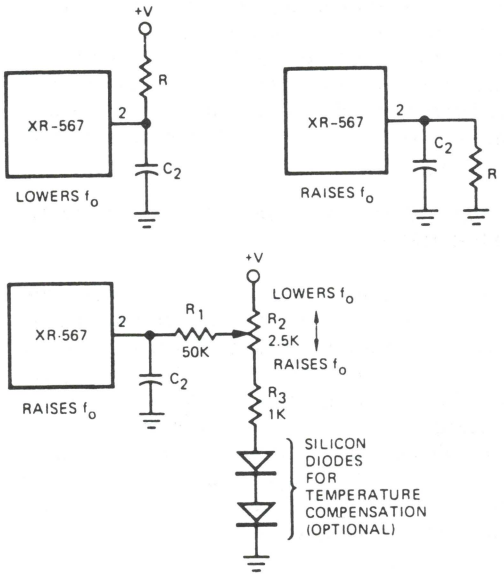


Figure 16. Connections to Reposition Detection Band

Output Latching

In order to latch the output of the XR-567 "on" after a signal is received, it is necessary to include a feedback resistor around the output stage, between pin 8 and pin 1, as shown in Figure 17. Pin 1 is pulled up to unlatch the output stage.

Bandwidth Reduction

The bandwidth of the XR-567 can be reduced by either increasing capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 18 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. The reduced impedance level at pin 2 will require a larger value of C_2 for a given cutoff frequency.

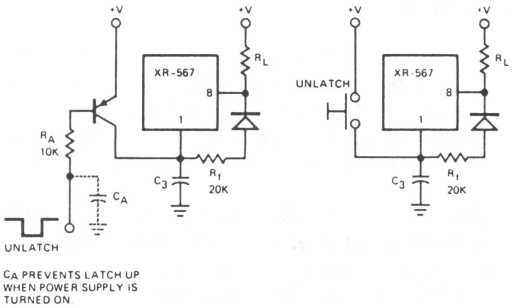
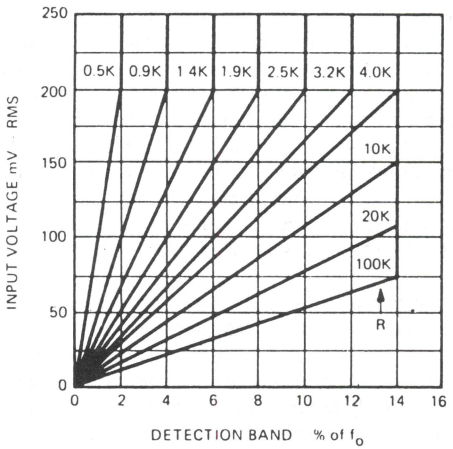


Figure 17. Output Latching



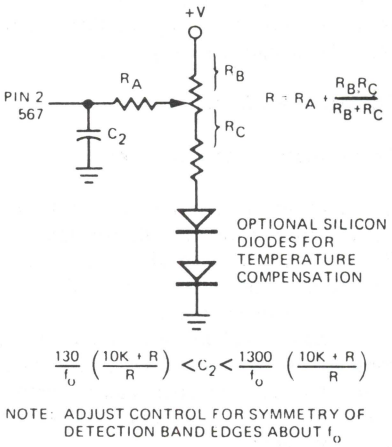


Figure 18. Bandwidth Reduction

Precautions

1. The XR-567 will lock on signals near (2n + 1) f_o and produce an output for signals near (4n + 1) f_o, for n = 0,1,2 - etc. Signals at 5 f_o and 9 f_o can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-567 in a reduced bandwidth mode of operation at input levels less than 200mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 12.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-567 in the high input level mode, above 200mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

ADDITIONAL APPLICATIONS

Dual Time Constant Tone Decoder

For some applications it is important to have a tone decoder with narrow bandwidth and fast response time. This can be accomplished by the dual time constant tone decoder circuit shown in Figure 19. The circuit has two low-pass loop filter capacitors, C_2 and C'_2. With no input signal present, the output at pin 8 is high, transistor Q_1 is off, and C'_2 is switched out of the circuit. Thus the loop low-pass filter is comprised Of C_2, which can be kept as small as possible for minimum response time.

When an in-band signal is detected, the output at pin 8 will go low, Q_1 will turn on, and capacitor C'_2 will be switched in parallel with capacitor C_2. The low-pass filter capacitance will then be $C_2 + C'_2$. The value Of C'_2 can be quite large in order to achieve narrow band-width. Notice that during the time that no input signal is being received, the bandwidth is determined by capacitor C_2.

NARROW BAND FM DEMODULATOR WITH CARRIER DETECT

For FM demodulation applications where the bandwidth is less than 10% of the carrier frequency, an XR-567 can be used to detect the presence of the carrier signal. The output of the XR-567 is used to turn off the FM demodulator when no carrier is present, thus acting as a squelch. In the circuit shown, an XR-215 FM demodulator is used because of its wide dynamic range, high signal/noise ratio and low distortion. The XR-567 will detect the presence of a carrier at frequencies up to 500kHz.

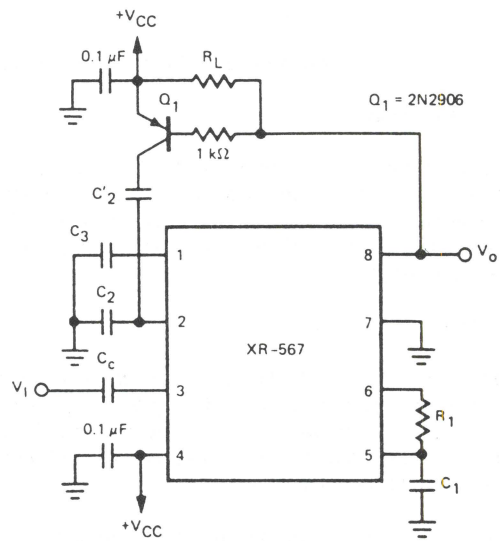


Figure 19. Dual Time Constant Tone Decoder

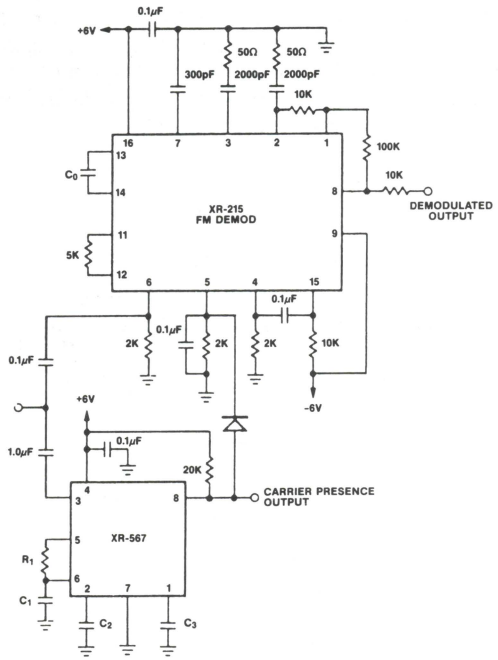


Figure 20. Narrow Band FM Demodulator with Carrier Detect

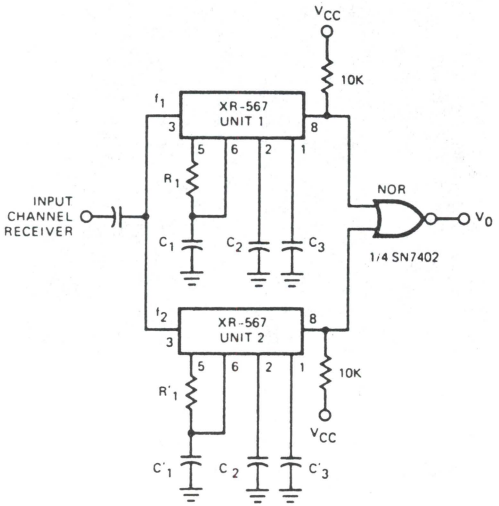


Figure 21. Dual Tone Decoder

Dual Tone Decoder

In dual tone communication systems, information is transmitted by the simultaneous presence of two separate tones at the input. In such applications two XR-567 units can be connected in parallel, as shown in Figure 21 to form a dual tone decoder. The resistor and capacitor values of each decoder are selected to provide the desired center frequencies and bandwidth requirements. Due to capacitor and device variation, it is not possible to use a fixed R_1 value in production applications.

Precision Oscillator

The current-controlled oscillator (CCO) section of the XR-567 provides two basic output waveforms as shown in Figure 22. The squarewave is obtained from pin 5, and the exponential ramp from pin 6. The relative phase relationships of the waveforms are also provided in the figure. In addition to being used as a general purpose oscillator or clock generator, the CCO can also be used for any of the following special purpose oscillator applications:

1. **High-Current Oscillator**

   The oscillator output of the XR-567 can be amplified using the output amplifier and high-current logic output available at pin 8.. In this manner, the circuit can switch 100mA load currents without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 23. The oscillator frequency can be modulated over ±6% in frequency by applying a control voltage to pin 2.

2. **Oscillator with Quadrature Outputs**

   Using the circuit connection of Figure 24 the XR-567 can function as a precision oscillator with two separate squarewave outputs (at pins 5 and 8, respectively) that are at nearly quadrature phase with each other. Due to the internal biasing arrangement the actual phase shift between the two outputs is typically 80°.

3. **Oscillator with Frequency Doubled Output**

   The CCO frequency can be doubled by applying a portion of the squarewave output at pin 5 back to the input at pin 3, as shown in Figure 25. In this manner, the quadrature detector functions as a frequency doubler and produces an output of 2 f_o at pin 8.

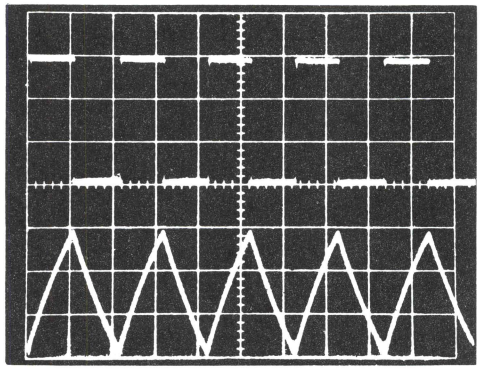


Figure 22. Oscillator Output Waveform Available from CCO Section
Top: Square Wave Output at Pin 5:
Amplitude = (V+ – 1.4V), pp.,
Avg. Value = V+ /2
Bottom: Exponential Triangle Wave at Pin 6:
Amplitude = 1V pp., Avg. Value = V+ /2

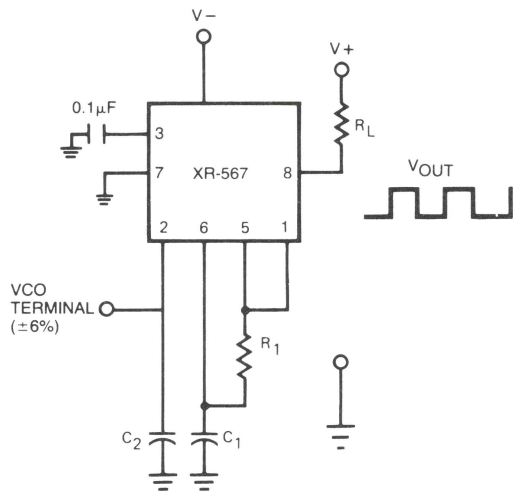


Figure 23. Precision Oscillator to Switch 100mA Loads

FSK Decoding

XR-567 can be used as a low speed FSK demodulator. In this application the center frequency is set to one of the input frequencies, and the bandwidth is adjusted to leave the second frequency outside the detection band. When the input signal is frequency keyed between the in-band signal and the out-band signal, the logic state of the output at pin 8 is reversed. Figure 26 shows the FSK input (f_2 = 3 f_1) and the demodulated output signals, with f_o = f_2 = 1kHz. The circuit can handle data rates up to f_o/10 baud.

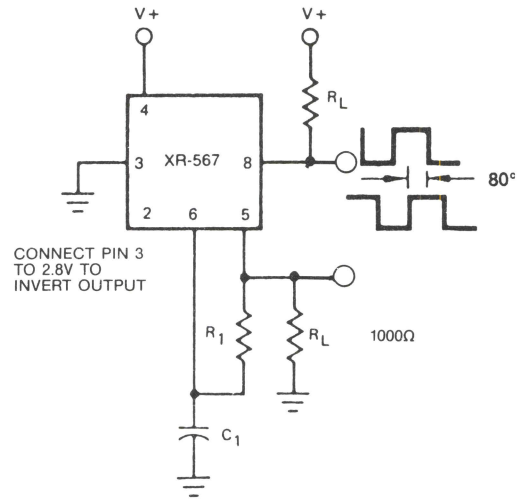


Figure 24. Oscillator with Quadrature Output

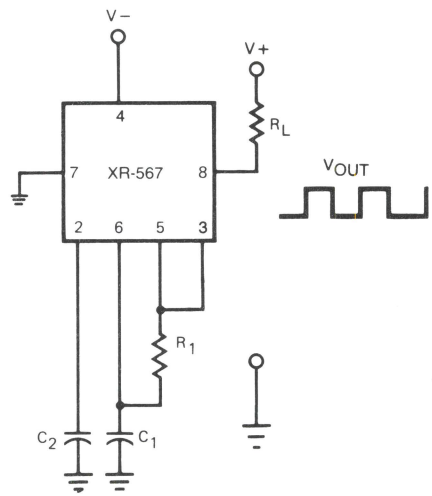


Figure 25. Oscillator with Double Frequency Output

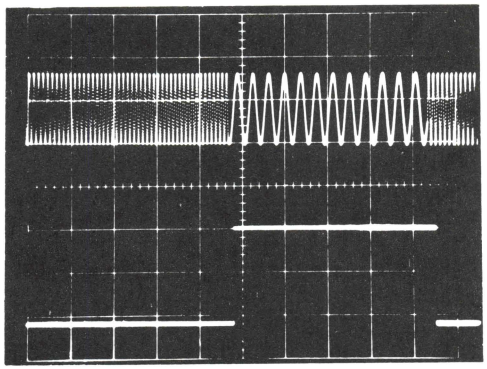
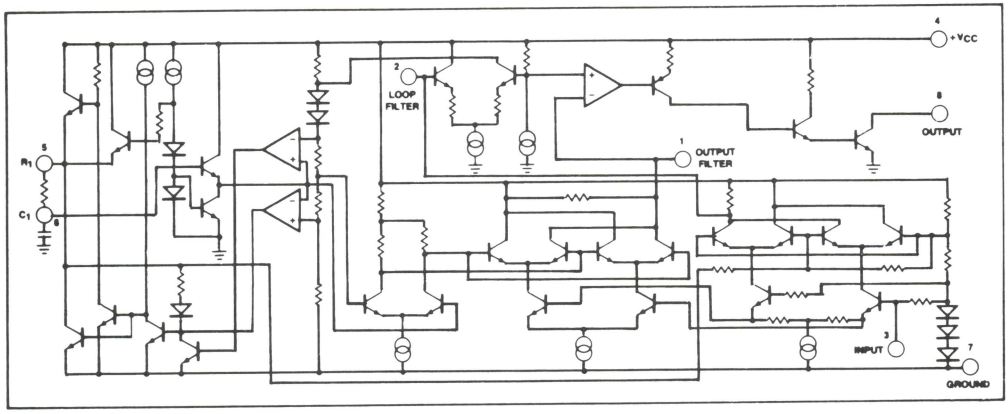


Figure 26. Input and Output Waveforms for FSK Decoding
Top: Input FSK Signal ($f_2 = 3f_1$)
Bottom: Demodulated Output

EQUIVALENT SCHEMATIC DIAGRAM



Precision Tone Decoder

GENERAL DESCRIPTION

The XR-567A provides all the necessary circuitry for constructing a variety of tone detectors and frequency decoders. Phase-locked loop circuit techniques are used to provide operation from 0.01Hz to 500kHz. The circuit also features an input preamp, a high-current logic output, and programmable output delay.

The XR-567A, available in an 8-Pin DIL package, is designed to offer improved frequency accuracy and drift characteristics over the standard industry 567. These changes offer improved overall circuit performance, while reducing initial circuit adjustments.

FEATURES

Programmable Detection Bandwidth	0% to 14%
Logic Output	100mA
Wide Center Frequency Range	0.01Hz to 500kHz

High Rejection of Out-of-Band Signals and Noise
Pin for Pin Replacement for Standard 567
Inherent immunity to Out-of-Band Signals & Noise

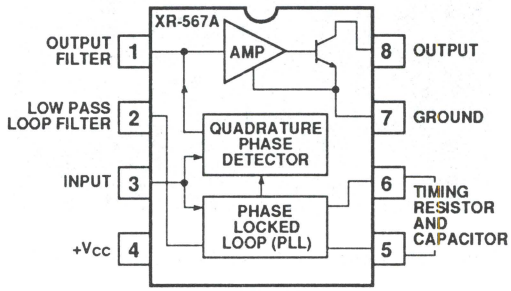
APPLICATIONS

Tone Detection
Touch-Tone® Decoding
Communications Paging
Ultrasonic Remote Control
Precision Oscillator
Wireless Intercom
Carrier-Tone Transceiver
FSK Demodulation
Dual Time Constant Tone Detector

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation	
Ceramic Package	385mW
Plastic Package	300mW
Derate above 25°C	2.5 mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567AM	Ceramic	–55°C to +125°C
XR-567ACN	Ceramic	0°C to +70°C
XR-567ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-567A is an improved version of the popular 567 tone decoder. Center frequency accuracy is guaranteed by design modifications and testing to 5%, and is typically better than 2%. Temperature drift of the center frequency is also improved. Thus, in most applications, no trimming is required.

The XR-567A monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output capable of sinking 100mA.

The input signal is applied to Pin 3 (20kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Band- width is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in band signal triggers the device.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		9.0	Vdc	
Supply Current					
Quiescent XR-567AM		6	8	mA	R_L = 20kΩ
Quiescent XR-567AC		7	10	mA	R_L = 20kΩ
Activated XR-567AM		11	13	mA	R_L = 20kΩ
Activated XR-567AC		12	15	mA	R_L = 20kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	
0°C < T_T < 70°C		±60		ppm/°C	not tested in production
−55°C < T_T < +125°C		±120		ppm/°C	
Supply Voltage					
XR-567AM		0.5	1.0	%/V	f_o = 100kHz
XR-567AC		0.7	2.0	%/V	f_o = 100kHz
Initial Accuracy		±2.0	±5.0	%	f_o = 80kHz
Center Frequency		1.06			nominal multiple of f_0 from $f = \frac{1}{RC}$ is recommended
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567AM	12	14	16	% of f_o	f_o = 100kHz, V_{IN} = 300μV rms
XR-567AC	10	14	18	% of f_o	f_o = 100kHz, V_{IN} = 300μV rms
Largest Detection Bandwidth Skew					
XR-567AM		1	2	% of f_o	
XR-567AC		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{IN} = 300mV rms
Supply Voltage		±1	±2	%/V	V_{IN} = 300mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L = 30mA, V_{IN} = 25mV rms
		0.6	1.0	V	I_L = 100mA, V_{IN} = 25mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON/OFF Cycling Rate		$f_o/20$			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

Note: Center Frequency Calculation differs from standard XR-567 devices as indicated.

Micropower Tone Decoder

GENERAL DESCRIPTION

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the XR-L567 can replace the popular 567-type decoder with only minor component value changes. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4mW at 5 volts. It operates over a wide frequency band of 0.01Hz to 60kHz and contains a logic compatible output which can sink up to 10 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

FEATURES

Very Low Power Dissipation (≈4mW at 5V).
Bandwidth Adjustable from 0 to 14%.
Logic Compatible Output with 10 mA Current Sinking Capability.
Highly Stable Center Frequency.
Center Frequency Adjustable from 0.01Hz to 60kHz.
Inherent Immunity to False Signals.
High Rejection of Out-of-Band Signals and Noise.
Frequency Range Adjustable Over 20:1 Range by External Resistor.

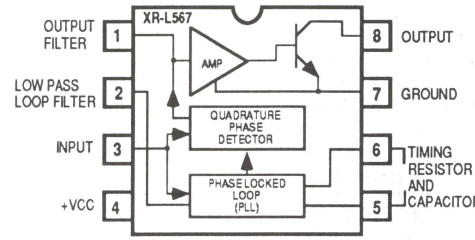
APPLICATIONS

Battery-Operated Tone Detection
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385mW
Plastic Package	300mW
Derate Above +25°C	2.5mW/°C
SO-8	220mW
Storage Temperature	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L567M	Ceramic	–55°C to +125°C
XR-L567CN	Ceramic	0°C to +70°C
XR-L567CP	Plastic	0°C to +70°C
XR-L567MD	Japanese SOIC	0°C to +70°C

SYSTEM DESCRIPTION

The XR-L567 monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependant upon the circuitry here. Pin 4 is + V_{CC} (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

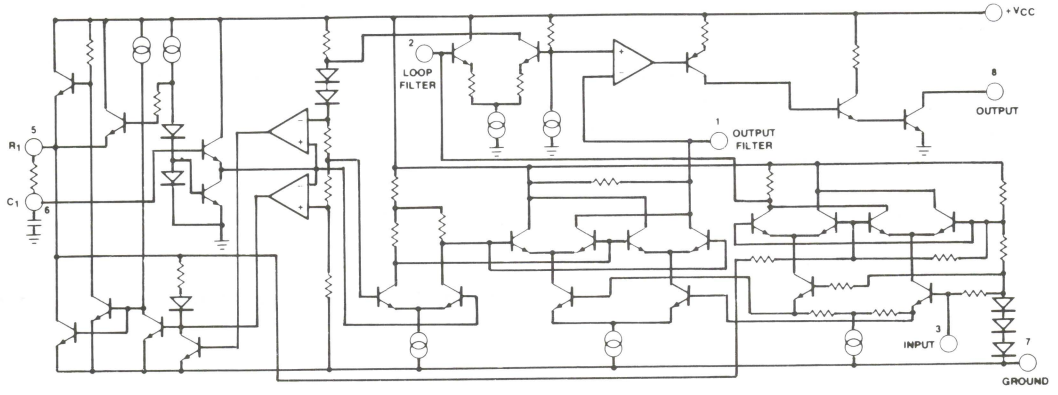
The XR-L567 is pin-for-pin compatible with the standard XR-567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test Circuit of Figure 1.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		8.0	V	
Supply Current					
Quiescent		0.6	1.0	mA	R_L = 20kΩ
Activated		0.8	1.4	mA	R_L = 20kΩ
CENTER FREQUENCY					
Highest Center Frequency	10	60		kHz	
Center Frequency Drift					
Temperature T_A = 25°C		–35		ppm/°C	See Figures 10 and 11
0 < T_A < 70°C		–150		ppm/°C	See Figures 10 and 11
Supply Voltage		0.5	3.0	%/V	f_o = 10kHz, V_{CC} = 5.25 ± 0.5V
DETECTION BANDWIDTH					
Largest Detection Bandwidth	10	14	18	% of f_o	f_o = 10kHz
Largest Detection Bandwidth Skew		2	3	% of f_o	See Figure 13 for Definition
Largest Detection Bandwidth Variation					
Temperature		0.1		%/°C	V_{IN} = 300mV rms
Supply Voltage		2		%/V	V_{IN} = 300mV rms
INPUTS					
Input Resistance		100		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 10mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		mV rms	I_L = 10mA, $f_i = f_o$
Greatest Simultaneous Outband Signal					
to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		–6		dB	B_n= 140kHz
OUTPUTS					
Output Saturation Voltage		0.2	0.4	V	I_L = 2mA, V_{IN} = 25mV rms
		0.3	0.6	V	I_L = 10mA, V_{IN} = 25mV rms
Output Leakage Current		0.01	25	µA	
Fastest On/Off Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 1kΩ
Output Fall Time		30		ns	R_L = 1kΩ

EQUIVALENT SCHEMATIC DIAGRAM



PRINCIPLES OF OPERATION

The XR-L567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature am detector, a voltage comparator, and an output logic driver.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic output at Pin 8 is an "open-collector" NPN transistor stage capable of switching 10mA current loads.

The logic output at Pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at Pin 8 goes to a "low" state.

Figure 3 shows the typical output response of the circuit for a tone-burst applied to the input, within the detection band.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to Pins 5 and 6, as shown in Figure 2. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2 (see Figure 10); and the output response speed is controlled by the output filter capacitor, C_3.

DEFINITION OF DEVICE PARAMETERS

Center Frequency f_o

f_o is the free-running frequency of the current- controlled oscillator with no input signal. It is determined by resistor R1 between Pins 5 and 6, and capacitor C_1 from Pin 6 to ground. f_o can be approximated by

$$f_0 \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

Detection Bandwidth (BW)

The largest detection bandwidth is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass loop filter at Pin 2. Typical dependence of detection bandwidth on the filter capacitance and the input signal amplitude is shown in Figures 10 and 11, or may be calculated by the approximation

$$BW(\%) \approx 338 \sqrt{\frac{V_i\,(RMS)}{f_o(Hz) \cdot C_2(\mu F)}}$$

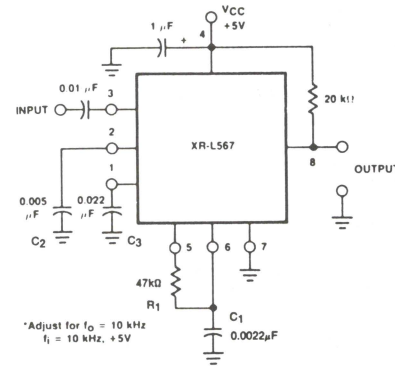


Figure 1. XR-L567 Test Circuit

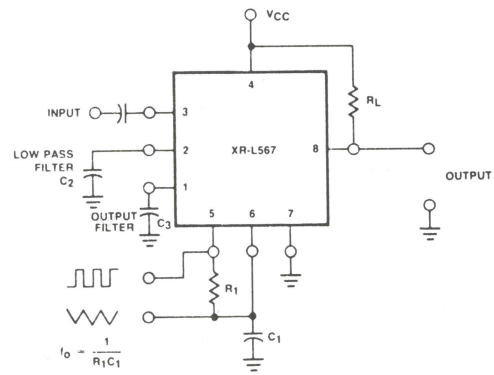


Figure 2. XR-L567 Generalized Connection Diagram

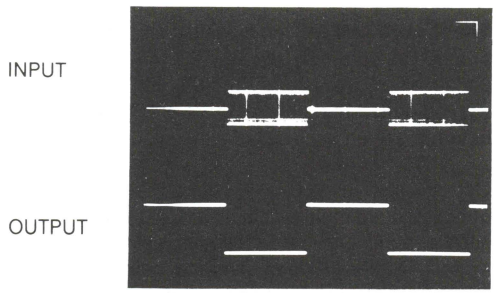
Largest Detection Bandwidth

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero stage at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

Detection Band Skew

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_o. This parameter is graphically illustrated in Figure 4. In the figure, f_{min} and f_{max} correspond to the lower and the upper ends of the largest detection band, and f_1 corresponds to the apparent center of the detection band, and is defined as the arithmetic average of f_{min} and f_{max} and f_o is the free- running frequency of the XR-L567 oscillator section. The bandwidth skew, Δf_x, is the difference between these frequencies. Normalized to f_o, this bandwidth skew can be expressed as:

$$\text{Bandwidth Skew} = \frac{\Delta f_x}{f_o} = \frac{(f_{max} + f_{min} - 2f_o)}{2f_o}$$



Response to 100mV rms tone burst.
R_L = 1KΩ

Figure 3. Typical Output Response to 100 mV Input Tone-Burst

If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

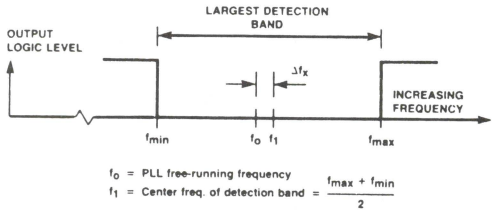


Figure 4. Definition of Bandwidth Skew

DESCRIPTION OF CIRCUIT CONTROLS

Input (Pin 3)

The input signal is applied to Pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 100kΩ.

Timing Resistor R_1 and Capacitor C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between Pins 5 and 6, and capacitor C_1 from Pin 6 to ground, as shown in Figure 2.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 5kΩ load may be driven from this point. The voltage at Pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of ≈ $(V_{CC} - 1.3)/3.5$ volts and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

Loop Filter — C_2 (Pin 2)

Capacitor C_2 connected from Pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-L567. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (100kΩ) is the impedance at Pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 10. For additional information see section on "Definition of Device Parameters."

The voltage at Pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 f_o to 1.05 f_o, with a slope of approximately 20mV/% frequency deviation.

Output Filter — C_3 (Pin 1)

Capacitor C_3 connected from Pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R3 (47kΩ) is the internal impedance at Pin 1.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output (Pin 8).

The average voltage (during lock) at Pin 1 is a function of the in-band input amplitude in accordance with the given transfer characteristic.

Logic Output (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, open-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from Pin 8 to the positive supply.

When an in-band signal is present the output transistor at Pin 8 saturates with a collector voltage of less than 0.6V at full rated output current of 10mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤ 15 volts.

OPERATING INSTRUCTIONS

Selection of External Components

A typical connection diagram for the XR-L567 is shown in Figure 2. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 20kΩ ≤ R_1 ≤ 200kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 10. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires V_i > 200mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.

3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C_3 is 2 C_2.

   Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

Precautions

1. The XR-L567 will lock on signals near (2n + 1) f_o and produce an output for signals near (4n + 1) f_o, for n = 0,1,2—etc. Signals at 5 f_o and 9 f_o can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-L567 in a reduced bandwidth mode of operation at input levels less than 200mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 13.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-L567 in the high input level mode, above 200mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

OPTIONAL CONTROLS

Programming

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

Speed of Response

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transients becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies where f_o is Hz.

$$C_2 = \frac{13}{f_o}, C_3 = \frac{26}{f_o} \quad \mu F$$

The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud. In situations where minimum turn-off is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 5 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

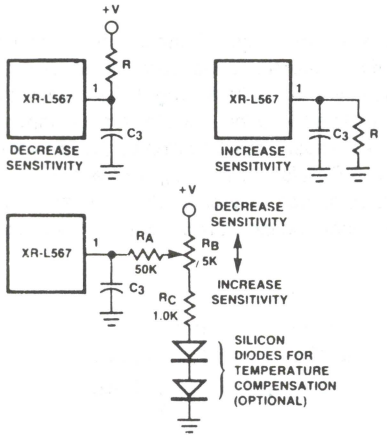


Figure 5. Adjustable Sensitivity Connections

Chatter

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (Pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

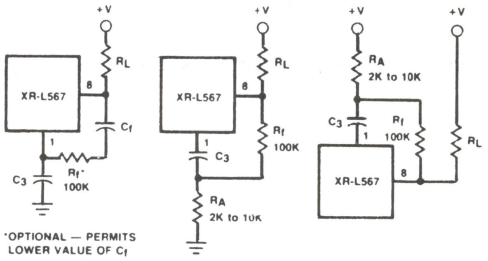


Figure 6. Methods of Reducing Chatter

Skew Adjustment

The circuits shown in Figure 7 can be used to change the position of the detection band (capture range) within the largest detection band (lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

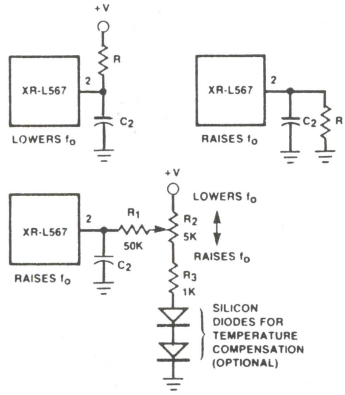


Figure 7. Detection Band Skew Adjustment

CHARACTERISTIC CURVES

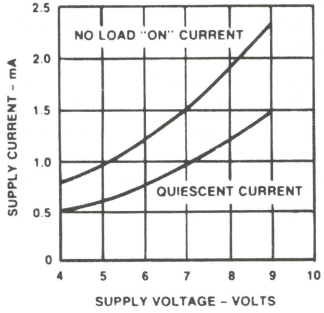


Figure 8. Supply Current Versus Supply Voltage

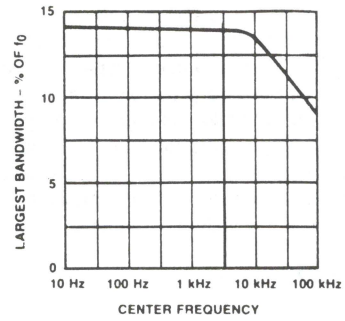


Figure 9. Largest Detection Bandwidth Versus Operating Frequency

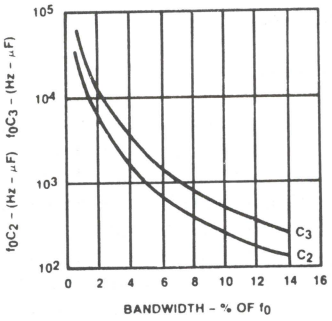


Figure 10. Detection Bandwidth as a Function of C_2 and C_3

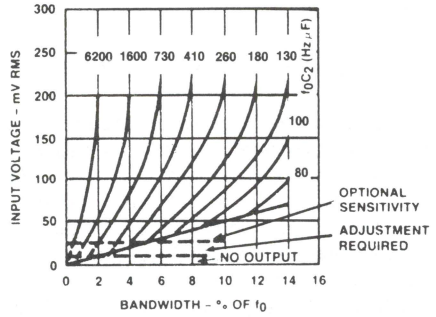


Figure 11. Bandwidth Versus Input Signal Amplitude (C_2 in μF)

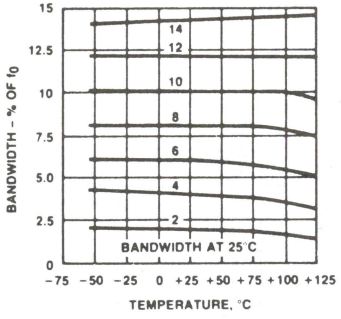


Figure 12. Bandwidth Variation with Temperature

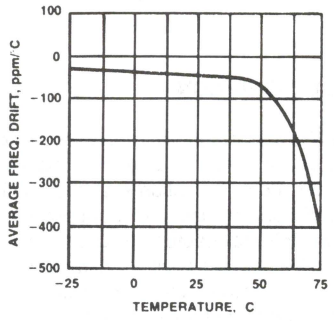


Figure 15. Typical Center Frequency Drift with Temperature (V^+ = 5V, R_1 = 80 kΩ, f_0 = 1kHz)

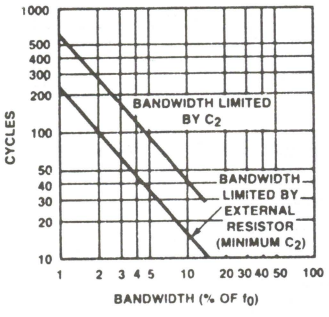


Figure 13. Greatest Number of Cycles Before Output

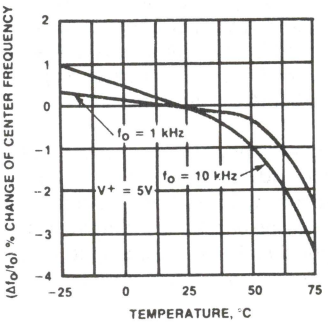


Figure 16. Typical Frequency Drift as a Function of Temperature

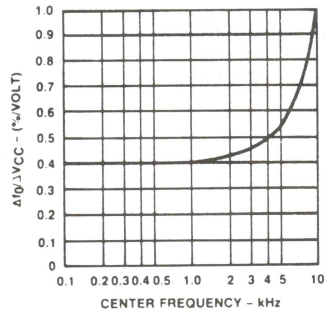


Figure 14. Power Supply Dependence of Center Frequency

Dual Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone decoder packages.

The XR-2567 operates over a frequency range of 0.01Hz to 500kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

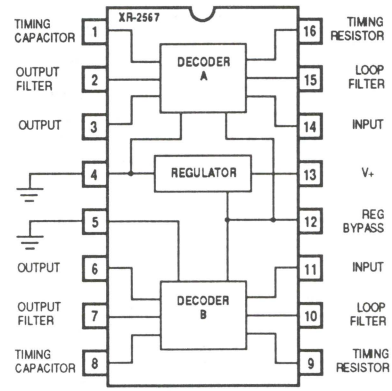
FEATURES

Replaces two 567-type decoders
Excellent temperature tracking between decoders
Bandwidth adjustable from 0 to 14%
Logic compatible outputs with 100mA sink capability
Center frequency matching (1% typ.)
Center frequency adjustable from 0.01Hz to 500kHz
Inherent immunity to false triggering
Frequency range adjustable over 20:1 range by external resistor.

APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Dual-Tone Decoding/Encoding
Communications Paging
Ultrasonic Remote-Control and Monitoring
Full-Duplex Carrier-Tone Transceiver
Wireless Intercom
Dual Precision Oscillator
FSK Generation and Detection

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Power Supply	
with Internal Regulator	14V
without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	
Ceramic Package	750mW
Derate Above +25°C	6mW/°C
Plastic Package	625mW/°C
Derate Above +25°C	5.5mW/°C
Storage Temperature	–65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2567M	Ceramic	–55°C to + 125°C
XR-2567CN	Ceramic	0°C to + 70°C
XR-2567CP	Plastic	0°C to + 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test circuit of Figure 2, S_1 closed unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range					
Without Regulator	4.75		7	V_{dc}	See Figure 5, S_1 closed.
With Internal Regulator	6.5		12	V_{dc}	See Figure 5, S_1 open.
Supply Current (both decoders)					See Figure 7,8
Quiescent XR-2567M		12	16	mA	R_L = 20 kΩ
XR-2567C		14	20	mA	R_L = 20 kΩ
Activated XR-2567M		22	26	mA	R_L = 20 kΩ
XR-2567C		24	30	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY (each decoder section)					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 14
0°C < T_T < 70°C *		±60		ppm/°C	See Figure 14
−55°C < T_T < +125°C*		±140		ppm/°C	See Figure 14
Supply Voltage					
Without Regulator					
XR-2567M		0.5	1.0	%/V	f_o = 100kHz
XR-2567C		0.7	2.0	%/V	f_o = 100kHz
With Internal Regulator					
XR-2567M		0.05		%/V	f_o = 100kHz, V_{CC} = 9V
XR-2567C		0.1		%/V	f_o = 100kHz, V_{CC} = 9V
DETECTION BANDWIDTH (each decoder section)					
Largest Detection Bandwidth					
XR-2567M	12	14	16	% of f_o	f_o = 100kHz
XR-2567C	10	14	18	% of f_o	f_o = 100kHz
Largest Detection Bandwidth Skew					
XR-2567M		1	2	% of f_o	
XR-2567C		1	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		% /°C	V_{IN} = 300mV rms
Supply Voltage		±2		%/V	V_{IN} = 300mV rms
INPUT (each decoder section)					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100mA, f_i = f_o
Greatest Simultaneous Outband					
Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		-6		dB	Noise BW = 140kHz
OUTPUT (each decoder section)					
Output Saturation Voltage		0.2	0.4	V	I_L = 30mA, V_{IN} = 25mV rms
		0.6	1.0	V	I_L = 100mA, V_{IN} = 25mV rms
Output Leakage Current		0.01	25	µA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω
MATCHING CHARACTERISTICS					
Center Frequency Matching		1		%	f_o = 10kHz
Temperature Drift Matching		±20		ppm/°C	0°C < T_A < 70°C
		±50		ppm/°C	−55°C < T_A < 125°C

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

SYSTEM DESCRIPTION

The XR-2567 dual monolithic tone decoder consists of two independant 567-type circuits and an on board voltage regulator. Each decoder has a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. Both devices have normally high open collector outputs capable of sinking 100mA.

The input signal is applied to Pin 14 (device A) or Pin 11 (device B), both with 20kΩ nominal input resistance. Free running frequency is controlled by an RC network at Pins 1 and 16 (device A) or Pins 8 and 9 (device B). A capacitor on Pin 2 (A), or Pin 7 (B) serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 15 (A), or Pin 10 (B); bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 13 is $+V_{CC}$ (4.75 to 12V nominal, 14V maximum); Pin 7 is ground; and Pin 3 (A) or Pin 6 (B) is the open collector output, pulling low when an in-band signal triggers the device.

The internal regulator needs to be bypassed for supply voltages below 7V. This is done by shorting Pin 12 to VCC. Supply voltages to Pin 12 which are over 7V need a bypass capacitor (1nF) to ground (see figure 2).

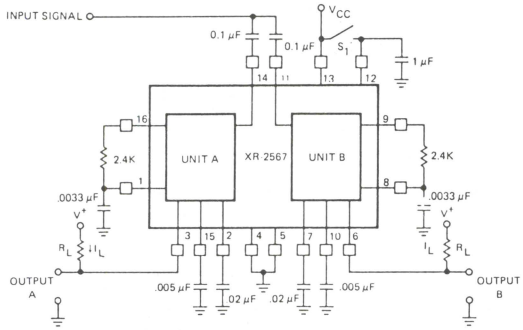
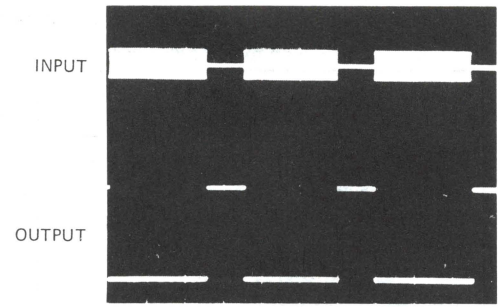


Figure 2. Test Circuit



Response to 100 mV rms tone burst
R_L = 100 ohms.

Figure 3. XR-2567 Typical Response

DEFINITIONS OF XR-2567 PARAMETERS

f_o is the *free-running frequency* of the current-controlled oscillator of the PLL with no input signal. It is determined by resistor R_1 and capacitor C_1; f_o can be approximated by

$$f_0 \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

The detection bandwidth is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20mV rms) will cause a "logic zero" state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_o, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_0 C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance in μF at Pins 10 or 15.

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

DESCRIPTION OF CIRCUIT CONTROLS

Input (Pins 11 and 14)

The input signal is applied to Pins 14 and/or 11 through a coupling capacitor, C_C. These terminals are internally biased at a dc level 2 volts above ground and they have an input impedance level of approximately 20kΩ.

Timing Resistor R_1 and Capacitor C_1 (Pins 1, 8, 9, and 16)

The center frequency, f_o, of each decoder section is set by a resistor R_1 and a capacitor C_1. R_{1A} is connected between Pins 1 and 16 in decoder section A, and R_{1B} between Pins 8 and 9 of decoder section B. C_{1A} is connected from Pin 1 to ground, and C_{1B} from Pin 8 to ground, as shown in Figure 4. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that $2k\Omega \leq R_1 \leq 20k\Omega$, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

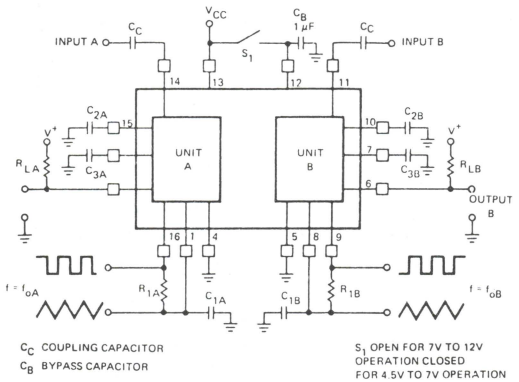


Figure 4. Circuit Connection Diagram

For decoder section A, the oscillator output can be obtained at either Pin 1 or 16. Pin 16 is the oscillator squarewave output which has a magnitude of approximately $V_{CC} - 1.4V$ and an average dc level of $V_{CC}/2$. A 1kΩ load may be driven from this point. The voltage at pin 1 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 1 to avoid disturbing the temperature stability or duty cycle of the oscillator. For section B, Pin 9 is the squarewave output and Pin 8 the exponential triangle waveform output.

Loop Filter, C_2 (Pins 10 and 15)

Capacitors C_{2A} and C_{2B} connected from Pins 15 and 10 to ground are the single-pole, low-pass filters for the PLL portion of decoder sections A and B. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10kΩ) is the impedance at Pins 10 or 15. The selection of C_2 is determined by the detection bandwidth requirements and input signal amplitude as shown in Figures 10 and 12. One approach is to select an area of operation from the graph and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i >$ 200mV rms. Then, as noted in Figure 10, bandwidth will be controlled solely by the f_oC_2 product. (For additional information, see Optional Controls Section, "Speed of Response" and "Bandwidth Reduction".)

Pins 10 and 15 correspond to the PLL phase detector outputs of sections A and B, respectively. The voltage level at these pins is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20mV/% frequency deviation.

Output Filter, C_3 (Pins 2 and 7)

Capacitors C_{3A} and C_{3B} connected from Pins 2 and 7 to ground form low-pass post detection filters for sections A and B respectively. The function of the post detection filter is to eliminate spurious outputs caused by out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7k) is the internal impedance at Pins 2 or 7.

TYPICAL CHARACTERISTICS

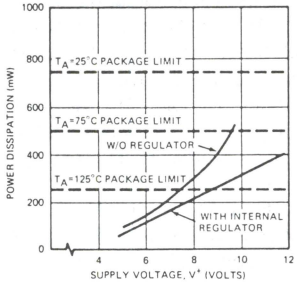


Figure 5. Internal Power Dissipation vs. Supply Voltage. Both Units Activated, R_L = 20 k

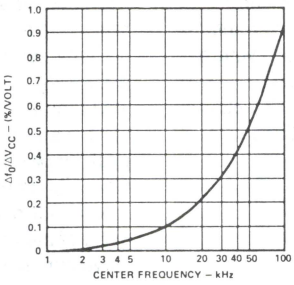


Figure 6. Power Supply Dependence of Center Frequency

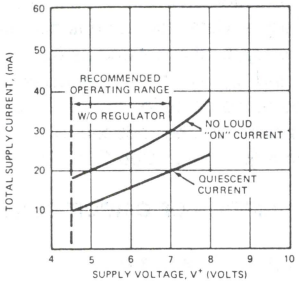


Figure 7. Total Supply Current vs. Supply Voltage for Operation without Internal Regulator (Pins 12 and 13 Shorted)

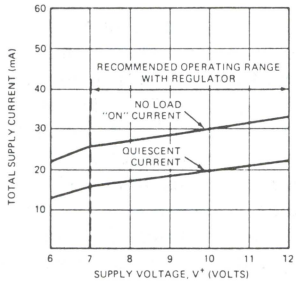


Figure 8. Total Supply Current vs. Supply Voltage for Operation with Internal Regulator (Pins 12 and 13 Not Connected)

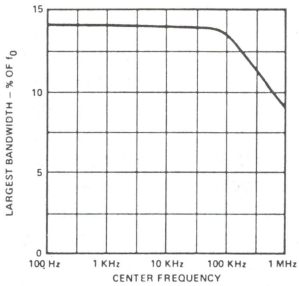


Figure 9. Largest Detection Bandwidth

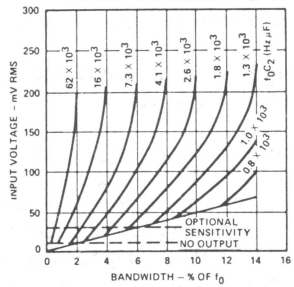


Figure 10. Bandwidth vs. Input Signal Amplitude (C_2 In μF)

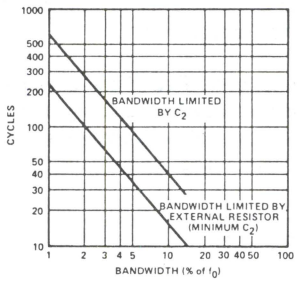


Figure 11. Greatest Number of Cycles Before Output

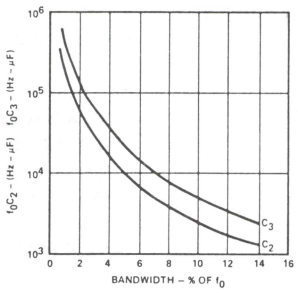


Figure 12. Detection Bandwidth as a Function of C_2 and C_3

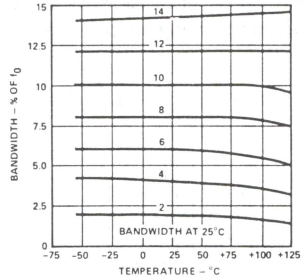


Figure 13. Bandwidth Variation with Temperature

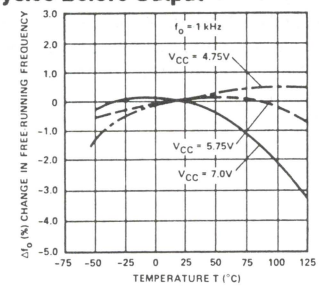


Figure 14. Frequency Drift with Temperature

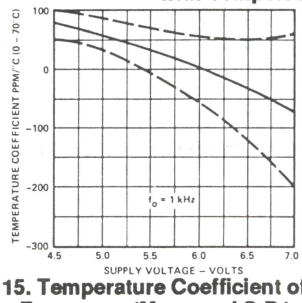


Figure 15. Temperature Coefficient of Center Frequency (Mean and S.D.)

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, a minimum value for C_3 is $2C_2$, where C_2 is the loop filter capacitance for the corresponding decoder section. If C_3 is smaller than $2C_2$, then frequencies adjacent to the detection band may switch the output stage "off" and "on" at the beat frequency, or the output may pulse "off" and "on" during the turn- on transient.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, this delay may be desirable as a means of suppressing spurious outputs. (For additional information, see Optional Controls Section, "Speed of Response" and "Chatter".)

Logic Output (Pins 3 and 6)

Output terminals 3 and 6 provide a binary logic output when an input signal tone is present within the detection-band of each respective decoder section. The logic outputs are uncommitted "bare-collector" power transistors capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from V_{CC} to Pins 3 or 6.

When an in-band signal is present, the output transistor at Pins 3 or 6 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+ higher than the V_{CC} supply. For safe operation, V+ ≤ 15 volts.

Regulator By-Pass (Pin 12)

This pin corresponds to the output of the voltage regulator section. For circuit operation with a supply voltage greater than 7V, Pin 12 should be ac grounded with a bypass capacitor ≥ 1μF. For circuit operation over a supply voltage range of 4.5 to 7V, the voltage regulator section is not required; Pin 12 should be shorted to V_{CC}.

Ground Terminals (Pins 4 and 5)

To eliminate parasitic interaction, each decoder section has a separate ground terminal. The internal regulator shares a common ground with decoder section A (Pin 4).

Independent ground terminals also allow additional flexibility for split supply operation. Pin 4 can be used as V-, and Pin 5 as ground, as shown in Figure 16. When the circuit is operated with split supplies, the positive supply should always be >6V, and the dc potential across Pins 13 and 14 should not exceed 15 volts.

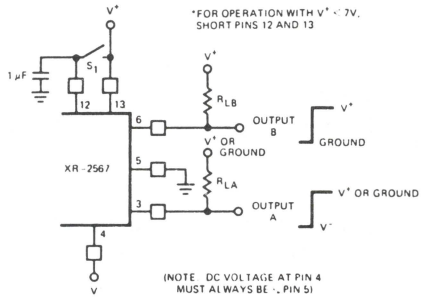


Figure 16. Split-Supply Operation Using Independent Ground Terminals of Units A and B. Unit A Operates Between V+ and V-: Unit B Operates Between V+ and Ground

OPTIONAL CONTROLS

Speed of Response

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus, maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}, C_3 = \frac{260}{f_o}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 17 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

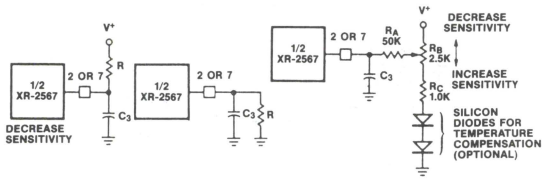


Figure 17. Optional Connections for Sensitivity Control

Chatter

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, "logic" may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input or, by increasing the size of capacitor C_3. Generally, the feed- back method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 18. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

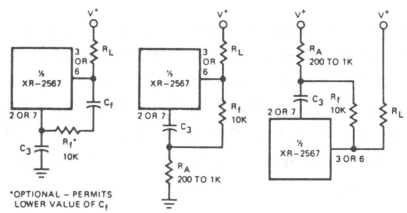


Figure 18. Methods of Reducing Chaffer

Skew Adjustment

The circuits shown in Figure 19 can be used to change the position of the detection band (capture range) within the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

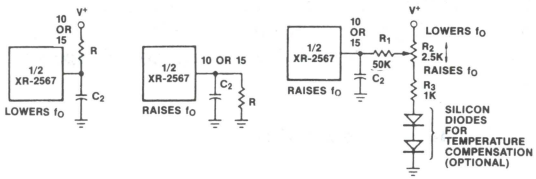


Figure 19. Connections to Reposition Detection Band

Output Latching

After a signal is received, the output of either decoder section can be latched "on" by connecting a 20kΩ resistor and diode from the "output" terminal to the "output filter" terminal as shown in Figure 20. The output stage can be unlatched by raising the voltage level at the output filter terminal.

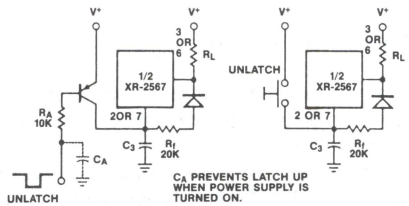
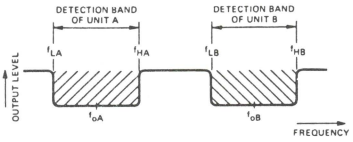


Figure 20. Output Latching

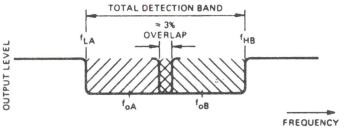
Positioning of Detection Bands

Figure 21 defines the respective band-edge and band-center frequencies for sections A and B of the dual tone decoder.

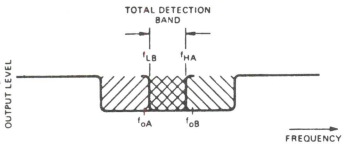
Frequencies f_L and f_H with appropriate subscripts refer to the low and the high band-edge frequencies for decoder sections A and B, and f_o is the center frequency.



(a) Independent Detection of Two Separate Tones



(b) Addition of Detection Bandwidth for Wide-Band Detection



(c) Subtraction of Bandwidths for Narrow-Band Detection

Figure 21. Positioning of Detection Bands

The two sections can be interconnected to form a single tone detector with an overall detection bandwidth equal to the sum or the difference of the detection bands for the two individual detector sections. For example, if the individual decoder sections are interconnected as shown in Figure 25, then the total detection bandwidth would be approximately equal to the sum of the respective bandwidths as shown in Figure 21(b). Similarly, if the decoders are interconnected as shown in Figure 23, then the overall detection band would be equal to the difference, or the overlap, between the respective bandwidths as shown in Figure 21(c).

Bandwidth Reduction

The bandwidth of each decoder can be reduced by either increasing the loop filter capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 22 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. Bandwidth reduction can also be obtained by subtracting overlapping bandwidths of the two decoder sections (see Figures 21(c) and 23).

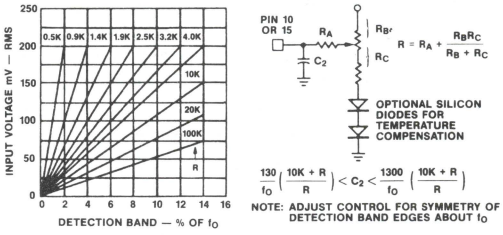


Figure 22. Bandwidth Reduction

APPLICATIONS

Dual-Tone Detection

In most dual-tone detection systems, the decoder output is required to change state only when both input tones are present simultaneously. This can be implemented by setting the detection bandwidth of each of the XR-2567 decoder sections to cover one of the input tones; and then connecting the respective outputs through a NOR gate, as shown in Figure 23. In this case, the output of the NOR gate will be "high" only when both input tones are present simultaneously. Due to capacitor and device variation, it is not possible to use a fixed R1 value in production applications.

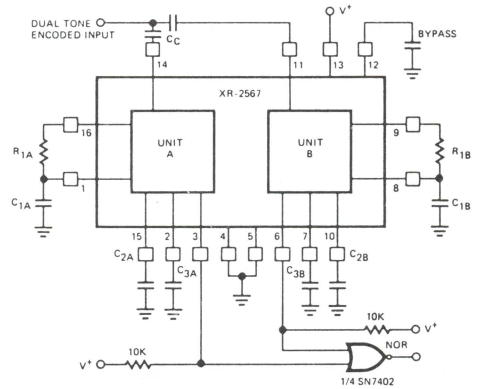


Figure 23. Connection for Decoding Dual-Tone Encoded Input Signals

Figure 24 shows additional circuit configurations which can be used for decoding multiple-tone input signals. In Figure 24(a), the output of Unit A is connected to the output filter (Pin 7) of Unit B through the diode D_1. If no input tone is present within the detection-band of Unit A, then its output (pin 3) is "high", which keeps diode D_1 conducting and "disables" Unit B by keeping its output (pin 6) "high". If an input tone is present within the detection-band of Unit A, Pin 3 is low, diode D_1 is reverse biased, and decoder B is no longer disabled. If under these conditions an input signal is present within the detection-band of Unit B, then its output at Pin 6 would be "low". Thus, the output at Pin 6 is "low" only when input tones within the detection-band of A and B are present simultaneously.

The dual-tone decoder circuit of Figure 24(b) makes use of the split-ground feature of the XR-2567. The output terminal of Unit A is used as a "switch" in series with the ground terminal (Pin 5) of Unit B. If the input tone A is not present, Pin 3 is at its high-impedance state, and the ground terminal of Unit B is open-circuited. When the input tone A is present, Pin 3 goes to a low-impedance state and Unit B is activated. In this manner, the output of Unit B will be "low" only when both tones A and B are present.

In the circuit connection of Figure 24(b), Unit B does not draw any current until it is activated. Therefore, its power dissipation in a stand-by condition is lower than other dual-tone decoder configurations. However, due to finite series resistance between Pin 3 and ground when Unit B is activated, the output current sink capability is limited to ≤ 10mA.

Sequential Tone Decoding

Dual-tone decoder circuits can also be used for sequential tone decoding where one tone must be present before the other for the circuit to operate. This can be achieved by making the output filter capacitance, C_3, of one of the sections large with respect to the other. For example, in the circuits of Figures 24(a) and 24(b), if C_{3A} is chosen to be much larger than C_{3B} ($C_{3A} \geq C_{3B}$), then Unit A will remain "on" and activate B for a finite time duration after tone A is terminated. Thus, the circuit will be able to detect the two tones only if they are present sequentially, with tone A preceding tone B.

The circuit of Figure 24(a) can also be modified for sequential tone decoding by addition of a diode, D_2, between pins 3 and 6. Once activated by Unit A, Unit B will stay "on" as long as tone B is present, even though tone A may terminate. Once tone B disappears, the circuit is reset to its original state and would require tone A to be present for activation.

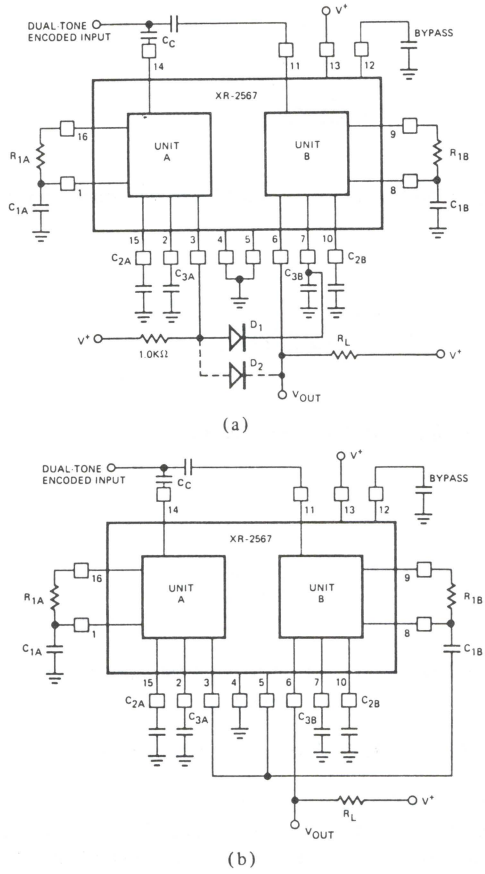


Figure 24. Additional Dual-Tone Decoding Circuits

High-Speed Narrow-Band Tone Decoder

The circuit of Figure 23 can be used as a narrow-band tone decoder by overlapping the detection bands of Units A and B (see Figure 21(c)). The output of the NOR gate will be high only when an input signal is present within the overlapping portions of the detection band. To maintain uniform response within the pass-band, the input signal amplitude should be ≥ 80mV rms. For minimum response time, PPL filter capacitors C_{2A} and C_{2B} should be:

$$C_{2A} = C_{2B} = \frac{130}{f_o\,(Hz)}\ \mu F$$

Under this condition, the worst-case output delay is ≈ 10 to 14 cycles of the input tone.

The practical matching and tracking tolerances of individual units limit the minimum bandwidth to ≈ 4% of f_o.

Wide-Band Tone Decoder

Figure 25 is a circuit configuration for increasing the detection bandwidth of the XR-2567 by combining the respective bandwidths of individual decoder sections. If the detection bands of each section are located adjacent to each other as shown in Figure 21(b), and if the two outputs (pins 3 and 6) are shorted together, then the resulting bandwidth is the sum of individual band-widths. In this manner, the total detection bandwidth can be increased to 24% of center frequency. To maintain uniform response throughout the pass band, the input signal level should be ≥ 80mV, rms, and the respective passbands of each section should have ≈ 3% overlap at center frequency.

Tone Transceiver

The XR-2567 can be used as a full-duplex tone transceiver by using one section of the unit as a tone detector and the remaining section as a tone generator. Since both sections operate independently, the circuit can transmit and receive simultaneously, A recommended circuit connection for transceiver applications is shown in Figure 26. In this case, Unit A is utilized as the receiver, and Unit B is used as the transmitter. The transmitter section can be keyed "on" and "off" by applying a pulse to pin 8 through a disconnect diode D_1. The oscillator section of Unit B will be keyed "off" when the keying logic level at pin 8 is at a "low" state.

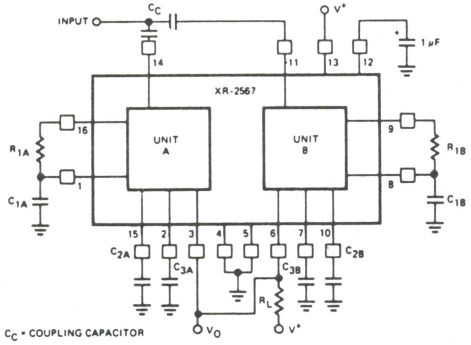


Figure 25. Wide-Band Tone Detection

The output of the transmitter section (Unit B) can also be frequency modulated over a +6% deviation range by applying a modulation signal to pin 10.

High Current Oscillator

The oscillator output of each section of XR-2567 can be amplified using the high current logic driver sections of the circuit. In this manner, each section of the circuit can switch 100mA loads, without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 27. The oscillator frequency can be modulated over 16% of f_o by applying a control voltage to pins 15 or 10.

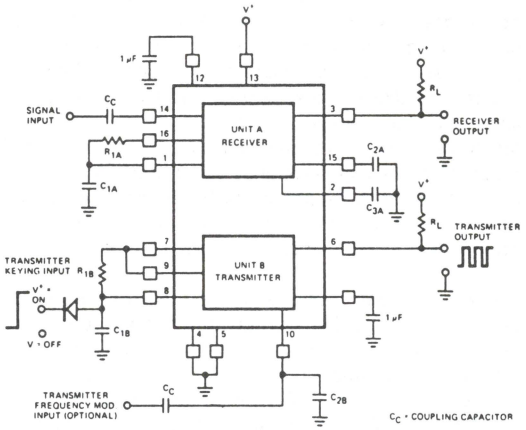


Figure 26. Tone Transceiver

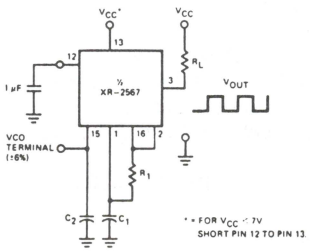


Figure 27. Precision Oscillator with High Current Output Capability

Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a preamplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/ buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR-2208 operates over a 0°C to 70°C temperature range. The XR-2208M is specified for operation over the military temperature range of –55°C to +125°C.

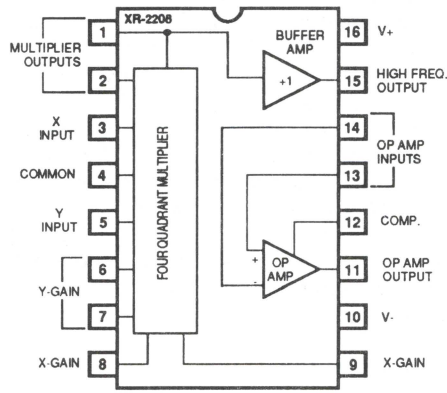
FEATURES

Maximum Versatility
  Independent Multiplier, Op Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB B.W. — 8MHz typ.
  3° Phase Shift B.W. — 1.2MHz typ.
  Transconductance B.W. — 100MHz typ.
Simplified Offset Adjustments
Wide Supply Voltage Range (±4.5V to ±16V)

ABSOLUTE MAXIMUM RATINGS

Power Supply V+	+18 Volts
V–	–18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625mW
Derate above + 25°C	5mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



APPLICATIONS

Analog Computation
  Multiplication
  Division
  Squaring
  Square-Root
Signal Processing
  AM Generation
  Frequency Doubling
  Frequency Translation
  Synchronous AM Detection
  Triangle-to-Sinewave Converter
  AGC Amplifier
  Phase Detector
Phase-Locked Loop (PLL)
Applications
  Motor Speed Control
  Precision PLL
  Carrier Detection
  Phase-Locked AM Demodulation

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2208M	Ceramic	–55°C to +125°C
XR-2208N	Ceramic	0°C to +70°C
XR-2208P	Plastic	0°C to +70°C
XR-2208CN	Ceramic	0°C to +70°C
XR-2208CP	Plastic	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-2208/ XR-2208M MIN	XR-2208/ XR-2208M TYP	XR-2208/ XR-2208M MAX	XR-2208C MIN	XR-2208C TYP	XR-2208C MAX	UNITS	FIGURES	CONDITIONS
GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	Vdc		See Figure 11
Supply Current		4	7		5	8	mA	2	Measured at Pin 16
MULTIPLIER SECTION									
Non-linearity (Output Error in % of Full Scale)									No external offset trim
		0.3	0.5		0.5	1.0	%	3	V_y = ±10V, −10V < V_x < +10V
		0.3	0.5		0.5	1.0	%		V_x = ±10V, −10V < V_y < +10V
		0.7	1.0		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1) f = 50Hz
Feedthrough									
a) With Offset Adj.									
X-input		45	80		70	120	mVp-p		V_x = 20 Vp-p, V_y = 0
Y-input		60	100		90	150	mVp-p		V_y = 20 Vp-p, V_x = 0
b) No Offset Adj.									
X-input		120			200		mVp-p		V_x = 20 Vp-p, V_x = 0
Y-input		120			200		mVp-p		V_y = 20 Vp-p, V_x = 0
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current									
X, Y input		2	6		3	8	µA	2	I_3,I_5 of Figure 2
Common input		4	12		6	16	µA	2	I_4 of Figure 2
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured looking into Pin 3 or Pin 5
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 2
Avg. Temp. Drift		0.5			0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response								5	See Definition Section
3-dB Bandwidth									
X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwdith		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into Pins 1 or 2
BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	4	Measured looking into Pin 15
Gain	1.0			1.0					
OPERATIONAL AMPLIFIER									
Input Offset Voltage		1	3		2	6	mV	6	R_S < 50Ω
Temperature Coefficient of Input Offset Voltage		6	20		9	30	µV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Input Offset Current		4	75		10	100	nA	6	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	6	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	6	$R_L \ge 2K$, V_o = ±10V, f = 20Hz
Differential Input Resistance	0.5	3			3		MΩ	6	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \ge 2K$, $T_{LOW} \le T_A \le T_{HIGH}$
Input Common	+12	+14		+12	+14				
Mode Range	−10	−12		−10	−12		V	6	
Common Mode Rejection	70	90		70	90		dB	6	f = 20 Hz
Output Resistance		2			2		kΩ	6	
Output Short	50	10	30		10		mA	5	Positive
Circuit Current	−30	−10	65		−10		mA	5	Negative
Slew Rate		0.5			0.5		V/µs	7	Gain = 1, $R_L \ge 2K$, $C_L \le 100pF$ C_C = 20pF
Power Supply Sensitivity		30			30		µV/V	6	$R_S \le 10K$

Note 1: T_{LOW} = −55°C, T_{HIGH} = +125°C for XR-2208M T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2208/XR-2208C

CAUTION: *When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 3, 4 and 5.*

SYSTEM DESCRIPTION

The XR-2208 operational multiplier contains a four-quadrant multiplier with a buffer amplifier for one of the differential outputs for applications requiring high frequency applications. The inputs have a dynamic response of 4MHz (8MHz for the X input) and a transconductance bandwidth of 100MHz for phase detector applications. The fully independent operational amplifier features high gain and a large common mode rejection ratio (90dB). The device can be powered by voltages from 4.5 VDC to 16 VDC.

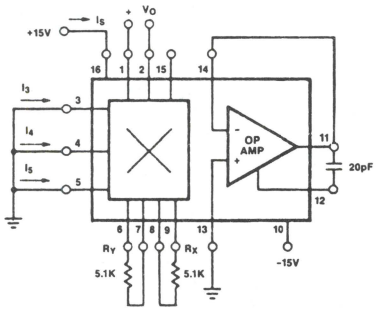


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage.

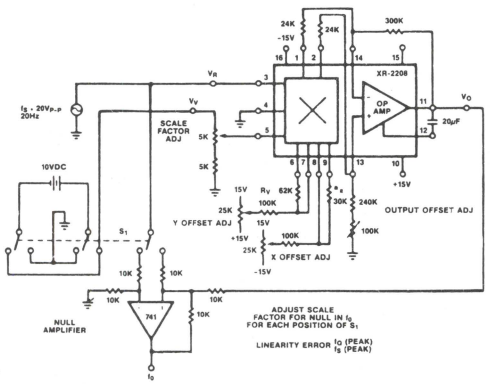


Figure 2. Linearity Test Circuit

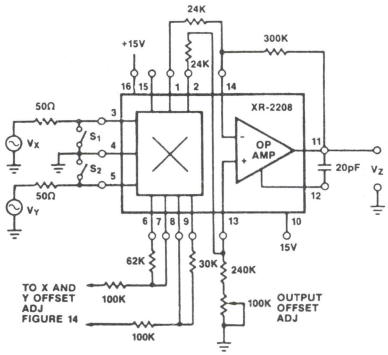


Figure 3. Test Circuit for Feedthrough Measurement
X-Input Feedthrough = V_Z with S_1, open, S_2 closed.
Y-Input Feedthrough = V_Z with S_1, closed, S_2 open.

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_Z = K[(Vx + \varnothing_X)\ (V_Y + \varnothing_Y)] + \varnothing_O$$

where $\varnothing_X$ and $\varnothing_Y$ are the offset voltages associated with the respective inputs, $\varnothing_O$ is the offset voltage of the output, V_Z is the multiplier output, V_X and V_Y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_Z, is related to the X and Y inputs as $V_Z = K(V_X \cdot V_Y)$. The scale factor K has the dimensions of (volts) – 1 and can be adjusted externally.

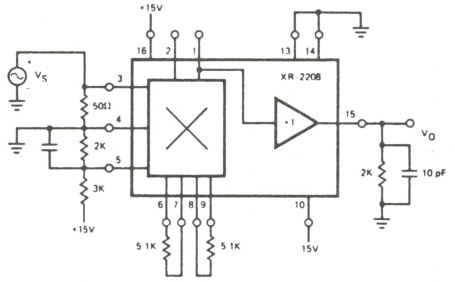


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (for Y-Input, reverse connections between Pin 3 and 5).

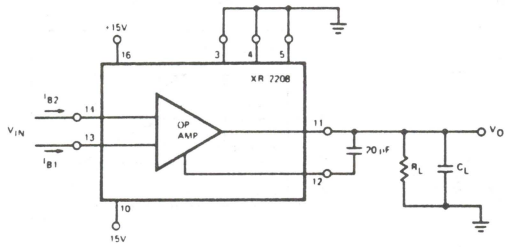


Figure 5. Test Circuit for Op Amp DC Parameters

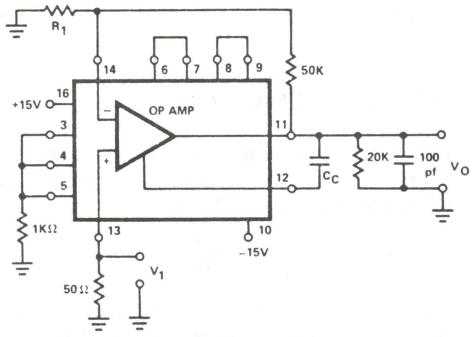


Figure 6. Op Amp AC Test Circuit

In most arithmetic applications the multiplier and op amp sections of the XR-2208 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_o}{V_x V_y}\right)\left(\frac{V_z}{V_o}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14, V_o is the multiplier output across pins 1 and 2, and V_z is the op amp output at pin 11. With reference to Figure 14, these gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y}\ (\text{volts})^{-1}; \qquad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kΩ.

Thus, overall scale factor K can be adjusted by varying R_x, R_y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

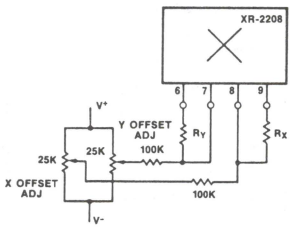


Figure 13. Offset Adjustment

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier bandwidth" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth:* Frequency where the multiplier output is 3-dB below its low frequency (f = 20Hz) level.

b) *3° Phase Shift Bandwidth:* Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth:* Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth:* Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

TYPICAL CHARACTERISTIC CURVES

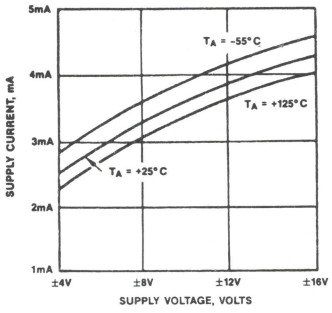


Figure 7. Supply Current vs Supply Voltage

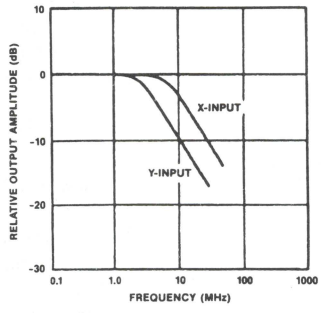


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 15 — See Fig. 4).

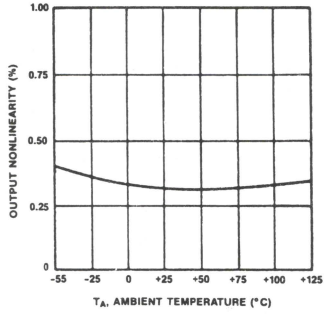


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2).

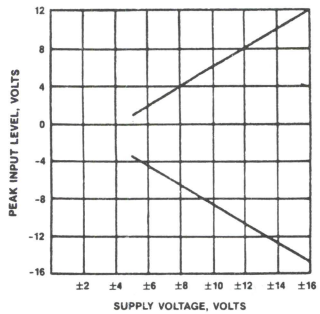


Figure 10. Multiplier Input Dynamic Range vs Power Supply

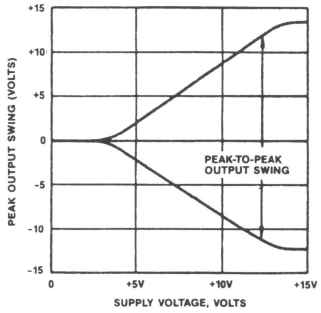


Figure 11. Op Amp Output Swing vs Power Supply

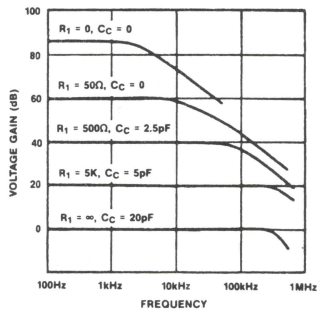


Figure 12. Op Amp Frequency Response

DESCRIPTION OF CIRCUIT CONTROLS

Multiplifer Inputs (Pins 3, 4, and 5)

The X and Y inputs to the multiplier are applied to pins 3 and 5 respectively. The third input (pin 4) is common to both X and Y portions of the multiplier, and in most applications serves as a "reference" or ground terminal. The typical bias current at the multiplier inputs is 3μA for the X- and Y-inputs and 6μA for the "common" terminal. In circuit applications such as "synchronous AM detection" or "frequency doubling" where the same input signal is applied to both X and Y inputs, pin 4 can be used as the input terminal since it is common to both X and Y sections of the multiplier.

Multiplier Outputs (Pins 1 and 2)

The differential output voltage, V_o, across these terminals is proportional to the linear product of voltages V_x and V_y applied to the inputs. V_o can be expressed as:

$$V_o \approx \left(\frac{25}{R_x R_y}\right)\left(V_x V_y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_x and R_y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply. One of the multiplier outputs (pin 1) is internally connected to the unity-gain buffer amplifier input for high-frequency applications.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 2 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_Z, is then obtained from the op amp output at pin 11, as shown in Figure 14.

X and Y Gain Adjust (Pins 6, 7, 8, 9)

The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_x and R_y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y} \text{ (volts)}^{-1}$$

where R_x and R_y are in kΩ.

X and Y Offset Adjust (Pins 7 and 8)

Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP Inputs (Pins 13 and 14)

Pin 13 is the non-inverting and pin 14 the inverting input for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 2). **Note: When the op amp section is not used, these terminals should be grounded.**

OP AMP Compensation (Pin 12)

The op amp section can be compensated for unconditional stability with a 20pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP Output (Pin 11)

This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2208 output, with the op amp inputs being connected to the multiplier outputs.

Buffer Amplifier Output (Pin 15)

The buffer amp is internally connected to the multiplier section. The buffer amp has unity voltage gain, and provides a low-impedance output at pin 15 for the multiplier section. The buffer amp is particularly useful for high frequency operation since it minimizes the capacitive loading effects at the multiplier outputs.

The buffer amplifier is activated by connecting a load resistor, R_1, from pin 15 to ground. When it is not used, pin 15 can be left open circuited. However, since the buffer amplifier output is a low impedance point, reasonable care should be taken to avoid burnout due to accidental short circuits. The maximum dc current drawn from pin 15 should be limited to 10mA. The dc voltage at pin 15 is typically 4.5 volts below V+.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 15 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply 0V to both inputs and adjust the output offset to 0V using the output offset control.
2. Apply 20Vp-p at 50Hz to the X-input and 0V to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.
3. Apply 20Vp-p to the Y-input and 0V to the X-input. Trim X-offset adjust for minimum peak-to-peak out-put.
4. Repeat step 1.
5. Apply +10V to both inputs and adjust scale factor for V_o = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

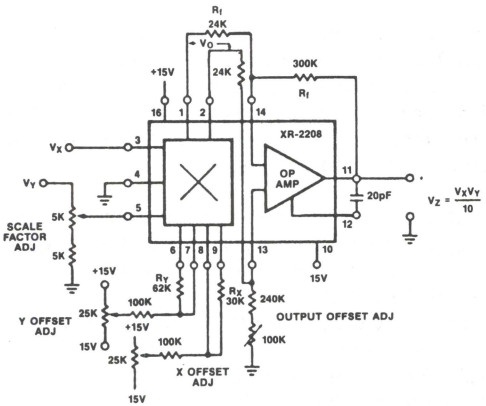


Figure 14. Multiplication Circuit

Squaring Circuit

The recommended circuit connection for squaring applications is shown in Figure 15. This circuit is the same as the basic multiplier circuit with both inputs tied together, except only one input offset adjustment is necessary. Trimming procedure for the squaring circuit is as follows:

1. Apply 0 volts to the input and adjust the output offset to zero.
2. Apply 1.0V to the input and adjust the Y-offset until $V_o = 0.10V$.
3. Apply 10V to the input and adjust the scale factor until $V_o = +10V$
4. Apply –10V to the input and check that $V_o = +10V$. If not, repeat steps 1 through 3. Some compromise may be necessary in scale factor adjustments given in

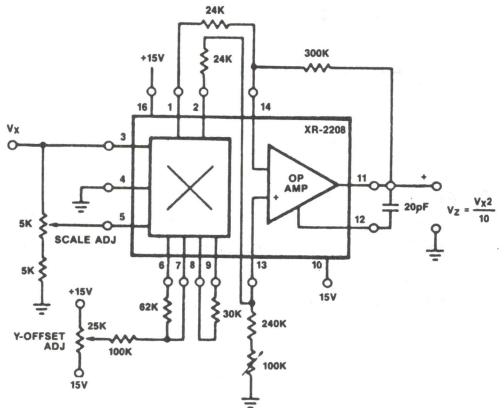


Figure 15. Squaring Circuit

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Figure 16. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_o = +10\ V_z/V_x$ where $V_x < 0$ and V_z can have either sign. Positive values of V_x are not allowed, since this will reverse the polarity of the feedback loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2208, and is common to all analog division circuits. The divide circuit is trimmed as follows:

1. Apply $V_z = 0$ and trim the output offset adjustment for constant output voltage as V_x is varied from –1V to –10V.
2. Keeping $V_z = 0$, and applying $V_x = –10V$, trim the Y-offset adjust until $V_o = 0$.
3. Let $V_z = V_x$ and/or $V_z = –V_x$ and trim the X-offset adjustment for constant output voltage as V_x is varied from –1V to –10V.
4. Repeat steps 1 and 2 if step 3 required a large initial adjustment.
5. Keeping $V_z = V_x$, adjust the scale factor trim for $V_o = –10V$ as V_x is varied from –1V to –10V.

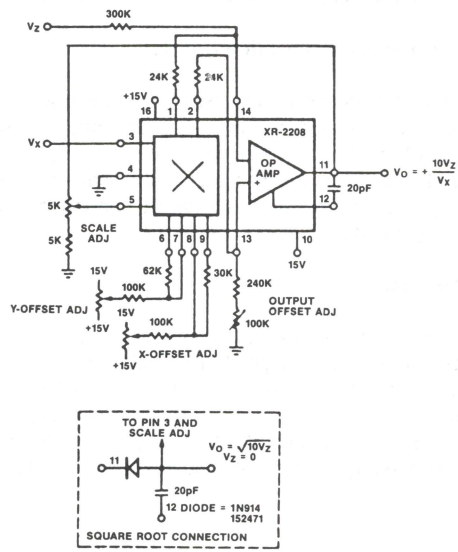


Figure 16. Dividing Circuit

Square Root Circuit

This is essentially the dividing circuit with the X input tied to the output. Thus, the voltage on the Z input is divided by the output voltage, i.e. the output is proportional to the square root of the input. A diode is included in series with the output to prevent a latchup condition which would result if V_z were allowed to go negative. The square root circuit may be trimmed as a divider by disconnecting the X-input from the output, keeping $V_z > 0$ and $V_x < 0$. The square root circuit may also be trimmed in the closed-loop mode by the following procedure:

1. Apply V_z = +0.10V and trim the output offset adjust for V_o = –0.316V.
2. Apply V_z = +0.9V and trim the X-offset adjust for V_o = –3.0V.
3. Apply V_z = +10V and trim the scale factor adjust for V_o = –10V.
4. Repeat steps 1 through 3 until desired accuracy is achieved.

EQUIVALENT SCHEMATIC DIAGRAM

PART II: SIGNAL PROCESSING

AM Generation

Figure 17 is the recommended circuit connection for generating double side-band (DSB) or suppressed carrier AM signals. Modulation and carrier inputs are applied to the X and Y inputs respectively. The carrier level at the output can be adjusted by the dc voltage applied to pin 3. For suppressed carrier operation, the carrier feedthrough can be further reduced by using the X and Y offset adjustments. In this application, the unity-gain buffer amplifier section will provide a low impedance output if desired. If the buffer amp is not used, pin 15 should be open circuited to reduce power dissipation.
Typical carrier suppression without offset adjustment is 40 dB for frequencies up to 1MHz, and 30dB for frequencies up to 10MHz. For low frequency applications (f < 10kHz), carrier suppression can be reduced to 60dB by using the offset adjustment controls.

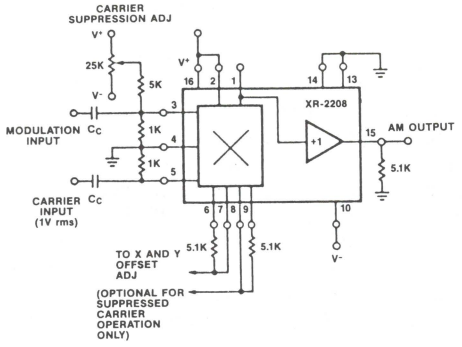


Figure 17. AM Generation

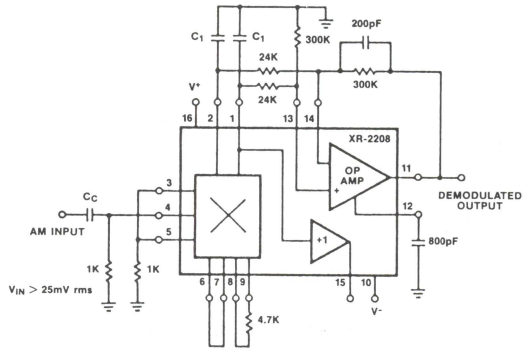


Figure 18. Synchronous AM Detector

Synchronous AM Detection

Figure 18 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100MHz. The AM input signal is applied to the multiplier "common" terminal (pin 4). The Y-gain terminals are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, at pins 1 and 2 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

Triangle-to-Sinewave Conversion

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2208. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 3). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave. For the component values shown in Figure 19, the recommended input signal level at pin 3 is ≃ 300mV pp in order to obtain a 2V pp sine wave output at pin 15. This waveform can be further amplified using the op amp section to provide high level (10V pp), low distortion output at pin 11.

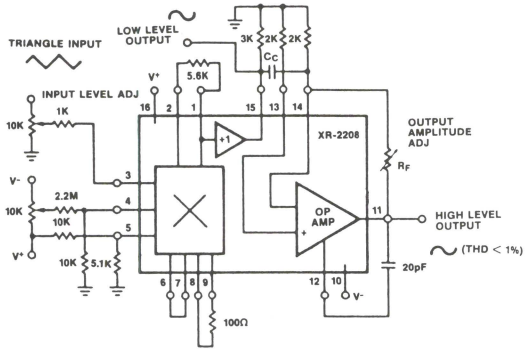


Figure 19. Triangle-to-Sine Converter

Phase Detection

The multiplier section can be used as a phase detector. A recommended circuit connection is shown in Figure 20. The reference input is applied to pin 5, and the input signal whose phase is to be detected is applied to pin 3. The differential dc voltage, $V_{ø}$, at the multiplier outputs (pins 1 and 2) is related to the phase difference, ø, between the two input signals, V_1 and V_2, as:

$$V_{ø} = K_d \cos ø$$

where K_d is the phase detector conversion gain. For input signals ≥ 50mV rms, K_d is ≈ 2V/radian and is independent of signal amplitude. For lower input amplitudes, K_d decreases linearly with the decreasing input level. The capacitors C_1 at pins 1 and 2 provide a low-pass filter with a time constant $T_1 = R_1C_1$, where R_1 = 6kΩ is the internal impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2208 to further amplify the output voltage, $V_{ø}$. The XR-2208 is suitable for phase detection for input frequencies up to 100MHz. Pins 1 and 2 are normally tied to an operational amplifier placed in a difference amplifier configuration.

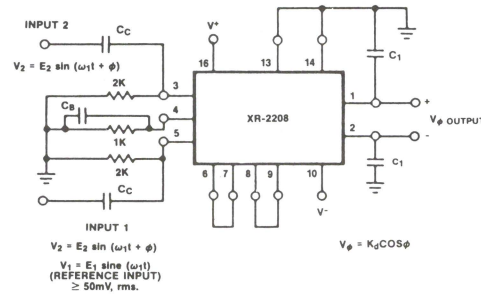


Figure 20. Phase-Detector Circuit

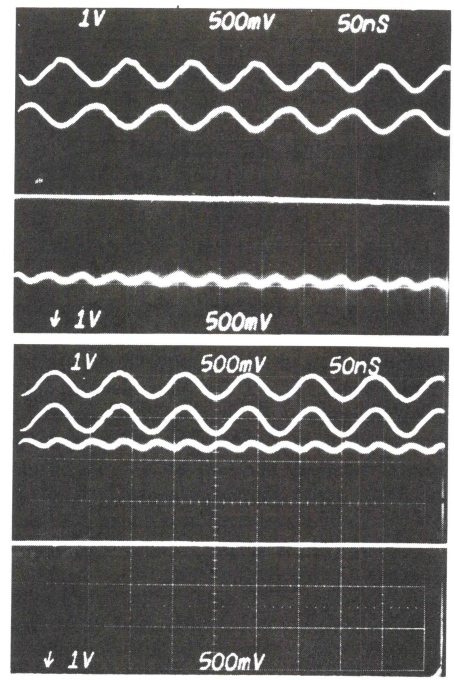


Figure 21. Shows the summed output of the phase detector circuit with pin 1 applied to the inverting input of oscilloscope; pin 2 applied to the noninverting input of oscilloscope.

C_1 = 12pF, f_{INPUT} = 12MHz, ø = 180°, V_0 = -2.5 V_{DC}, (a) ø = 0°, (b) V_0 = +2.5 V_{DC}.

Motor Speed Control

A motor speed control where the frequency of the motor is "phase-locked" to the input reference frequency, f_r, is shown in Figure 22. The multiplier section of the XR-2208 is used as a phase-comparator, comparing the phase of the tachometer output signal with the phase of the reference input. The resulting error voltage across pins 1 and 2 is low-pass filtered by capacitors C_1 and amplified by the op amp section. This error signal is then applied to the motor field-winding to phase-lock the motor speed to the input reference frequency.

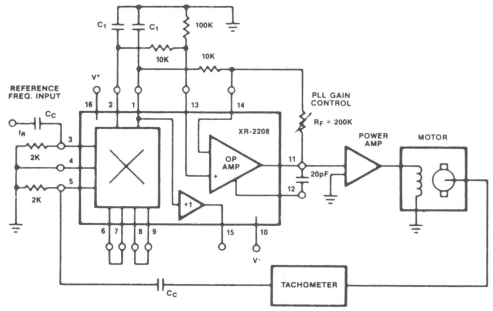


Figure 22. Motor Speed Control Circuit

Precision PLL

A precision phase-locked loop may be constructed using an XR-2207 voltage controlled oscillator and an XR-2208. (See Figure 23.) Due to the excellent temperature stability and wide sweep range of the XR-2207 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2208 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30ppm/°C.

Phase-Locked AM and Carrier Detection

The XR-2208 can be used as a "quadrature detector" in conjunction with monolithic PLL circuits to perform phase-locked AM demodulation and for carrier-level detection. Figure 24 shows a recommended circuit connection for such applications. The XR-210 or XR-215 monolithic PLL circuits can be adjusted to lock on the desired input AM signal and re-generate the unmodulated carrier. This carrier frequency appears across the timing capacitor, C_o, of the PLL and is used as the "reference input" to the XR-2208 multiplier. The AM signal is applied simultaneously to the PLL input and to the XR-2208 multiplier input (pin 3), as shown in Figure 24.

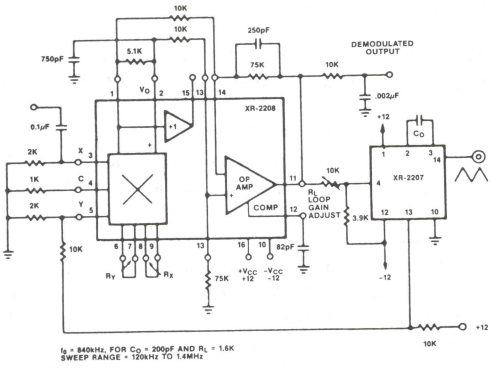


Figure 23. Precision PLL

The demodulated signal is then low-pass filtered by capacitor C_1 at the multiplier output, and can be amplified further to the desired audio level by using the op amp section of the XR-2208.

In the carrier detector applications, the op amp is used as a voltage comparator and produces a "high" or "low" level logic signal at the op amp output when the input carrier level reaches a detection threshold level set by an external potentiometer. The output from the carrier detector can then be used to enable the "logic-output" stage of the XR-210 FSK modem.

The phase-locked AM or carrier detector system of Figure 23 shows a high degree of frequency selectivity, as determined by the monolithic PLL "capture" band-width.

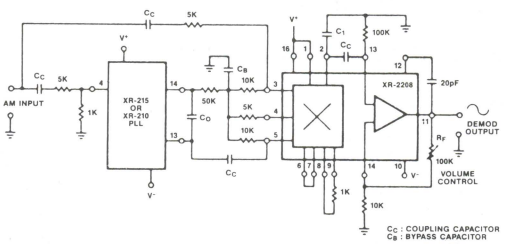


Figure 24. Phase-Locked AM Demodulation or Carrier Detection

Monolithic Multiplier/Detector

GENERAL DESCRIPTION

The XR-2228 is a monolithic multiplier/detector circuit especially designed for interfacing with integrated phase-locked loop (PLL) circuits, to perform synchronous AM detection and triangle-to-sinewave conversion. It combines a four-quadrant analog multiplier (or modulator) and a high-gain operational amplifier in a single monolithic circuit.

As shown in the equivalent schematic diagram, the four-quadrant multiplier section is designed with fully differential X- and Y-inputs and differential outputs. For maximum versatility, the multiplier and the operational amplifier sections are not internally connected. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post-detection amplifier for synchronous demodulation, phase-detection or for sine-shaper applications.

FEATURES

Independent Multiplier and 0p Amp Sections
Differential X and Y Inputs
Interfaces with all PLL and VCO Circuits
Wide Common Mode Range
Wide Transconductance Bandwidth (100MHz, Typ.)
Wide Supply Voltage Range (±4.5V to ±16V)

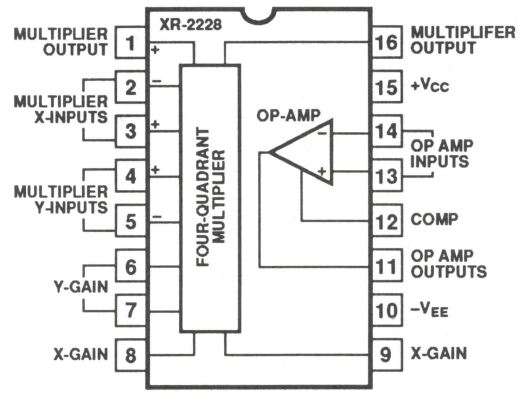
APPLICATIONS

Phase-Locked Loop Design
Phase Detection
Synchronous AM Detection
AM Generation
Triangle-to-Sinewave Conversion
Frequency Translation

ABSOLUTE MAXIMUM RATINGS

Power Supply	±18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625mW
Derate above +25°C	5mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2228CN	Ceramic	0°C to + 70°C
XR-2228CP	Plastic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-2228 multiplier/detector contains a four quadrant multiplier and a fully independent operational amplifier. The four quadrant multiplier has fully differential X and Y inputs and outputs. Both inputs have 3MHz dynamic response and 100MHz transconductance band- width. The operational amplifier features high gain and a large common mode range. The device is powered by 4.5V to 16V split supplies.

For higher frequency applications, consider the XR- 2208.

ELECTRICAL CHARACTERISTICS

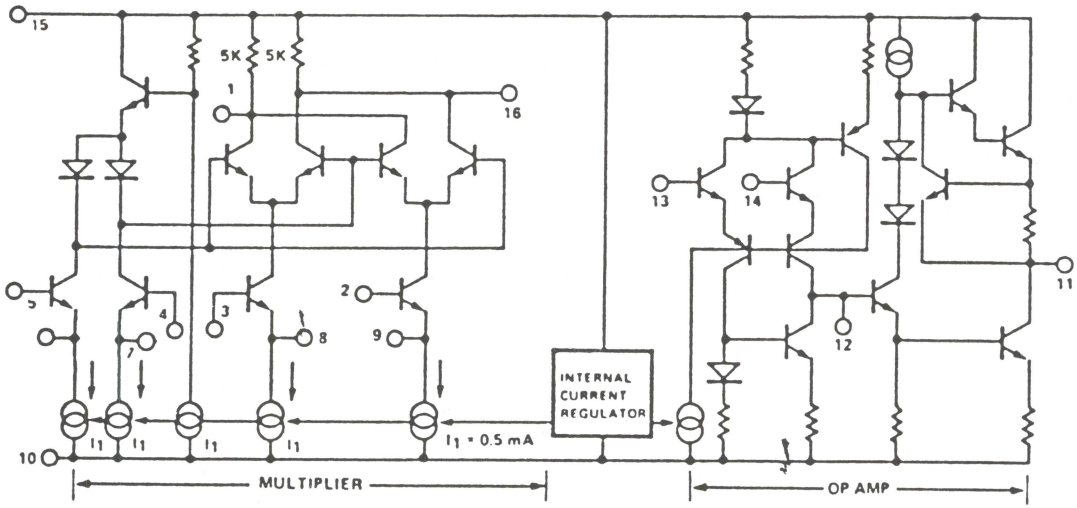
Test Conditions: Supply Voltage = ±15V. T_A = 25°C, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	FIGURE	CONDITIONS
I. GENERAL						
Supply Voltage	±4.5		±16	V dc		See Figure 11
Supply Current		5	8	mA	1	Measured at Pin 15
II. MULTIPLIER/MODULATOR SECTION						
Non-linearity						No external offset trim
(Output Error in % of Full Scale)		0.5	1.0	%	2	V_y = ±10V, −10V < V_x < +10V
		0.5	1.0	%		Vx = ±10V, −10V < V_y < +10V
		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
						f = 50Hz
Feedthrough						
a. With Offset Adj.						
X-input		70	120	mVp-p	3	V_x = 20 Vp-p V_y = 0
Y-input		90	150	mVp-p		V_y = 20 Vp-p, V_x = 0
b. No Offset Adj.						
X-input		200		mVp-p		V_x = 20 Vp-p, V_x = 0
Y-input		200		mVp-p		V_y = 20 Vp-p, V_x = 0
Temperature Coefficient of Scale Factor		±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current						
X or Y inputs		3	8	µA	1	Measured at Pins 2, 3, 4 or 5.
Input Resistance		1.0		MΩ	2	Measured at Pins 2, 3, 4 or 5.
Output Offset Voltage		80	140	mV	2	Measured across Pins 1 and 16
Avg. Temp. Drift		0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response					4	See definition section, and Note 1
3-dB Bandwidth						
X-input	1	3		MHz		
Y-input	1	3		MHz		
3° Phase-Shift Bandwidth		1		MHz		
1% Absolute Error Bandwidth		30		kHz		
Transconductance Bandwidth		100		MHz		
Output Impedance		5		kΩ		Measured looking into Pins 1or 16
III. OPERATIONAL AMPLIFIER SECTION						
Input Offset Voltage		2	6	mV	5	R_S < 50Ω
Temp. Coef. of Input Offset Voltage		9	30	µV/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Offset Current		10	100	nA	5	$I_{B1} - I_{B2}$
Input Bias Current		50	300	nA	5	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		dB	5	$R_L \ge 2K$, V_o = ±10V, f = 20Hz
Differential Input Resistance		3		MΩ	5	
Output Voltage Swing	±10	±12		V		$R_L \ge 2K$, $T_{LOW} \le T_A \le T_{HIGH}$
Input Common Mode	+12	+14				
Range	−10	−12		V	5	
Common Mode Rejection	70	90		dB	5	f = 20Hz
Output Resistance		2		kΩ	5	
Slew Rate		0.5		V/µs	5	Gain = 1, $R_L \ge 2K$, $C_L \le 100pF$, C_C = 20pF
Power Supply Sensitivity		30		µV/V	5	$R_S \le 10K$

Note 1: T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2228C; not tested in production

CAUTION: *When using only the op amp or only the multiplier section of the XR-2228, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 2, 3, 4 and 5.*

EQUIVALENT SCHEMATIC DIAGRAM



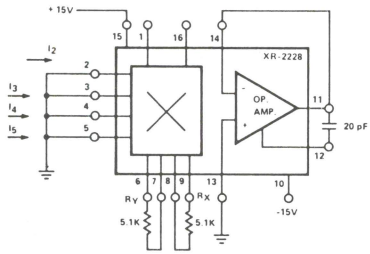


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage

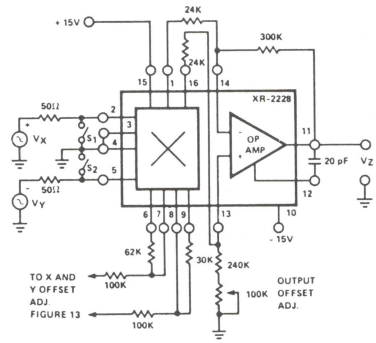


Figure 3. Test Circuit for Feedthrough Measurement. X-Input Feedthrough = V_Z with S_1, open S_2 closed. Y-Input Feedthrough = V_Z with S_1 closed, S_2 open.

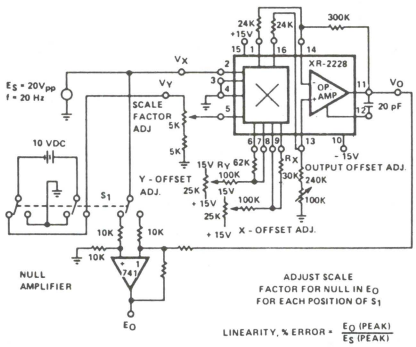


Figure 2. Linearity Test Circuit

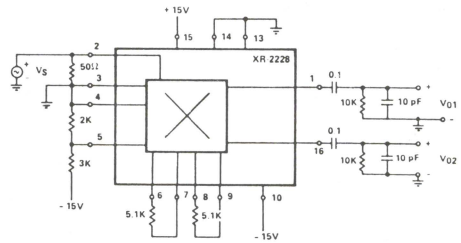


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (For Y-Input, reverse connections between Pins 2 and 5)

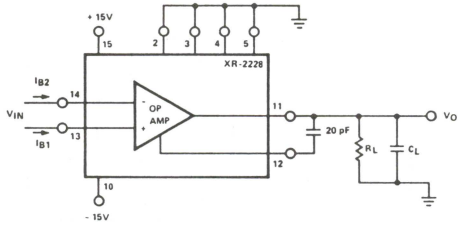


Figure 5. Test Circuit for Op Amp DC Parameters

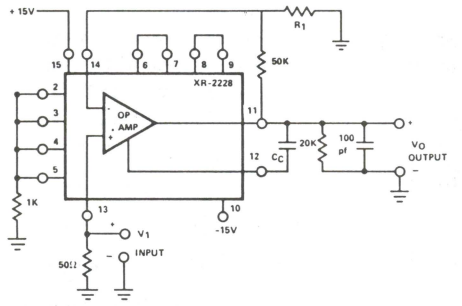


Figure 6. Op Amp AC Test Circuit

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_z = K[(V_x + \varnothing_x)(V_y + \varnothing_y)] + \varnothing_0$$

where $\varnothing_x$ and $\varnothing_y$ are the offset voltages associated with the respective inputs, $\varnothing_0$ is the offset voltage of the output. V_z is the multiplier output, V_x and V_y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_z, is related to the X and Y inputs as $V_z = K(V_x \cdot V_y)$. The scale factor K has the dimensions of $(volts)^{-1}$ and can be adjusted externally.

In most arithmetic applications the multiplier and op amp sections of the XR-2228 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_o}{V_x V_y}\right)\left(\frac{V_z}{V_o}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14. V_o is the multiplier output across pins 1 and 16, and V_z is the op amp output at pin 11. With reference to Figure 14, the gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y}\ (volts)^{-1}; \qquad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kilo-ohms.

Thus, overall scale factor K can be adjusted by varying R_x, R_y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier band-width" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth:* Frequency where the multiplier output is 3-dB below its low frequency (f = 20Hz) level.

b) *3° Phase Shift Bandwidth:* Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth:* Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth:* Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

TYPICAL CHARACTERISTICS CURVES

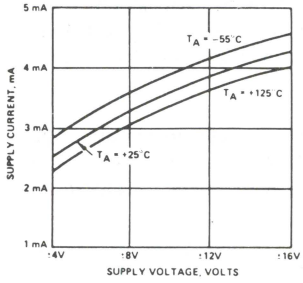


Figure 7. Supply Current vs Supply Voltage

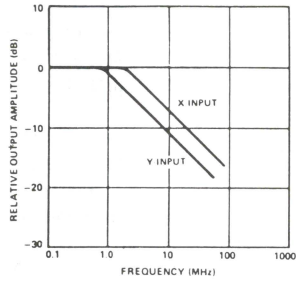


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 16-See Fig. 4)

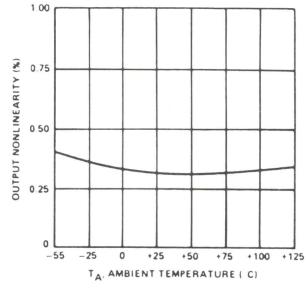


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2)

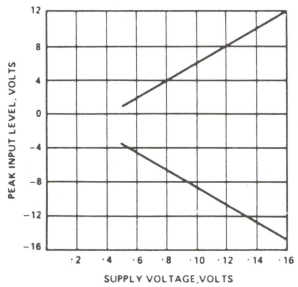


Figure 10. Multiplier Input Dynamic Range vs Power Supply

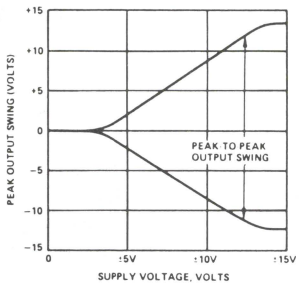


Figure 11. Op Amp output Swing vs Power Supply

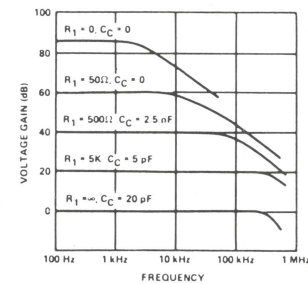


Figure 12. Op Amp Frequency Response

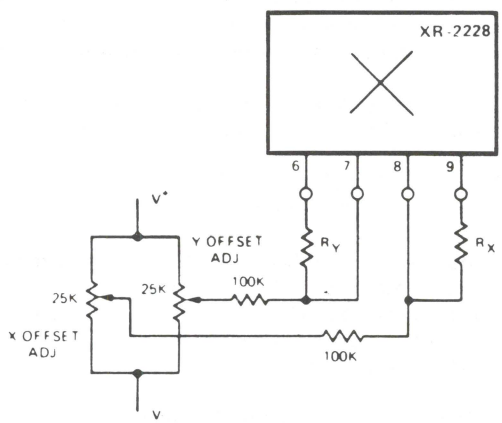


Figure 13. Offset Adjustment

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (Pins 2, 3, 4 and 5): These four terminals provide the differential inputs to the X- and Y-sections of the multiplier, respectively. The output will be a linear product of the two voltages, Vx and Vy, applied differentially across pins (2,3) and (4,5). Typical input bias current at the multiplier inputs is approximately 3μA, for each of the four inputs. In circuit applications requiring single-ended, rather than differential, input signals, pins 3 and 4 can be shorted together and connected to a common bias point.

MULTIPLIER OUTPUTS (Pins 1 and 16): The differential output voltage, V_o, across these terminals is proportional to the linear product of voltages V_x and V_y applied to the inputs. V_o can be expressed as:

$$V_o \approx \left(\frac{25}{R_x R_y}\right)\left(V_x V_y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_x and R_y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 16 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_z, is then obtained from the op amp output at pin 11, as shown in Figures 14 and 15.

X AND Y GAIN ADJUST (Pins 6, 7, 8, 9): The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_x and R_y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y} \text{ (volts)}^{-1}$$

where R_x and R_y are in kΩ.

X AND Y OFFSET ADJUST (Pins 7 and 8): Two of the gain- control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP INPUTS (Pins 13 and 14): Pin 13 is the non-inverting and pin 14 the inverting inputs for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 16). Note: When the op amp section is not used, these terminals should be grounded.

OP AMP COMPENSATION (Pin 12): The op amp section can be compensated for unconditional stability with a 20pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP OUTPUT (Pin 11): This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2228 output, with the op amp inputs being connected to the multiplier outputs.

APPLICATIONS INFORMATION

PART 1: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 14 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply 0V to both inputs and adjust the output offset to 0V using the output offset control.

2. Apply 20V p-p at 50Hz to the X-input and 0V to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.

3. Apply 20V p-p to the Y-input and 0V to the X-input. Trim X-offset adjust for minimum peak-to-peak output.

4. Repeat step 1.

5. Apply +10V to both inputs and adjust scale factor for V_o = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

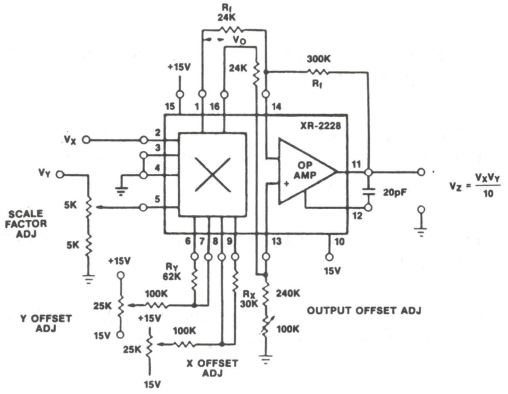


Figure 14. Multiplication Circuit

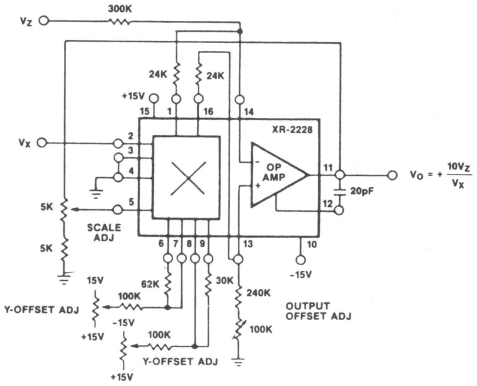


Figure 15. Dividing Circuit

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Figure 15. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_O = +10\ V_Z/V_X$ where $V_X < 0$ and V_Z can have either sign. Positive values of V_X are not allowed, since this will reverse the polarity of the feed- back loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2228, and is common to all analog division circuits. The divider circuit is trimmed as follows:

1. Apply $V_Z = 0$ and trim the output offset adjustment for constant output voltage as V_X is varied from –1V to –10V.

2. Keeping $V_Z = 0$, and applying $V_X = -10V$, trim the Y-offset adjust until $V_O = 0$.

3. Let $V_Z = V_X$ and/or $V_Z = -V_X$ and trim the X-offset adjustment for constant output voltage as V_X is varied from –1V to –10V.

4. If step 3 requires a large initial adjustment, repeat steps 1, 2 and 3.

5. Keeping $V_Z = V_X$, adjust the scale factor trim for V_O = –10V as V_X is varied from –1V to –10V.

PART II: ANALOG SIGNAL PROCESSING

Phase Detection

The multiplier section of the XR-2228 can be used as a linear phase-discriminator. A recommended circuit connection for this application is shown in Figure 16. In this case, the reference input (input 1) is applied to pin 2, and the input signal whose phase is to be detected (input 2) is applied to pin 5. For input signal amplitudes ≥ 50mV rms, the differential output voltage, V_O across pins 1 and 16 is directly proportional to the phase difference, ø, between the two input signals. It can be expressed as

$$V_o(\phi) = 5\left(\frac{2\phi}{\pi} - 1\right)$$

here ø is the phase difference expressed in radians. Even though the op amp is, in this application, not used, it is necessary to bias its inputs within their common mode range. This is easily accomplished in the phase detector circuit of pin 16 by tying pins 13 and 14 to pin 3 (which puts pins 13 and 14 at half supply).

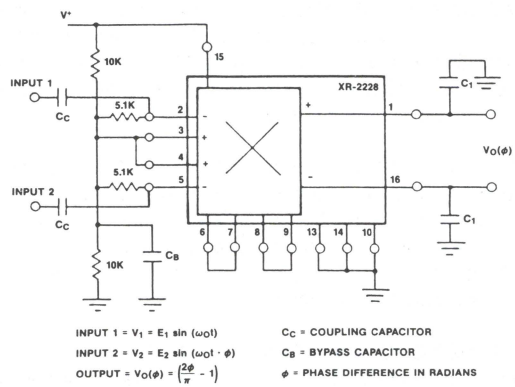


Figure 16. Phase-Detector Circuit

The capacitors C_1 at pins 1 and 16 provide a low-pass filter with a time constant $T_1 = R_1C_1$, where $R_1 = 5k\Omega$ is the international impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2228 to further amplify the output voltage, $V_o(\phi)$. The XR-2228 is suitable for phase detection of input frequencies up to 100MHz.

Synchronous AM Detection

Figure 17 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100MHz. The AM input signal is applied to the multiplier X- and Y-input terminals (pins 3 and 4) simultaneously.

The Y-gain terminals (pins 6 and 7) are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, and at pins 1 and 16 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

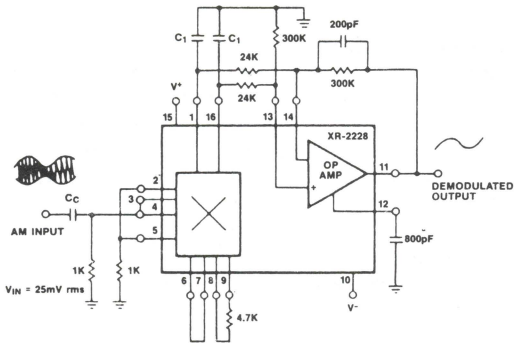


Figure 17. Synchronous AM Detector

Precision Phase-Locked Loop Design

A precision phase-locked loop may be constructed using an XR-2209 voltage controlled oscillator and the XR-2228. (See Figure 18.) Due to the excellent temperature stability and wide sweep range of the XR-2209 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2228 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30ppm/°C.

Triangle-to-Sinewave Conversion

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2228. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 2). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave.

For the component values shown in Figure 19, the recommended input signal level at pin 2 is ≅ 300mV pp, in order to obtain a 2V pp signal at pins 1 or 16, with R_X set at approximately 100Ω. The dc level at pin 5 can be used for adjusting the output amplitude, or providing amplitude modulation. The sensitivity of the output amplitude to the dc voltage level at pin 5 is inversely proportional to the external resistor across pins 6 and 7.

If higher amplitude output signal is required, the op amp section of XR-2228 can be used to provide additional amplification. If the op amp is not used, its inputs must be biased within common mode range to ensure proper device operation.

Phase-Locked AM Detection

The XR-2228 can be used in conjunction with any one of the commercially available monolithic phase-locked loop (PLL) IC's to provide phase-locked AM detection. In this manner, frequency-selective detection capabilities of PLL circuits can be extended to AM signals.

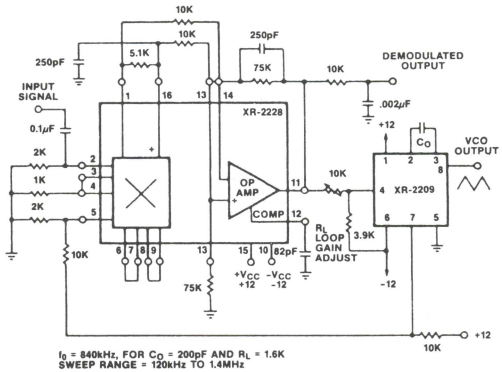


Figure 18. Precision PLL

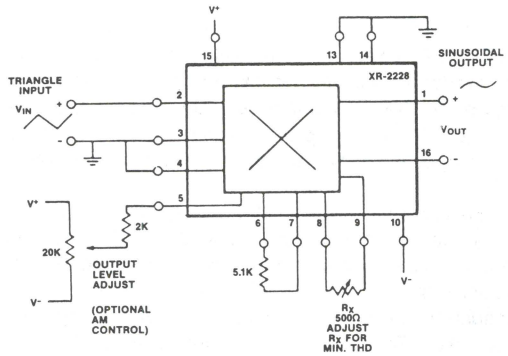


Figure 19. Triangle-to-Sinewave Converter

Figure 20 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit is useful as a phase-locked AM detector for carrier frequencies up to 20MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate "quadrature" output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (pins 13 and 14) of XR-215. The Y-input of the XR-2228 is operated with maximum gain, since the Y-gain control terminals (pins 6 and 7) are shorted together. This causes the triangular waveform across the timing capacitor, C_0, to be converted to an effective "quadrature" drive.

The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X-inputs of the XR-2228, are biased at approximated one-half of V_{CC}, by means of an external resistive divider.

In Figure 20, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier,

The Y-input of the XR-2228 is operated in its switching mode, with the Y-gain terminals (pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; the output of the multiplier, at pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal. In the circuit, R_X sets the amplifier demodulation gain, C_3 serves as the low-pass post-detection filter.

A detailed description of the circuit operation, and the design equations for calculating the external component values are given in Exar's Application Note AN-13, entitled "Frequency Selective AM Detection using Monolithic Phase-Locked Loops."

Phase-Locked Loop Tone Detection

The XR-2228 multiplier/detector can be used in conjunction with the XR-210 or the XR-215 high-frequency PLL circuits, to provide high-frequency tone or carrier-detect systems. The generalized circuit connection for such an application is given in Figure 21. The circuit, as shown, can operate with a single power supply, from 10V, to 20V, or with split supplies in the range of ±5V to ±10V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 21 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used and to the X-input terminal (pin 2) of the XR-2228.

The Y-inputs (pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at pins 13 and 14 of the PLL IC) which is AC coupled to pins 4 and 5 of the XR-2228 multiplier input. the differential DC voltage level at the multiplier output terminals (pins 1 and 16) is offset by means of an external resistor, R_A. This initial offset causes the op amp output of the XR- 2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 21, the op amp output (pin 11) would be at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (i.e., near $+V_{CC}$) when the PLL circuit is "locked" on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across pins 1 and 16 of the multiplier outputs, serves as the post- detection low-pass filter. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

A detailed description of the principle of operation of the circuit of Figure 21 is given in Exar's Application Note AN-12 entitled: "Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits".

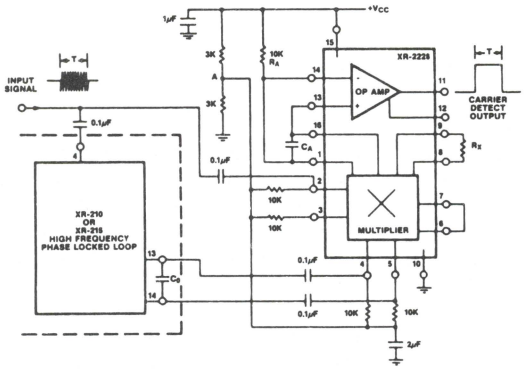


Figure 21. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone or Carrier-Detector Application

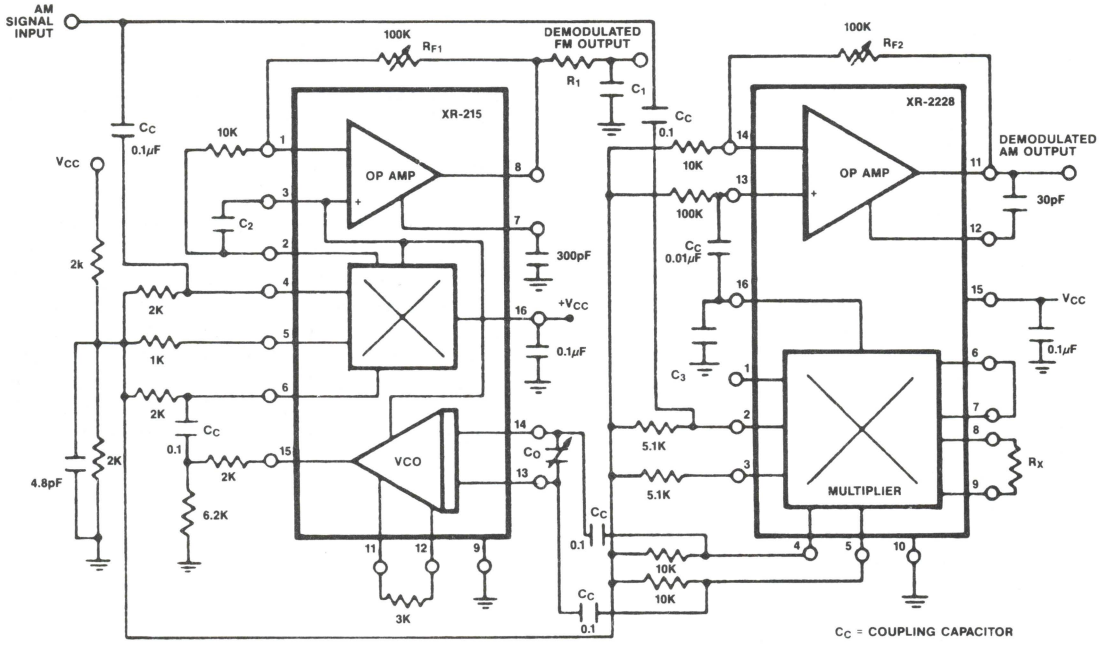


Figure 20. Phase-Locked AM Detection Using XR-215 Monolithic PLL and XR-2228 Multiplier/Detector

Monolithic Waveform Generator

GENERAL DESCRIPTION

The XR-205 is a highly versatile, monolithic waveform generator designed for diverse applications in communication and telemetry equipment, as well as in systems design and testing. It is a self-contained, totally monolithic signal generator that provides sine, square, triangle, ramp and sawtooth output waveforms, which can be both amplitude and frequency modulated.

The circuit has three separate sections: a voltage-controlled oscillator (VCO) which generates the basic periodic waveforms; a balanced modulator which provides amplitude or phase modulation; a buffer amplifier section which provides a low impedance output with high current drive capability.

FEATURES

High Frequency Operation
AM and FM Capabilities
Sine, Triangle, Square, Sawtooth, Ramp and Pulse Waveforms
Wide Supply Range 8V to 26V
Split Supply Capability

APPLICATIONS

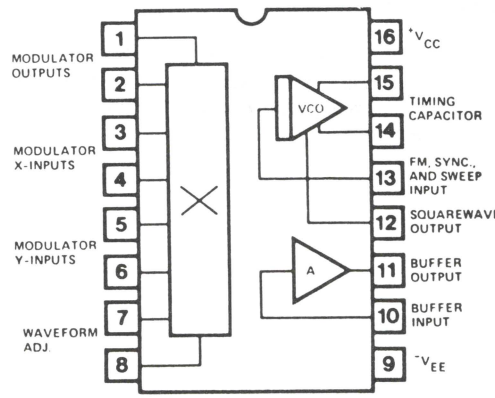
Waveform Generation
- Sinewave
- Triangle
- Square
- Sawtooth
- Ramp
- Pulse

AM Generation Double Sideband Suppressed Carrier
FM Generation
Sweep Generation
Tone Burst Generation
Simultaneous AM/FM
Frequency-Shift Keyed (FSK) Signal Generation
Phase-Shift Keyed (PSK) Signal Generation
On-Off Keyed Oscillation
Clock Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750mW
Derate above +25°C	6mW/°C
Temperature	
Storage	–65°C to + 150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-205	Ceramic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-205 is a high frequency monolithic function generator capable of sine, square, triangle, ramp, saw-tooth, and pulse waveforms with frequencies ranging to 4MHz. Operating frequency is determined by a single capacitor and may be externally swept over a 10:1 range. Duty cycle is variable from 10% to 90%. Amplitude modulation, up to 100%, is accomplished using the modulator X inputs (Pins 3 and 4). The on board buffer amplifier features 50Ω output resistance and 20mA output capability. The XR-205 operates with either single or split supplies.

ELECTRICAL SPECIFICATIONS

Test Conditions: Supply Voltage = 12V (single supply) T_A = 25°C, f = 10kHz, R_L = 3kΩ, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I — GENERAL CHARACTERISTICS					
Supply Voltage:					
Single Supply	8		26	Vdc	See Figure 1
Split Supply	±5		±13	Vdc	See Figures 2 and 3
Supply Current	8	10	12	mA	w/o buffer amp
Frequency Stability:					
Power Supply		0.2	0.5	%/V	$\|V_{CC}-V_{EE}\| > 10V$
Temperature		300	600	ppm/°C	Sweep input open circuit
Frequency Sweep Range	7:1	10:1			See Figure 7
Output Swing:					
Single Ended	2	3		Vpp	Measured at pin 1 or 2
Differenlial	4	6		Vpp	Measured across 1 and 2
Output Diff. Offset Voltage		0.1	0.4	Vdc	Measured across 1 and 2
Amplitude Control Range		60		dB	Controlled by R_q (see Figure 1)
Buffer Amplifier Output Resistance		50		ohms	R_L = 750Ω
Output Current Swing	±6	±10		mA	
II — Output Waveforms					
Sinusoidal:					
Upper Frequency Limit	2	4		MHz	Measured at Pin 11
Peak Output Swing	2	3		Vpp	S_1, S_3 closed. S_2 open
Distortion (THD)		2.5	4	%	closed S_2 Open
Triangle:					
Peak Swing	2	4		Vpp	Measured at Pin 11
Non-Linearity		±1		%	S_1, S_2 open, S_3 closed
Asymmetry		±1		%	f = 10kHz
Sawtooth:					
Peak Swing	2	3		Vpp	See Figure 1, S_2 closed;
Non-Linearity		1.5		%	S_2 and S_3 Closed
Ramp:					
Peak-Swing	1	1.4		Vpp	See Figure 1, S_2 and S_3 open
Non-Linearity		1		%	pin 10 connected to pin 15
Squarewave (Low Level):					
Output Swing	0.5	0.7		Vpp	See Figure 1, S_2 and S_3 Open,
Duty Cycle Asymmetry		±1	±4	%	pin 10 connected to pin 12
Rise Time		20		ns	10pF connected from pin 11
Fall Time		200		ns	to ground
Squarewave (High Level):					
Peak Swing	2	3		Vpp	See Figure 3, S_2 Open
Duty Cycle Asymmetry		±1	±4	%	
Rise Time		80		ns	10pF connected from pin 11
Fall Time		60		ns	to ground
Pulse Output:	2	3		Vpp	See Figure 3, S_2 closed
Peak Swing	2	3		Vpp	See Figure 3, S_2 closed
Rise Time		80		ns	
Fall Time		60		ns	
Duty Cycle Range		20-80		%	Adjustable (see Figure 6)
III — Modulation Characteristics (sine, triangle and squarewave):					
Amplitude Modulation:					
Double Sideband					
Modulation Range		0-100		%	See Figure 2 S_3 dosed
Linearity		0.5		%	for 30% modulation
Sideband Symmetry		1.0		%	
Suppressed Carrier					
Carrier Suppression		52		dB	f < 1MHz after R_q adjustment
Frequency Modulation:					
Distortion		0.3		%	See Figure 2 (±10 frequency deviations)

TEST CIRCUITS

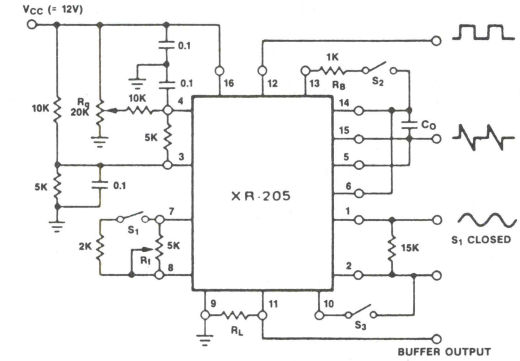


Figure 1. Test Circuit for Single-Supply Operation

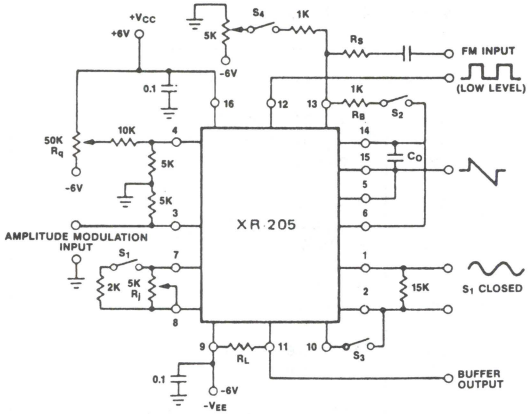


Figure 2. Test Circuit for Split-Supply Operation and AM/FM Modulation

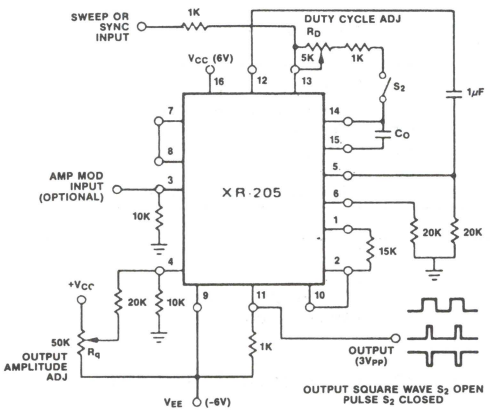


Figure 3. Test Circuit for High-Level Pulse and Squarewave Output

DESCRIPTION OF CIRCUIT CONTROLS

(Refer to functional block diagram)

TIMING CAPACITOR (PINS 14 AND 15)

The oscillator frequency is inversely proportional to the value of the timing capacitor, C_o, connected between pins 14 and 15. With the sweep input open circuited, frequecy f_o can be approximated as: $f_o = 400/C_o$ where f_o is in Hz and C_o is in microforads. (See Figure 4.)

MODULATOR Y-INPUTS (PINS 5 AND 6)

These inputs are normally connected to the oscillator outputs. For sinewave or trianglewave outputs, they are dc coupled to pins 14 and 15 (see Figure 1); for high-level squarewave or pulse output, ac coupling is used as shown in Figure 3.

MODULATOR X-INPUTS (PINS 3 AND 4)

Modulator output (at pins 1 or 2) is proportional to a dc voltage applied across these inputs — (see Figure 5). These inputs can be used for amplitude modulation or, as an output amplitude control. The phase of the output voltage is reversed if the polarity of the dc bias across pins 3 and 4 is reversed; therefore these inputs can be used for phase-shift keyed (PSK) modulation.

MODULATOR OUTPUTS (PINS 1 AND 2)

All of the high level output waveforms are obtained at these terminals. The output waveforms appear differentially between pins 1 and 2. The terminals can, therefore, be used for either in-phase or out-of-phase outputs. Normally, a 15KΩ load resistor should be connected between these terminals to prevent the output from saturating or clipping at large output voltage swings. This output has a high output impedance and should be buffered.

LOW LEVEL SQUAREWAVE OUTPUT (PIN 12)

The output at this pin is a symmetrical squarewave with 0.7V amplitude and 20 ns rise time. It can be used directly as an output waveform, or amplified to a 3Vpp signal level using the modulator section of the XR-205 as an amplifier (see Figure 3).

SWEEP OR FM INPUT (PIN 13)

The oscillator frequency increases linearly with an increasing negative voltage, V_s, applied to this terminal. Normally a series resistor, R_s ($R_s \approx$ approx. 1 KΩ) is connected in series with this terminal to provide current limiting and linear voltage-to-frequency transfer characteristics. The frequency deviation (for any given modulation level) is inversely proportional to R_s. Typical sweep characteristics of the circuit are shown in Figure 7. For proper operation of the circuit with R_s = 1KΩ, the sweep voltage, V_s, must be within range: $(V_{so} - 6) < V_s < (V_{so} + 1)$ where V_{so} is the open circuit voltage at pin 13.

WAVEFORM ADJUSTMENT (PINS 7 AND 8)

The shape of the output waveform at pins 1 and 2 is controlled by a potentiometer, R_j, connected between these terminals as shown in Figure 1. For sinewave outputs at pins 1 and 2, the value of R_j is adjusted to minimize the harmonic content of the output waveform. This adjustment is independent of frequency and needs to be done only once. The output can be converted to a symmetrical triangle waveform by increasing the effective resistance across these terminals. This can be done without changing the potentiometer setting, by opening the switch S_2 as shown in Figures 1-3.

BUFFER INPUT AND OUTPUT (PINS 10 AND 11)

The buffer amplifier can be connected to any of the circuit outputs (pins 1, 2, 12, 14 or 15) to provide low output impedance and high current drive capability. For proper operation of the buffer amplifier, pin 11 must be connected to the most negative potential in the circuit, with an external load resistor R_L (0.75KΩ < R_L < 10KΩ). The maximum output current at this pin must not exceed 20mA.

DUTY CYCLE ADJUSTMENT

The duty-cycle of the output waveforms can be adjusted by connecting a resistor RB across pins 13 and 14, as shown in Figures 1-3. With switch S_2 open, the output waveform will be symmetrical. Duty cycle is reduced as R_B is decreased. (See Figure 6.)

ADDITIONAL GAIN CONTROL

For amplitude modulated output signals, the dc level across pins 3 and 4 is fixed by the modulation index required. In this case, the output amplitude can be controlled without effecting the modulation by connecting a potentiometer between pins 1 and 2.

ON-OFF KEYING

The oscillator can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_s = 1KΩ, oscillations will stop if the applied potential at pin 13 is raised 3 volts above its open-circuit value.

OUTPUT WAVEFORMS

TRIANGLE OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switches S_1 and S_2 open.

SINEWAVE OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switch S_2 open and S_1 closed. The output waveform is adjusted for minimum harmonic distortion using trimmer resistor R_j connected across pins 7 and 8. Sinusoidal output is obtained from pins 1 or 2 (or pin 11 if the buffer amplifier is used). The amplitude of the output waveform is controlled by the differential dc voltage appearing between pins 3 and 4. This bias can be controlled by potentiometer R_q. for a differential bias between these terminals of 12 volts or greater, the output amplitude is maximum and equal to approximately 3Vp-p.

SAWTOOTH OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switch S_1 open and S_2 closed. Closing S_2 places resistor R_B across pins 13 and 14. This changes the duty cycle of the triangle output and converts it to a saw-tooth waveform. The polarity of the sawtooth can be changed by reversing the polarity of the dc bias across pins 3 and 4. If S_1 is closed, the linear sawtooth waveform is converted to the sinusoidal sawtooth waveform of Figure 9.

Ramp Output (Figure 9B)

For ramp outputs, switch S_3 of Figure 1 or 2 is opened, and pin 10 is shorted to pin 14. This results in a 1.4Vp-p ramp output at pin 11. The duty cycle of this ramp can be controlled by connecting R_B across pins (13-14) or (13-15).

Squarewave and Pulse Outputs

For squarewave outputs, the circuit is connected as shown in Figure 3, with S_2 open. The output can be converted to a pulse by closing S_2. The duty cycle of the pulse output is controlled by potentiometer R_D. The amplitude and polarity of either the pulse or squarewave output can be controlled by potentiometer R_q.

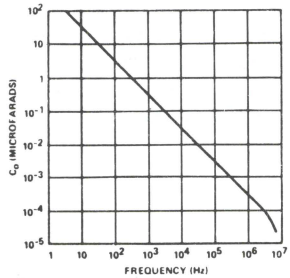


Figure 4. Frequency as a Function of C_o across Pins 14 and 15

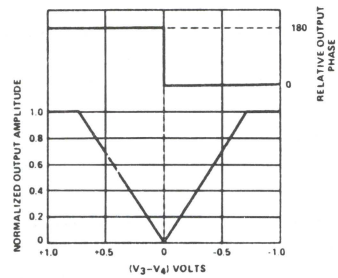


Figure 5. Modular Section Phase and Amplitude Transfer Characteristics

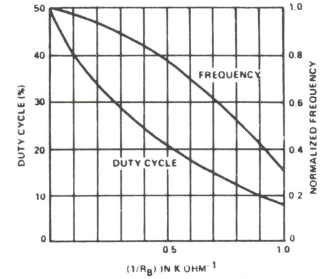


Figure 6. Duty-Cycle and Frequency Variation as a Function of Resistor R_B Connected Across Pins 13 and 14

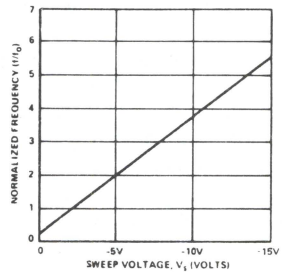
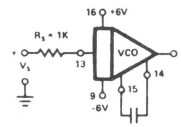


Figure 7. Normalized Frequency vs. Sweep Voltage



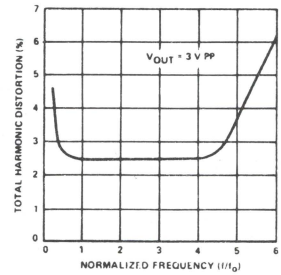


Figure 8. Sinusoidal Output Distortion as a Function of Frequency Sweep

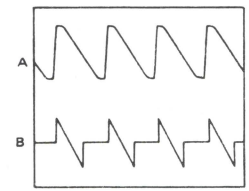
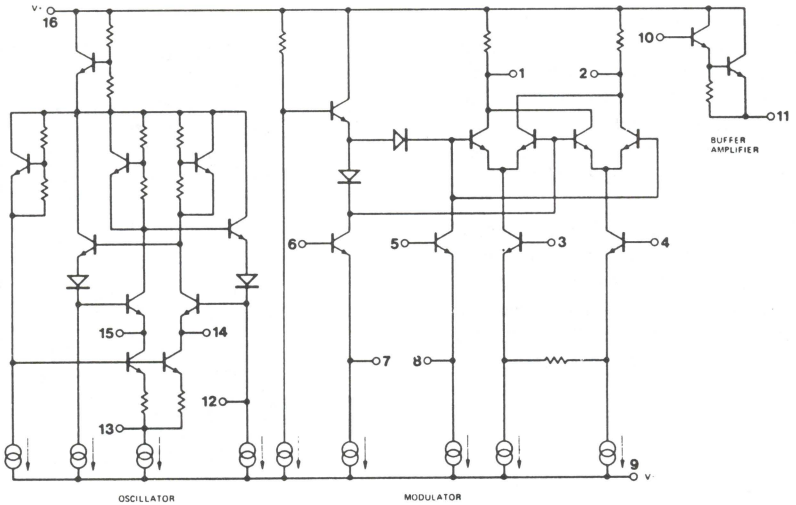


Figure 9. Sinusoidal Sawtooth and Linear Ramp Outputs

EQUIVALENT SCHEMATIC DIAGRAM



Monolithic Function Generator

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

FEATURES

Low-Sine Wave Distortion	0.5%, Typical
Excellent Temperature Stability	20ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Low-Supply Sensitivity	0.01%V, Typical
Linear Amplitude Modulation	
TTL Compatible FSK Controls	
Wide Supply Range	10V to 26V
Adjustable Duty Cycle	1% to 99%

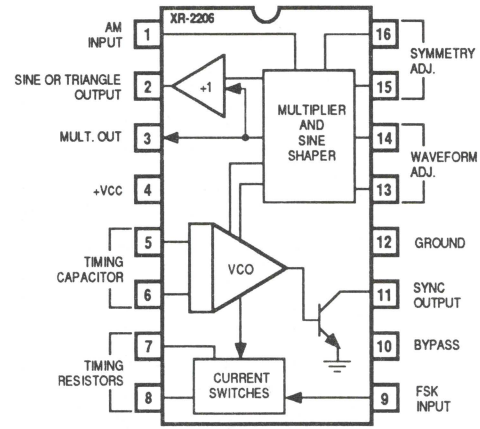
APPLICATIONS

Waveform Generation
Sweep Generation
AM/FM Generation
V/F Conversion
FSK Generation
Phase-Locked Loops (VCO)

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750mW
Derate Above 25°C	5mW/°C
Total Timing Current	6mA
Storage Temperature	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	–55°C to +125°C
XR-2206N	Ceramic	0°C to +70°C
XR-2206P	Plastic	0°C to +70°C
XR-2206CN	Ceramic	0°C to +70°C
XR-2206CP	Plastic	0°C to +70°C
XR-2206D	JEDEC SOIC	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = 12V$, $T_A = 25°C$, $C = 0.01\mu F$, $R_1 = 100k\Omega$, $R_2 = 10k\Omega$, $R_3 = 25k\Omega$ unless otherwise specified. S_1 open for triangle, closed for sine wave.

PARAMETERS	XR-2206M			XR2206C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	±5		113	15		113	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10k\Omega$
OSCILLATOR SECTION								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000pF$, $R_1 = 1k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\mu F$, $R_1 = 2M\Omega$
Frequency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability Frequency		110	±50		±20		ppm/°C	$0°C \leq T_A \leq 70°C$
								$R_1 = R_2 = 20k\Omega$
Sine Wave Amplitude Stability		4800			4800		ppm/°C	See Note 2.
Supply Sensitivity		0.01	0.1		0.01		%/V	$V_{LOW} = 10V$, $V_{HIGH} = 20V$,
								$R_1 = R_2 = 20k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ $R_1 = 1k\Omega$
								f_L @ $R_1 = 2M\Omega$
Sweep Linearity								
10:1 Sweep		2			2		%	$f_L = 1kHz$, $f_H = 10kHz$
1000:1 Sweep		8			8		%	$f_L = 100kHz$, $f_H = 100kHz$
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	µF	See Figure 4.
Timing Resistors: R_1 & R_2	1		2000	1		2000	kΩ	
Triangle Sine Wave Output								See Note 1, Figure 2.
Triangle Amplitude		160			160		mV/kΩ	Figure 1, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/kΩ	Figure 1, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	$R_1 = 30k\Omega$
With Adjustment		0.4	1.0		0.5	1.5	%	See Figures 6 and 7.
Amplitude Modulation								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		nsec	$C_L = 10pF$
Fall Time		50			50		nsec	$C_L = 10pF$
Saturation Voltage		0.2	0.4		0.2	0.6	V	$I_L = 2mA$
Leakage Current		0.1	20		0.1	100	µA	$V_{11} = 26V$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 2.

Note 2: For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

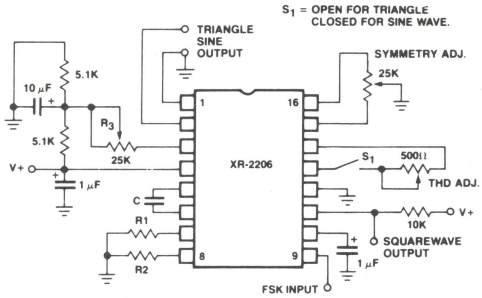


Figure 1. Basic Test Circuit.

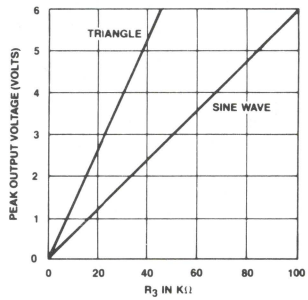


Figure 2. Output Amplitude as a Function of the Resistor, R_3, at Pin 3.

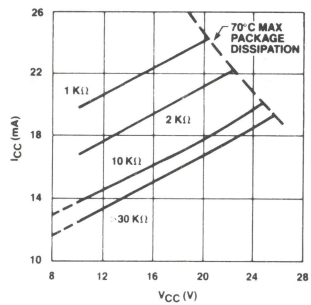


Figure 3. Supply Current vs Supply Voltage, Timing, R.

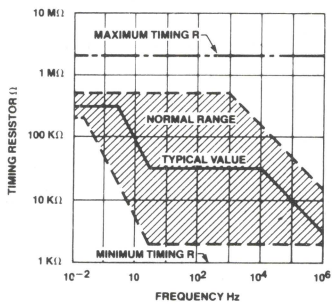


Figure 4. R vs Oscillation Frequency.

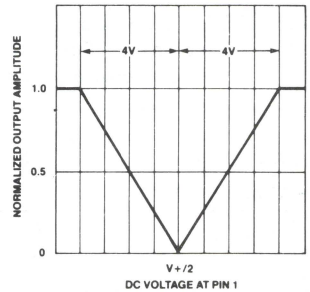


Figure 5. Normalized Output Amplitude vs DC Bias at AM Input (Pin 1).

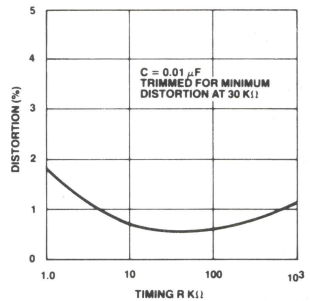


Figure 6. Trimmed Distortion vs Timing Resistor

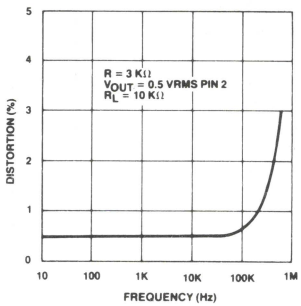


Figure 7. Sine Wave Distortion vs Operating Frequency with Timing Capacitors Varied.

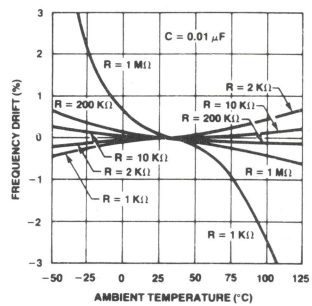


Figure 8. Frequency Drift vs Temperature.

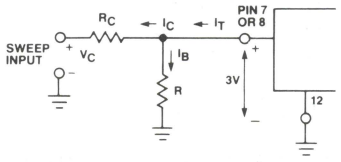


Figure 9. Circuit Connection for Frequency Sweep

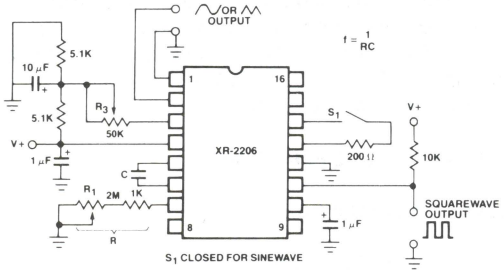


Figure 10. Circuit tor Sine Wave Generation without External Adjustment. (See Figure 2 for Choice of R_3)

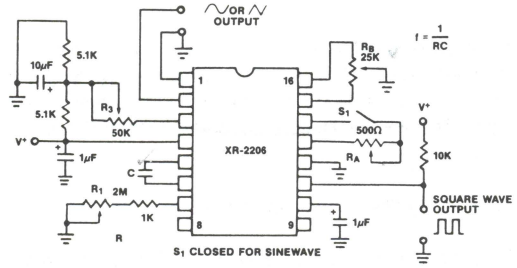


Figure 11. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing — See Figure 2)

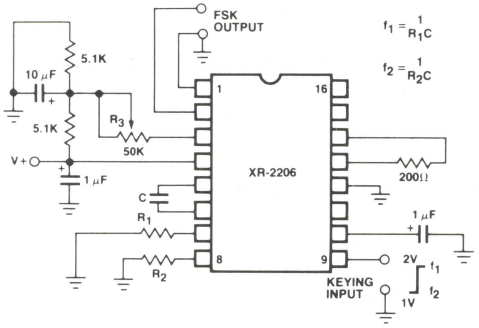


Figure 12. Sinusoidal FSK Generator

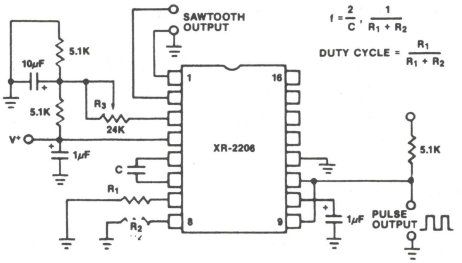


Figure 13. Circuit for Pulse and Ramp Generation

Frequency-Shift Keying:

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in Figure 12. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage ≥ 2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is ≤ 1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels. f_1 and f_2, as:

$$f_1 = 1/R_1C \text{ and } f_2 = 1/R_2C$$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-.

Output DC Level Control:

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In Figures 10, 11 and 12, Pin 3 is biased midway between V+ and ground, to give an output dc level of ≈ V+/2.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment:

Figure 10 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than V+/2, and the typical distortion (THD) is < 2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 10 can be converted to split-supply operation, simply by replacing all ground connections with V−. For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to –0.5% by additional adjustments as shown in Figure 11. The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of Figures 10 and 11 can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 12 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V−.

Pulse and Ramp Generation

Figure 13 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1kΩ to 2MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in Figure 4. Temperature stability is optimum for 4kΩ < R < 200kΩ. Recommended values of C are from 1000pF to 100μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320\ I_T\ (\text{mA})}{C\ (\mu\text{F})} \text{ Hz}$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with I_T, over a wide range of current values, from 1μA to 3mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in Figure 9. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right) \text{Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f/\partial V_C = -\frac{0.32}{R_C C} \quad Hz/V$$

CAUTION: For safety operation of the circuit, I_T should be limited to ≤ 3mA.

Output Amplitude:

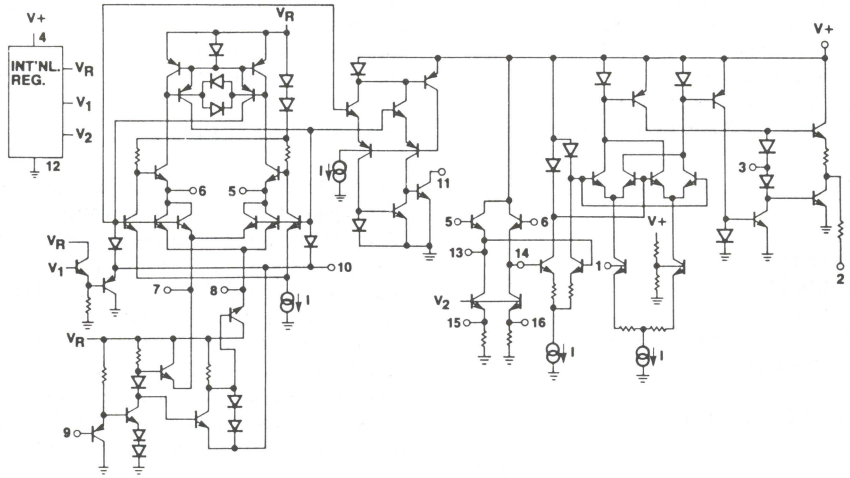
Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see Figure 2). For sine wave output, amplitude is approximately 60mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160mV peak per kΩ of R_3. Thus, for example, R_3 = 50kΩ would produce approximately 13V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within 14 volts of V+/2 as shown in Figure 5. As this bias level approaches V+/2, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55dB.

CAUTION: AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of V+.

EQUIVALENT SCHEMATIC DIAGRAM



Voltage-Controlled Oscillator

GENERAL DESCRIPTION

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01Hz to 1MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

The XR-2207 has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

FEATURES

Excellent Temperature Stability (20ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (3000:1 Typical)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (14V to 113V)
Low Supply Sensitivity (0.1% /V)
Wide Frequency Range (0.01Hz to 1MHz)
Simultaneous Triangle and Squarewave Outputs

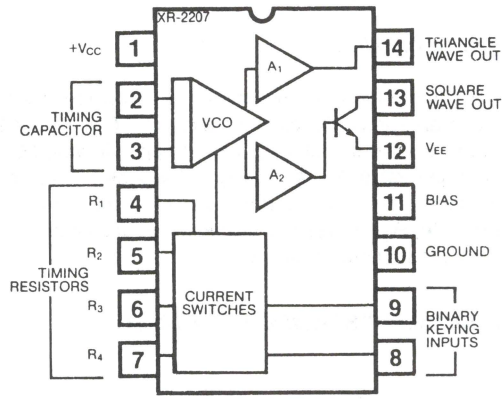
APPLICATIONS

FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750mW
Derate above +25°C	6.0mW/°C
Plastic package	625mW
Derate above +25°C	5mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2207M	Ceramic	–55°C to +125°C
XR-2207N	Ceramic	0°C to +70°C
XR-2207P	Plastic	0°C to +70°C
XR-2207CN	Ceramic	0°C to +70°C
XR-2207CP	Plastic	0°C to +70°C
XR-2207D	JEDEC SOL-16	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2207 utilizes four main functional blocks for frequency generation. These are a voltage controlled oscillator (VCO), four current switches which are activated by binary keying inputs, and two buffer amplifiers for triangle and squarewave outputs. The VCO is actually a current controlled oscillator which gets its input from the current switches. As the output frequency is proportional to the input current, the VCO produces four discrete output frequencies. Two binary input pins determine which timing currents are channelled to the VCO. These currents are set by resistors to ground from each of the four timing terminals.

The triangle output buffer provides a low impedance output (10Ω TYP) while the squarewave is an open-collector type. A programmable reference point allows the XR-2207 to be used in either single or split supply configurations.

ELECTRICAL CHARACTERISTICS

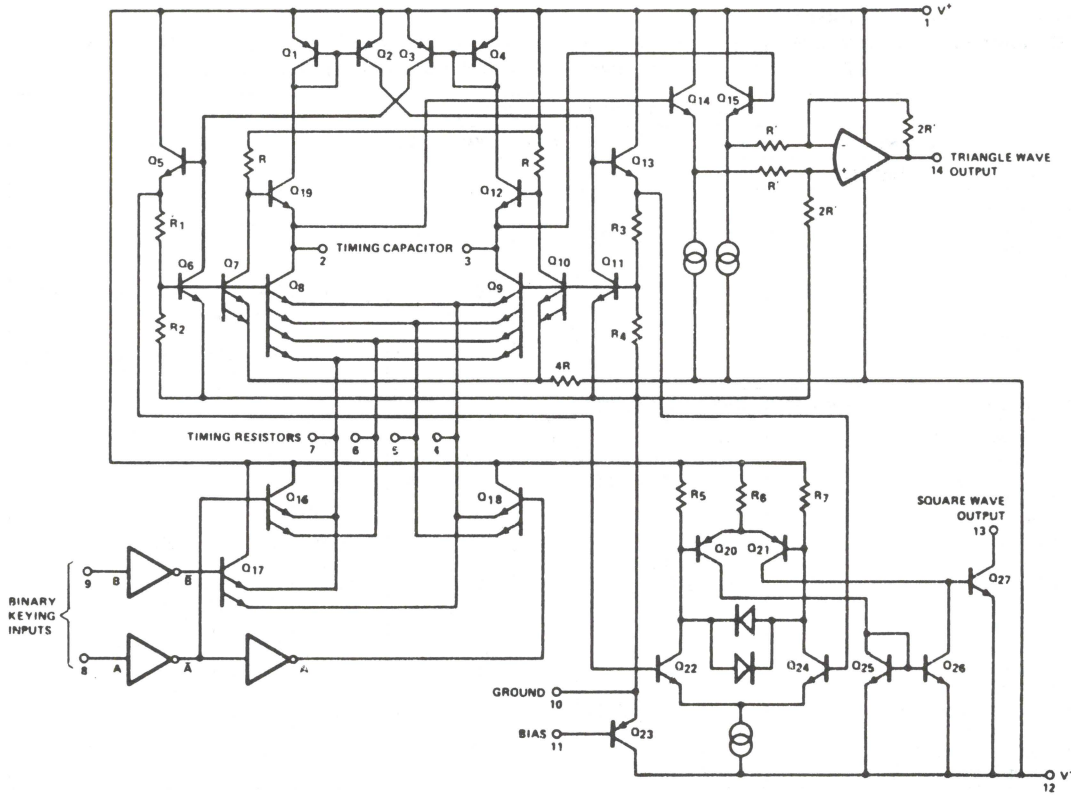
Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, $C = 5000pF$, $R_1 = R_2 = R_3 = R_4 = 20k\Omega$, $R_L = 4.7k\Omega$, Binary Inputs grounded, S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2207/XR-2207M			XR2207C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	8		26	8		26	V	See Figure 3
Split Supplies	±4		±13	±4		±13	V	
Supply Current								
Single Supply		5	7		5	8	mA	Measured at pin 1, S_1 and S_2 open See Figure 2
Split Supplies								
Positive		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	7	mA	Measured at pin 12, S_1, S_2 open
OSCILLATOR SECTION — FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	C = 500pF, R_3 = 2KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50µF, R_3 = 2MΩ
Frequency Accuracy		±1	±3		±1	±5	% of f_o	
Frequency Matching		0.5			0.5		% of f_o	
Frequency Stability								
Temperature		20	50		30		ppm/°C	0°C < T_A < 70°C
Power Supply		0.15			0.15		%N	
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	R_3 = 1.5 KΩ for f_{H1} R_3 = 2MΩ for f_L
Sweep Linearity							%	C = 5000pF
10:1 Sweep		1	2		1.5			f_H= 10kHz, f_L= 1kHz
1000:1 Sweep		5			5			f_H= 100kHz, f_L= 100Hz
FM Distortion		0.1			0.1		%	110% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	KΩ	See Characteristic Curves
Impedance at Timing Pins		75			75		Ω	Measured at pins 4, 5, 6, or 7
DC Level at Timing Terminals		10			10		mV	
BINARY KEYING INPUTS								
Switching Threshold	1.4	2.2	2.8	1.4	2.2	2.8	V	Measured at pins 8 and 9, Referenced to pin 10
Input Impedance		5			5		kΩ	
OUTPUT CHARACTERISTICS								
Triangle Output								Measured at pin 13
Amplitude	4	6		4	6		Vpp	
Impedance		10			10		Ω	
DC Level		+100			+100		mV	Referenced to pin 10
Linearity		0.1			0.1		%	From 10% to 90% to swing
Squarewave Output								Measured at pin 13, S_2 closed
Amplitude	11	12		11	12		Vpp	
Saturation Voltage		0.2	0.4		0.2	0.4	V	Referenced to pin 12
Rise Time		200			200		nsec	$C_L \leq 10pF$
Fall Time		20			20		nsec	$C_L \leq 10pF$

PRECAUTIONS

The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely affect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pins 4, 5, 6, and 7 be limited to ≤ 6mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10mA.
2. Terminals 2, 3, 4, 5, 6, and 7 have very low internal impedance and should, therefore, be protected from ages.
3. The keying logic pulse amplitude should not exceed the supply voltage.



EQUIVALENT SCHEMATIC DIAGRAM

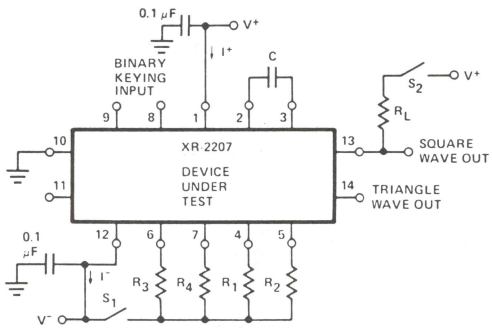


Figure 1. Test Circuit For Split Supply Operation

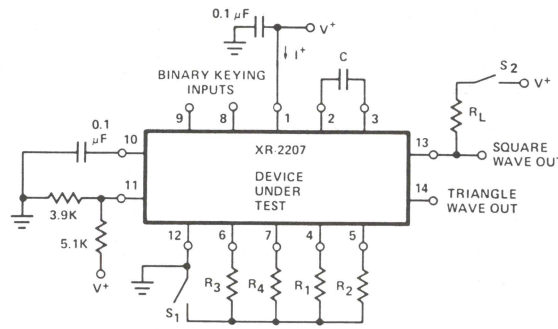


Figure 2. Test Circuit For Single Supply Operation

PRINCIPLES OF OPERATION

Timing Capacitor (Pins 2 and 3)

The oscillator frequency is inversely proportional to the timing capacitor, C, as indicated in Figure 8. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100pF to 100μF. The capacitor should be non-polar.

Timing Resistors (Pins 4, 5, 6, and 7)

The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 2KΩ to 2MΩ; however, for optimum temperature and power supply stability, recommended values are 4KΩ to 200KΩ (see Figures 4, 5, and 7). To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1μF capacitors.

Supply Voltage (Pins 1 and 12)

The XR-2207 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced (see Figures 3 and 4). Performance is optimum for ±6V, or 12V single supply operation.

Binary Keying Inputs (Pins 8 and 9)

The internal impedance at these pins is approximately 5KΩ. Keying levels are < 1.4V for "zero" and > 3V for "one" logic levels referenced to the dc voltage at pin 10 (see Figure 8).

Bias for Single Supply (Pin 11)

For single supply operation, pin 11 should be externally biased to a potential between V+/3 and V+/2 volts (see Figure 2). The bias current at pin 11 is nominally 5% of the total oscillation timing current, I_T.

Ground (Pin 10)

For split supply operation, this pin serves as circuit ground. For single supply operation. pin 10 should be ac grounded through a 1μF bypass capacitor. During split supply operation, a ground current of $2I_T$ flows out of this terminal, where I_T is the total timing current.

Squarewave Output (Pin 13)

The squarewave output at pin 13 is a "open-collector" stage capable of sinking up to 20mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1KΩ to 100KΩ.

Triangle Output (Pin 14)

The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits.

Bypass Capacitors

The recommended value for bypass capacitors is 1μF, although larger values are required for very low frequency operation.

Split Supply Operation

Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R_1 through R_4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in the logic table (Table 1). If a single timing resistor is activated, the frequency is 1/RC. Otherwise, the frequency is either $1/(R_1||R_2)C$ or $1/(R_3||R_4)C$.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5KΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of V+/2.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6 volt supplies. For operation with unequal supply voltages, see Figure 3.

Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

Single Supply Operation

The circuit should be interconnected as shown in Figure 11 for single supply operation. Pin 12 should be grounded, and pin 11 biased from V+ through a resistive divider to a value of bias voltage between V+/3 and V+/2. Pin 10 is bypassed to ground through a 1μF capacitor.

For single supply operation, the dc voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B. the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

For a fixed frequency of $f_3 = 1/R_3C$, the external circuit connections can be simplified as shown in Figure 11b.

Table 1
Logic Table for Binary Keying Controls

LOGIC LEVEL 8	LOGIC LEVEL 9	SELECTED TIMING PINS	FREQUENCY	DEFINITIONS
0	0	6	f_1	$f_1 = 1/R_3C$, $\Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C$, $\Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 = >3V

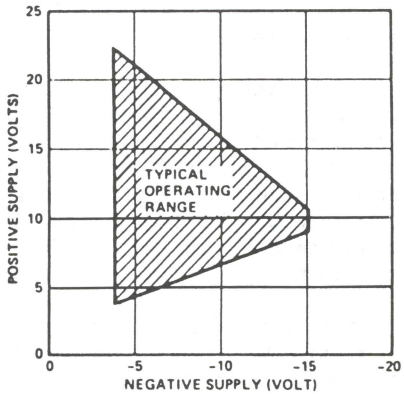


Figure 3. Typical Operating Range For Split Supply Voltage

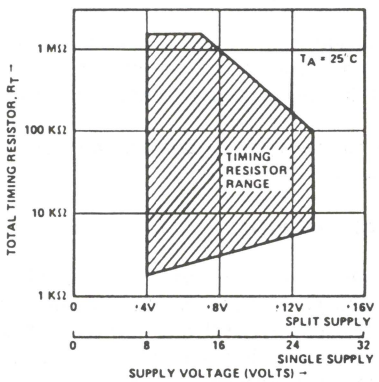


Figure 4. Recommended Timing Resistor Value vs. Power Supply Voltage*

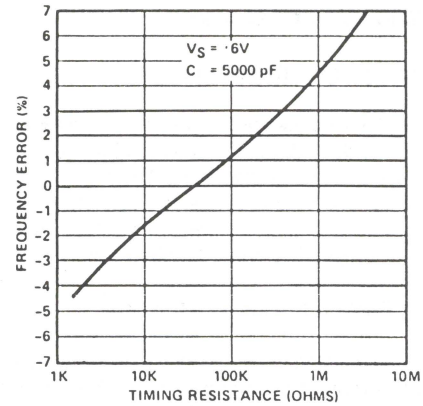


Figure 5. Frequency Accuracy vs. Timing Resistance

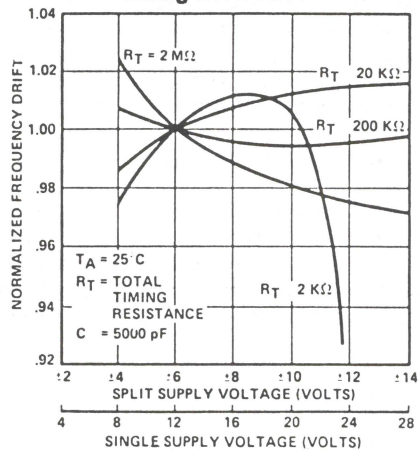


Figure 6. Frequency Drift vs. Supply Voltage

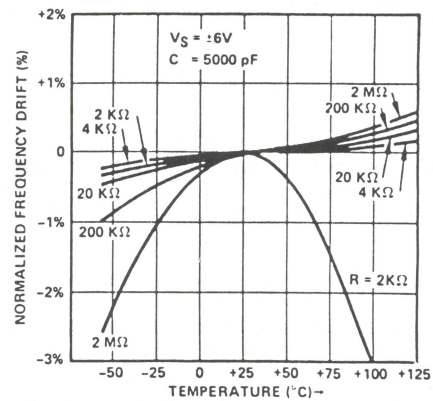


Figure 7. Normalized Frequency Drift with Temperature

LOGIC LEVEL A	B	SELECTED TIMING PINS	FRE-QUENCY	DEFINITIONS
0	0	6	f_1	$f_1 = 1/R_3C$, $\Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C$, $\Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 = >3V

Figure 8. Logic Table For Binary Keying Controls
Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

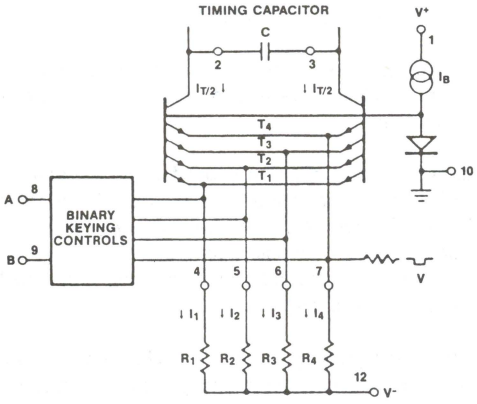


Figure 9. Simplified Schematic of Frequency Control Mechanism

Frequency Control (Sweep and FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figures 12 & 13.

For split supply operation, a negative control voltage, V_C, applied to the circuits of Figures 15 & 16 causes the total timing current, I_T, and the frequency, to increase,

As an example, in the circuit of Figure 12, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation, normally $f = \frac{1}{R_3C}$, is now proportional to the control voltage, V_C, and determined as:

$$f = \frac{1}{R_3C}\left[1 - \frac{V_C R_3}{R_C V^-}\ \text{Hz}\right]$$

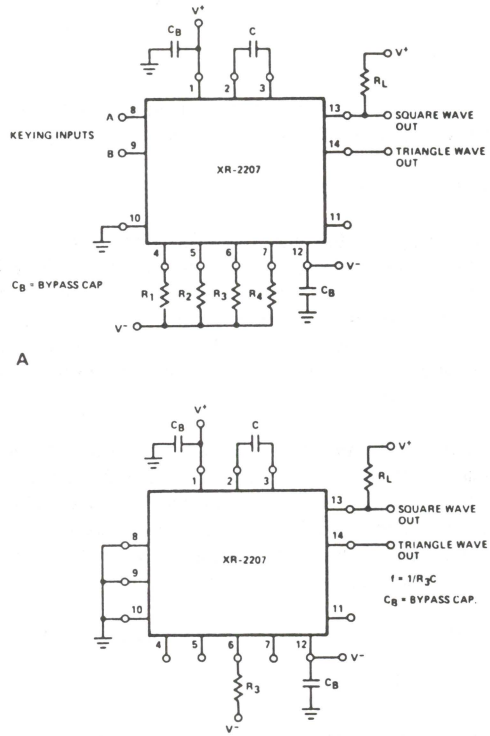


Figure 10. Split-Supply Operation:
(a) General
(b) Fixed Frequency

The frequency f will increase as the control voltage is made more negative. If R_3 = 2 MΩ, R_C = 2KΩ, C = 5000pF, then a 1000:1 frequency sweep would result for a negative sweep voltage $V_C \approx V^-$.

The voltage to frequency conversion gain, K, is controlled by the series resistance R_C and can be expressed as:

$$K = \frac{\Delta f}{\Delta V_C} = -\frac{1}{R_C C V^-}\ \text{Hz/volt}$$

The circuit of Figure 12 can operate both with positive and negative values of control voltage. However, for positive values of V_C with small (R_C/R_3) ratio, the direction of the timing current I_T is reversed and the oscillations will stop.

Figure 13 shows an alternate circuit for frequency control where two timing pins, 6 and 7, are activated. The frequency and the conversion gain expressions are the same as before, except that the circuit would operate only with negative values of V_C. For $V_C > 0$, pin 7 becomes deactivated and the frequency is fixed at $f = \frac{1}{R_3C}$.

Caution

For operation of the circuit, total timing current I_T must be less than 6mA over the frequency control range.

Duty Cycle Control

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 14 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0, 0" and the "1, 0" logic states given in Figure 11. Timing pin 5 is activated when the output is "high," and the timing pin is activated when the squarewave output goes to a low state.

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R_2}{R_2 + R_3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R_2 + R_3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R_2 and R_3 to a common control voltage V_C, instead of to V^- (see Figure 15). The sawtooth and the pulse output waveforms are shown in Figure 15.

On-Off Keying

The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1Hz) residual oscillations in the "off" state due to internal bias currents. If this effect is undesirable, it can be eliminated by connecting a 10MΩ resistor from pin 3 to V+.

Two-Channel FSK Generator (Modem Transmitter)

The multi-level frequency shift-keying capability of XR-2207 makes it ideally suited for two-channel FSK generation. A recommended circuit connection for this application is shown in Figure 16.

For two-channel FSK generation, the "mark" and "space" frequencies of the respective channels are determined by the timing resistor pairs (R_1, R_2) and (R_3–R_4). Pin 8 is the "channel-select" control in accord with Figure 11. For a "high" logic level at pin 8, the timing resistors R_1 and R_2 are activated. Similarly, for a "low" logic level, timing resistors R_3 and R_4 are enabled.

The "high" and "low" logic levels at pin 9 determine the respective high and low frequencies within the selected FSK channel.

Recommended component values for various commonly used FSK frequencies are given in Table 1. When only a single FSK channel is used, the remaining channel can be deactivated by connecting pin 8 to either V+ or ground. In this case, the unused timing resistors can also be omitted from the circuit.

The low and high frequencies, f_1 and f_2, for a given FSK channel can be fine tuned using potentiometers connected in series with respective timing resistors. In fine tuning the frequencies, f_1 should be set first with the logic level at pin 9 in a "low" level.

Typical frequency drift of the circuit for 0°C to 75°C operation is 10.2%. Since the frequency stability is directly related to the external timing components, care must be taken to use timing components with low temperature coefficients.

FSK Transceiver (Full-Duplex Modem)

The XR-2207 can be used in conjunction with the XR-210, FSK demodulator, to form a full-duplex FSK transceiver, or modem. A recommended circuit connection for this application is shown in Figure 20. Table 1 shows the recommended component values for 300-Baud (103-type) and 1200-Baud (202-type) Modem applications.

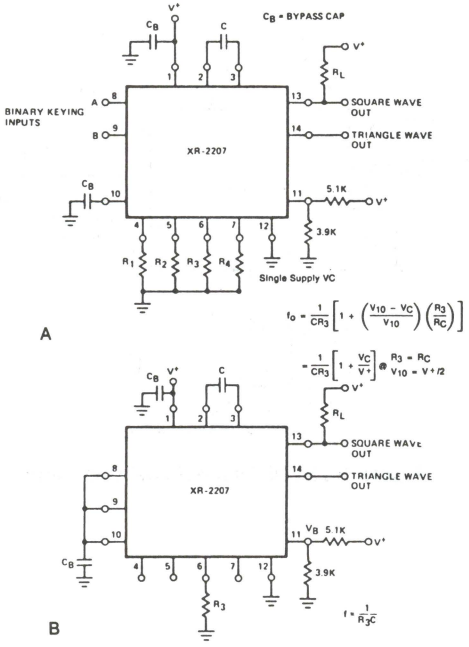


Figure 11. Single Supply Operation:
(a) General
(b) Fixed Frequency

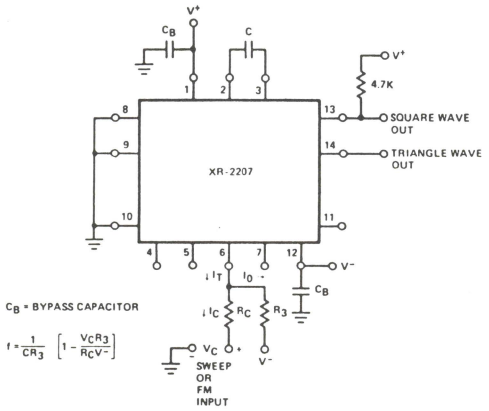


Figure 12. Frequency Sweep Operation

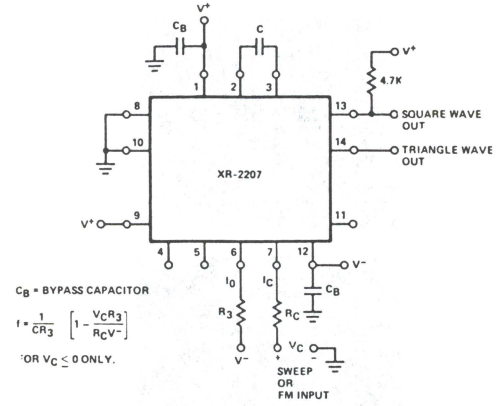


Figure 13. Alternate Frequency Sweep Operation

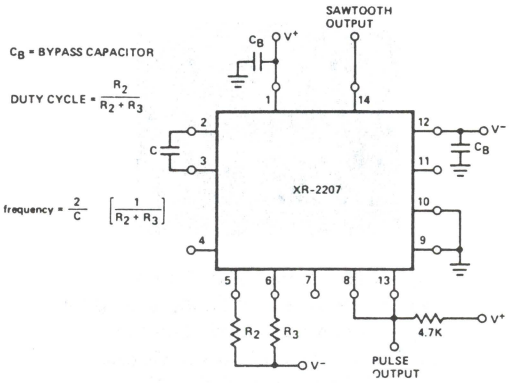


Figure 14. Sawtooth and Pulse Outputs

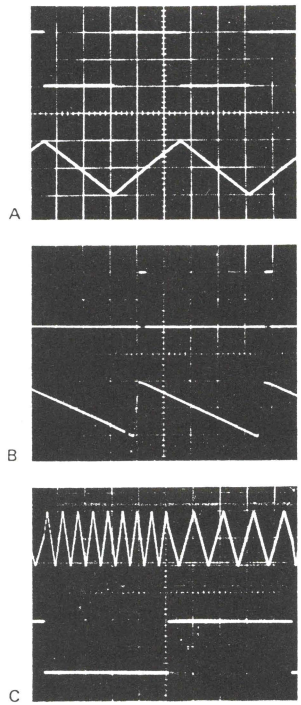


Figure 15. Output Waveforms:
(a) Squarewave and Triangle Outputs
(b) Pulse and Sawtooth Outputs
(c) Frequency-Shift Keyed Output
Top: FSK Output With $f_2 = 2f_1$
Bottom: Keying Logic Input

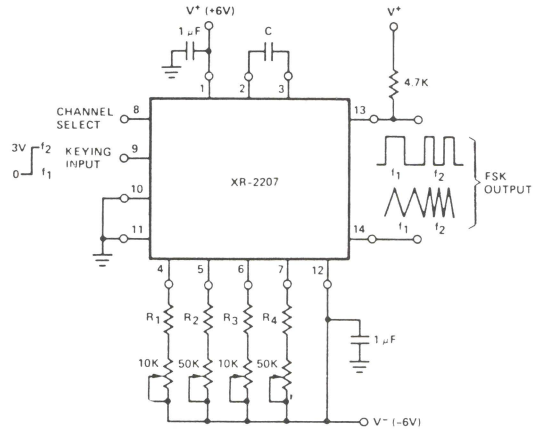


Figure 16. Multi-Channel FSK Generation

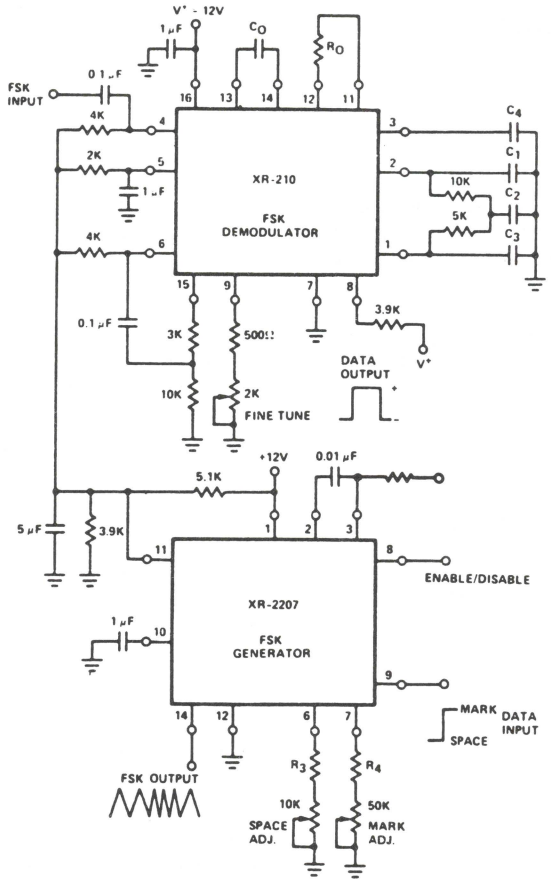


Figure 17. Full Duplex FSK Modem Using XR-210 and XR-2207 (See Table 1 For Component Values)

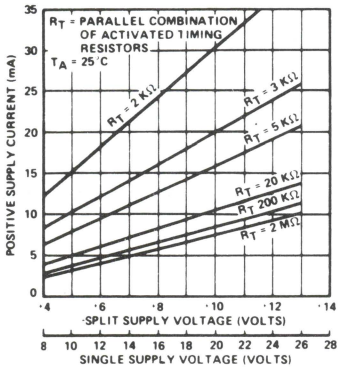


Figure 18. Positive Supply Current, I+ (Measured at Pin 1) vs. Supply Voltage

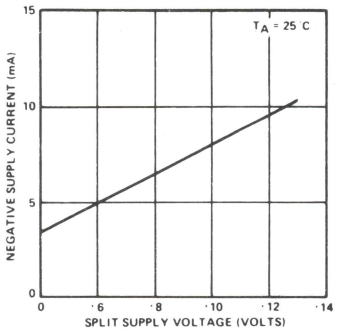


Figure 19. Negative Supply Current, I− (Measured at Pin 12) vs. Supply Voltage

***Note: R_T = Parallel Combination of Activated Timing Resistors**

Precision Oscillator

GENERAL DESCRIPTION

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01Hz to 1MHz. The frequency is set by an external RC product. It is ideally suited for frequency modulation, voltage to frequency or current to frequency conversion, sweep or tone generation as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR- 2208.

FEATURES

Excellent Temperature Stability (20ppm/°C)
Linear Frequency Sweep
Wide Sweep Range (1000:1 Min)
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01Hz to 1MHz)
Simultaneous Triangle and Squarewave Outputs

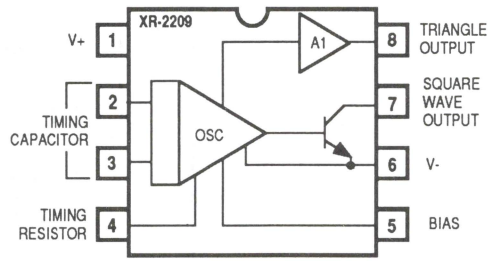
APPLICATIONS

Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (package limitation)	
Ceramic Package	385mW
Plastic Package	300mW
Derate above +25°C	8.3mW/°C
Operating Temperature Range	
XR-2209M	–55°C to +125°C
XR-2209C	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2209M	Ceramic	–55°C to + 125°C
XR-2209CN	Ceramic	0°C to + 70°C
XR-2209CP	Plastic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-2209 precision oscillator is comprised of three functional blocks: a variable frequency oscillator which generates the basic periodic waveforms and two buffer amplifiers for the triangle and the squarewave outputs. The oscillator frequency, set by an external capacitor, C, and the timing resistor, R, operates over 8 frequency decades, from 0.01Hz to 1MHz. With no sweep signal applied. the frequency of oscillation is equal to 1/RC.

The XR-2209 has a typical drift specification of 20ppm/°C. Its frequency can be linearly swept over a 1000:1 range with an external control signal. Output duty cycle is adjustable from less than 1% to over 99%. The device may operate from either single or split supplies from 8V to 26V (±4V to ±13V).

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, C = 5000pF, R – 20KΩ, $R_L = 4.7k\Omega$. S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2209M			XR2209C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	8		26	8		26	V	See Figure 2
Split Supplies	±4		±13	±4		±13	V	See Figure 1
Supply Current								
Single Supply		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open See Figure 2
Split Supplies								
Positive		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	7	mA	Measured at pin 4, S_1, S_2 open
OSCILLATOR SECTION — FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	C = 500pF, R = 2KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50µF, R = 2MΩ
Frequency Accuracy		±1	±3		±1	±5	% of f_o	
Frequency Stability								
Temperature		20	50		30		ppm/°C	0°C < T_T < 70°C*
Power Supply		0.15			0.15		%/V	
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	R =1.5KΩ for f_{H1} R = 2MΩ for f_L
Sweep Linearity							%	C = 5000 pF
10:1 Sweep		1	2		1.5			f_H = 10kHz, f_L = 1kHz
1000:1 Sweep		5			5			f_H = 100kHz, f_L = 100Hz
FM Distortion		0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	KΩ	See Characteristic Curves
Impedance at Timing Pin		75			7.5		Ω	Measured at pin 4
OUTPUT CHARACTERISTICS								
Triangle Output								Measured at pin 8
Amplitude	4	6		4	6		Vpp	
Impedance		10			10		Ω	
Linearity		0.1			0.1		%	10% to 90% of swing
Squarewave Output								Measured at pin 7, S_2 closed
Amplitude	11	12		11	12		Vpp	
Saturation Voltage		0.2	0.4		0.2	0.4	V	Referenced to pin 6
Rise Time		200			200		nsec	$C_L \leq$ 10pF, R_L = 4.7KΩ
Fall Time		20			20		nsec	$C_L \leq$ 10pF

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

PRECAUTIONS

The following precautions should be observed when operating the XR-2209 family of integrated circuits:

1. Pulling excessive current from the timing terminal will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pin 4 be limited to ≤ 6mA.

2. Terminals 2, 3, and 4 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.

3. Triangle waveform linearity is sensitive to parasitic coupling between the square and the triangle-wave outputs (pins 7 and 8). In board layout or circuit wiring care should be taken to minimize stray wiring capacitances between these pins.

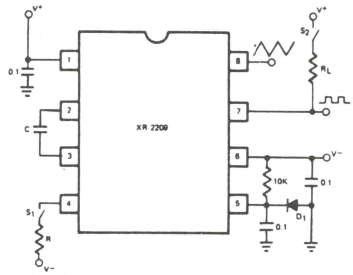


Figure 1. Test Circuit for Split Supply Operation (D_1 = 1N4148 or Equivalent)

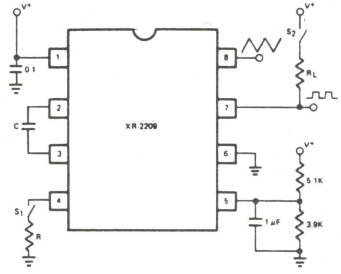


Figure 2. Test Circuit for Single Supply Operation

CHARACTERISTIC CURVES

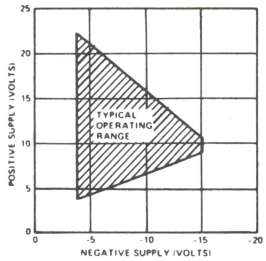


Figure 3. Typical Operating Range for Split Supply Voltage

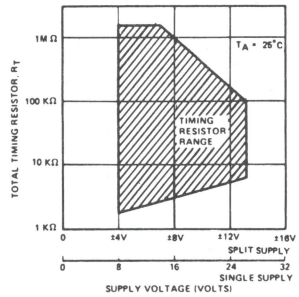


Figure 4. Recommended Timing Resistor Value vs. Power supply Voltage*

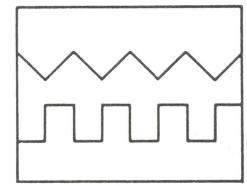


Figure 5. Output Waveforms Top: Triangle Output (Pin 8) Bottom: Squarewave Output (Pin 7)

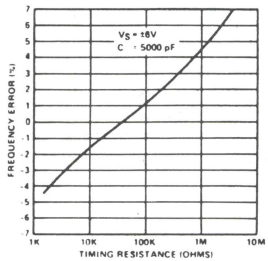


Figure 6. Frequency Accuracy vs. Timing Resistance

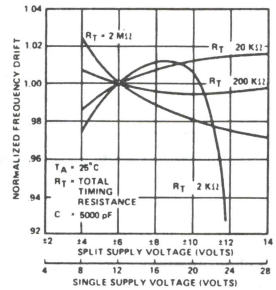


Figure 7. Frequency Drift vs. Supply Voltage

*** Note: R_T = Timing Resistor at Pin 4**

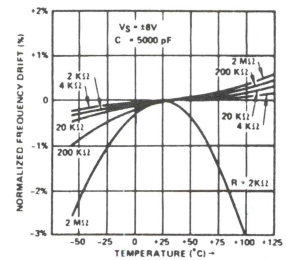


Figure 8. Normalized Frequency Drift With Temperature

RECOMMENDED CIRCUIT CONNECTIONS

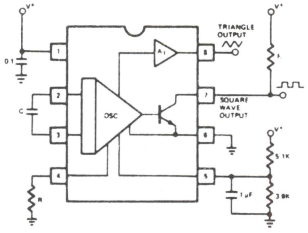


Figure 9. Circuit Connection for Single Supply Operation

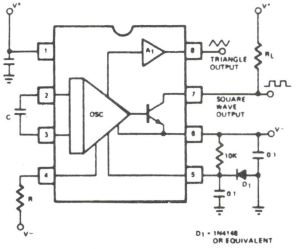


Figure 10. Generalized Circuit Connection for Split Supply Operation

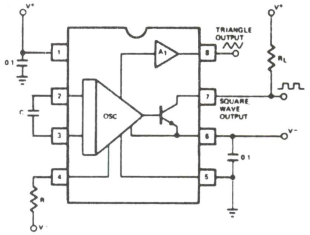


Figure 11. Simplified Circuit Connection for Split Supply Operation With $V_{CC} - V_{EE} > 17V$
(Note: Triangle wave output has +0.6V offset with respect to ground.)

DESCRIPTION OF CIRCUIT CONTROLS

Timing Capacitor (Pins 2 and 3)

The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100pF to 100µF. The capacitor should be non-polar.

Timing Resistor (Pin 4)

The timing resistor determines the total timing current, I_T, available to charge the timing capacitor. Values for the timing resistor can range from 1.5KΩ to 2MΩ; however, for optimum temperature and power supply stability, recommended values are 4KΩ to200 KΩ (see Figures 4, 7, and 8). To avoid parasitic pick up, timing resistor leads should be kept as short as possible.

Supply Voltage (Pins 1 and 6)

The XR-2209 is designed to operate over a power supply range of 14V to 113V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced (see Figures 3 and 4). Performance is optimum for 16V, or 12V single supply operation.

Bias for Single Supply (Pin 5)

For single supply operation, pin 5 should be externally biased to a potential between V+/3 and V+/2 volts (see Figure 9). The bias current at pin 5 is nominally 5% of the total oscillation timing current, I_T, at pin 4. This pin should be bypassed to ground with 0.1µF capacitor. To prevent triangular clipping the voltage at pin 5 should be 5V above V⁻.

Squarewave Output (Pin 7)

The squarewave output at pin 7 is a "open-collector" stage capable of sinking up to 20mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1KΩ to 100KΩ).

Triangle Output (Pin 8)

The output at pin 8 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 8 has a very low output impedance of 10Ω and is internally protected against short circuits.

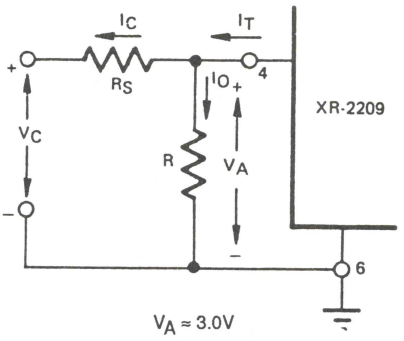


Figure 12. Frequency Sweep Operation

OPERATING INSTRUCTIONS

Split Supply Operation

The recommended circuit for split supply operation is shown in Figure 10. Diode D_1 in the figure assures that the triangle output swing at pin 8 is symmetrical about ground. This circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs at ±6V supplies. See Figure 3 for operation with unequal supplies.

Simplified Connection

For operation with split supplies in excess of 17 volts, the simplified circuit connection of Figure 11 can be used. This circuit eliminates the diode D_1 used in Figure 10; however the triangle wave output at pin 8 now has a +0.6 volt DC offset with respect to ground.

Single Supply Operation

The recommended circuit connection for single-supply operation is shown in Figure 9. Pin 6 is grounded; and pin 5 is biased from V+ through a resistive divider as shown in the figure, and is bypassed to ground with a 1µF capacitor.

For single supply operation, the DC voltage at the timing terminal, pin 4, is approximately 0.6 volts above V_B, the bias voltage at pin 5.

The frequency of operation is determined by the timing capacitor C and the timing resistor R, and is equal to 1/RC. The squarewave output is obtained at pin 7 and has a peak-to-peak voltage swing equal to the supply voltage. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5KΩ) to V+. The triangle waveform obtained at pin 8 is centered about a voltage level V_O where:

$$V_O = V_B + 0.6V$$

where V_B is the bias voltage at pin 5. The peak-to-peak output swing of triangle wave is approximately equal to V+/2.

Frequency Control (Sweep and FM)

The frequency of operation is proportional to the total timing current I_T drawn from the timing pin, pin 4. This timing current, and the frequency of operation can be modulated by applying a control voltage, V_C, to the timing pin, through a series resistor, R_S, as shown in Figure 12. If V_C is negative with respect to V_A, the voltage level at pin 4, then an additional current I_O is drawn from the timing pin causing I_T to increase, thus increasing the frequency. Conversely, making V_C higher than V_A causes the frequency to decrease by decreasing I_T.

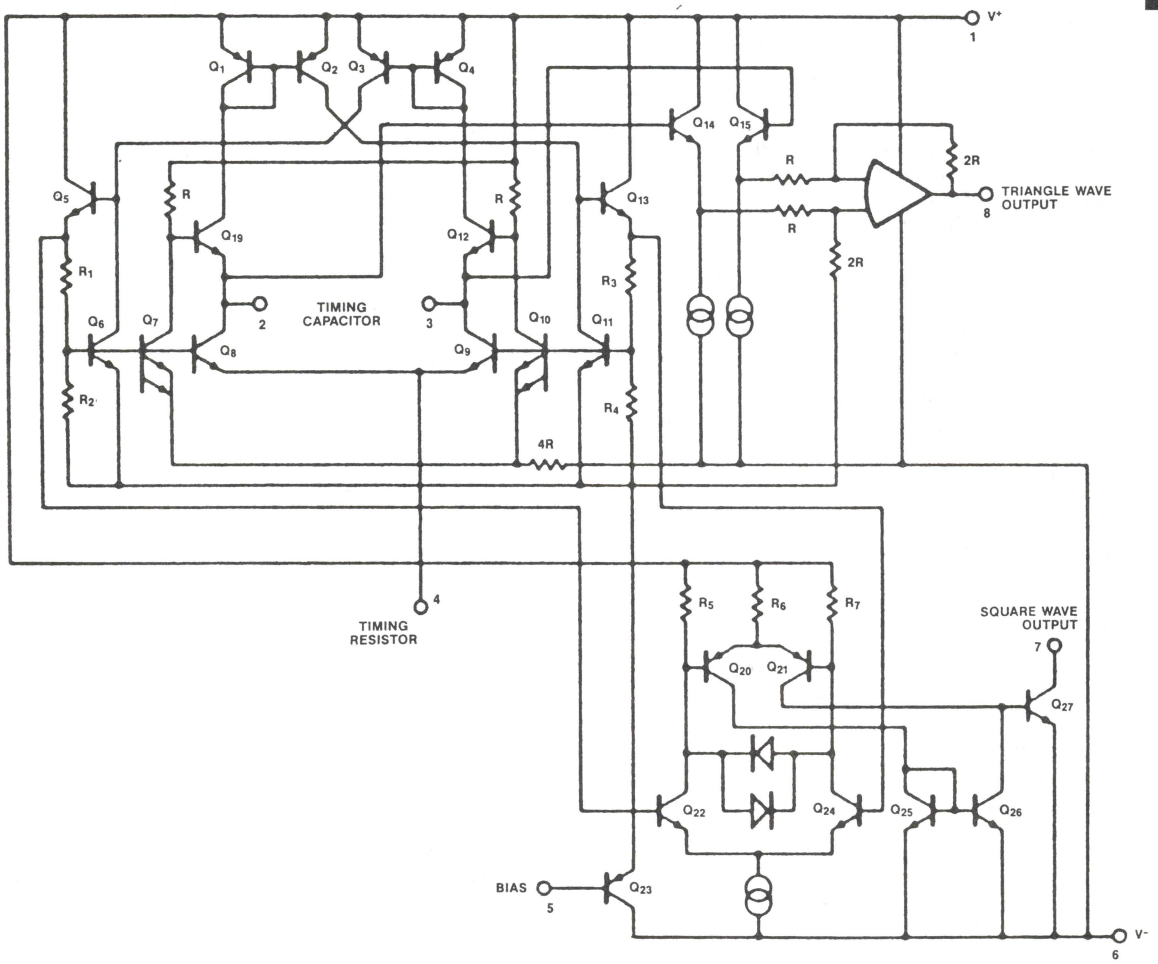
The frequency of operation, is determined by:

$$f = f_o\left[1 + \frac{R}{R_S} - \frac{V_C}{V_A}\frac{R}{R_S}\right]$$

where $f_o = 1/R_C$.

$$V_A = 3.0V$$

EQUIVALENT SCHEMATIC DIAGRAM



Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038 is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth and pulse waveforms with a minimum number of external components and adjustments. Its operating frequency can be selected over eight decades of frequency, from 0.001Hz to 200KHz by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. Both full frequency sweeping as well as smaller frequency variations (FM) can be accomplished with an external control voltage. Each of the three basic waveforms, i.e., sinewave, triangle and square wave outputs are available simultaneously, from independent output terminals.

The XR-8038 monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2208, to form stable phase-locked loop circuits.

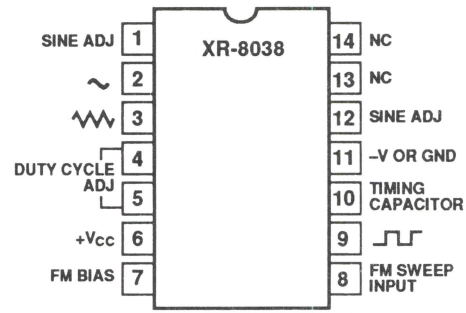
FEATURES

Pin for pin replacement for Intersil 8038
With Improved Sweep Range, Frequency Drift (50 ppm/°C Typ.), and Max. Operating Frequency
Simultaneous Sine, Triangle and Square-Wave Outputs
Low Sine Wave Distortion — THD ≃ 1%
High FM and Triangle Linearity
Wide Frequency Range — 0.001Hz to 200KHz
Variable Duty-Cycle — 2% to 98%

APPLICATIONS

Precision Waveform Generation: Sine, Triangle, Square, Pulse
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic package	750mW
Derate above +25°C	6.0mW/°C
Plastic package	625mW
Derate above +25°C	5mW/°C
SO-14	390mW
Derate above +25°C	3mW/°C
Storage Temperature Range	–66°C to +150°C

Note: Combinations of V_{CC}, V_{EE} and timing resistors may exceed the above value. Caution is recommended.

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038M	Ceramic	–55°C to +125°C
XR-8038N	Ceramic	0°C to +70°C
XR-8038P	Plastic	0°C to +70°C
XR-8038CN	Ceramic	0°C to +70°C
XR-8038CP	Plastic	0°C to +70°C
XR-8038MD	Japanese SOIC	0°C to +70°C

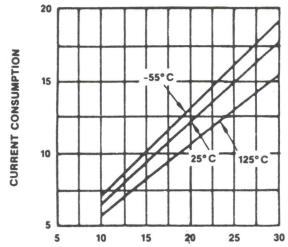
ELECTRICAL CHARACTERISTICS

Test Conditions: $V_S = \pm5V$ to $\pm15V$, $T_A = 25°C$, $R_L = 1M\Omega$, $R_A = R_B = 10k\Omega$, $C_1 = 3300pF$, S_1 closed, unless otherwise specified. See Test Circuit of Figure 1.

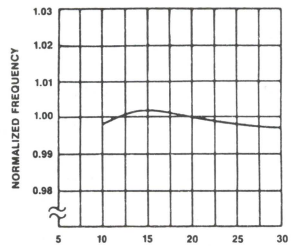
PARAMETERS	XR-8038M/XR8038			XR8038C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage, V_S								
Single Supply	10		30	10		30	V	
Dual Supplies	±5		±15	±5		±15	V	
Supply Current		12	15		12	20	mA	$V_S = \pm10V$. See Note 1.
FREQUENCY CHARACTERISTICS (Measured at Pin 9)								
Range of Adjustment								
Max. Operating Frequency	200			200			KHz	$R_A = R_B$, = 1.5kΩ, C_1 = 680pF R_L = 10kΩ
Lowest Practical Frequency		0.001			0.001		Hz	$R_A = R_B = 1M\Omega$, C_1= 500 µF (Low Leakage Capacitor)
Max. Sweep Frequency of								
FM Input		100			100		kHz	
FM Sweep Range		1000:1			1000:1			S_1 Open. See Notes 2 and 3.
FM Linearity 10:1 Ratio		0.1			0.2		%	S_1 Open. See Note 3.
Range of Timing Resistors	0.5		1000	0.5		1000	kΩ	Values of R_A and R_B
Temperature Stability								
XR-8038M		50	100	—	—	—	ppm/°C	T_T = 0°C to 70°C *See note 8
XR-8038AM		125	150				PPm/°C	T_T = –55°C to +125°C *See note 8
XR-8038		50	100	—	—	—	ppm/°C	
XR-8038C	—	—	—		50		ppm/°C	T_T = 0°C to 70°C *See note 8
Power Supply Stability		0.05			0.05		%/V	See Note 4.
OUTPUT CHARACTERISTICS								
Square-Wave								Measured at Pin 9.
Amplitude (Peak-to-Peak)	0.9	0.98		0.9	0.98		X V_{SPLY}	R_L = 100kΩ
Saturation Voltage		0.2	0.4		0.2	0.5	V	I_{sink} = 2mA
Rise Time		100			100		nsec	R_L = 4.7kΩ
Fall Time		40			40		nsec	R_L = 4.7kΩ
Duty Cycle Adj.	2		98	2		98	%	
Triangle/Sawtooth/Ramp								Measured at Pin 3.
Amplitude (Peak-to-Peak)	0.3	0.33		0.3	0.33		X V_{SPLY}	R_L = 100kΩ
Linearity		0.05			0.1		%	
Output Impedance		200			200		Ω	I_{OUT} = 5mA
Sine-Wave Amplitude (Peak-to-Peak)	0.2	0.22		0.2	0.22		X V_{SPLY}	R_L = 100kΩ
Distortion								
Unadjusted		0.7	1.5		0.8	3	%	R_L = 1MΩ See Note 5, 6 and 7.
Adjusted		0.5			0.5		%	R_L = 1MΩ

Note 1: Currents through R_A and R_B not included.
Note 2: $V_{SUPPLY} = 20V$.
Note 3: Apply sweep voltage at Pin 8.
$V_{CC} - (1/3\ V_{SUPPLY} - 2) \leq V_{PIN\ 8} \leq V_{CC}$
V_{SUPPLY} = Total Supply Voltage across the IC
Note 4: $10V \leq V_s < 30V$ or $\pm5V \leq V_s \leq 15V$.
Note 5: 82kΩ resistor connected between Pins 11 and 12.
Note 6: Triangle duty cycle set at 50%, use R_A and R_B.
Note 7: As R_L is decreased distortion will increase, R_L min ≈ 50kΩ.
Note 8: Guaranteed but not tested.

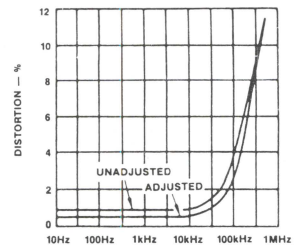
CHARACTERISTIC CURVES



Supply Voltage Power Dissipation vs. Supply Voltage



Supply Voltage Frequency Drift vs. Power Supply



Sinewave THD vs. Frequency

SYSTEM DESCRIPTION

The XR-8038 precision waveform generator produces highly stable and sweepable square, triangle, and sine waves across eight frequency decades. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, buffers, and a sine wave converter. Three identical frequency waveforms are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7%, with Pin 1 open and 82kΩ from Pin 12 to Pin 11 (–V or ground). Sine wave distortion may be improved by including two 100kΩ potentiometers between V_{CC} and –V (or ground), with one wiper connected to Pin 1 and the other connected to Pin 12.

Small frequency deviation (FM) is accomplished by applying modulation voltage to Pins 7 and 8; large frequency deviation (sweeping) is accomplished by applying voltage to Pin 8 only Sweep range is typically 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches 0.22 of the supply voltage.

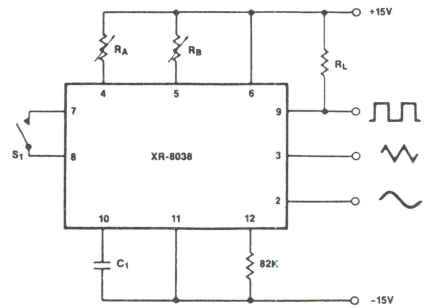


Figure 1. Generalized Test Circuit

PRINCIPLES OF OPERATION

This circuit operates through the charging and discharging of external capacitor C by the currents I_A and $2I_B$. See Figure 3. When switch S is open, current I_A charges capacitor C from V_{CC} – 2/3 V_{SUPPLY} to V_{CC} – 1/3 V_{SUPPLY} (V_{SUPPLY} being the total supply voltage across the chip), at which point comparator #1 switches, causing the flip-flop to change state. As a result of the flip-flop changing state, switch S closes, causing capacitor C to be discharged by the current $2I_B - I_A$ since both current sources are now connected to the capacitor. Capacitor C is discharged from V_{CC} – 1/3 V_{SUPPLY} to V_{CC} – 2/3 V_{SUPPLY}, at which point comparator #2 switches, causing the flip-flop to again change state. Switch S opens, and the cycle begins again with the charging of capacitor C. The charging and discharging of capacitor C creates a triangle wave voltage across the capacitor, which is connected to pin 10. This pin 10 signal is buffered, and the result is the triangle wave output appearing at pin 3. This buffered triangle wave is passed through a sine-converter

network, thus creating the sine wave output at pin 2. The square wave output at pin 9 is simply the buffered output of the flip-flop, which changes its output state as a result of the charge and discharge of capacitor C.

Producing a 50% duty cycle square wave output, a symmetrical triangle (as opposed to sawtooth) wave output, and a symmetrically-shaped sine wave output, require that current I_A be chosen equal to current I_B. When I_A is set equal to I_B, the current I_A charging the capacitor is equal to the net current $2I_B - I_A = I_A$ which alternately discharges the capacitor. As a result of this, the waveform appearing at pin 10 is a symmetrical triangle wave, as is the buffered triangle wave output at pin 3. This symmetrical triangle wave output at pin 3 produces a symmetrically-shaped sine wave output at pin 2. Also, the symmetrical triangle wave at pin 10 causes the flip-flop to produce a 50% duty cycle square wave output at pin 9. Sawtooth wave and asymmetrically-shaped sine and square wave outputs can be produced by setting up currents I_A and I_B to be unequal.

In order to understand how magnitudes for currents I_A and I_B are determined, refer to Figure 4. For typical operation of the 8038, Pin 7, the output of the internal voltage divider, is connected to Pin 8. As a result, a voltage of

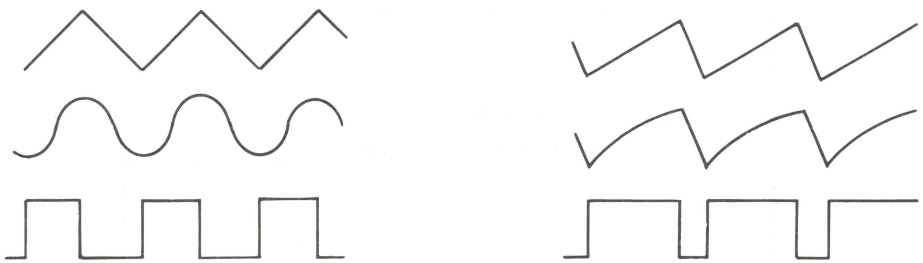
$$V_{CC} - \frac{R_2 V_{SUPPLY}}{R_1 + R_2} = V_{CC} - \frac{V_{SUPPLY}}{5}$$

is present at the ends of both timing resistors R_A and R_B (the ends of R_A and R not connected to the positive supply). Consequently,

$$I_A = \frac{V_{CC} - (V_{CC} - \frac{V_{SUPPLY}}{5})}{R_A}$$

$$I_A = \frac{V_{SUPPLY}}{5R_A}$$

$$I_B = \frac{V_{SUPPLY}}{5R_AB}$$



(a) Symmetrical Waveforms

(b) Asymmetrical Waveforms

Figure 2. Phase Relationship of the Triangle, Sine Wave, and Square Wave Outputs

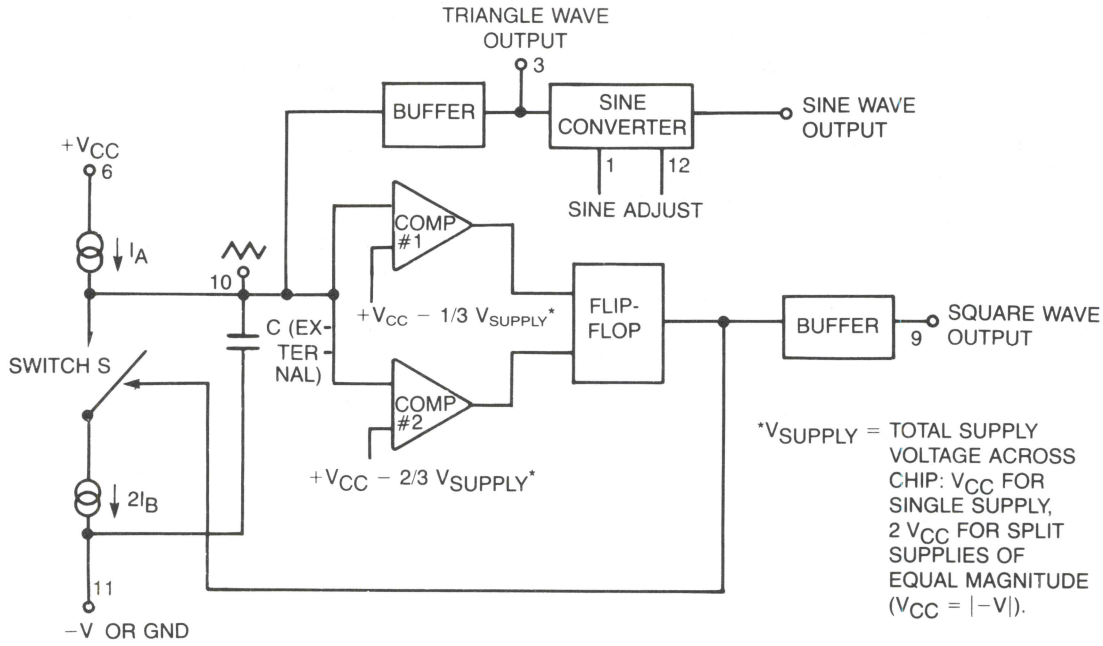


Figure 3. Functional Block Diagram

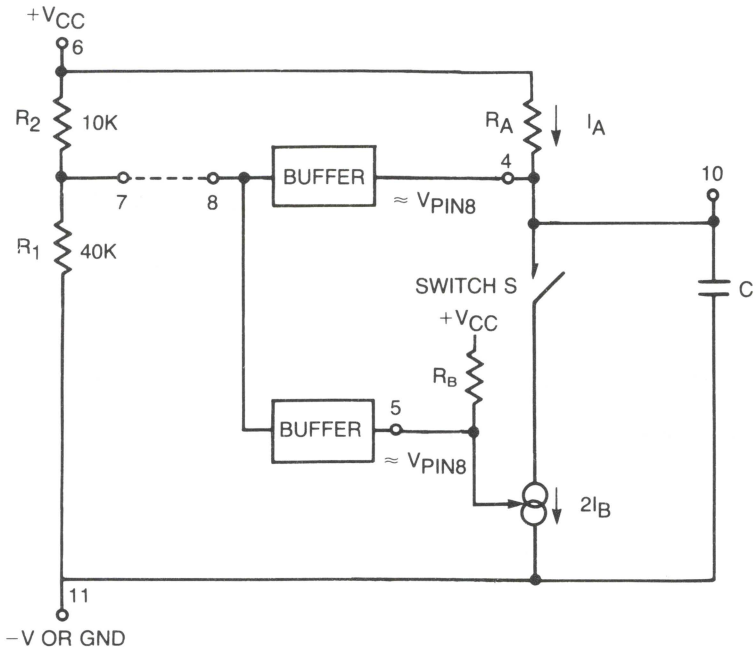


Figure 4. Detailed View of Current Sources I_A and $2I_B$

For the case of SINGLE-SUPPLY operation, these equations can be simplified to

$$I_A = \frac{V_{CC}}{5R_A} \quad \text{and} \quad I_B = \frac{V_{CC}}{5R_B} \quad .$$

For the case of SPLIT-SUPPLY operation, where the negative and positive supplies are equal in magnitude, the equations for I_A and I_B can be simplified to

$$I_A = \frac{2V_{CC}}{5R_A} \quad \text{and} \quad I_B = \frac{2V_{CC}}{5R_B}.$$

Waveform Adjustment

The equations pertinent to waveform adjustment are derived here assuming single-supply operation (and the connection of pin 7 to pin 8). However, these same equations for t_1, t_2, and f apply to split-supply operation also, regardless of whether the magnitudes of the positive and negative supplies are equal.

The symmetry of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figures 5a and 5b. Best results are obtained by keeping the timing resistors R_A and R_B separate (5a). R_A controls the rising portion of the triangle and sine waves and the "high" state of the square wave.

Referring to Figure 3, it is apparent that the pin 10 triangle wave will have a minimum amplitude of 1/3 V_{CC} and a maximum amplitude of 2/3 V_{CC}; therefore, the duration of the rising portion of the triangle wave is

$$t_1 = \frac{C \times |\Delta V|}{I_A} = \frac{C \times |2/3\ V_{CC} - 1/3\ V_{CC}|}{\frac{V_{CC}}{5R_A}}$$

$$= \frac{5}{3} R_A C.$$

The duration of the falling portion of the triangle and sine wave and the "low" state of the square wave is

$$t_1 = \frac{C \times |\Delta V|}{2I_B - I_A} = \frac{C \times |1/3\ V_{CC} - 2/3\ V_{CC}|}{\frac{2V_{CC}}{5R_B} - \frac{V_{CC}}{5R_A}}$$

$$= \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B} \quad .$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

It the duty cycle is to be varied over a small range, centered around a duty cycle of 50%, the connection shown in Figure 5b is slightly more convenient. It no adjustment of the duty cycle is desired, pins 4 and 5 can be shorted together, as shown in Figure 5c. This connection, however, carries an inherently larger variation of the duty cycle as frequency is varied.

With two separate timing resistors the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{5/3\ R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)};$$

or, if $R_A = R_B = R$

$f = 0.3/RC$ (for Figure 5a)

If a single timing resistor is used (Figure 5b and c), the frequency is

$f = 0.15/RC.$

The frequency accuracy of the 8038 is typically within ±8.5% of the frequency calculated using the above formula $f = 0.3/RC$ (under the test conditions shown at the top of the electrical characteristics section and $V_{SUPPLY} = 20V$) For tighter frequency accuracies, Pin 8 can be disconnected from Pin 7 and set at $V_{PIN8} = V_{CC} - \frac{V_{SUPPLY}}{5}$. Using this approach, the frequency accuracy of the part is typically within ±4% of the calculated frequency (tested at $V_{CC} = V_{SUPPLY} = 20V$, $V_{PIN8} = 16V$).

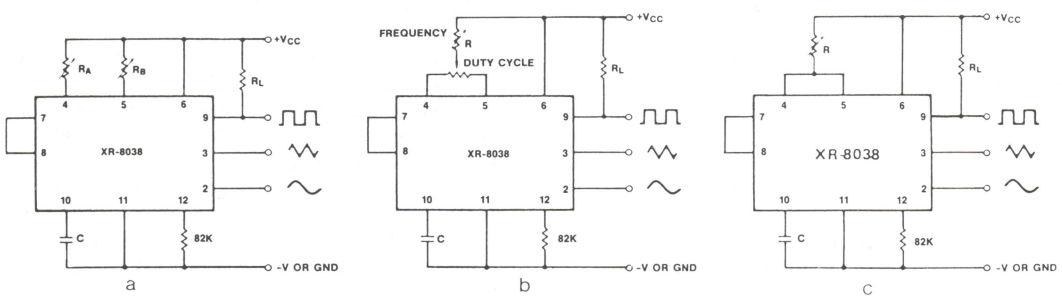


Figure 5. Possible Connections for the External Timing Resistors

Timing Component Constraints

For any given output frequency, there is a wide range of RC combinations that will work. However, certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 0.1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly large errors. Optimum performance will be obtained for charging currents of 1μA to 1mA. To determine the magnitudes of the charging currents I_A and I_B, see the Principles of Operation section.

When the duty cycle is chosen to be greater than 60% or less than 40%, the device may not oscillate every time unless the rise time of the positive supply is ten times slower than the time constant R_A C, for the 60% duty cycle case, or ten times slower than the time constant R_B C, for the 40% duty cycle case. If the rise time of the positive supply is faster than what is required, oscillation can be guaranteed by tying a 0.1μF capacitor from Pins 7 and 8 to ground.

Distortion Adjustment

To minimize sine-wave distortion the 82kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6. This configuration allows a reduction of sine-wave distortion close to 0.5%.

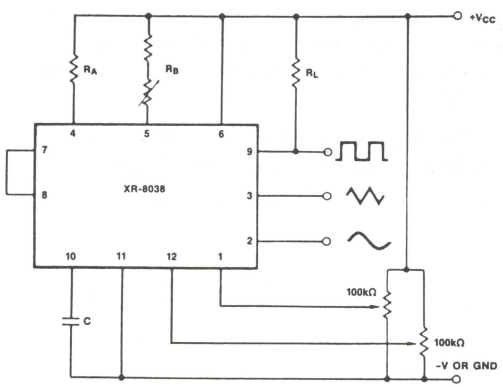


Figure 6. Connection to Achieve Minimum Sine-Wave Distortion

Single-Supply and Split-Supply Operation

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between $+V_{CC}$ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (36V). In this way, the square-wave output will be TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a higher supply voltage.

Frequency Modulation and Sweep

The frequency of the waveform generator is an inverse function of the DC voltage at pin 8. In other words, the frequency increases as the pin 8 voltage is swept from its upper limit of V_{CC} (and slightly higher) to its lower limit of approximately $V_{CC} - (1/3\ V_{SUPPLY} - 2)$.

For small deviations (e.g., ±10%), the modulating signal can be applied to pin 8 through a capacitor while pin 8 is connected to pin 7 (or while pin 8 and pin 7 are connected together through a resistor). This mode of operation (shown in Figure 7a) makes use of the DC bias provided by pin 7 and thus eliminates the need for the modulating signal to have a particular DC level. The external resistor between pins 7 and 8 can be used to increase input impedance. Without this resistor (i.e., pins 7 and 8 connected together), the input impedance is 8KΩ; with it, this impedance increases to (R + 8KΩ).

For larger FM deviations or for frequency sweeping, Pin 7 is not used. Instead, the entire bias for the 8038 current sources is created by the modulating signal at Pin 8. The circuit of Figure 7b, which shows this mode of operation, will allow a sweep range of typically 1000:1, the frequency approaching 0Hz when the voltage at Pin 8 is equal to V_{CC} and the frequency reaching its maximum at the lower Pin 8 voltage limit of $V_{CC} - (1/3\ V_{SUPPLY} - 2)$. Waveform symmetry variations which occur when the frequency is swept can be reduced by adding a large fixed resistor (e.g., 10M) or potentiometer from Pin 5 to Pin 11 (GND or –V). Even with this resistor added, there will still be some symmetry variation at lower frequencies (e.g., 200Hz and lower).

Care must be taken to regulate the supply voltage, as frequency becomes dependent on the supply voltage in this configuration. The frequency of oscillation of this circuit is given by

$$f = \frac{1}{t_1 + t_2}$$

where $t_1 = \dfrac{R_A C\, V_{SUPPLY}}{3(V_{CC} - V_{PIN8})}$,

and $t_2 = \dfrac{R_A R_B C\, V_{SUPPLY}}{3(V_{CC} - V_{PIN8})\,(2R_A - R_B)}$;

or, if $R_A = R_B = R$

$$t_1 = \frac{RC\, V_{SUPPLY}}{3(V_{CC} - V_{PIN8})}$$

and $t_2 = \dfrac{RC\, V_{SUPPLY}}{3(V_{CC} - V_{PIN8})}$,

V_{SUPPLY} being the total supply voltage across the chip (e.g., V_{SUPPLY} = 20V for ±10V split supplies).

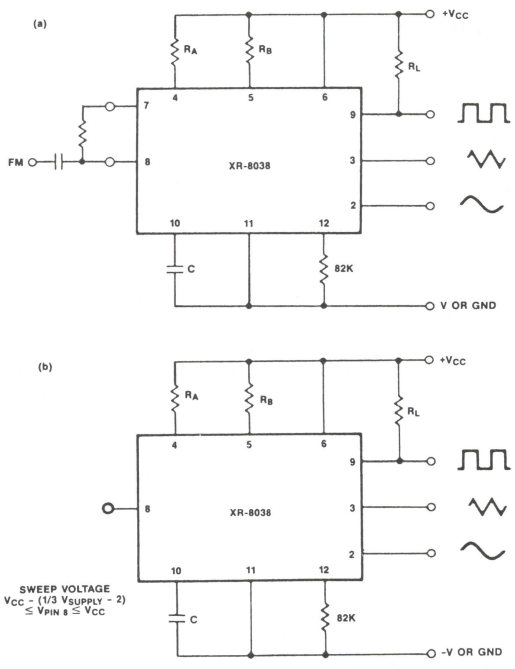


Figure 7. Connections for Frequency Modulation (a) and Sweep (b)

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038A is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth, and pulse waveforms, with a minimum number of external components and adjustments. The 8038A allows the elimination of the external distortion adjusting resistor which greatly improves the temperature drift of distortion, as well as lowering external parts count. Its operating frequency can be selected over eight decades of frequency, from 0.001Hz to 200KHz, by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. Both full frequency sweeping as well as smaller frequency variations (FM) can be accomplished with an external control voltage. Each of the three basic waveform outputs, (i.e., sine, triangle and square) are simultaneously available from independent output terminals.

The XR-8038A monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2228 to form stable phase-locked circuits.

FEATURES

Low Frequency Drift	50ppm/°C, Typical
Simultaneous Sine, Triangle, and Square Wave Outputs	
Low Sine Wave Distortion — THD ≃ 1%	
High FM and Triangle Linearity	
Wide Frequency Range	0.001Hz to 200KHz
Variable Duty Cycle	2% to 98%
Low Distortion Variation with Temperature	

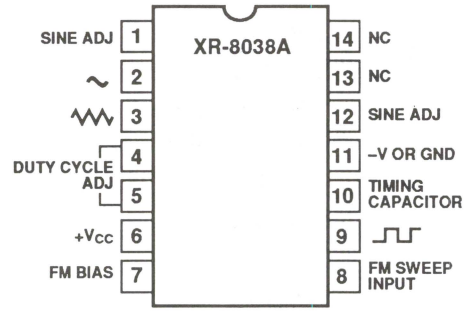
APPLICATIONS

Precision Waveform Generation
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic Package	750mW
Derate Above +25°C	6.0mW/°C
Plastic Package	625mW
Derate Above +25°C	5mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038AM	Ceramic	–55°C to +125°C
XR-8038AN	Ceramic	0°C to +70°C
XR-8038AP	Plastic	0°C to +70°C
XR-8038ACN	Ceramic	0°C to +70°C
XR-8038ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-8038A precision waveform generator produces highly stable and sweepable square, triangle, and sine waves across eight frequency decades. The XR-8038A is an advanced version of the XR-8038, with improved sine distortion temperature drift. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, buffers, and a sine wave convertor. Three identical frequency outputs are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7% with the sine wave distortion adjust pin (Pin 1) open. Distortion levels may be improved by including a 100kΩ potentiometer between the supplies, with the wiper connected to Pin 1.

Small frequency deviation (FM) is accomplished by applying modulation voltage to Pins 7 and 8; large frequency deviation (sweeping) is accomplished by applying voltage to Pin 8 only. Sweep range is typically 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches 0.22 of the supply voltage.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_S = ±5V to ±15V, T_A = 25°C, R_L = 1MΩ, R_A = R_B = 10kΩ, C_1 = 3300pF, S_1 closed, unless otherwise specified.

PARAMETERS	8038AM/8038A			8038AC			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage, V_S								
Single Supply	10		30	10		30	V	
Dual Supplies	±5		±15	±5		±15	V	
Supply Current		12	15		12	20	mA	V_S = ±10V (Note 1)
FREQUENCY CHARACTERISTICS (Measured at Pin 9)								
Range of Adjustment								
Max. Operating Frequency	200			200			KHz	$R_A = R_B$, = 1.5kΩ, C_1 = 680pF R_L = 10K
Lowest Practical Frequency		0.001			0.001		Hz	$R_A = R_B$ = 1MΩ, C_1= 500µF (Low Leakage Capacitor)
Max. Sweep Frequency of FM Input		100			100		kHz	
FM Sweep Range		1000:1			1000:1			S_1 Open (Notes 2 & 3)
FM Linearity 10:1 Ratio		0.1			0.2		%	S_1 Open (Note 3)
Range of Timing Resistors	0.5		1000	0.5		1000	kΩ	Values of R_A and R_B
Temperature Stability								
XR-8038AM		50		—	—	—	ppm/°C	T_A = −55°C to +125°C
XR-8038A		50	100					
XR-8038AC					50		ppm/°C	T_A = 0°C to +70°C
Power Supply Stability		0.05			0.05		%/V	(Note 4)
OUTPUT CHARACTERISTICS								
Square-Wave								Measured at Pin 9
Amplitude (Peak-to-Peak)	0.9	0.98		0.9	0.98		x V_{SPLY}	R_L = 100kΩ
Saturation Voltage		0.2	0.4		0.2	0.5	V	I_{sink} = 2mA
Rise Time		100			100		nsec	R_L = 4.7kΩ
Fall Time		40			40		nsec	R_L = 4.7kΩ
Duty Cycle Adjustment	2		98	2		98	%	
Triangle/Sawtooth/Ramp								Measured at Pin 3.
Amplitude (Peak-to-Peak)	0.3	0.33		0.3	0.33		x V_{SPLY}	R_L = 100kΩ
Linearity		0.05			0.1		%	
Output Impedance		200			200		Ω	I_{OUT} = 5mA
Sine-Wave Amplitude (Peak-to-Peak)	0.2	0.22		0.2	0.22		x V_{SPLY}	R_L = 100kΩ
Distortion		0.7	1.5		0.8	3	%	R_L = 1MΩ (Notes 5, 6 & 7)
Unadjusted		0.5			0.5		%	R_L = 1MΩ (Notes 5, 6 & 7)
Adjusted		0.5			0.3		%	
ΔTHD/ΔT								

Note 1: Currents through R_A and R_B not included.
Note 2: V_{SUPPLY} = 20V.
Note 3: Apply sweep voltage at Pin 8.
$V_{CC} - (1/3\ V_{SUPPLY} - 2) \leq V_{PIN\ 8} \leq V_{CC}$
V_{SUPPLY} = Total Supply Voltage across the IC
Note 4: 10V ≤ V_S ≤ 30V or ±5V ≤ V_S ≤ 15V.
Note 5: Pin 12 open circuited (No. 82kΩ resistor as standard 8038).
Note 6: Triangle duty cycle set at 50%, use R_A and R_B.
Note 7: As R_L is decreased distortion will increase, R_L min ≈ 50kΩ.

Voltage-to-Frequency Converter

GENERAL DESCRIPTION

The XR-4151 is a device designed to provide a simple, low-cost method for converting a DC voltage into a proportional pulse repetition frequency. It is also capable of converting an input frequency into a proportional output voltage. The XR-4151 is useful in a wide range of applications including A/D and D/A conversion and data transmission.

FEATURES

Single Supply Operation (+8V to +22V)
Pulse Output Compatible with All Logic Forms
Programmable Scale Factor (K)
Linearity ±0.05% Typical-Precision Mode
Temperature Stability ±100% ppm/°C Typical
High Noise Rejection
Inherent Monotonicity
Easily Transmittable Output
Simple Full Scale Trim
Single-Ended Input, Referenced to Ground
Also Provides Frequency-to-Voltage Conversion
Direct Replacement for RC/RV4151

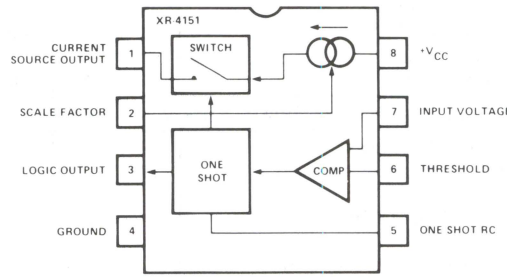
APPLICATIONS

Voltage-to-Frequency Conversion
A/D and D/A Conversion
Data Transmission
Frequency-to-Voltage Conversion
Transducer Interface
System Isolation

ABSOLUTE MAXIMUM RATINGS

Power Supply	22V
Output Sink Current	20mA
Internal Power Dissipation	500mW
Input Voltage	–0.2V to $+V_{CC}$
Output Short Circuit to Ground	Continuous

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4151P	Plastic	–40°C to +85°C
XR-4151CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-4151 is a precision voltage to frequency converter featuring 0.05% conversion linearity (precision mode), high noise rejection, monotonicity, and single supply operation from 8V to 22V. An RC network on Pin 5 gets the maximum full wale frequency. Input voltage on Pin 7 is compared with the voltage on Pin 6 (which is generally controlled by the current source output, Pin 1). Frequency output is proportioned to the voltage on Pin 7. The current source is controlled by the resistance on Pin 2 (nominally 14kΩ with I = 1.9 V/R. The output is an open collector at Pin 3.

ELECTRICAL CHARACTERISTICS

Test Condtions: (V_{CC} = 15V, T_A = +25°C, unless otherwise specified)

PARAMETERS	XR-4151CP		XR-4151P		TYP	UNITS	CONDITIONS
	MIN	MAX	MIN	MAX			
Supply Current	2.0	6.0	2.0	6.0	3.5	mA	8V < V_{CC} < 15V
	2.0	7.5	2.0	7.5	4.5	mA	15V < V_{CC} < 22V
Conversion Accuracy	0.90	1.10	0.92	1.08	1.00	kHz/V	Circuit of Fig. 3, V_I = 10V
Scale Factor							R_S = 14.0k
Drift with Temperature	–	–	–	–	±100	ppm/°C	Circuit of Fig. 3. V_I = 10V
Drift with V_{CC}	–	–	–0.9	0.9	0.2	%/V	Circuit Fig. 3, V_I = 1.0V
							8V < V_{CC} < 18V
Input Comparator							
Offset Voltage	–	10	–	10	5	mV	
Offset Current	–	±100	–	±100	±50	nA	
Input Bias Current	–	–300	–	–300	–100	nA	
Common Mode Range (Note 1)	0	V_{CC}–3.0	0	V_{CC}–3.0	0 to V_{CC} –2	V	
One-Shot							
Threshold Voltage, Pin 5	0.63	0.70	0.63	0.70	.667	xV_{CC}	
Input Bias Current, Pin 5	–	–500	–	.500	–100	nA	
Reset V_{SAT}	–	50.0	–	50.0	0.15	V	Pin 5.1 = 2.2mA
Current Source							
Output Current	–	–	–	–	138.7	µA	Pin 1, V = 0, RS = 14.0kΩ
Change with Voltage	–	2.5	–	2.5	1.0	µA	Pin 1, V= 0V to V = 10V
Off Leakage	–	50.0		50.0	0.15	nA	Pin 1, V = 0V
Reference Voltage	1.70	2.08	1.70	2.08	1.9	V	Pin 2
Logic Output							
V_{SAT}	–	0.50	–	0.50	0.15	V	Pin 3, 1 = 3.0mA
V_{SAT}	–	0.30	–	0.30	0.10	V	Pin 3, 1 = 3.0mA
Off Leakage	–	1.0	–	1.0	.1	µA	

Note 1: Input Common Mode Range includes ground.

PRINCIPLES OF OPERATION

Single Supply Mode Voltage-to-Frequency Converter

In this application, the XR-4151 functions as a standalone voltage-to-frequency converter operating on a single positive power supply. Refer to the functional block diagram and Figure 3, the circuit connection for single supply voltage-to-frequency conversion. The XR-4151 contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current 1. At the end of the one shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge Q = I_OT into the network R_B–C_B. If this charge has not increased the voltage V_B such that $V_B > V_I$, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B–C_B network. This process continues until $V_B > V_I$. When this condition is achieved, the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at a rate fast enough to keep $V_B \geq V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/ R_B, the frequency at which the system runs will be proportional to the input voltage.

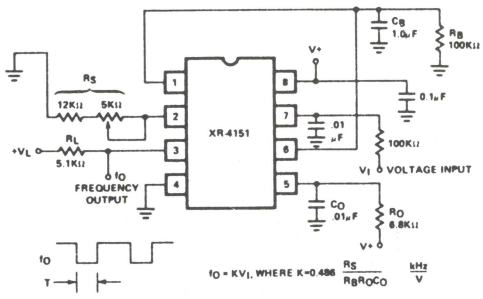


Figure 3. Voltage-to-Frequency Converter

TYPICAL APPLICATIONS

Single Supply Voltage-to-Frequency Converter

Figure 3 shows the simplest type of VFC that can be made with the XR-4151. The input voltage range is from 0 to +10V, and the output frequency is from 0 to 10kHz. The full scale frequency can be tuned by adjusting R_S, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_BC_B. For the component values shown in Figure 3, response time for a step change input from 0 to +10V will be 135msec. For applications which require fast response time and high accuracy, use the circuit of Figure 4. C_B should have a high stability dielectric (mica, polystyrene, polyester).

Precision Voltage-to-Frequency Converter

In this application (Figure 4) the XR-4151 is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to −10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at V_I = −10V for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of −10mV.

The operational amplifier integrator improves linearity of this circuit over that of Figure 3 by holding the output of the source, Pin 1, at a constant 0V. Therefore, the linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at pin 7 of the XR-4151 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an XR-3403 ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass pin 6 of the XR-4151 with .01μF.

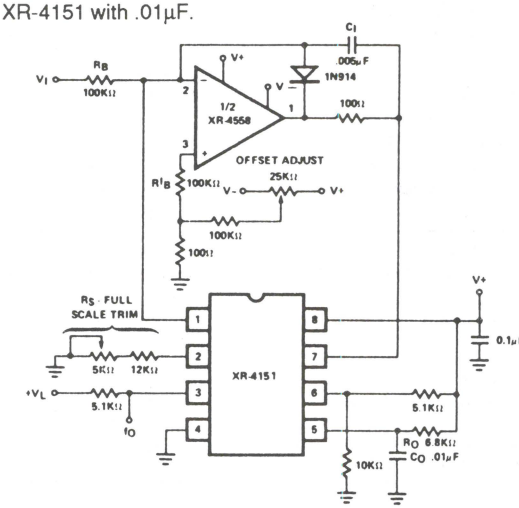


Figure 4. Precision Voltage-to-Frequency Converter

Frequency-to-Voltage Conversion

The XR-4151 can be used as a frequency-to-voltage converter. Figure 5 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, the pulse width must be less than the period of the one-shot, $T = 1.1\ R_OC_O$. For a 5Vp-p square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator can be used to "square-up" sinusoidal input signals before they are applied to the XR-4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network R_BC_B filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 6, the precision FVC configuration. Trim the offset to give –10mV out with 10Hz in and trim the full scale adjust for –10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode and the scale factor can be programmed by the choice of component values. A tradeoff exists between the amount of output ripple and the response time, through the choice or integration capacitor C_1. If $C_1 = 0.1\mu F$ the ripple will be about 100mV. Response time constant $\tau_R = R_B C_I$. For R_B = 100kΩ and $C_I = 0.1\mu F$, τ_R = 10msec.

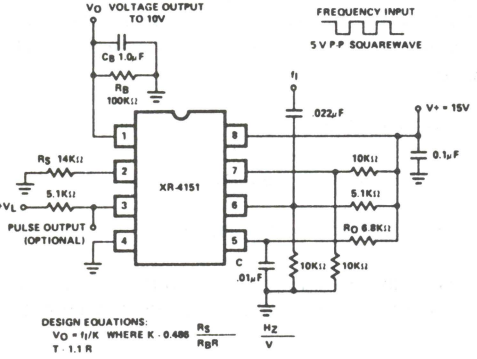


Figure 5. Frequency-to-Voltage Converter

Precautions

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.

2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and $+V_{CC}$ can cause overheating and eventual destruction.

3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if the current in pin 2 exceeds 5mA.

4. Avoid stray coupling between pins 5 and 7; it could cause false triggering. For the circuit of Figure 3, bypass pin 7 to ground with at least 0.01μF. This is necessary for operation above 10kHz.

5. C_B for stability overtime should have a silver mica, polystyrene or polyester di-eletric.

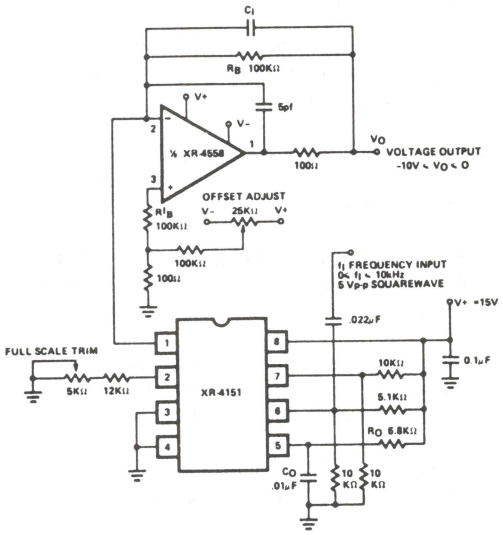


Figure 6. Precision Frequency-to-Voltage Converter

Programming the XR-4151

The XR-4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set R_S = 14kΩ or use a 12k resistor and 5k pot as shown in the figures. (The only exception to this is Figure 4.)

2. Set T = 1.1 R°C^0 = 0.75[1/fo] where fo is the desired full scale frequency. For optimum performance make $6.8k\Omega > R_0 > 680k\Omega$ and $0.001\mu F < C_0 < 1.0\mu F$.

3. a) For the circuit of Figure 3 make $C_B = 10^{-2}$ [1/fo] Farads.

   Smaller values of C_B will give a faster response time, but will also increase the frequency offset and nonlinearity.

b) For the active integrator circuit make

$C_I = 5 \times 10^{-5}$ [1/fo] Farads.

The op-amp integrator must have a slew rate of at least 135×10^{-6} [$1/C_1$] volts per second where the value of C_1 is in Farads.

4. a) For the circuit of Figure 4 keep the values of R_B and R_B as shown and use an input attenuator to give the desired full scale input voltage.

b) For the precision mode circuit of Figure 4, set $R_B = V_{IO}/100\mu A$ where V_{IO} is the full scale input voltage.

Alternately, the op-amp inverting input (summing node) can be used as a current input with the full scale input current $I_{IO} = -100\mu A$.

5. For the FVC's, pick the value of C_B or C_I to give the optimum tradeoff between the response time and output ripple for the particular application.

Design Example

I. Design a precision VFC (from Figure 5) with fo = 100kHz and $V_{IO} = -10V$.

1. Set $R_S = 14.0k\Omega$

2. $T = 0.75$ [$1/10^5$] = 7.5μsec

Let $R_0 = 6.8k\Omega$ and $C_0 = 0.001\mu F$.

3. $C_I = 5 \times 10^5$ [$1/10^5$] = 500pF.

Op-amp slew rate must be at least

SR = 135 x 106 [1/500pF] = 0.27V/μsec

4. $R_B = 10V/100\mu A = 100k\Omega$.

II. Design a precision VFC with fo = 1Hz and $V_{IO} = 10V$.

1. Let $R_S = 14.0k_Q$

2. T = 0.75 [1/1] = 0.75 sec

Let $R_0 = 680k\Omega$ and C^0 = 1.0μF.

3. $C_I = 5 \times 10^{-5}$ [1/1]F = 50μF.

4. $R_B = 100k_Q$.

III. Design a single supply FVC to operate with a supply voltage of 9V and full scale input frequency fo = 83.3Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

1. Set $R_S = 14.0k\Omega$

2. T = 0.75 [1183.3] = 9msec

Let $R_0 = 82k\Omega$ and $C_O = 0.1\mu F$.

3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.

4. $R_B = 5V/100\mu A = 50k\Omega$.

5. Output response time constant is $\tau_R \leq 200$msec.

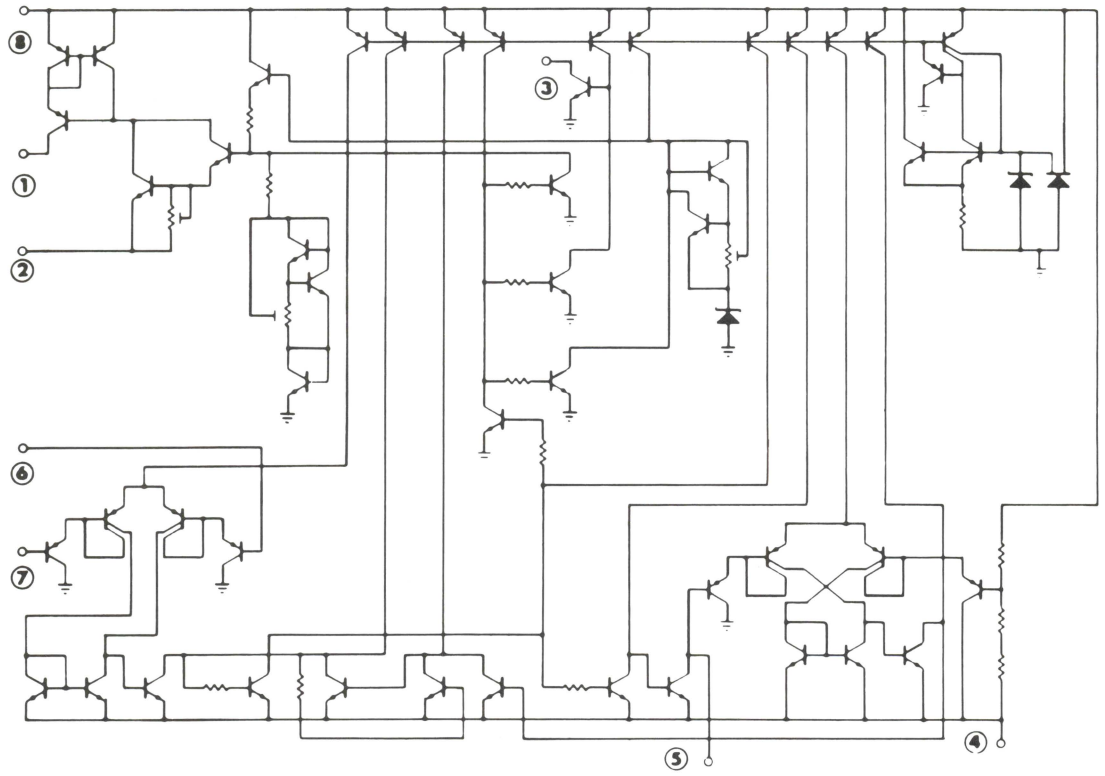
Therefore,

$C_B \leq \tau_R/R_B = (200 \times 10^{-3})/(50 \times 10^3) = 4\mu F$.

Worst case ripple voltage is

$V_R = (9ms \times 135\mu A)/4\mu F = 304mV$.

EQUIVALENT SCHEMATIC DIAGRAM





NOTES



Stable FSK Modems featuring the XR-2207, XR-2206 and XR-2211

Application Note

INTRODUCTION

Frequency-shift keying (FSK) is the most commonly used method for transmitting digital data over telecommunications links. In order to use FSK, a modulator/ demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again. This application note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application.

The devices featured in this application note are the XR-2206 and XR-2207 FSK Modulators, and the XR-2211 FSK demodulator with carrier detect capability. Because of the superior frequency stability of these devices (typically 20ppm/°C), a properly designed modem will be virtually free of the temperature and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modem designs shown in this application note can be used with mark and space frequencies, anywhere from several Hz to 100kHz.

PRINCIPLES OF OPERATION

THE XR-2206 FSK MODULATOR

Features

Typically 20ppm/°C Temperature Stability
Choice of 0.5% THD Sine Wave, Triangle, or Square Wave Output
Phase-Continuous FSK Output
Inputs are TTL and CMOS Compatible
Low-Power Supply Sensitivity (0.01%)
Low-Power Supply Sensitivity (0.01%/V)
Split or Single Supply Operation
Low External Parts Count

The XR-2206 is ideal for FSK applications requiring the spectral purity of a sinusoidal output waveform. It offers TTL and CMOS compatibility, excellent frequency stability, and ease of application. The XR-2206 can typically provide a 3-volt p-p sine wave output. Total harmonic distortion can be trimmed to 0.5%. If left untrimmed, it is approximately 2.5%.

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to Pin 9. A high-level signal selects the frequency ($1/R_6C_3$) Hz; a low level signal selects the frequency ($1/R_7C_3$) Hz, (resistors in ohms and capacitors in farads). For optimum stability, R_6 and R_7 should be within the range of 10kΩ to 100kΩ. The voltage applied to Pin 9 should be selected to fall between ground and V+.

Note: *Over and under voltage may damage the device.*

Potentiometers, R_8 and R_9, should be adjusted for minimum total harmonic distortion. In applications where minimal distortion is unnecessary, Pins 15 and 16 may be left open-circuited and R_8 may be replaced by a fixed 200Ω resistor.

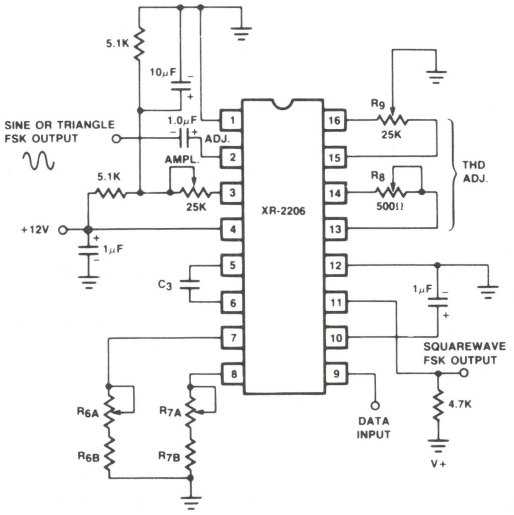


Figure 1. The XR-2206 Sinusoidal FSK Generator.

In applications where a triangular output waveform is satisfactory, Pins 13 through 16 may be left open-circuited.

The output impedance at Pin 2 is about 600Ω, with ac coupling normally being used, in single supply operation.

THE XR-2207 FSK MODULATOR

Features

Typically 20ppm/°C Temperature Stability
Phase-Continuous FSK Output
Provides Both Triangle and Square Wave Outputs
Operates Single-Channel or Two-Channel Multiplex
Inputs are TTL and CMOS Compatible
Split- or Single-Power Supply Operation
Low-Power Supply Sensitivity (0.15%/V)
Low External Parts Count

The XR-2207 is a stable FSK generator which is designed for those applications where only a triangle or square wave output is required. It is capable of either single-channel or two-channel multiplex operation, and can be used easily with either split- or single-power supplies.

Figure 2 shows the XR-2207 using a single-supply and Figure 3 shows split-supply operation. When used as an FSK modulator, Pin 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and CMOS logic forms. When used with a single-supply, the threshold is near mid-supply and is CMOS compatible. Table 1 shows how to select the timing resistors, R_1 through R_4, to determine the output frequency based on the logic levels applied to Pin 8 and 9. For optimum stability, the values of R_1 and R_3 should be selected to fall between 10kΩ and 100kΩ.

With Pin 8 grounded, Pin 9 serves as the data input. A high-level signal applied to Pin 8 will disable the oscillator. When used in this manner, Pin 8 of the XR-2207 serves as the channel select input. For two-channel multiplex operation, Pin 4 and 5 should be connected as shown by the dotted lines. (For single channel operation, Pin 4 and 5 should be left open-circuited.)

The XR-2207 provides two outputs: a square wave at Pin 13 and a triangle wave at Pin 14. (For safe operation, current into Pin 13 should be limited to 20mA.) When used with a split-supply, the triangle wave peak-to-peak amplitude is equal to V^- and the dc level is near ground. Direct coupling is usually used. With a single-supply, the peak-to-peak amplitude is approximately equal to one-half/V^+, the dc level is approximately at mid-supply, and ac coupling is usually necessary. In either case, the output impedance is typically 10Ω and is internally protected against short circuits.

The square wave output has an npn open-collector configuration. When connected as shown in Figure 2 and 3, this output voltage will swing between V^+ and the voltage at Pin 12.

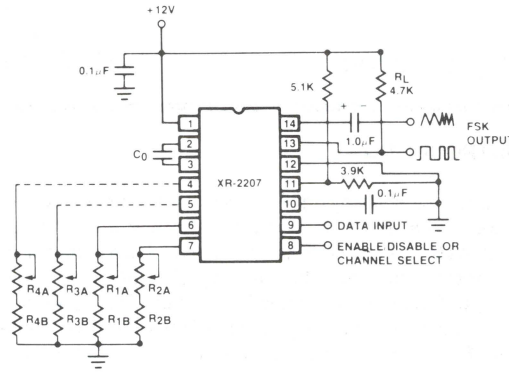


Figure 2. The XR-2207 FSK Modulator Single-Supply Operation

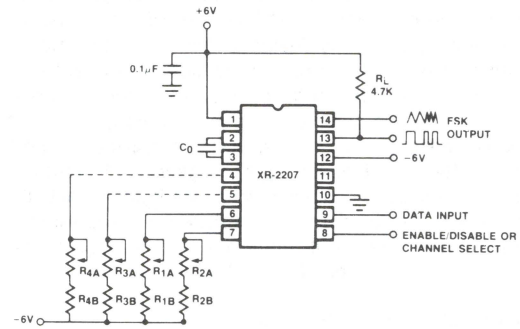


Figure 3. The XR-2207 FSK Modulator Split-Supply Operation

Table 1. XR-2207 FSK Input Control Logic

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_oR_1}$
L	H	Pins 6 and 7	$\frac{1}{C_oR_1} + \frac{1}{C_oR_2}$
H	L	Pin 5	$\frac{1}{C_oR_3}$
H	H	Pins 4 and 5	$\frac{1}{C_oR_3} + \frac{1}{C_oR_4}$

Units: Resistors — Ohms; Capacitqrs — Farads; Frequency — Hz

THE XR-2211 FSK DEMODULATOR

Features

Typically 20 ppm/°C Temperature Stability
Simultaneous FSK and Carrier-Detect output
Outputs are TTL and CMOS Compatible
Wide Dynamic Range (2mV to 3Vrms)
Split or Single Supply Operation
Low-Power Supply Sensitivity (0.05%/V)
Low External Parts Count

The XR-2211 is an FSK demodulator which operates on the phase-locked loop principle. Its performance is virtually independent of input signal strength variations, over the range of 2mV to 3Vrms.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by $f_o = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. Calculation for f_o should fall mid-way between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula: $\Delta f = (R_4 f_o/R_5)$ Hz. Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an R_4 between 10kΩ and 100kΩ.

The capture range ($\pm\Delta f_c$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop filter time constant. In most modem applications, Δf_c = (80%–99%)Δf.

The loop-damping factor (ζ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. it is determined by $\zeta = 1/4\ C_1/C_2$. For most modem applications, choose $\zeta \approx 1/2$.

The FSK output filter time constant (τ_F) removes chatter from the FSK output. The formula is: $\tau_F = R_F C_F$. Normally calculate τ_F to be approximately equal to [3/(baud rate)] seconds.

The lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510kΩ, the minimum value of C_D can be determined by: $C_D(\mu F) \approx 16$/capture range in Hz.

Note: Excessive values of C_D will unnecessarily slow the lock-detect response time.

The XR-2211 has three npn open-collector outputs, each of which is capable of sinking up to 5mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output which goes low when a carrier is detected, and Pin 6 is the Q lock-detect output which goes high when lock is detected. If Pin 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied, and will be LOW when no carrier is present. If the lock-detect feature is not required, Pins 3, 5 and 6 may be left open-circuited.

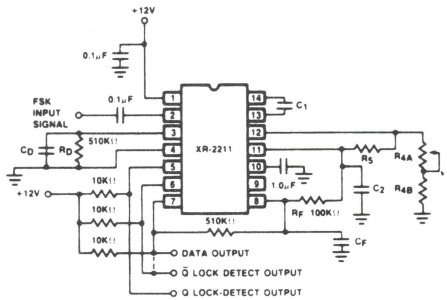
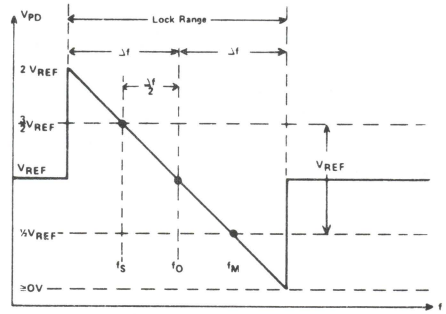


Figure 4: The XR-2211 FSK Demodulator with Carrier Detect



XR-2211 Tracking Characteristics

As seen above, the XR-2211 produces at its phase detector output a voltage V_{PD}, which has a peak to peak value equal to about V_{REF} for a frequency swing from f_M (mark) to f_S (space). The DC level V_{PD} will be about $V_{REF}\left(\frac{V^+ - .65}{2}\right)$.

Circuit Design

Table 2 shows recommended component values for the three most commonly used FSK bands. In many instances, system constraints dictate the use of some non-standard FSK bands. The XR-2206/XR-2207/XR- 2211 combination is suitable for any range of frequencies from several Hertz to 100 KiloHertz.

Here are several guidelines to use when calculating non-standard frequencies:

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55 % of the upper frequency (less than a 2:1 ratio).
- For minimum demodulated output pulse-width jitter, select an FSK band whose mark and space frequencies are both high, compared to the baud rate. (i.e. for a 300 baud channel, mark and space frequencies of 2025Hz and 2225Hz would result in significantly less pulse-width jitter than 300Hz and 550Hz).
- For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship mark-space frequency difference (Hz) – < 83% maximum data rate (baud) should be observed.

For narrower spacing, the minimum ratio should be about 67%. As spacing is reduced, tuning difficulties (of the XR-2211) increase. Signal-to-noise performance will be degraded as well.

The values shown in Table 2 may be scaled proportionately for mark and space frequencies, maximum baud rate, and (inversely) capacitor value. It is best to retain (approximately) the resistor values shown.

Design Examples

I. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.

A. Frequency Calculation
Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore chose an upper frequency:

$$\frac{83 \times 10{,}000}{45} = 18.444\text{kHz} \approx 18.5\text{kHz}.$$

and the lower frequency:

$0.55 \times 18.5\text{kHz} = 10.175\text{kHz}$.

B. Component Selection
1. For the XR-2207 FSK modulator, set $R_1 \approx 30\text{k}\Omega$. Now, select a value of C_o to generate 10.175kHz with R_1:

$10.175\text{kHz} = 1/(C_o \times 30{,}000)$; $C_o = 3300\text{pF}$.

To choose R_2:

$18.500\text{kHz} - 10.175\text{kHz} = 8.325\text{kHz} = 1/C_oR_2$; $R_2 = 36\text{k}\Omega$.

A good choice would be to use 10kΩ potentiometers for R_{1A} and R_{2A}, and to set $R_{1B} = 24\text{k}\Omega$ and $R_{2B} = 30\text{k}\Omega$.

Table 2. Recommended Component Values for Typical FSK Bands V_{CC} = 12 VDC, V_{EE} = 0V

FSK Band			XR-2207					XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{1A} R_{3A}	R_{1B} R_{3B}	R_{2A} R_{4A}	R_{2B} R_{4B}	C_O	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_{4A}	R_{4B}	R_5	C_1	C_2	C_F	C_D
300	1070	1270	10	20	100	100	.039	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
300	2025	2225	10	18	150	160	.022	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05
1200	1200	2200	20	30	20	36	.022	10	16	20	30	.022	10	18	30	.027	.0033	.0022	.01

Units: Frequency — Hz; Resistors — kΩ; Capacitors — μF

2. For the XR-2206, we can make R_7 equal to R_1, and C_3 equal to C_O above. To determine R_6:

   $18.5kHz = 1/R_6C_3$; $R_6 = 16k\Omega$

   Use at $10k\Omega$ potentiometer for R_{6A} and set $R_{6B} = 13k\Omega$.

3. For the XR-2211 demodulator, we need to first determine R_4 and C_1. First, $f_o = (f_L + f_H)/2 = (10.175 + 18.500)/2 = 14.338kHz$. If we make $R_4 = 25k\Omega$, then $1/(C1 \times 25,000) = 14,338$; $C_1 = 2790pF \approx 2700pF$. With that value of C_1, the precise value of R_4 is now $25.8k\Omega$. Select $R_{4B} = 18k\Omega$ and use a $10k\Omega$ for R_{4A}.

C. Frequency Component Selection

1. To calculate R_5, we first need our Δf, which is 18,500 – 10.175, or 8.325kHz:

   $8325 = (25,800 \times 14,338)/R_5$
   $R_5 = 44.4k\Omega \approx 47k\Omega$.

2. To determine C_2 use $\zeta = 1/2 = 1/4\ C_1/C_2$. Then, $C_2 = 1/4C_1$; $C_2 = 670pF$:

3. To select C_F, we use τ_F = [0.3/(baud rate)] seconds:

   $\tau_F = 3/10,000 = 30\ \mu sec.$

   with

   $R_F = 100k\Omega$, $C_F = 300pF$

D. Lock Range Selection
To select C_D, let us start with the actual lock range:

$\Delta f = R_4f_o/R_5$ Hz = 7870Hz

If we assume a capture range of 80%:

$\Delta f_C = 6296Hz$

therefore, our total capture range of $\pm\Delta f_C$ is 12,592Hz. Our minimum value for C_D is (16/12,592) μF or $0.0013\mu F$.

E. Completed Circuit Example
See Figure 5.

II. Design a 3 kilobaud modem to operate with low output jitter. The bandwidth available is 13kHz.

For this modem, we can take the values from two for the 300 baud modem operating at 1070Hz and 1270Hz, multiply our baud rate and mark and space frequencies by ten, and divide all capacitor values on the table by ten. Resistor values should be left as they are.

III. Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600Hz and 900Hz, and 1400 and 1700Hz (each of these channels could handle about 400 baud).

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between $10k\Omega$ and $100k\Omega$: R_1, R_1/R_2, R_3 and R_3/R_4. The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about $20k\Omega$, we have: $1700 = 1/(C_o \times 20,000)$; $C_o = 0.029\ \mu F$ which is approximately equal to $0.033\mu F$.

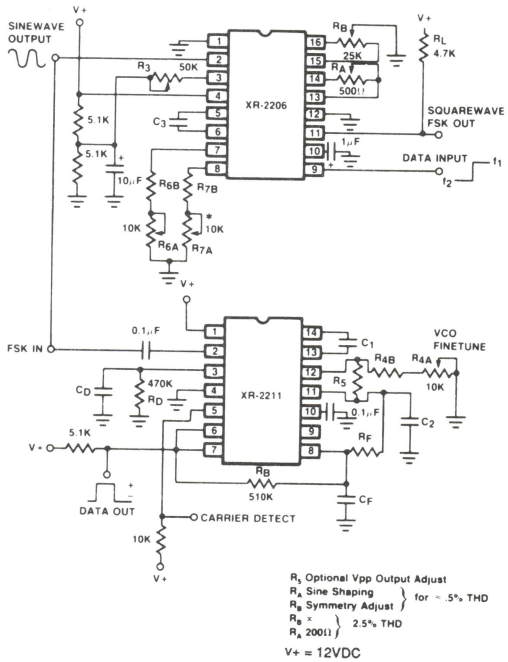


Figure 5: Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values)

Calculating R_1 using 600Hz and 0.033µF, we get R_1 = 50,5kΩ. We can use R_{1B} = 47kΩ and R_{1A} = 10kΩ. For R_2, we get 101kΩ. Use R_{2B} = 91kΩ and R_{2A} = 20kΩ. To determine R_3, use: 1400Hz = $1/R_3C_o$, which gives us R_3 = 21.6kΩ. Use R_{3B} = 18kΩ and R_{3A} = 5kΩ. R_4 must generate a 300Hz shift in frequency, the same as R_2. Therefore, set R_4 equal to R_2.

For 5VDC single supply operation of the XR-2211 R_S should be within the range 100kΩ ≤ R_S ≤ 1MΩ. Timing capacitor C_1 and loop damping capacitor C_2; as well as timing resistors R_{4A} and R_{4B} should be adjusted as needed by recalculating their values.

Adjustment Procedure

The only adjustments that are required with, any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

The XR-2207: Always adjust the lower frequency first with R_{1B} or R_{3B} and a low level on Pin 9. Then with a high level on Pin 9, adjust the high frequency using R_{2B} or R_{4B}. The second adjustment affects only the high-frequency, whereas the first adjustment affects both the low- and the high-frequencies.

The XR-2206: The upper and lower frequency adjustments are independent, and the sequence is not important.

The XR-2211: With the input open-circuited, the loop-phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_o can be monitored:

1. Apply an alternating mark and space frequency pattern and adjust until an alternating pattern is obtained.
2. Short Pin 2 to Pin 10 and measure f_o at Pin 3 with C_D disconnect; or
3. Open R_5 and monitor Pin 13 or 14 with a high-impedance probe

Note: *Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.*

For further information regarding the use of the XR- 2207, XR-2206 and XR-2211 refer to the individual product data sheets.

XR-C240 Monolithic PCM Repeater

Application Note

INTRODUCTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rates on T1 type PCM lines. The device is packaged in hermetic 16-pin DIP package and is designed to operate over a temperature range of –40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities. Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

THE T-1 REPEATER SYSTEM

The TI Repeater Line is designed to provide a transmission capability for 24 two-way voice frequency signals which are transmitted digitally using a Pulse-Code Modulation (PCM) technique. The system operates at a data rate of 1.544 MBPSs, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772kHz is less than 36dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end crosstalk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The details of the T-1 type PCM systems are well covered in the literature listed in References 1 through 5.

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The dc power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

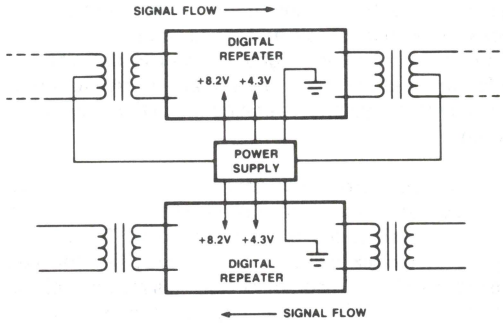


Figure 1. Block Diagram of a Bi-directional Digital Repeater System

The XR-C240 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C240 ICs; one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C240 monolithic IC.

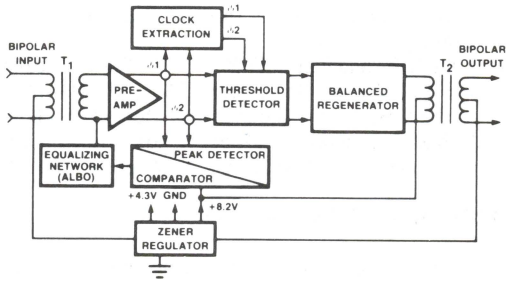


Figure 2. Functional Block Diagram of a Digital PCM Repeater Section

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization , in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse is in turn applied to a discrete switch which is used to drive the next section of the paired cable.

REFERENCES ON PCM REPEATERS

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25–97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99–143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1–25.
4. Fultz, K. E., and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405–1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5–46-10.

OPERATION OF THE XR-C240

The XR-C240 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line (DIP) package.

The circuit is designed to operate with two positive supply voltages, V++ and V+ which are nominally set to be 8.2V and 4.3V, respectively, Figure 4 gives a typical recommended power supply connection for the circuit.

The supply currents I_A and I_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 8.2V supply voltage, I_A:

$1.1mA \leq I_A \leq 2.5mA$

b. Current from 4.3V supply voltage, I_B:

$6mA \leq I_B \leq 11mA$

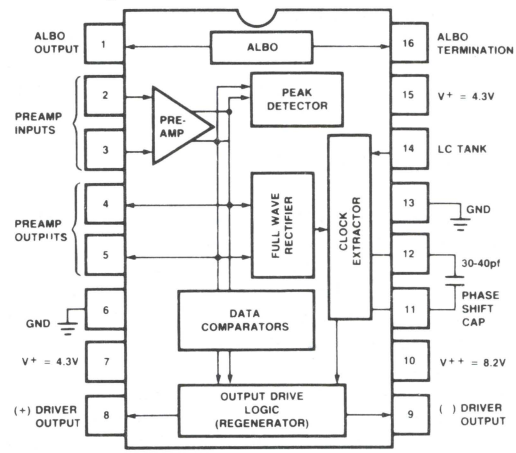


Figure 3. Package Diagram of XR-C240 Monolithic PCM Repeater

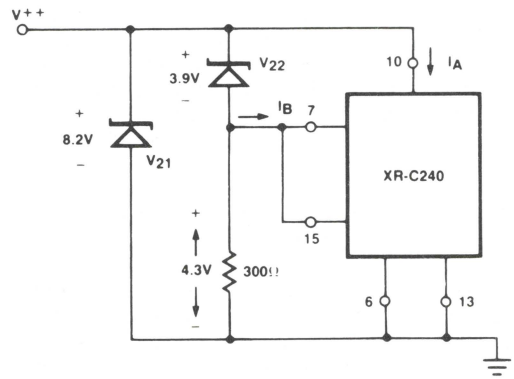


Figure 4. Recommended supply Voltage Connection for XR-C240. (Note: See Figure 6 for Recommended bypass capacitors)

ELECTRICAL CHARACTERISTICS

(Measured at 25°C with V++ = 8.2V, V+ = 4.3V, unless specified otherwise)

PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
Supply Voltage:				
V++	7.79	8.61	V	Measured at Pin 10
V+	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current:				See Figure 4
I_A	1.1	2.5	mA	Supply = 8.2V
I_B	6	11	mA	Supply = 4.3V
Total Current	7.1	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	db	
Input Bias Current, I_B		4	µA	
Input Offset Current, I_{OS}		2	µA	
Input Impedance, R_{IN}	50		kΩ	
Comparator Thresholds				See Figure 8 Measured Differentially Across Pins 4 and 5
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				See Figure 10
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	µA	
"One" Signal Current	80	220	µA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	−18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero
Output Drive Section				See Figure 12 Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100Ω
Low Output Voltage	0.65	0.95	V	Referenced to Pin 7, I_L = 30mA
Output Leakage Current		50	µA	
Output Pulse				See Figure 13
Maximum Pulse Width Error		±30	ns	
Rise and Fall Times		80	ns	

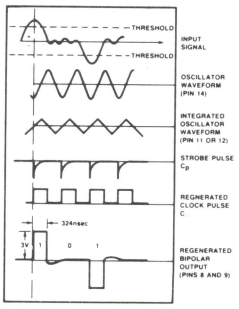


Figure 13. Typical Timing Waveforms for a 1-0-1 Input Data Pattern

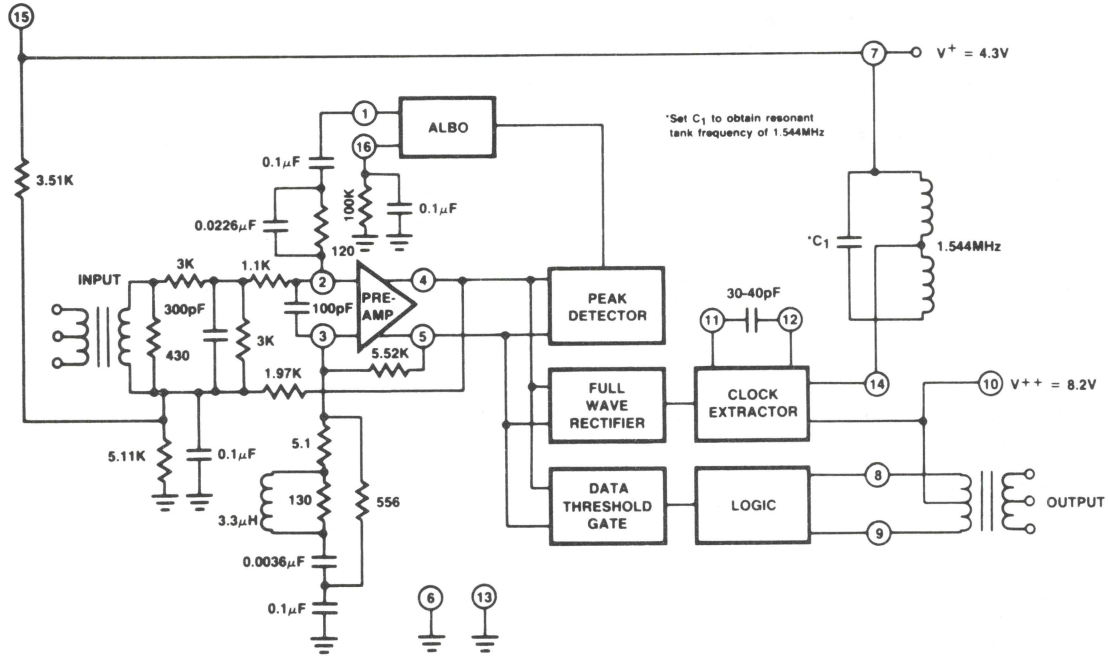


Figure 5. External Components Necessary for Circuit Operation

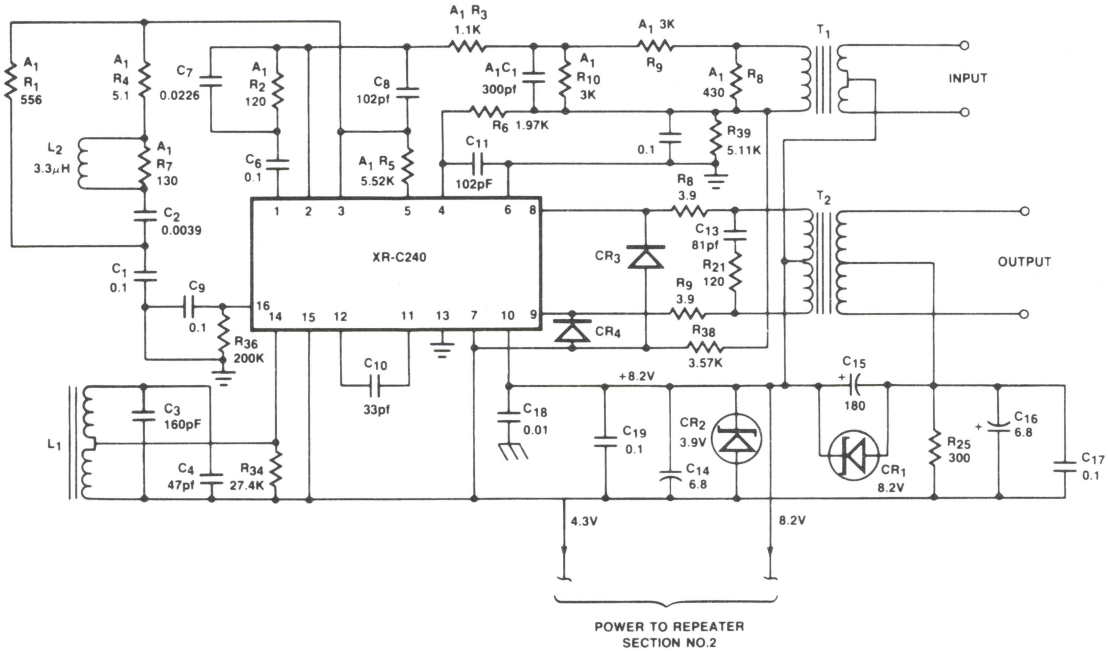


Figure 6. A typical Circuit Connection for XR-C240 in 1.544MHz T-1 Repeater System

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 6 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 4).

Figure 6 shows a practical circuit connection for the XR-C240 in an actual PCM repeater application for 1.544MBPS T-1 Repeater application. For simplification purposes, the lightening protection circuitry and the second repeater section are not shown in the figure.

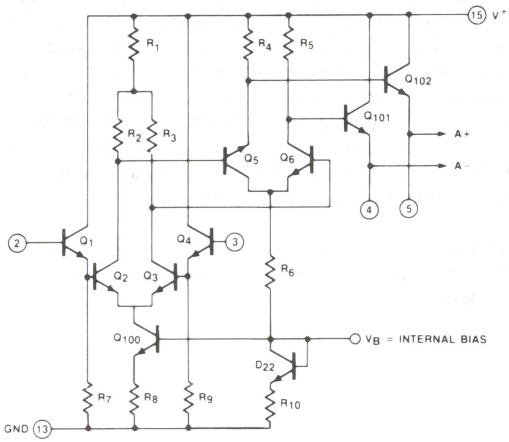


Figure 7. Circuit Diagram of Preamplifier Section

DESCRIPTION OF CIRCUIT OPERATION

This section gives a brief description of the internal circuitry contained within the XR-C240 monolithic IC.

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband voltage gain of 52dB. The differential outputs of the preamplifier (Pins 4 and 5) are internally connected to the peak-detector, full-wave rectifier and the threshold detector sections of the XR-C240 as shown in Figure 8.

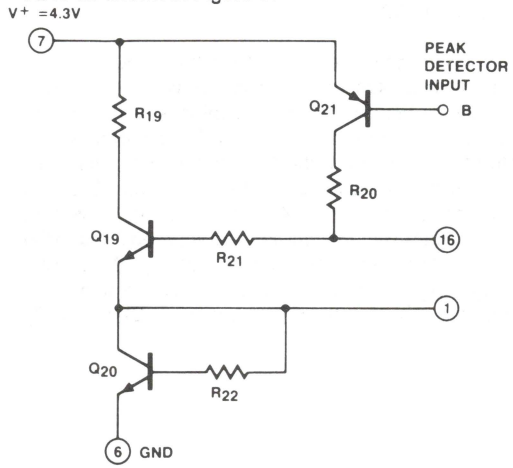


Figure 9. Automatic Line Build-Out (ALBO) Section

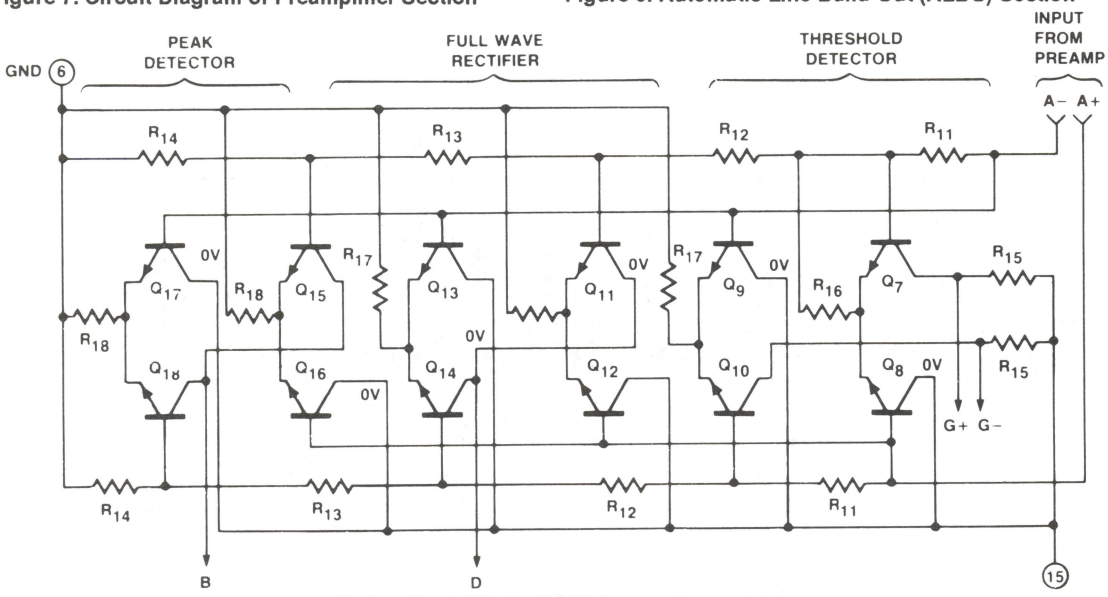


Figure 8. Circuit Diagram of Threshold-Detector, Full-Wave Rectifier and Peak-Detector Sections

The peak-detector output (terminal B of Figure 8) is internally connected to the Automatic Line Build Out (ALBO) section of the circuit and controls the DC bias current through the ALBO diodes Q_{19} through Q_{20}, as shown in Figure 9.

The full-wave rectifier output (output D of Figure 8) is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (Pin 14) of the injection locked oscillator. The threshold-detector outputs (G+ and G– of Figure 8) provide the differential logic drive to the data latches of the logic section of XR-C240.

The clock-extractor section of XR-C240 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{23}, through terminal D which is internally connected to the output of the threshold comparator. This signal in turn controls the current in the resonant L-C tank circuit connected to Pin 14. The sinusoidal waveform across the tank is then amplified and squared through the cascaded differential gain stages made up of Q_{31}, Q_{32} and Q_{35}, Q_{36}. The output swing of the second gain stage is "integrated" by the phase- shift capacitor, C_1, externally connected to Pins 11 and 12. (See timing diagrams of Figure 13.) The nominal value of this capacitor is in the 30 to 40pF range. The triangular waveform across Pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the "strobe" signal, C_p, and the clock pulse C_ϕ, which is applied to the data latches of the logic section.

The strobe and clock pulses out of the clock-regenerator section are applied to the output data latches shown in Figure 11. The two parallel output R-S flip-flops are driven by the differential inputs (G+ and G–) from the data comparator of Figure 8. The two sets of differential data signals, F_1, $\overline{F_1}$ and F_2, $\overline{F_2}$ are then applied to the output driver amplifier shown in Figure 12. The high-current outputs of the driver stage (Pins 8 and 9) are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage spread, i.e.:
Peak Output Swing = $(V^{++}) - (V^{+}) - (V_{BE}) \simeq 3.2V$

The output stage is designed to work into a nominal load impedance of 100Ω, and can handle peak load currents of 30mA.

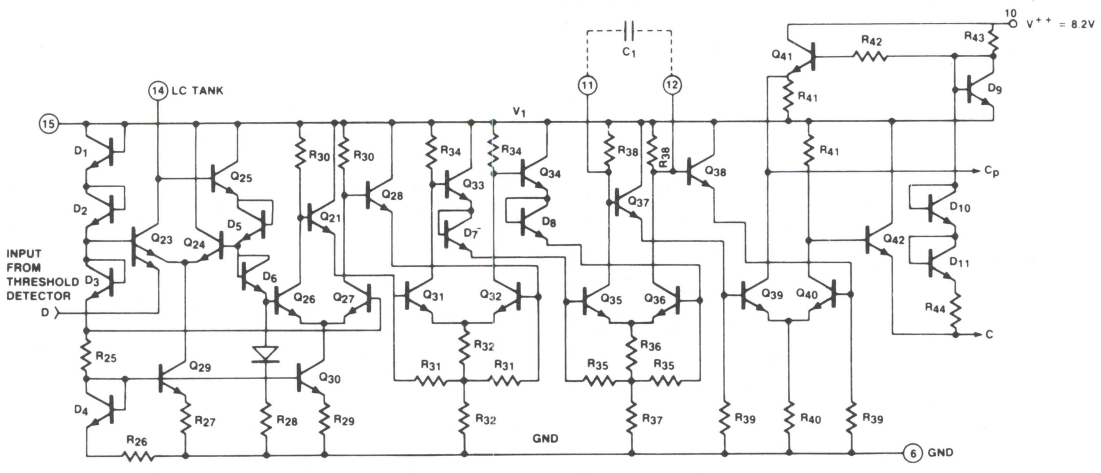


Figure 10. Circuit Diagram of Clock Extractor Section

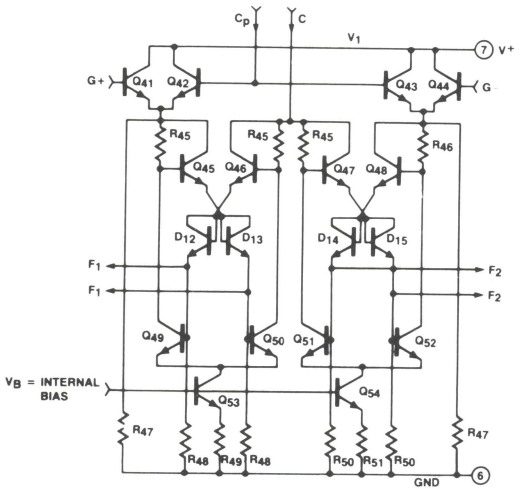


Figure 11. Data Output Latches (Logic Section)

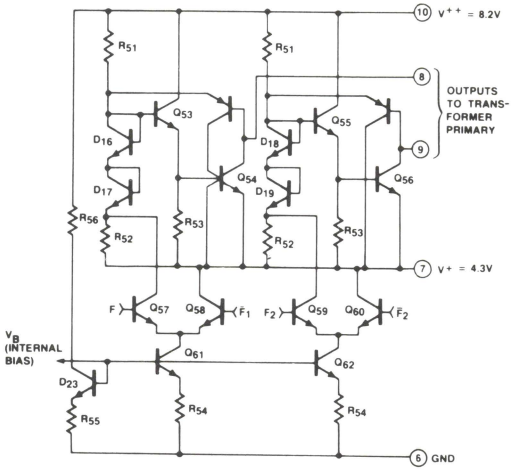


Figure 12. Output Driver Section



NOTES



XR-C277 Low-Voltage PCM Repeater IC

Application Note

INTRODUCTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of –40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltages (6.3 volts and 4.4 volts) with a supply current of less than 13mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

FUNDAMENTALS OF PCM REPEATERS

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. The XR-C277 monolithic IC replaces about 90% of the electronic components and circuitry within the digital repeater sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C277 IC's, one for each direction of information flow.

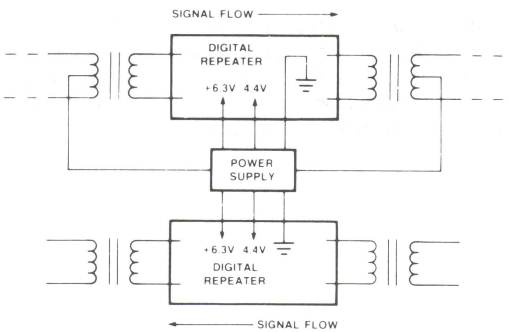


Figure 1. Block Diagram of a Bi-Directional Digital Repeater System

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C277 monolithic IC.

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium, is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

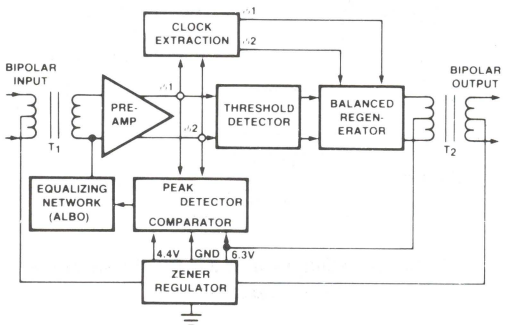


Figure 2. Functional Block Diagram of a PCM Repeater System

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse in turn applied to a discrete output transformer which is used to drive the next section of the paired cable.

Additional References on PCM Repeaters:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals,: B.S.T.J., Vol. 41, January, 1962, pp. 25–97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant,: B.S.T.J., Vol. 41, January, 1962, pp. 99–143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks,: B.S.T.J., Vol. 41, January, 1962, pp. 1–25.
4. Fultz, K. E. and Penick, D. B., "The T-1 Carrier System,: B.S.T.J., Vol. 44, September, 1965, pp. 1405–1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 – 46-10.

OPERATION OF THE XR-C277

The XR-C277 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16- pin dual-in-line package.

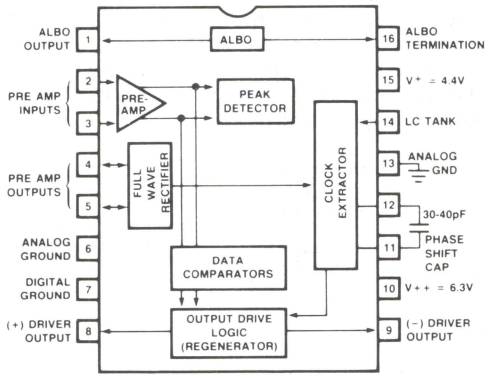


Figure 3. Package Diagram of XR-C277 Monolithic PCM Repeater

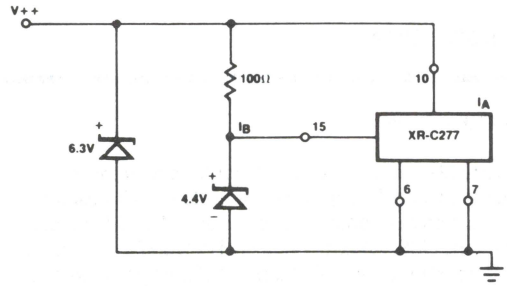


Figure 4. Recommended Supply Voltage Connection tor XR-C277 (Note: See Figure 6 for Recommended Bypass Capacitors)

The circuit is designed to operate with two positive supply voltages, V++ if and V+ which are nominally set to be 6.3V and 4.4V, respectively. Figure 4 gives the recommended power supply connection for the circuit. The supply currents 1_A and 1_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 6.3V supply voltage, I_A:

$2.5mA \leq I_A \leq 4.0mA$

b. Current from 4.4V supply voltage I_B:

$7mA \leq I_B \leq 9mA$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 5 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 3).

Figure 6 shows a practical circuit connection for the XR-C277 in an actual PCM repeater application for 1.544Mbps T-1 Repeater application. For simplification purposes, the lightning protection circuitry and the second repeater section are not shown in the figure.

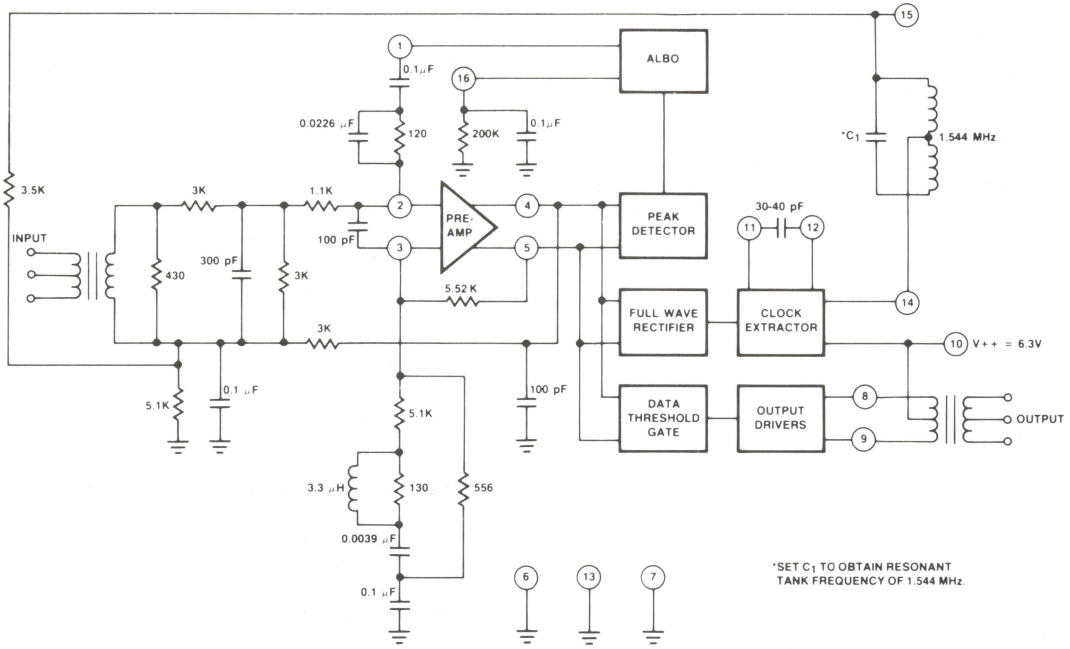


Figure 5. External Components Necessary for Circuit Operation in 1.544MHz T-1 Repeater

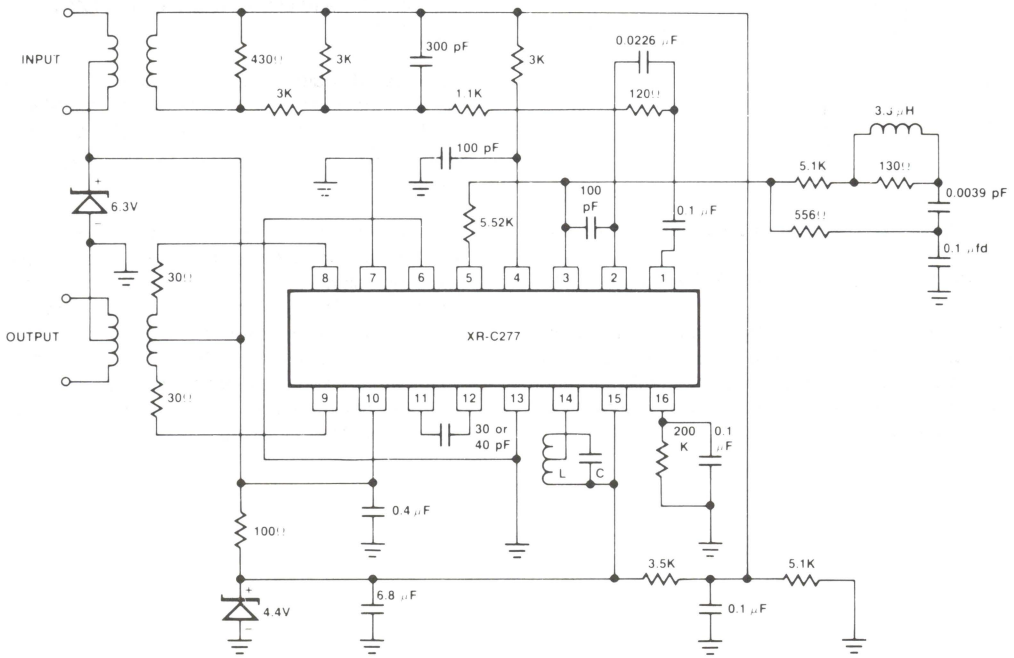


Figure 6. Typical Circuit Connection of XR-C277 in 1.544MHz T-1 Repeater System. (Note: Set L and C to Form a High Q Tank Resonant at 1.544MHz. It is Recommended that Q?100, and C ≈ pF for most applications)

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Fig. 7):

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband differential voltage gain of 52 dB. The differential outputs of the preamplifier, Pins 4 and 5, are internally connected to the peak-detector, full-wave rectifier and the data threshold detector sections of the XR-C277.

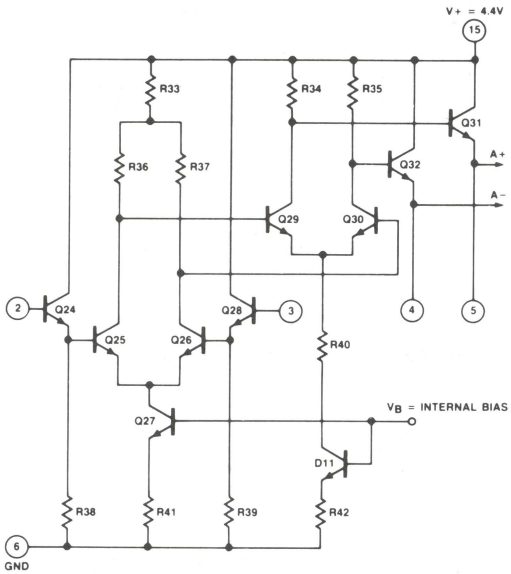


Figure 7. Circuit Diagram of Preamplifier Section

Automatic Line Build-Out (ALBO) Section (Fig. 8):

The ALBO function is achieved by controlling the dynamic impedance of ALBO diodes (Q_{21} and Q_{22}). The current which sets this dynamic impedance is supplied through Q_{21} and is controlled by the peak-detector output level applied to base of Q_{23}.

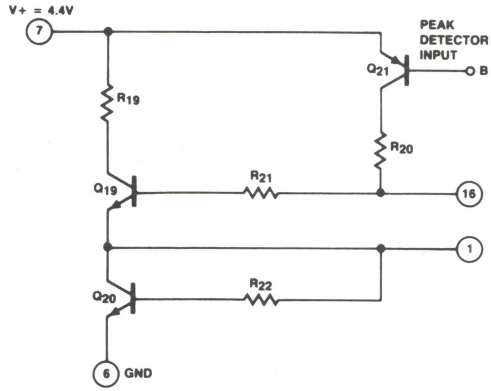


Figure 8. Automatic Line Build-Out (ALBO) Section

Data-Threshold Detector; Full-Wave Rectifier and Peak Detector Sections (Figure 9):

The level detector and peak rectifier sections of the XR-C277 are made up of two sets of gain stages which are driven differentially with the (A+) and (A−) outputs of the preamplifier section. The outputs of the data threshold comparators, D+ and D− activate the data latches shown in Figure 11.

The peak-detector output, terminal B of Figure 9, is internally connected to the Automatic Line Build-Out (ALBO) section of the circuit and controls the dc bias current through the ALBO diodes Q_{21} through Q_{22}, as shown in Figure 8.

The full-wave rectifier output is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (Pin 14) of the injection locked oscillator. The detection thresholds of the comparators are set by the resistor chains (R_{45}, R_{47}, R_{51}, R_{55}) and (R_{46}, R_{48}, R_{52}, R_{56}). The resistor ratios are chosen such that the data threshold is 50% of the ALBO threshold; and the clock extractor threshold is 73% of the ALBO threshold.

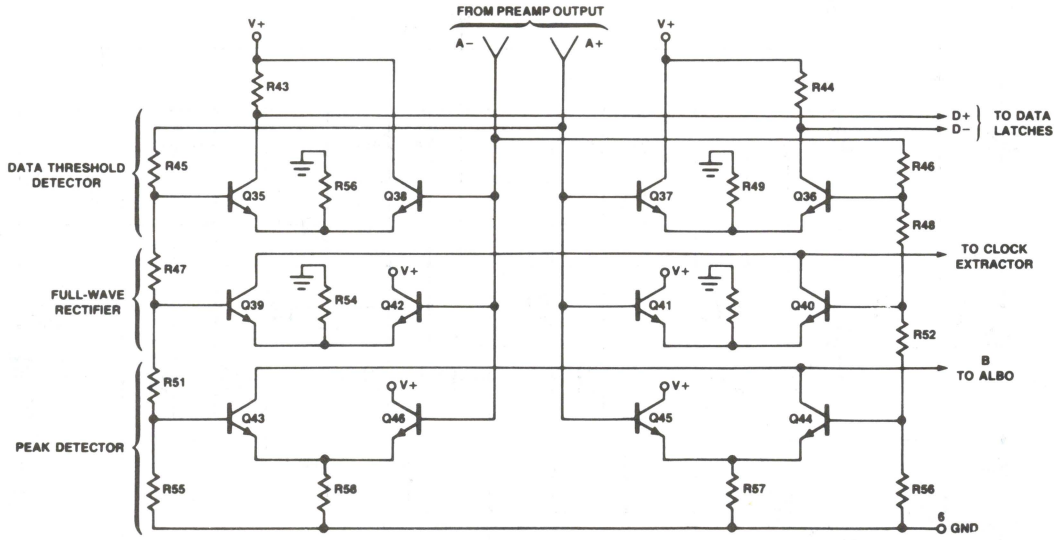


Figure 9. Data-Threshold Detector, Full-Wave Rectifier and the Peak Detector Sections of XR-C277

Clock Extractor Section (Figure 10):

The clock-extractor section of XR-C277 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{1B}, from the output of the full-wave rectifier. This signal in turn controls the current in the resonant L-C tank circuit connected to Pin 14. The sinusoidal waveform across the tank is then amplified and squared through two cascaded differential gain stages made up transistors Q_3 through Q_9. The output swing of the second gain stage is integrated by the phase-shift capacitor, C_1, externally connected to Pins 11 and 12. See timing diagrams of Figure 13. The nominal value of this capacitor is in the 30 to 40pF range. The triangular waveform across Pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the strobe signal, C_D, and the clock pulse C_ϕ, which are applied to the data latches of the logic section.

Data-Latch and Output Driver Sections (Figures 11 and 12):

The data-latch section consists of two parallel flip-flops, driven by the D+ and D− inputs from the data-threshold detector. When the D+ input is at a low state, the sampling or strobe pulse, C_p, is steered through Q_{47A} and sets Flip-Flop 1, on the leading edge of C_p. Conversely, when D- input is at a low state, the sampling pulse is steered through Q_{47B} to set Flip-Flop 2. Each flip-flop section is then reset at the trailing edge of the clock pulse input, C_ϕ. The flip-flop outputs, (F_1, F_1) and (F_2, F_2) are then used to drive the output drivers. This logic arrangement results in an output pulse width which is the same as the extracted clock pulse width (See timing diagram of Figure 13.)

The outputs of the two data latches drive the two output driver stages shown in Figure 12. The high-current outputs of the driver stage, Pins 8 and 9, are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage at Pin 10. The output stages are designed to work into a nominal load impedance of 100Ω, and can handle peak load currents of 30mA.

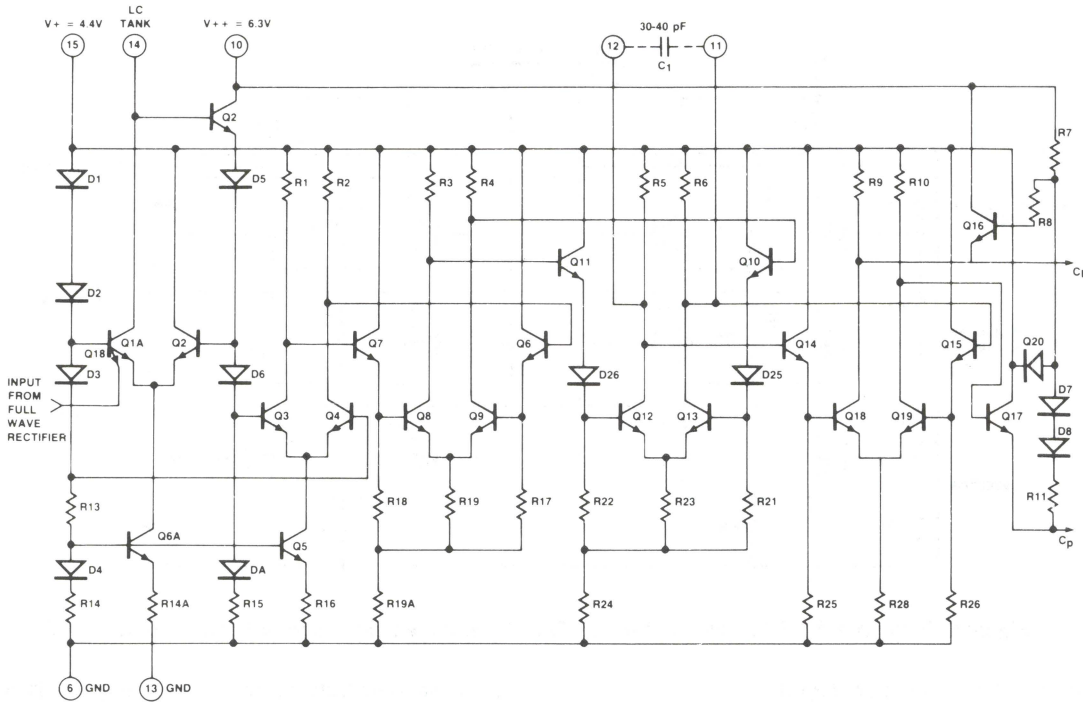


Figure 10. Circuit Diagram of Clock Exctractor

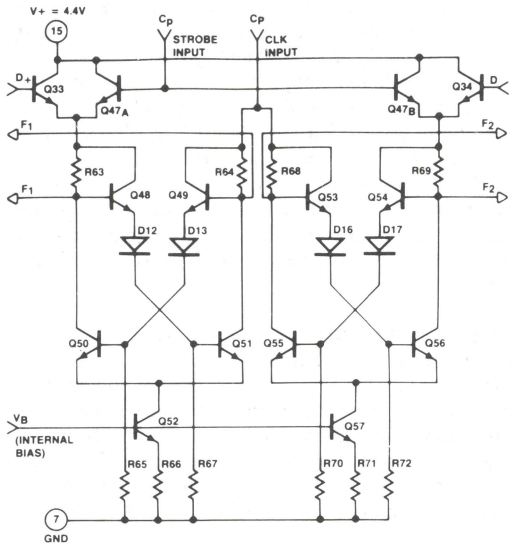


Figure 11. Data-Latch Section of XR-C277

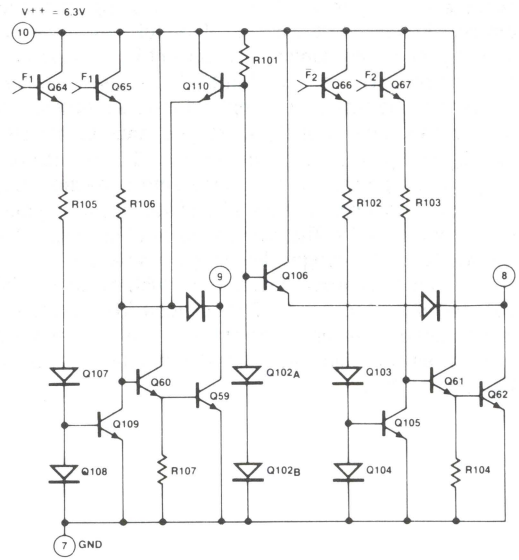


Figure 12. Output-Driver Section

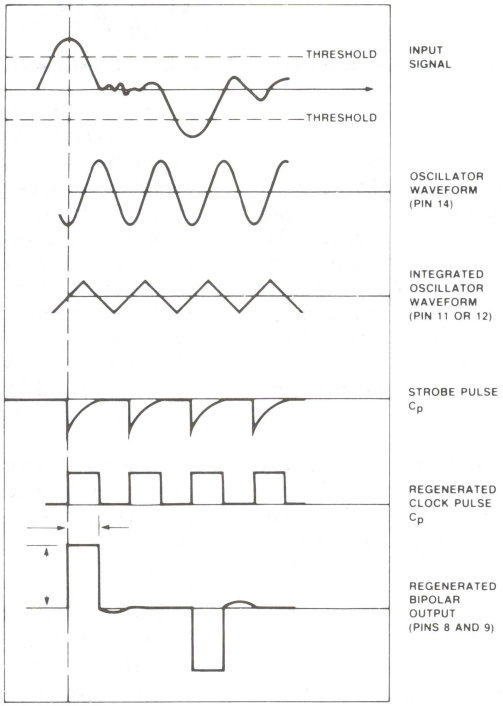


Figure 13. Typical Timing Waveforms for a 1-0-1 Input Data Pattern

Three-State FSK Modem Design Using XR-2207 and XR-2211

Application Note

INTRODUCTION

This application note describes the design principle, and the operation of three-state frequency-shift keyed (FSK) modems for industrial process control systems. Compared to conventional bi-state modems, which utilize only the mark and space frequencies, the three- state modems utilize a third frequency, the carrier signal, for additional command and control functions. This carrier-control feature allows each modem system connected to a central processor (CPU) to be interrogated or activated, one at a time, without interference from the other modem transmitters or receivers within the same system.

The design and operation of conventional bi-state FSK modems using the XR-2206 modulator, and the XR- 2211 demodulator, are covered in Exar's Application Note, AN-01. This application note extends these basic concepts to the design of FSK modulators or demodulators with three-state operation capability.

PRINCIPLES OF OPERATION

In a wide variety of industrial process control applications, it is necessary to have a number of separate sensors and controllers activated by a centralized computer or processing unit (CPU). This can be achieved by operating a number of separate FSK modulator/demodulator (modem) stations over a common set of telephone lines, and address them one at a time from the CPU. The simplified block diagram of such a process controlled system is shown in Figure 1. In many such cases, such a process control system also makes use of the distributed-intelligence concept by employing a separate data acquisition system at each control station. Such an intelligent data acquisition system is normally made up of a microprocessor, along with its A/ D and D/A converter circuitry, which will interface with the sensors and the control machinery. An FSK modem will interface with the telephone wires going back to the central command unit, the CPU.

In the conventional operation of FSK modems, they operate in their bi-state mode, i.e., the information to be transmitted or received is available in two states, corresponding to either a mark or a space frequency. In a complex process control system, such as the one shown in Figure 1, the versatility of the system can be greatly enhanced by operating the FSK modulator/ demodulator in three-state mode, where the information to be transmitted or received is available in three states, i.e., a mark or space frequency, or a carrier signal, which is normally a tone having a frequency halfway between the mark and space frequencies.

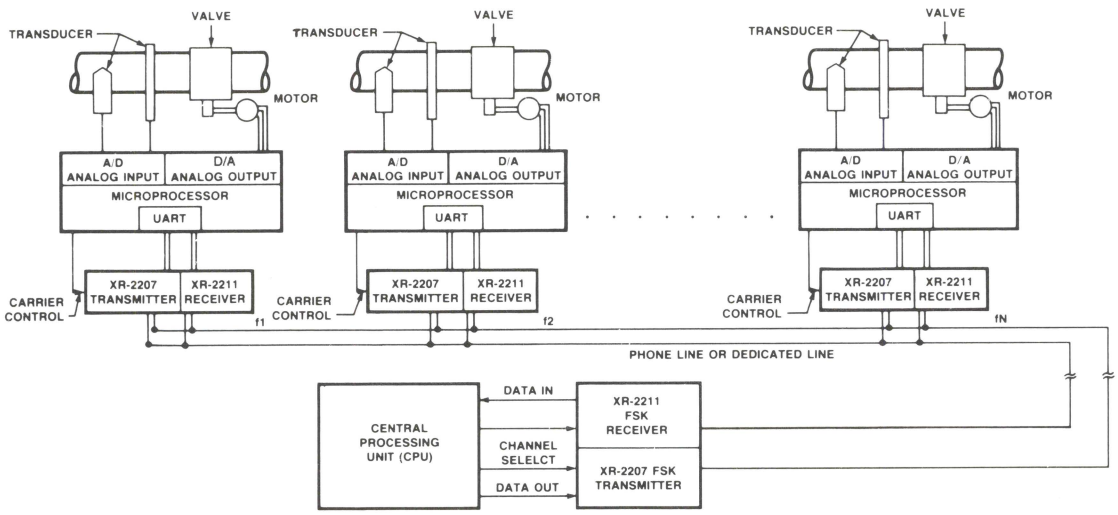


Figure 1. Simplified Block Diagram of a Complex Process Control System with Multiple FSK Modems

Figure 2 shows a detailed block diagram of a complete three-state FSK modem system. The system is made up of five blocks:

(a) FSK transmitter or encoder which converts the input data or logic signals into transmitted mark, space, and carrier tones.

(b) FSK receiver or decoder which converts the frequency signals sent over the telephone lines into binary logic signals.

(c) Transmitter bandpass filter which band-limits the frequency output of the transmitter to the allocated transmitter bandwidth.

(d) Receiver bandpass filter which limits the incoming signals to those frequencies which fall within the allocated receiver bandwidth.

(e) A line hybrid, or a 4-wire to 2-wire transformer, which isolates or decouples the transmitter output from the receiver input.

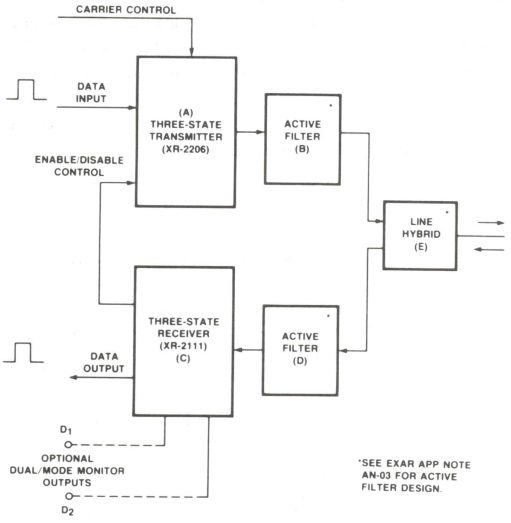


Figure 2. Block Diagram of a Three-State FSK Modem System

The first 2 blocks, the FSK transmitter and the receiver, are the essential part of the modem system. The remaining three blocks, namely the active filters and the line-hybrid, are support circuits, depending on the frequency-band requirements or the necessary telephone line interconnections. Detailed descriptions and design examples for these active filters are given in Exar's Application Note, AN-03. Switched capacitor filters, such as the XR-1010 can be used as well.

The three-state modem is designed to operate in two separate frequency bands: A transmit-band for the transmitted data, and a receive-band for the incoming frequencies. In certain operating modes, such as the half-duplex operation, these frequency bands may be one and the same. In its most general case, the frequency information associated with the three-state modem system (Figure 2) is concentrated in three discrete frequencies in each of the transmit- and receive-bands. These are:

Transmit-Band (transmitter output):

f_{T1} = Transmitter mark frequency

f_{T2} = Transmitter space frequency

f_{T0} = Transmitter carrier or center frequency

Receive-Band (receiver input):

f_{R1} = Receiver mark frequency

f_{R2} = Receiver space frequency

f_{R0} = Receiver carrier or center frequency

Normally, the mark and space frequencies are chosen to be near the opposite edges of the receive- or transmit-band, and the carrier frequency is chosen to be at the center of the corresponding band.

When activated by the enable/disable control, the three-state transmitter generates either the FSK mark/space frequencies, f_{T1} and f_{T2}, or the carrier frequency, f_{T0}. The carrier frequency is activated by the carrier control input, and can override the input data.

The three-state receiver provides two outputs: A binary data output, when activated by the input mark/space frequencies, f_{R1} and f_{R2}, and a logic signal, to control or enable the transmitter when the receiver-carrier frequency, f_{R0}, is present. As an option, it may have a dual-mode operation capability which can provide serial data outputs for half-bandwidth deviations of the input signal, i.e., for FSK signals comprised of center-to-mark or center-to-space frequency shifts. The data outputs corresponding to this mode of operation are shown as outputs, D_1 and D_2 of Figure 2.

CIRCUIT OPERATION

The generalized three-state modem system of Figure 2 can operate in a multiplicity of modes. Some of these are outlined below:

Answerback Under CPU Control

The modem will be in a standby mode with the transmitter disabled, and the receiver in a standby condition with its data output disabled. It will be activated only when an interrogate tone at the receiver center frequency, f_{R0}, is transmitted by the control modem unit associated with the CPU (see Figure 1). This tone is detected by the receiver; it activates the transmitter via its enable/disable control, and instructs the local microprocessor to transmit its status information via the local transmitter. This data is transmitted as an FSK signal made up of the transmit mark and space frequencies f_{T1} and f_{T2}. When the information transmission is complete, or when the interrogate tone is discontinued, the entire modem system again reverts back to its standby mode.

Receive Under CPU Control

In this mode of operation, the transmitter remains disabled, the receiver is at its standby mode with its data output disabled. When the FSK data is sent by the CPU modem transmitter, at the mark/space frequencies, f_{R1} and f_{R2}, the data output is enabled, and the decoded binary data is fed into the local microprocessor. Since the center receive-frequency, f_{R0}, is not transmitted, the transmitter remains disabled.

Priority-Transmit Request

In an emergency situation, the local transmitter can be activated by its carrier-control input, which causes it to transmit a tone, f_{T0}, at its center frequency. When this tone is received by the CPU, it will be treated as a priority request to transmit information; the CPU will immediately interrogate the corresponding local modem by sending out its address tone at frequency, f_{R0}.

Dual-Channel Receive

As an option, the receiver can provide serial data outputs, through separate terminals, D1 and D2 of Figure 2, for half-bandwidth deviations of the input FSK signals. In this mode, the input data will be in the form of center-to-mark frequency shifts for one channel, and center-to-space shifts for the other. This mode of operation allows two separate sets of data or control instructions to be transmitted within the same channel bandwidth, provided that only one of these channels is used at any one time.

Dual-Channel Transmit

As an option, the transmitter can also transmit two separate channels, using half-bandwidth deviations of the transmit signal. In this case, the outgoing data will be encoded with center-to-mark transitions of the transmitter frequency in one of the channels, and center-to-space transitions in the other. However, similar to the case of the receiver, only one or the other, and not both, of these half-bandwidth channels can be on at a given time.

XR-2207 As A Three-State FSK Transmitter

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) circuit with excellent temperature stability. It provides simultaneous triangle and square wave outputs, and can be keyed to any one of four preprogrammed frequencies by means of external logic signals. These four discrete frequencies are preprogrammed by the choice of four external timing resistors.

Figure 3 shows a functional block diagram of the XR-2207 monolithic FSK generator chip. The circuit is comprised of four functional blocks: A variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs, and buffer amplifiers for both the triangle and square wave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors, to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals.

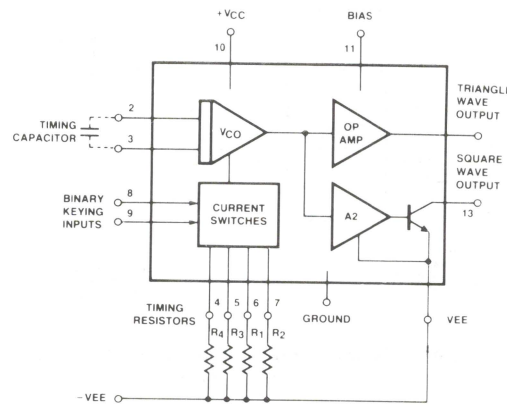


Figure 3. Functional Diagram of XR-2207 Monolithic FSK Generator

The frequency of oscillation is set by an external timing capacitor, and by the combination of one or more of the external timing resistors, R_1 through R_4. The keying terminals switch these external resistors in and out of the circuit and thus control the operating frequency. Table 1 shows the four discrete frequencies which can be obtained as a function of four logic states at Pin 8 and 9. It should be noted that the frequency is inversely proportional to the timing resistor connected to the activated timing pin. For example, if only one of the timing pins, say Pin 5, is activated and its associated resistor, R_3, is left open-circuited (i.e., $R_3 = \infty$) the oscillator will be keyed OFF since this corresponds to a zero-frequency state.

Table 1. Output Frequency of the XR-2207 as a Function of the Keying Logic

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pins 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

(* Frequency in Hz, R in Ohms and C in Farads.)

Figure 4 shows the recommended circuit connection of the XR-2207, for its operation as a three-state FSK transmitter. The three resistors, R_1, R_2 and R_4, are used to set the three discrete frequencies to be transmitted in accordance with the frequency expressions given in Table 1, where:

$$f_{T1} = \frac{1}{C_0R_1} \quad f_{T2} = \frac{1}{C_0R_1} + \frac{1}{C_0R_2} \quad f_{T0} = \frac{1}{C_0R_4}$$

It should be noted that Pin 5 is left open circuited (i.e., $R_3 = \infty$). This allows the circuit to be keyed OFF, or disabled, by applying a high-logic state to Pin 8, and a low-logic state to Pin 9 (see Table 1).

The functions of the three control terminals can be described as follows:

a. **FSK Data Input:** The serial binary data is applied to this terminal. With the carrier control at low- and enable/disable control at high-state, the binary data causes the transmitter to generate the mark and space frequencies, f_{T1} and f_{T2}.

b. **Enable/Disable Control:** When this input is at low-state, the transmitter is disabled.

c. **Carrier-Control:** When this terminal is at high-state, the transmitter generates a continuous tone at frequency, f_{T0}.

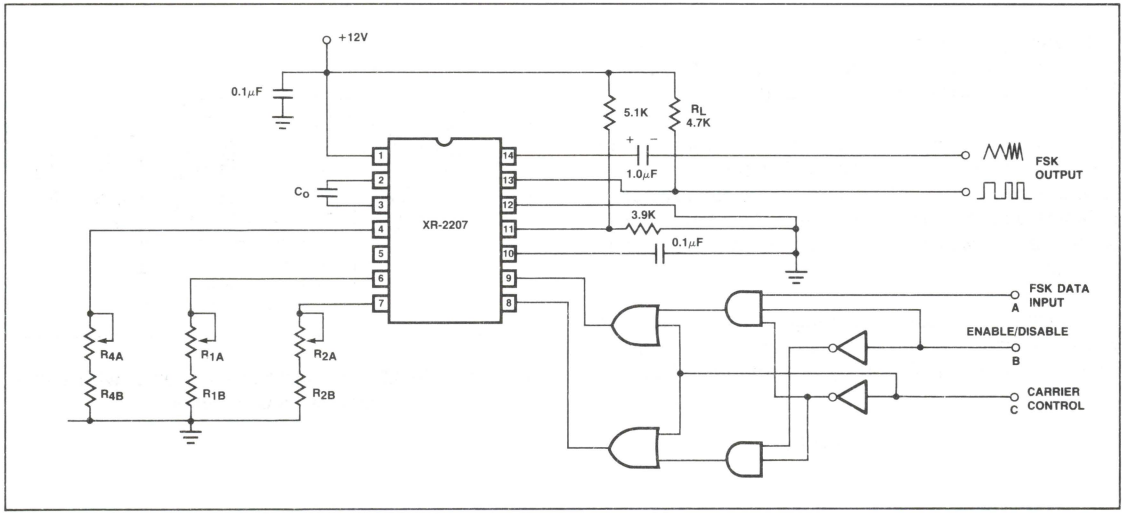


Figure 4. Three-State FSK Transmitter Using the XR-2207

With the external logic circuitry shown in Figure 4, carrier-control can override both the enable/disable or the FSK data inputs. A detailed truth-table of the circuit outputs is given in Table 2, for various states of the three control inputs.

Table 2. Three-State Transmitter Operating Modes as a Function of Control Inputs

Control Input States			Level at Pin 9	Level at Pin 9	Transmitter Output Frequency	Transmitter Operating Mode
A	B	C				
L	L	L	L	H	OFF	Transmitter
H	L	L	L	H	OFF	Off
L	H	L	L	L	f_{T1}	Transmit
H	H	L	H	L	f_{T2}	Data
L	L	H	H	H	f_{T0}	Transmit
L	H	H	H	H	f_{T0}	Carrier
H	H	H	H	H	f_{T0}	Only

XR-2211 As A Three-State Receiver

The XR-2211 is a monolithic FSK demodulator which operates on the phase-locked loop principle. In addition to the basic PLL system, the monolithic chip also contains a quadrature-detector circuit which produces a logic signal when a carrier signal, or tone, is present within the capture range of the PLL. A simplified functional block diagram of the circuit is shown in Figure 5.

Basic Bi-State Operation

The basic operation of the XR-2211, in conventional bi-state modems, is described in detail in Exar's Application Note, AN-01. It will be briefly reviewed below.

The basic circuit connection for the XR-2211 for bi-state FSK detection is shown in Figure 6. The center frequency is determined by $f_o = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. Calculations for f_o should fall midway between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain a lock with a swept input signal. This range is determined by the formula:

$$\Delta f = (R_4 f_o / R_5)\ \text{Hz}$$

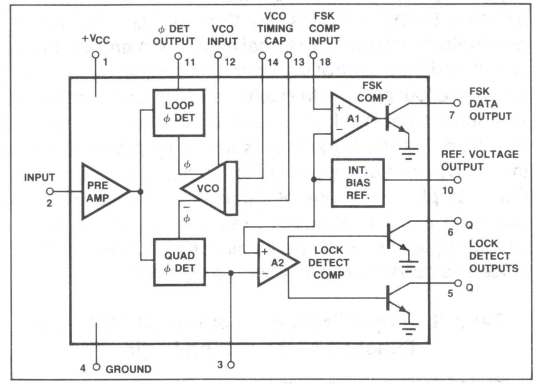


Figure 5. Functional Block Diagram of XR-2211 FSK and Tone Detector

Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, the recommended range of values for R_4 is between 10kΩ and 100kΩ. The capture range ($\pm\Delta f_c$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop-filter time constant. In most modern applications, Δf_c is chosen to be ≈80% to 95% of the tracking range, Δf.

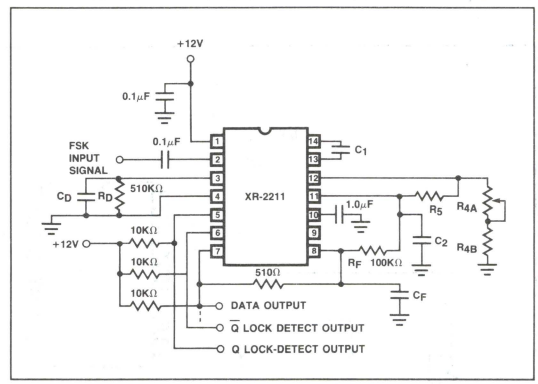


Figure 6. XR-2211 as a Bi-State Receiver with Tone-Detection Capability

The bi-state FSK data filter, made up of R_F and C_F, removes the jitter from the demodulated FSK signal. Similarly, the lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With $R_D = 510k\Omega$, the minimum value of C_D can be determined by: $C_D(\mu f) \approx$ 16/capture range in Hz. The XR-2211 has three npn open-collector outputs, each of which is capable of sinking up to 5mA. Pin 7 is the FSK data output, Pin 5 is the 0 lock-detect output which goes low when a carrier is detected, and Pin 6 is the Q lock-detect output which goes high when lock is detected. If Pin 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied, and will be low when no carrier is present.

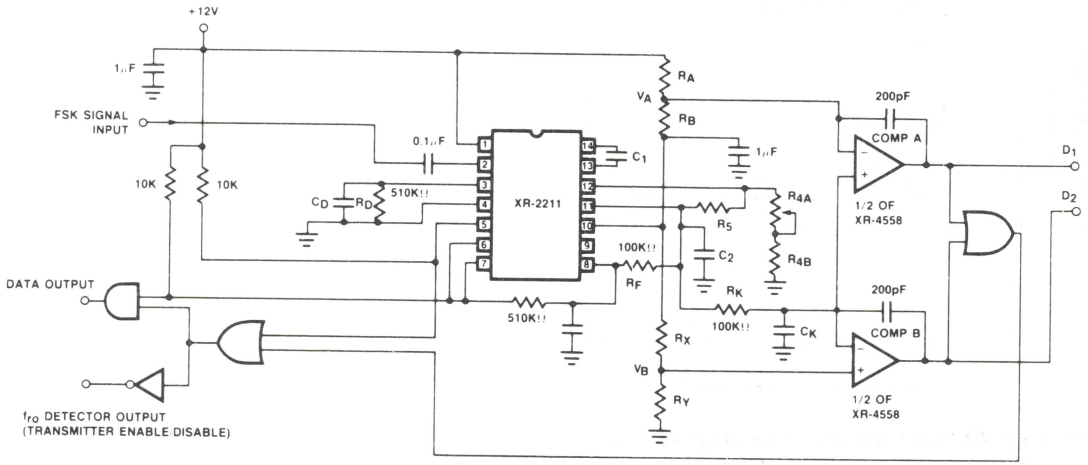


Figure 7. Circuit Connection for Operating XR-2211 as a Three-State FSK Receiver

Three-State Operation

The XR-2211 FSK demodulator circuit can be made to operate as a three-state receiver (see Block C of Figure 2), using the circuit configuration shown in Figure 7. With reference to the Figure, the basic operation of the circuit can be described as follows: The basic FSK decoding function, converting the incoming mark and space signals at frequencies f_{R1} and f_{R2}, is performed in the same manner as in the bi-state case, and the resulting output is available at Pin 7 of XR-2211. Pin 7 is connected to the tone-detect output, and then gated by the complement of the carrier-detect output. Thus, the data output terminal will be enabled only when the mark and space frequencies are present, but not when the receive-carrier, f_{R0}, is present.

The external voltage comparators shown in Figure 7 are added to the circuit to distinguish PLL output voltage levels corresponding to various input frequencies. The function of the XR-2211 frequency-to-voltage transfer characteristics can be understood by referring to Pin 11 in Figure 8. The voltage levels and polarities shown are relative to the XR-2211 internal reference voltage, V_{10}, at Pin 10. The mark and space frequencies, f_{R1} and f_{R2}, generate the maximum dc level shifts. V_{R1} and V_{R2}, sensed by the internal FSK comparator (see Figure 5) which is internally biased from the reference voltage, V_{10}. The external comparators, Comp. A and Comp. B of Figure 7, are biased at voltage levels, V_A and V_B, approximately halfway between V_{R1} and V_{R2}, to trip at frequencies f_A and f_B, which are halfway between mark-to-center and space-to-center frequency shifts. This biasing is achieved with the external resistive dividers, R_A, R_B, R_X, and R_Y of Figure 7, which generate the reference voltage levels, V_A and V_B, with respect to the XR-2211 internal reference at Pin 10. It should be noted that the value of the resistors ($R_A + R_B$) and ($R_X + R_Y$) must be as large as possible (typically in excess of 100kΩ) to avoid disturbing the voltage level at Pin 10.

The output of Pin 11 is filtered by R_K and C_K, and is used to drive the external voltage comparators. The outputs of these comparators are then connected through the external logic gates, to produce the carrier- detect or the enable/disable signal. The resulting logic output will be normally at a low state, and will go high only when the carrier signal, f_{R0}, is present. This logic signal is normally used for transmitter enable/disable control, as shown in Figure 2.

The logic level changes, at the external comparator outputs, correspond to mark-to-carrier or space-to-carrier frequency shifts (see Figure 8); thus, these outputs can be utilized as optional dual-mode monitor outputs, D_1 and D_2 of Figure 2.

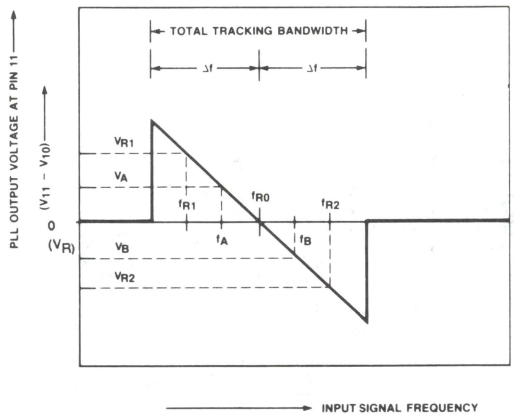


Figure 8. XR-2211 Frequency-to-Voltage Transfer Characteristics. (Note: V_{11} and V_{10} are the dc voltage levels at Pins 11 and 10, respectively.)

Master-Slave Operation

If a common 2 wire line is desired between each modem, a repeater arrangement is needed for the line hybrid interface.



NOTES



Precision PLL System Using the XR-2207 and the XR-2208

Application Note

INTRODUCTION

The phase-locked loop (PLL) is a versatile system block, suitable for a wide range of applications in data communications and signal conditioning. In most of these applications, the PLL is required to have a highly stable and predictable center frequency and a well-controlled bandwidth. Presently available monolithic PLL circuits often lack the frequency stability and the versatility required in these applications.

This application note describes the design and the application of two-chip PLL system using the XR-2207 and the XR-2208 monolithic circuits. The XR-2207 is a precision voltage controlled oscillator (VCO) circuit with excellent temperature stability (± 20 ppm/°C, typical) and linear sweep capability. The XR-2208 is an operational multiplier which combines a four quadrant multiplier and a high gain operational amplifier in the same package. Both circuits are designed to interface directly with each other with a minimum number of external components. Their combination functions as a high performance PLL, with the XR-2207 forming the VCO section of the loop, and the XR-2208 serving as the phase- detector and loop amplifier.

As compared with the presently available single-chip PLL circuits such as the XR-210 or the Harris HI-2820, the two-chip PLL system described in this paper offers approximately a factor of 10 improvement in temperature stability and center frequency accuracy. The system can operate from 0.01 Hz to 100 kHz, and its performance characteristics can be tailored to given design requirements with the choice of only four external components.

DEFINITIONS OF PLL PARAMETERS

The phase-locked loop (PLL) is a unique and versatile feedback system that provides frequency selective tuning and filtering without the need for coils or inductors. It consists of three basic functional blocks; phase comparator, low-pass filter, and voltage-controlled oscillator, interconnected as shown in Figure 1. With no input signal applied to the system, the error voltage, V_d, is equal to zero. The VCO operates at a set "free-running" frequency, f_o. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is

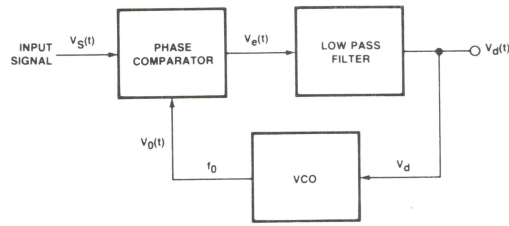


Figure 1. Block Diagram of a Phase-Locked Loop

then filtered and applied to the control terminal of the VCO. If the input signal frequency, f_S, is sufficiently close to f_o, feedback causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a phase-locked loop system are its "lock" and "capture" ranges. These can be defined as follows:

Lock Range: The band of frequencies in the vicinity of f_o over which the PLL can maintain lock with an input signal. It is also known as the "tracking" or "holding" range. Lock range increases as the overall loop gain of the PLL is increased.

Capture Range: The band of frequencies in the vicinity of fo where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. The capture is always smaller than the lock range. It is related to the low pass filter bandwidth and decreases as the low pass filter time constant increased.

The PLL responds to only those input signals sufficiently close to the VCO frequency, f_0, to fall within the "lock" or "capture" ranges of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_0. Figure 2 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly, over a broad frequency range covering both the "lock" and the "capture" ranges of the PLL. The vertical scale corresponds to the filtered loop error voltage, V_d, appearing at the VCO control terminal.

As the input frequency, f_S, is swept up (Figure 2(a)) the system does not respond to the input signal until the input frequency reaches the lower end of capture range, f_{CL}. Then, the loop suddenly locks on the input signal, causing a positive jump in the error voltage V_d. Next, V_d varies at a slope equal to the reciprocal of VCO voltage-to-frequency conversion gain, (K_v), and goes through zero at $f_s = f_0$. The loop tracks the input frequency until f_s reaches the upper edge of the lock range, f_{LH}. Then the PLL loses lock, and the error voltage drops to zero. If the input frequency is swept back slowly, from high towards low frequencies the cycle repeats itself, with the characteristics shown in Figure 2(b). The loop captures the signal at the upper edge of the capture range, f_{CH}, and tracks it down the lower edge of the lock range, f_{LL}. With reference to the figure, the "lock" and the "capture" ranges can be defined as:

Lock Range = $\Delta f_L = f_{LH} - f_{LL}$
Capture Range = $\Delta f_C = f_{CH} - f_{CL}$

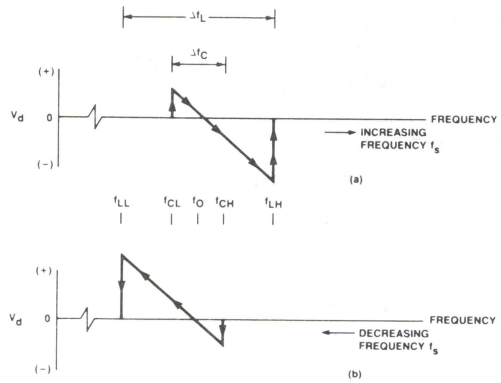


Figure 2. Frequency to Voltage Transfer Characteristics of a PLL System; (a) Increasing Input Frequency; (b) Decreasing Input Frequency

The gain parameters associated with the PLL are defined as follows:

Phase Detector Gain, Kø: Phase detector output per unit of phase difference between the two signals appearing at the phase detector inputs. It is normally measured in volts per radian.

VCO Conversion Gain, K_v: VCO frequency change per unit of input voltage. It is normally measured in radians/sec./volt.

Loop Gain, K_L: Total dc gain around the feedback loop. It is equal to the product of Kø and K_v.

Loop Damping Factor, ζ: Defines the response of the loop error voltage V_d, to a step change in frequency. If $\zeta < 1$, the loop is underdamped; and the error voltage V_d will exhibit an underdamped response for a step change of signal frequency.

The lock range of the phase-locked loop is controlled by the loop gain, K_L. The capture range and the damping factor are controlled by both the loop gain and the low pass filter.

2

PRECISION PLL USING XR-2207 AND XR-2208

The XR-2207 VCO and the XR-2208 operational multiplier can be inter-connected as shown in Figure 3, to form a highly stable PLL system. The circuit of Figure 3 operates with supply voltages in the range of +12V to +26V; and over a frequency range of 0.01Hz to 100kHz. In the PLL system of Figure 3, all the basic performance characteristics of the PLL can be controlled and adjusted by the choice the choice of 4 external components identified as resistors R_0 and R_1 and capacitors C_0 and C_1. C_0 and R_0 control the VCO canter frequency: R_1 and C_1 determine the tracking range and the low pass filter characteristics. The two-chip PLL system can be readily converted to split supply operation by interconnecting the circuit as shown in Figure 4. The PLL circuit of Figure 4 operators over a supply voltage range of ±6 volts to ±13 volts.

For best results, the timing resistor R_0 should be in the range of 5k to 100k, and $R_1 > R_0$. Under these conditions, the basic parameters of the PLL can be easily calculated from the design equations listed in Table 1.

Design Example

As an example, consider the design of a PLL system using the circuit of Figure 3, to meet the following nominal performance specifications:

a) Center Frequency = 10kHz
b) Tracking Range = 20% (9kHz to 11kHz)
c) Capture Range = 10% (9.5kHz to 10.5kHz)

Solution:

a) Set Center Frequency:
Choose R_0 = 10k (Arbitrary choice for 5k < R_0 < 100k)

Then, from equation 1 of Table 1:

$C_0 = (1/f_0R_0) = 0.01\mu F$

b) Set Lock Range:
From equation 2 of Table 1:

$R_1 = (0.45)\ R_0 = 45k$

c) Set Capture Range:
Since capture range is significantly smaller than Lock range, equation 8(a) applies.

Solving equation 8(a) for C_1, one obtains:

$C_1 = 0.032\mu F$

PRECISION SINE WAVE OUTPUT PLL USING XR-2208 AND XR-2206

The interconnection of the XR-2208 and XR-2206 as shown in Figure 5 forms a precision phase-locked loop system with a sine wave output. The phase-locked loop characteristics are adjusted with the same four external components as previously described. Equation 2 in Table 1 is modified to:

$$(2)\ \text{Lock Range } (\Delta f_L/f_0) = (0.5)\ (R_0/R_1)$$

This change is because the reference of the XR-2206 is internally set. The clamp network with Q_1 has been added to adjust the swing to the VCO to compensate for this reference. The sine wave characteristics are adjusted by R_4 and R_5, which adjust sine-shaping and symmetry respectively. Sine wave distortion levels are typically 2.5% unadjusted with $R_4 = 200\Omega$ and R_5 open, and 0.5% adjusted using R_4 and R_5. Sine wave amplitude is adjusted by R_3 with the conversion gain equalling typically:

$$\frac{60mV_{p\text{-}p}}{K\Omega \text{ of } R_3}$$

The phase-locked loop input characteristics allow locking to input signal levels of 50mV RMS to 2V RMS.

Table 1. Phase-Locked Loop Design Equations*

(1) Center Frequency: $f_0 = \frac{1}{R_0C_0}$ Hz	(7) Loop Damping: $= \frac{1}{2\tau K_L} = \sqrt{\frac{2C_0}{C_1}}$
(2) Lock Range: $(\Delta f_L/f_0)=(0.9)(R_0/R_1)$	(8) Capture Range: a) Underdamped Loop ($\zeta < 1/2$): $(\Delta f_c/f_0) = \frac{0.8R_0}{R_1}\frac{C_0}{C_1}$ b) Overdamped Loop ($\zeta > 1$): $(\Delta f_c/f_0) = 0.8(R_0/R_1)$ *See Figures 3 and 4 for component designation.
(3) Phase Detector Gain: $K\phi = 0.5\ V_{CC}$ volts/radian Where $V_{CC} = V^+$ for split supply; $V_{CC} = V^+/2$ for single supply.	
(4) VCO Conversion Gain: $K_V = -\frac{1}{2\ V_{CC}C_0R_1}$ rad/sec/volt	
(5) Loop Gain: $K_L = K\phi K_V = \frac{0.25}{C_0R_1}$ sec^{-1}	
(6) Low Pass Filter Time Constant: $\tau = \frac{C_1R_1}{2}$ sec.	

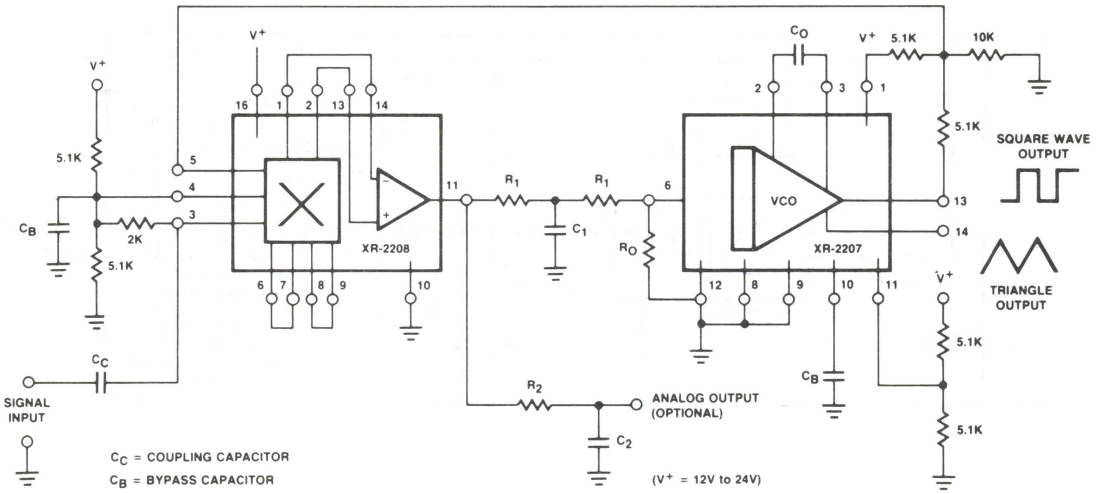


Figure 3. Circuit Interconnections for Single Supply Operation

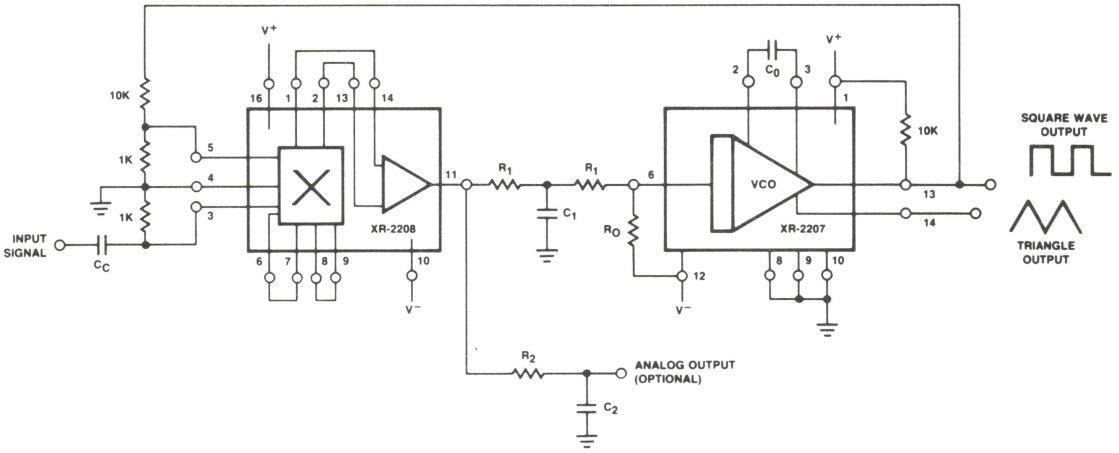


Figure 4. Circuit Interconnections for the Precision PLL System using the XR-2207 and the XR-2208 Monolithic Circuits. (Split-Supply operation, ±6V to ±13V)

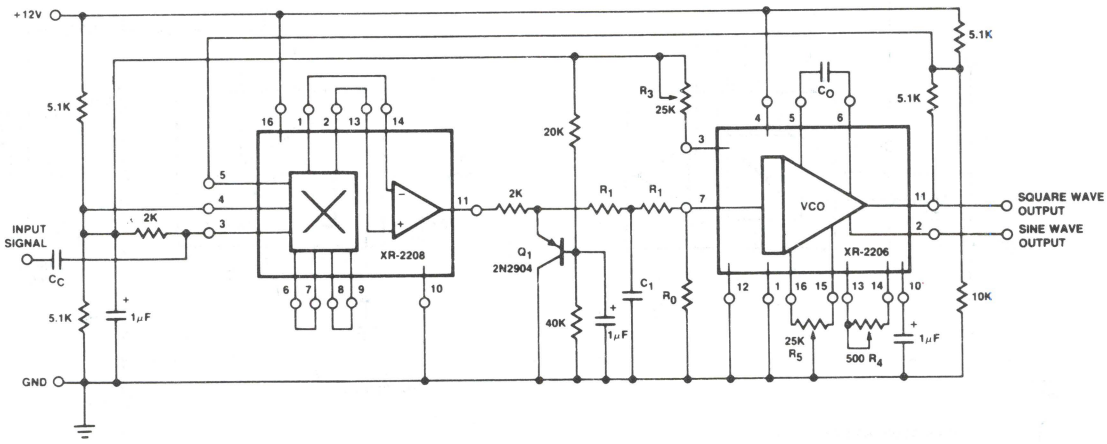

+12V
5.1K
INPUT SIGNAL
C_C
2K
5.1K
1μF
GND
XR-2208
2K
20K
Q_1
2N2907
40K
1μF
R_3
25K
R_1
R_1
C_1
R_0
C_O
VCO
XR-2206
5.1K
5.1K
10K
25K R_5
500 R_4
1μF
SQUARE WAVE OUTPUT
SINE WAVE OUTPUT

Figure 5.

Dual Tone Decoding with XR-567 and XR-2567

Application Note

INTRODUCTION

Two integrated tone decoders, XR-567 units, can be connected (as shown in Figure 1A) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R'_1C'_1$ are chosen, respectively, for Tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C_3 is made very large to delay turn-off of Unit 1 until Unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since Unit 2 will turn off before Unit 1 comes on. Figure 1B shows a circuit variation which eliminates the NOR gate. The output is taken from Unit 2, but the Unit 2 output stage is biased off by R_2 and CR_1 until activated by Tone 1. A further variation is given in Figure 1C. Here, Unit 2 is turned on by the Unit 1 output when Tone 1 appears, reducing the standby power to half. Thus, when Unit 2 is on, Tone 1 is or was present. If Tone 2 is now present, Unit 2 comes on also and an output is given. Since a transient output pulse may appear during Unit 1 turn-on, even if Tone 2 is not present, the load must be slow in response to avoid a false output due to Tone 1 alone.

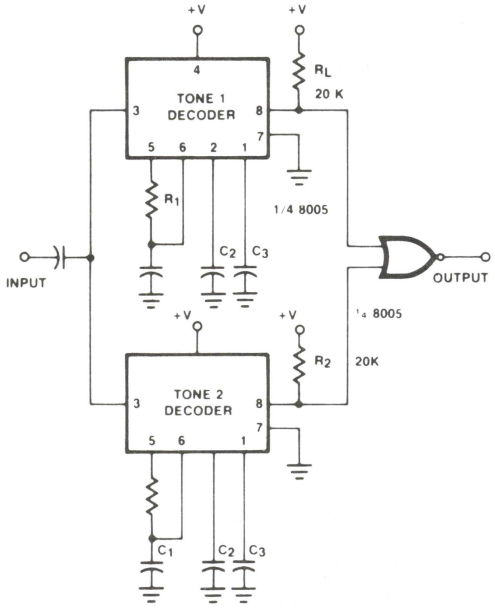


Figure 1A. Detection of Two Simultaneous or Sequential Tones

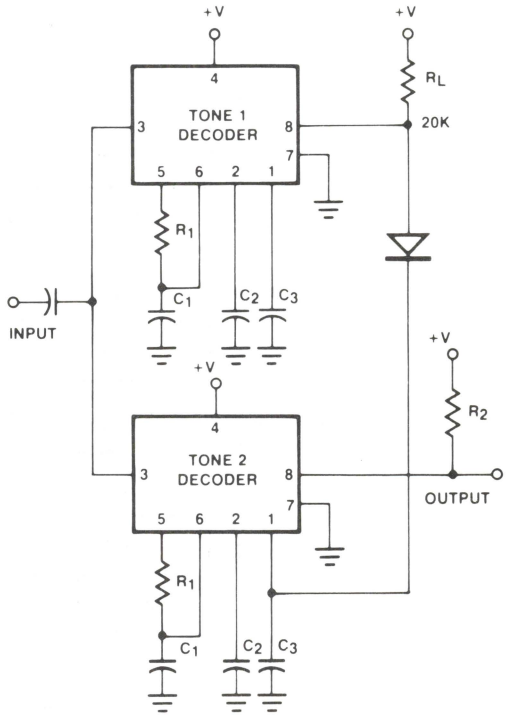


Figure 1B

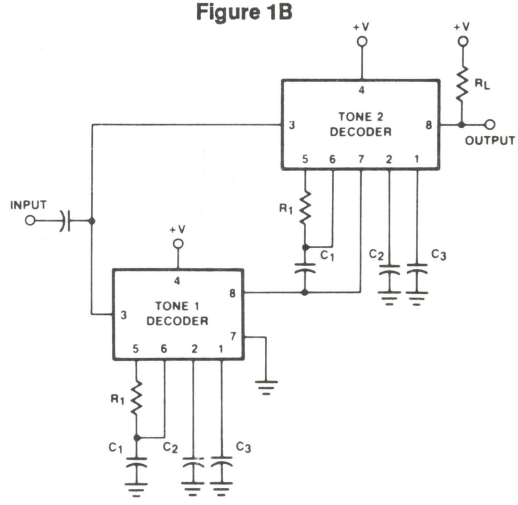


Figure 1C

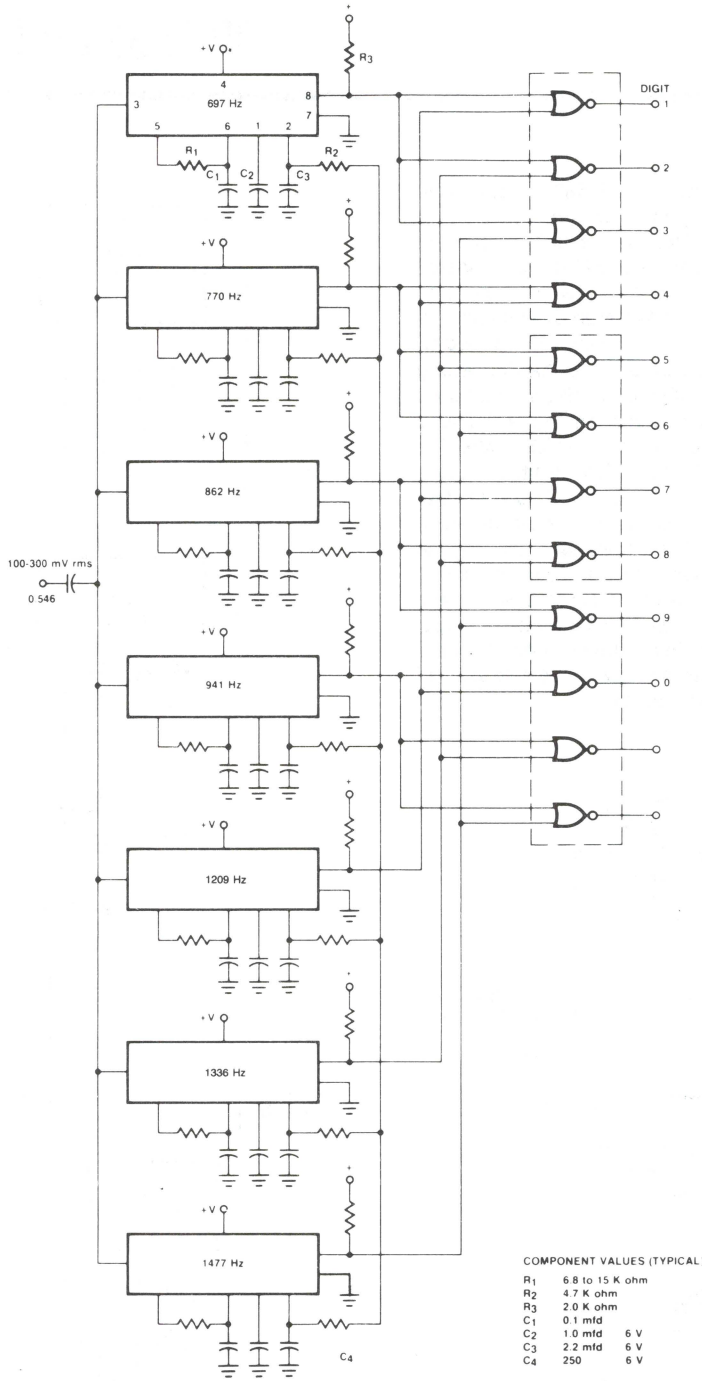


Figure 2. Low-Cost Touch Tone® Decoder

The XR-2567 Dual Tone Decoder can replace two integrated tone decoders in this application.

HIGH SPEED, NARROW BAND TONE DECODER

The circuit of Figure 1 may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_o$ and $1300/f_o$ mfd where f_o is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

TOUCH-TONE DECODER

Touch-Tone decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every tone. A low-cost decoder can be made as shown in Figure 2. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% of 100mV and 5% at 50mV rms. Capacitor C_4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltages (50 to 10mV rms), the bandwidth can be controlled in the normal manner by selecting C_2, thereby eliminating the seven R_2 resistors and C_4. In this case, C_2 would be 4.7 mfd for the three lower frequencies or 2.2 mfd for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under Alternate Method of Bandwidth Reduction, the external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R_2 resistors. In effect, the five 567's which are not being activated during the decoding process serve bias voltage sources for the R_2 resistors of the two 567's which are being activated. Capacitor C_4 (Optional) decouples the ac currents at the common point.

LOW COST FREQUENCY INDICATOR

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no/go frequency meter. Unit 1 is set 6% above the desired sensing frequency and Unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either Unit 1 or Unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

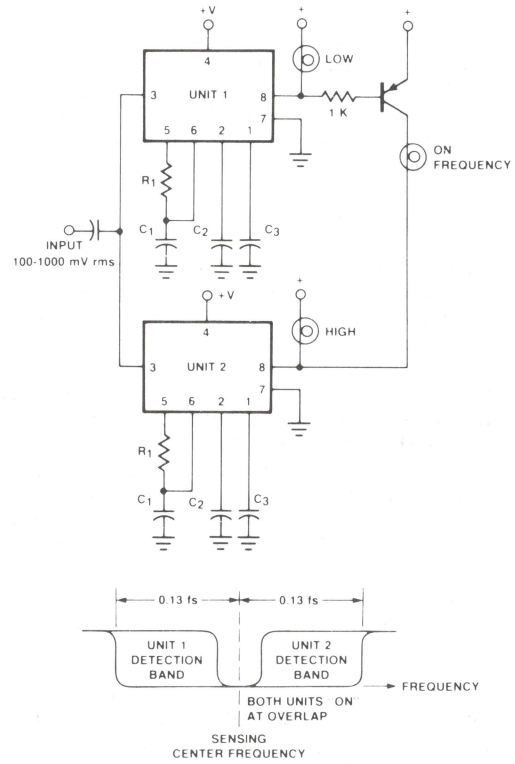


Figure 3. Frequency Meter with Low-Cost Lamp Readout

Sinusoidal Output from XR-215 Monolithic PLL Circuit

Application Note

INTRODUCTION

In a wide range of communication or signal conditioning applications, it is necessary to obtain a sinusoidal output signal which is synchronized to a desired reference or clock input. This can be achieved by using the XR-215 type monolithic PLL circuit and an additional sine-shaping network.

When a periodic input signal is present within the capture range of the XR-215 PLL, the system will lock on the input; and the VCO section of the PLL will synchronize with the input frequency. The output of the oscillator section of the PLL can then be converted to a low distortion sine wave by a relatively simple sine-shaping circuit.

GENERAL DESCRIPTION

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self-contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5Hz to 35MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

Figure 2 shows the simplified circuit schematic of the XR-215 phase-locked loop IC. The VCO part of XR-215, shown in the center section of Figure 2, is an emitter-coupled multivibrator circuit, whose frequency is set by an external capacitor, C_0, connected across the timing terminals (Pins 13 and 14). In this type of an oscillator, the differential voltage waveform across the timing capacitor, C_0, is a linear triangle, with a peak-to-peak amplitude of 1.4 volts. This output amplitude across the timing capacitor is independent of supply voltage.

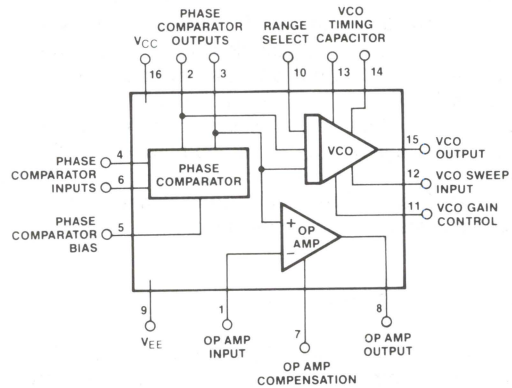


Figure 1. Functional Block Diagram of XR-215 Monolithic PLL Circuit

This triangular waveform can be shaped into a low distortion sine wave by passing it through a simple differential gain stage, as shown in Figure 3. By adjusting the potentiometer R_9 of Figure 3, the input transistors T_1 and T_2 of the differential stage can be brought to the verge of cutoff at the positive and the negative extremities of the input triangle wave. This causes the peaks of the triangle waveform to be rounded, resulting in a nearly sinusoidal output waveform from the differential stage. If the transistor characteristics and the current levels in the differential gain stage are well matched, one can reduce the total harmonic distortion (THD) of the sinusoidal output waveform to less than 3%.

The sine-shaper circuit of Figure 3 can be designed by using the XR-D101 NPN transistor array, which provides five identical NPN transistors in a single IC package. Figure 4 shows the package diagram of XR-D101 chip, in terms of its 16-pin DIP package.

The five independent transistors contained in the XR- D101 transistor array can be interconnected, as shown in Figure 5, to form the differential sine wave-shaping circuit of Figure 3. The inputs of the sine-shaper can be directly connected to the timing capacitor terminals (Pins 13 and 14) of the XR-215 PLL.

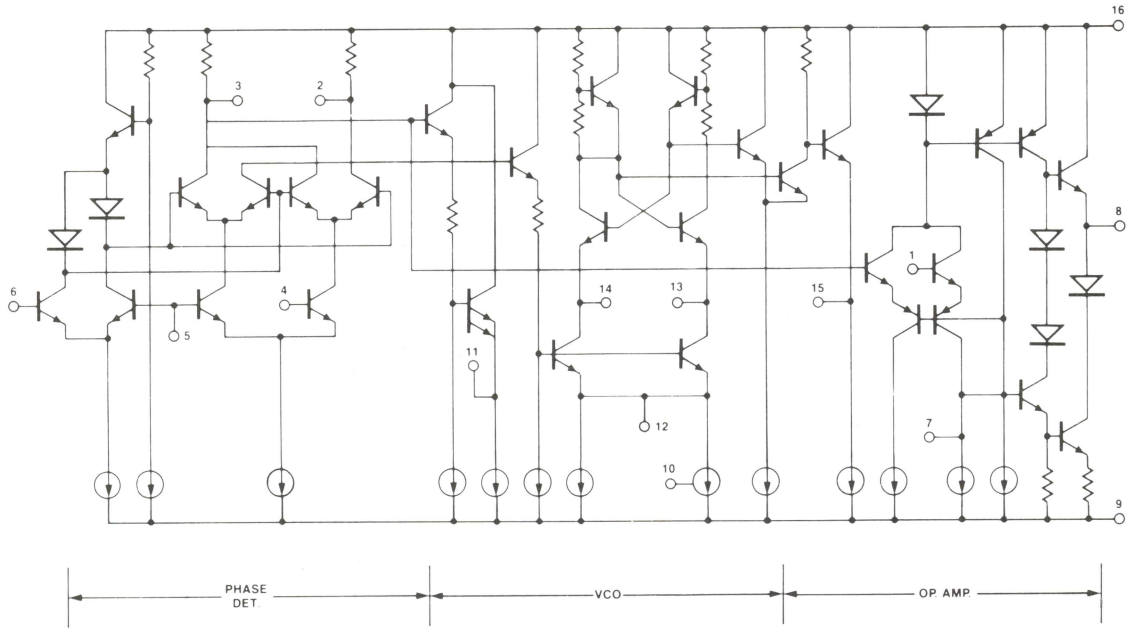


Figure 2. Simplified Schematic of XR-215

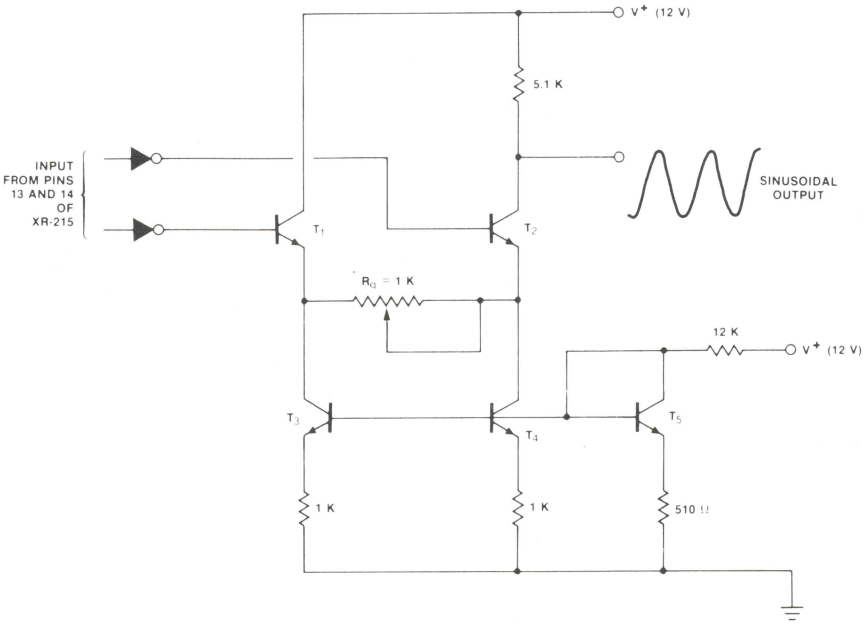


Figure 3. A Simple Triangle-to-Sine Wave Converter Using a Differential Gain Stage

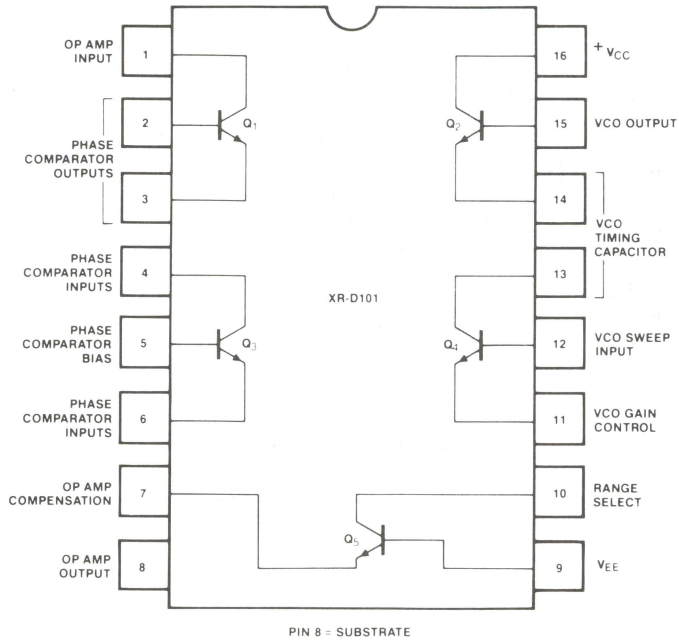


Figure 4. Package Diagram for XR-D101 Matched NPN Transistor Array

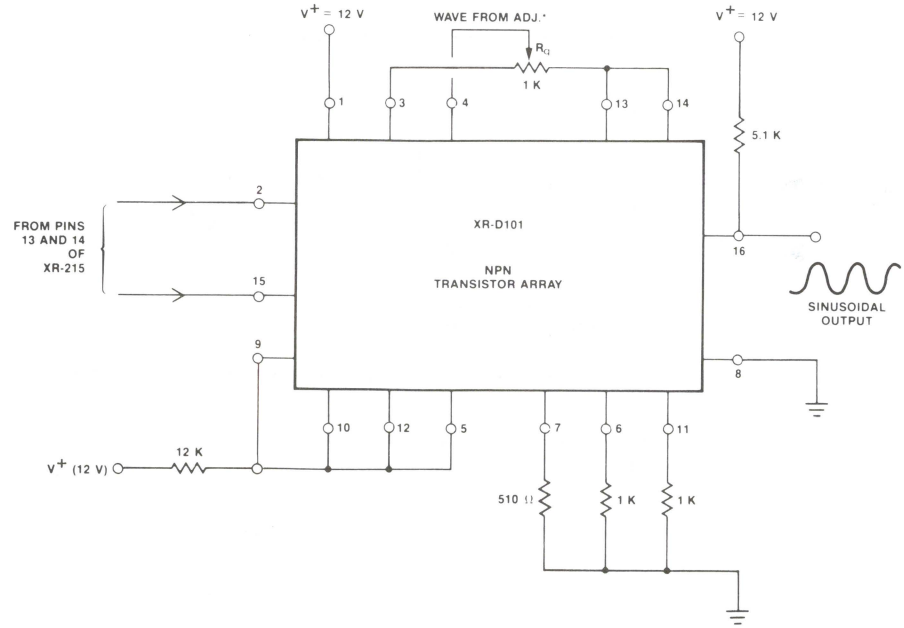


Figure 5. Use of XR-D101 Transistor Array to Obtain Sinusoidal Output from XR-215 PLL

XR-C262 High-Performance PCM Repeater IC

Application Note

INTRODUCTION

The XR-C262 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (MBPS) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of –40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Built-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The XR-C262 operates with a single 6.8-volt power supply, and with a typical supply current of 13mA. It provides bipolar output drive with high-current handling capability. The clock extractor section of XR-C262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to "off" state automatically when there is no input signal present. Compared to conventional repeater designs using discrete components, the XR-C262 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost. This application note outlines the basic design principles and the electrical characteristics of the XR-C262 monolithic repeater IC. In addition, circuit connections and applications information are provided for its utilization in T-1 type 1.544 Megabit PCM repeater systems.

FUNDAMENTALS OF PCM REPEATERS

The Pulse-Code Modulation (PCM) telephone systems are designed to provide a transmission capability for multiple-channel two-way voice frequency signals which are transmitted in a digital PCM format. In order to minimize error rates, and provide transmission over long distances, this digital signal must be regenerated at periodic intervals, using a regenerative repeater system. Figure 1 shows the block diagram of a bi- directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. In the United States, the most widely used PCM telephone system is the T-1 type system which operates at a data rate of 1.544 Mbps, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole-mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772kHz is less than 36dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

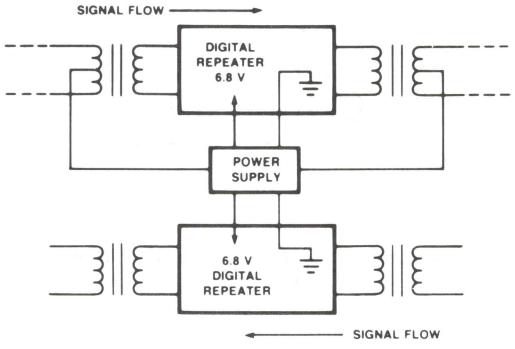


Figure 1. Block Diagram of a Bi-Directional Digital Repeater System

The T-1 type transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end cross-talk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The XR-C262 monolithic IC replaces about 90% of the electronic components and circuitry within the digital repeater sections of Figure 1. Thus, a bi-directional repeater system should require two XR-C262 ICs, one for each direction of information flow.

OPERATION OF THE XR-C262

The XR-C262 monolithic repeater is packaged in a 16-pin dual-in-line hermetic package, and is fabricated using bipolar process technology. The functions of the circuit terminals are defined in Figure 2, in terms of the monolithic IC package.

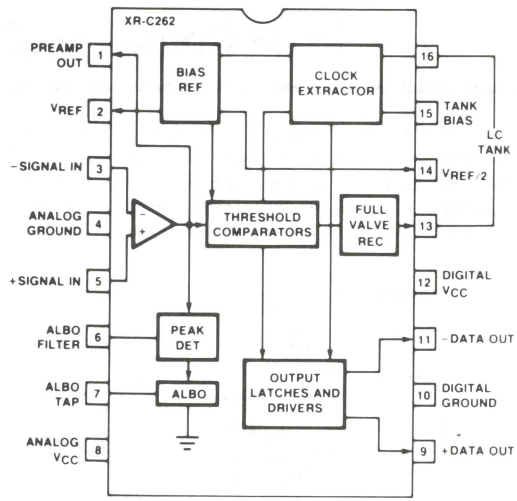


Figure 2. Package Diagram of XR-C262 Monolithic PCM Repeater

A more detailed system block diagram for the monolithic repeater system is given in Figure 3. The system blocks shown within the dotted area are included on the monolithic chip. The numbers on the circuit terminals correspond to the pin numbers of the 16-pin IC package containing the repeater chip, In terms of the system block diagram of Figure 3, the overall repeater operation can be briefly explained as follows.

The bipolar PCM signals which are attenuated and distorted due to the preceding transmission medium are applied to the input of a preamplifier (Block 1) through an Automatic Line Build-Out (ALBO) circuit. The impedance, Z_1, corresponds to the passive section of the ALBO network. The preamplifier section, along with the passive equalizer networks Z_2 and Z_3 connected in feedback around it, provides gain to compensate for line losses and band-limiting to reject unwanted noise as well as gain and phase equalization to shape received pulses.

The ALBO circuitry provides attenuation and shaping to automatically adjust for varying cable characteristics. The output of the preamplifier is controlled to swing between

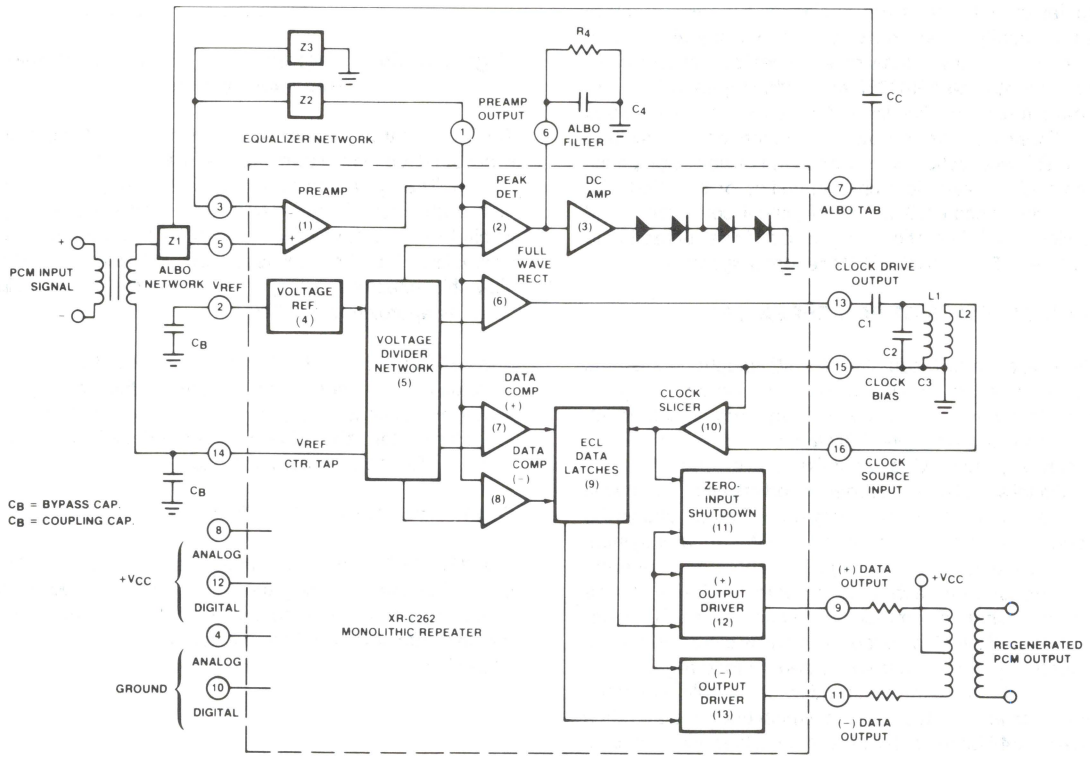


Figure 3. Detailed Block Diagram of the XR-C262 Monolithic Repeater System

two established peak levels. This is accomplished by feedback circuitry, and is similar in concept to automatic gain control. When the preamplifier output passes through the peak thresholds it is detected by the peak detector (Block 2) and produces a signal which is used to control a feedback loop establishing the attenuation and shaping of the ALBO network. The actual circuit design associated with this function is described in more detail in the discussion of peak detection and ALBO circuitry.

The output of the preamplifier drives a set of data comparators which are internally biased from a voltage reference (Block 4) and the precision voltage divider network (Block 5). Thus, the preamplifier output is "sliced" at various voltage levels to eliminate the effects of the baseline noise. This output is full-wave rectified and amplified through Block 6 of Figure 3. The resulting signal has a strong Fourier component at the clock frequency and is used to drive a high Q (≈100) resonant circuit tuned to that frequency. The output of the resonant circuit is transformer-coupled to a zero-crossing detector and clock limiter (Block 10). The resultant output is the desired recovered timing. This resonant circuit is driven by a low impedance amplifier, and the resulting clock edges are in phase with the peak of the received pulses.

The regeneration of the data is achieved through the two data comparators (Blocks 7 and 8) and the ECL latches (BLock 9) which function as tracking flip-flops. The positive and negative data paths are separate; and, with the exception of the data limiter and slicer levels, identical in design. The preamplifier output is sliced at about 45 percent of the peak voltage and its amplitude is limited to provide digital data pulses. The data is applied to one of the inputs to the tracking flip-flop, whose state is latched and unlatched by the clock. During acquisition, the flip-flop acquires data; during hold, further data transitions are ignored and the state of the flip-flop output determines whether an output pulse is transmitted. The implication of using the clock to perform data sampling is that path delays of the data and clock must be controlled to be equal. The monolithic integrated circuit technology affords this control. The advantage of this technique is that the need for clock shifting or strobe pulse generating circuitry for accurate sampling alignment is eliminated. Actual circuit implementation resulted in a 40ns misalignment of clock and data. This 40ns error in sampling time amounts to less than 0.4dB degradation in SNR performance. Figure 4 shows the idealized timing and signal waveforms within the circuit.

The output drivers use latched data and clock to produce an output pulse-width which is accurately controlled by the duration of the clock. Non-saturating output drivers (Blocks 12 and 13) insure that output pulse rise and fall times are less than 100ns. The zero input shut-down circuitry (Block 11) guarantees that in the event incoming data disappears, the output switches will not latch in the "on" state. When no input signal is present, the absence of clock is sensed and the output drivers are held in the "Off" state.

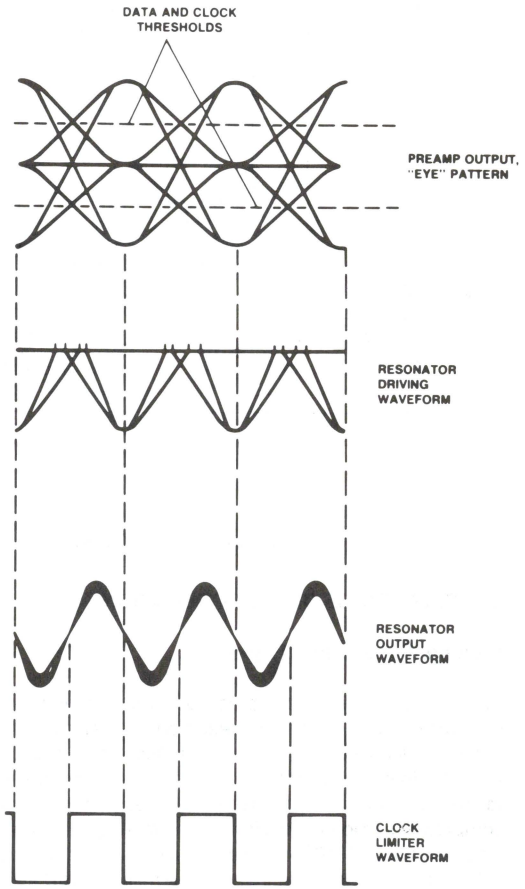


Figure 4. Timing Diagrams of Voltage Waveforms within the Clock Regeneration Section

Figure 5 shows a practical circuit connection for the XR-C262 in an actual PCM repeater application for 1.544 Mbps T-1 repeater system. For simplification purposes, the lightening protection circuitry and the second repeater section for the reverse channel are not shown in the figure.

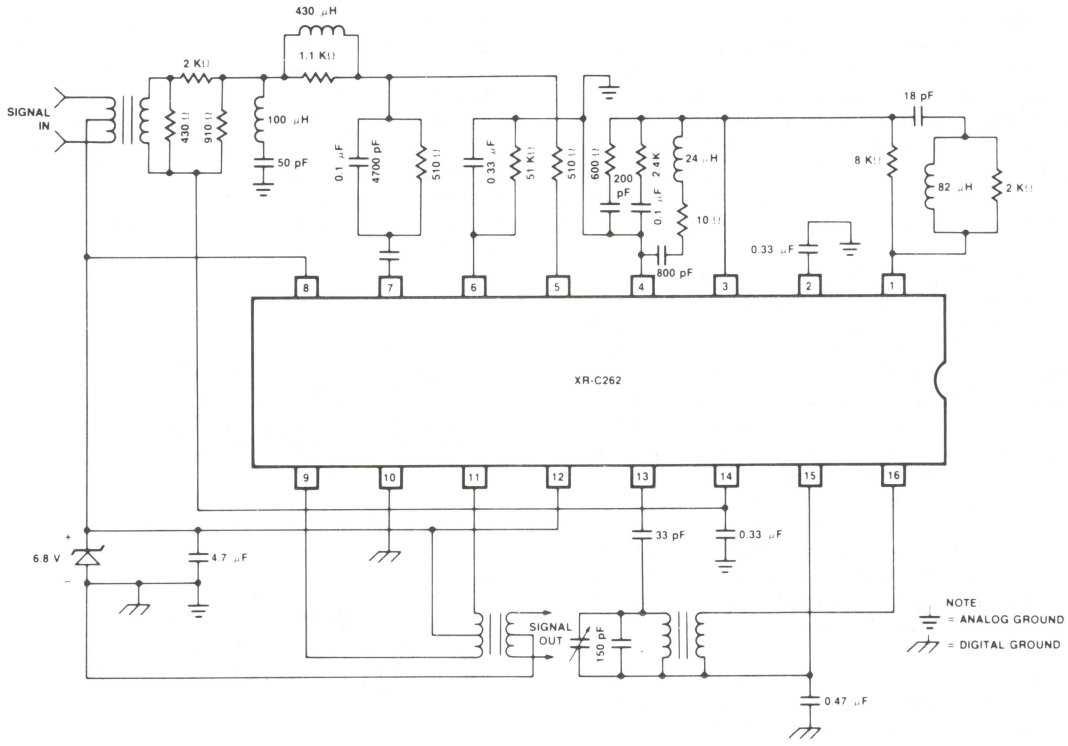


Figure 5. A Recommended Circuit Connection Diagram for T-1 Type Repeater Application

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Figure 6):

The circuit diagram of the preamplifier section is shown in Figure 6. This section is designed as a single-stage high-gain amplifier with differential inputs and a single-ended output. The amplifier output is internally connected to the peak-detector, full-wave rectifier and the data-comparator sections. The circuit exhibits a high differential input resistance (≈10^6 ohms) and a low output impedance (≈80 ohms). It has a nominal voltage gain of 69dB at DC and ≥ 50dB at 1MHz. The frequency response of the circuit exhibits a single-pole roll-off characteristic.

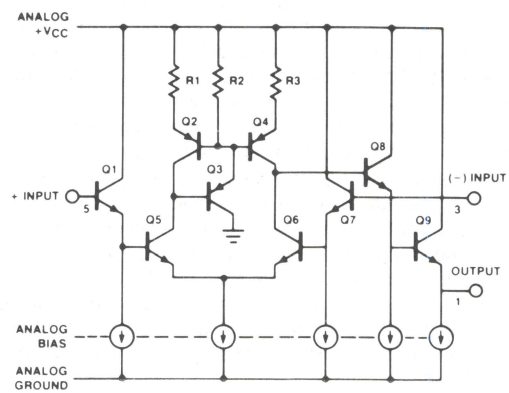


Figure 6. Circuit Diagram of Preamplifier Section

Peak-Detector and ALBO Section (Figure 7):

The peak-detector circuit is designed to detect the peaks of the preamplifier output, provided that these peaks exceed the internal detection threshold levels. This peak information is then low-pass filtered and is used to control the current in a diode string which acts as a variable-loss or "variolosser' element in a feed-back path. In the circuit, the comparators conduct whenever the preamp output exceeds the (+) threshold in a positive direction or the (–) threshold in a negative direction. Transistor Q_5 then injects a pulse of current into the ALBO filter. In the steady state, DC level across the ALBO filter controls the current through the diode string; and the dynamic resistance of the diodes acts as the variolosser element. The usable linear resistance range in this application is almost three orders of magnitude ranging from 11Ω to ≈ 6KΩ.

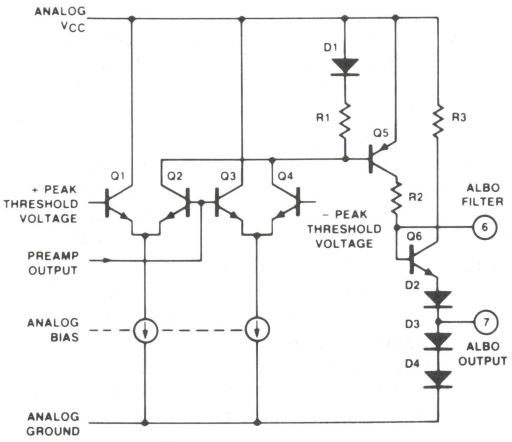


Figure 7. Circuit Diagram of the Peak-Detector and the ALBO Sections

Data Latches (Figure 8):

The data latches are required to be impervious to data transitions in the latch mode, and to be "transparent:" (i.e., tracking the input data) during the tracking mode. Figure 8 shows the basic circuit configuration used in the XR-C262, which meets the above-mentioned performance requirements. During the time when the clock pulse is high, the acquisition transistors Q_1 and Q_2 are differentially switched with data transitions, and the data is coupled to the respective bases of Q_3 and Q_4. When the clock pulse goes low at the sample time (see Figure 4), the information is regeneratively latched into Q_3 and Q_4. While the clock is low, further data transitions have no effect upon the state of the flip-flop. A more detailed description of the timing waveforms is given in Figure 13.

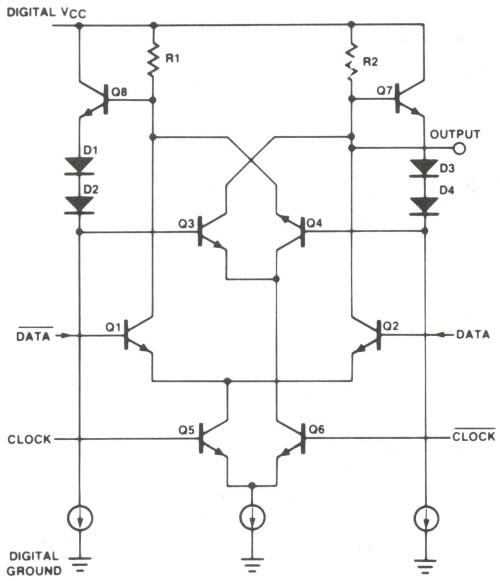


Figure 8. Circuit Configuration for Tracking Data Latches

Threshold Circuitry (Figure 9):

Threshold circuitry is a low impedance voltage-divider circuit corresponding to Block 5 of Figure 3, and it establishes the fixed levels required for data, clock and peak detection. It is important that the thresholds are insensitive to temperature variations, and that they are of sufficiently low impedance to guarantee that there is no threshold variation due to changing signal conditions. The reference voltages of the peak-detector, data, and clock thresholds are set by a resistor chain which divides down the voltage of the on-chip zener diode. The ratios of data threshold to peak-detector threshold and that of clock threshold to peak-detector threshold are both set at 45 percent. In the actual circuit implementation, as shown in Figure 10, a compound connection of PNP's and NPN's are used to reduce the output impedance of the reference levels. The currents through the NPN and PNP transistor strings are set so as to insure that the base emitter voltage drops of the NPN's and PNP's are nominally the same. The output impedance of the resulting reference voltage taps are about 300 ohms. The center tap of the buffered divider is brought to a separate package terminal (Pin 14 of Figure 3) for biasing the preamplifier input.

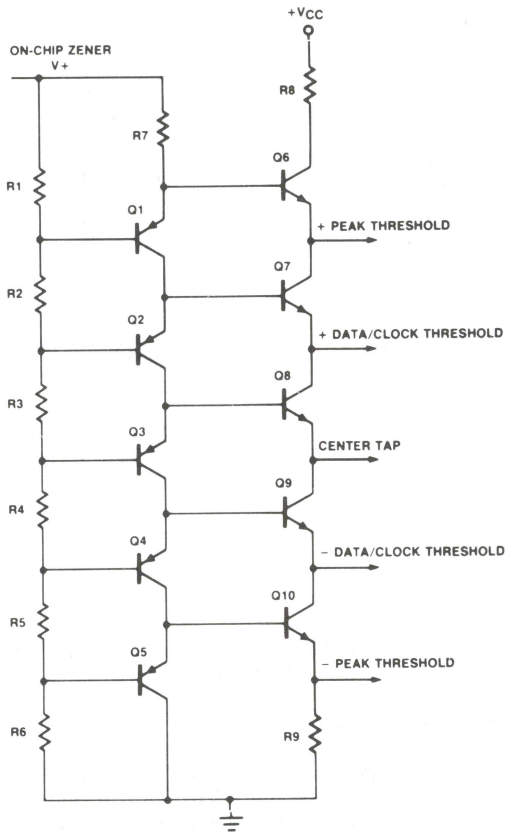


Figure 9. Internal Voltage-Divider Network for Comparator Threshold Setting

Clock Recovery Section (Figure 10):

Clock recovery circuity consists of a full-wave rectifier, an external L-C resonant circuit, a zero crossing detector, and limiting amplifier, as shown in Figure 10. The full-wave rectifier circuit, comprising of cross-coupled transistor pairs Q_1 through Q_4 has a net voltage gain of 2, which is obtained by setting $R_1 = R_2 = (1/2)R_3$. The rectified output is then buffered by the Darlington emitter-follower stage made up of Q_5 and Q_6, and applied to the external L-C resonant circuit. Q_6 is operated at a high bias current level to provide an output impedance of less than 15Ω. This low impedance is required to insure that the L-C tank-drive circuitry looks like a voltage source.

The inductor of the resonant tank circuit is also a transformer which couples the sine wave signal to the zero crossing detector and limiting amplifier. The zero crossing detector is a differential amplifier with a nominal voltage gain of 20 and input impedance of 4MΩ. The sine wave from the resonant circuit is sliced to produce a square wave with sharp transitions at the zero crossings. This eliminates timing variations that may be caused by amplitude changes of the sine wave signal. The output of the zero crossing detector is further enhanced by the limiter which is another differential pair with a nominal voltage gain of 30. The output of this amplifier is a 1.5V peak-to-peak square wave clock which drives the data latches and the output drivers.

Zero-input Protection Circuit (Figure 11):

The zero input protection circuitry accomplishes the dual task of preventing the output switches from latching in an "on" state, as well as reducing the likelihood of output pulses with no input signal. The data, clock, and regenerator circuitry are all balanced DC coupled circuits. Controlling the steady state, no-signal condition of these circuits without building an unacceptable offset into the path is not practical. Instead, a retrigerable one-shot that uses the saturation characteristics of PNP transistors is used to control the level of the clock into the output switches. This technique uses the band- pass characteristics of the timing recovery resonant circuit to reject out of band signals, thus minimizing the chance of producing output pulses with no input signal and the presence of noise. Figure 11 shows the basic implementation of the zero-input protection circuit. Q_1 and Q_2 function as a simple retriggerable one-shot. The transistor Q_2 is a lateral PNP device with a limited frequency capability and long storage-time delay. The existence of the 1.544MHz clock causes Q_2 to saturate and remain in saturation while clock pulses are present. The comparatively long time constant associated with Q_2 coming out of saturation (≈ 5μs) insures that, when data is present, the zero input protection has no effect upon operation. When data disappears there is no clock to retrigger the one-shot, thus Q_2 comes out of saturation, causing Q_3 to saturate which pulls the respective clock lines high, and disables both output drivers in their "off" state.

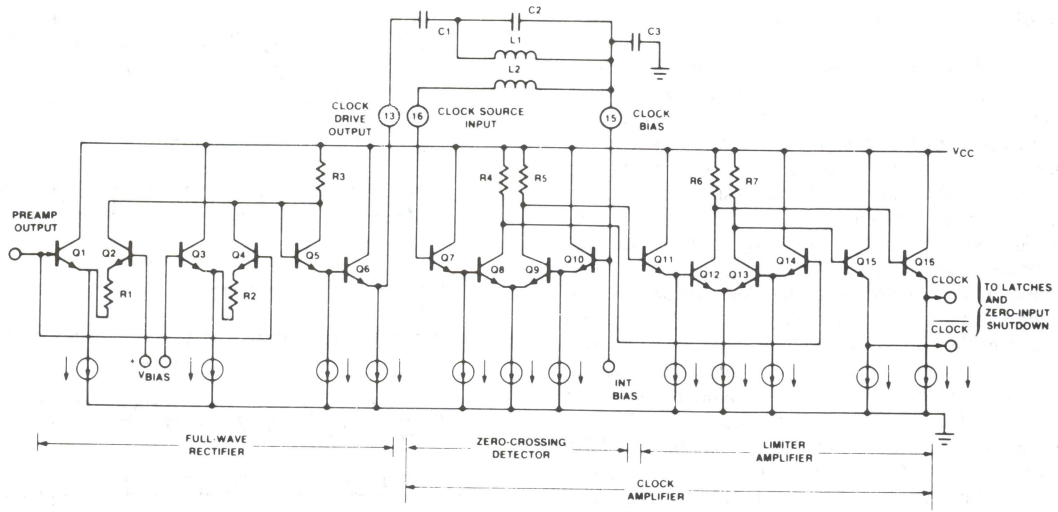


Figure 10. Circuit Diagram of the Clock Recovery Section

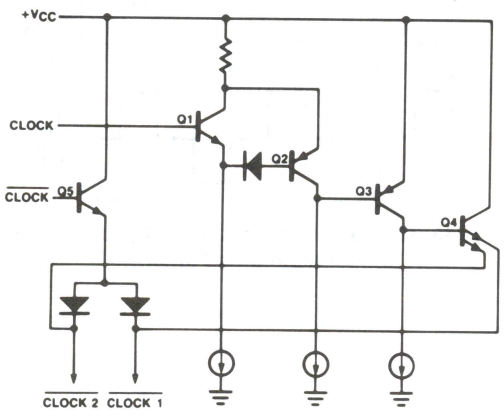


Figure 11. Zero-input Shutdown Circuit for Output Protection

Output Drive Circuitry (Figure 12):

The output drive circuitry is made up of two identical channels as indicated in the block diagram of Figure 2. The circuit configuration for each of these driver sections is shown in Figure 12. The output would follow the data input from the latches only when the clock input is at a "high" state, i.e., with Q_2 off and Q_3 on. In this manner, the output pulse-width is controlled by the clock. To provide the fast turn-on and turn-off of the output drivers, all the transistors operate in a nonsaturating state. Q_4 forms an active clamp to reduce voltage swing at the base of Q_6, and the clamp diode D_5 prevents the saturation of the output driver Q_7. Because of the biasing scheme mentioned above, the amplitude of the clock and the latched data are insensitive to supply voltage and temperature changes. Thus, the variations of the regenerated pulse-width over temperature and supply are minimized.

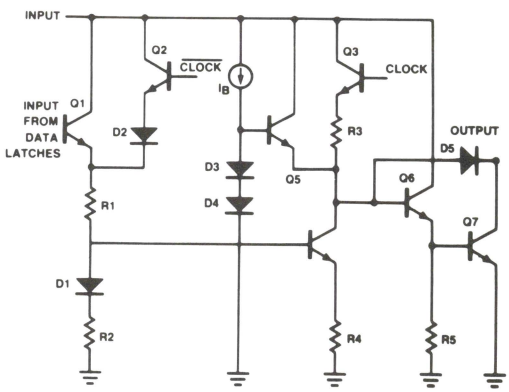


Figure 12. Circuit Configuration for the Output Drivers

Timing Waveforms (Figure 13):

Figure 13 illustrates the relative time and phase relationships between the signal levels at various points within the circuit. For the purpose of illustration an input data pattern comprised of a string of "ONE"s is assumed, which looks like a nearly sinusoidal input after having traveled through a dispersive transmission medium such as a long cable. Waveform (1) is the output of the preamplifier; Waveforms (2) through (5) are the outputs of the two data comparators driven by the preamplifier output (see Figure 3). Waveform (6) is the low-level clock signal obtained from the resonant tank circuit, at Pin 16 which is then amplified and sliced by the clock-recovery circuit (see Figure 11) and appears as the internal clock signals shown as Waveforms (7) and (8). Waveform (9) shows the output of one of the data latches (Figure 8) as a function of the clock and data inputs. The output of the latch tracks +DATA when the clock is low, and stays latched in that condition when the block goes high. The output drive at Pin 9, which is shown as Waveform (1 0) will then go low only when the Waveforms (8) and (9) are low. Waveform (1 1) shows the second output available at Pin 1 1. These two outputs are then differentially combined by the output transformer (see Figure 3) to provide the regenerated bipolar output pulses shown in Waveform (1.2) of Figure 13.

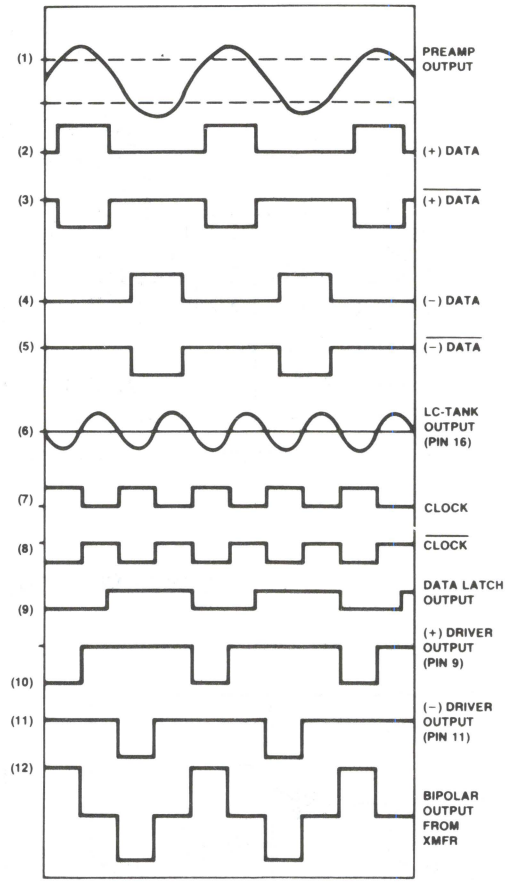


Figure 13. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern

ELECTRICAL CHARACTERISTICS $+V_{CC} = 6.8V$, $T_A = -40°C$ to $+85°C$.

CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	–15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	µA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	$R_L = 400Ω$
Output Low Swing	0.6	0.7	0.9	V	$I_L = 15mA$
Leakage Current			100	µA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Power Dissipation	750mW
Derate above + 25°C	6 mW/°C
Storage Temperature Range	–65°C to +150°C

A Universal Sine Wave Converter Using the XR-2208 and the XR-2211

Application Note

INTRODUCTION

A universal sine wave converter is a system block which can convert any periodic input signal waveform to a low-distortion sine wave, whose frequency is identical to the repetition rate of the periodic input signal. Such universal sine wave converters find applications in communications and telemetry systems. They are particularly useful for converting transducer output waveforms, or pulses, into clean sine wave signals over a band of frequencies. This conversion to sine wave is often necessary to reduce the required system bandwidth for signal transmission by eliminating the harmonic frequencies of the signal.

In the cases where the input frequency is known, and does not change, the universal sine wave converter can be replaced by a simple high-Q filter, tuned to the input frequency. However, in many cases the input frequency, or the repetition rate, is not constant, but varies as a function of time or input data. In such cases a fixed-frequency filter is not feasible, and one is forced to use a universal sine wave converter which is essentially a "tracking regenerative filter".

In this application note, the design principle and the performance characteristics of a regenerative sine wave converter circuit is described. The circuit operates on the phase-locked loop (PLL) principle and can be implemented using the XR-2211 monolithic PLL tone decoder and the XR-2208 multiplier IC.

PRINCIPLES OF OPERATION

Figure 1 shows the functional block diagram of a regenerative sine wave converter system, comprised of four functional blocks: (1) a phase-locked loop (PLL), (2) a sine-shaper, (3) a keyed amplifier, and (4) a lock-detect circuit. With reference to the figure 1, the principle of operation of the entire system can be briefly explained as follows:

When a periodic input signal is present at the input, within the tracking range of the PLL, the circuit would "lock" to the input signal; and the output of the voltage-controlled oscillator (VCO) section of the PLL will duplicate the frequency of the input signal. However, the VCO output waveform will have a fixed wave shape (normally a triangle wave) independent of the input waveform or amplitude. The output of the oscillator section then can be connected to a triangle-to-sine wave converter which converts it to a low-distortion sine wave. The output of the triangle-to-sine converter is then applied to a variable-gain amplifier which sets the desired output amplitude. Since the oscillator section of the PLL is always running, the circuit also contains a "lock-detect" section which enables the output amplifier only when there is an input signal. Thus, with no input signal present within the bandwidth of the PLL, the lock-detect section will keep the output amplifier in the "off" state, and the circuit will not produce an output signal.

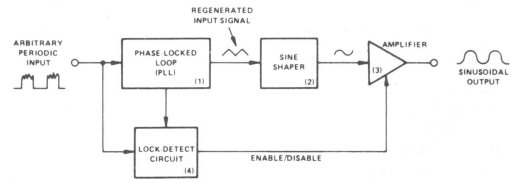


Figure 1. Basic Concept of a Regenerative Sinewave Converter

CIRCUIT DESIGN

The basic regenerative sine wave converter system of Figure 1 can be easily implemented using the XR-2211 monolithic tone decoder and the XR-2208 monolithic multiplier IC's, with only a minimum number of external components.

The XR-2211 is a monolithic PLL circuit especially designed for FSK and tone detection. Thus, it contains the complete PLL and lock-detect sections (Blocks 1 and 4 of Figure 1) on the same chip. Its overall block diagram is shown in Figure 2. The circuit is packaged in a 14-pin dual-in-line package; and the functions of the circuit terminals are given in Figure 3 in terms of the monolithic IC package. In the sine wave converter application, the FSK detector portion of the circuit is not used; only the basic phase-locked loop and the lock-detector sections are utilized. Figure 4 illustrates the necessary external components for its application in the sine wave converter system. The oscillator section of the XR-2211 is an emitter-coupled multivibrator which oscillates by charging and discharging the external timing capacitor, C_o, (connected across pins 13 and 14) through internal constant-current stages. Thus, the output waveform, taken differentially across the timing

capacitor, is a linear triangle wave. This waveform can then be converted to a low-distortion sine wave by the XR-2208 multiplier.

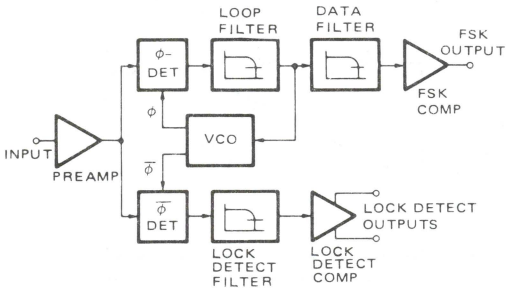


Figure 2. Block Diagram of XR-2211 Phase-Locked Loop FSK and Tone Decoder IC

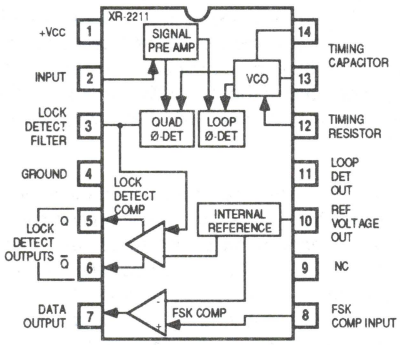


Figure 3. Package Diagram of XR-2211 PLL Circuit

The XR-2208 is a monolithic multiplier circuit which contains a four-quadrant analog multiplier, an op amp, and a unity-gain buffer amplifier in a 16-pin dual-in-line package. Its functional block diagram and equivalent circuit schematic are given in Figures 5 and 6, respectively.

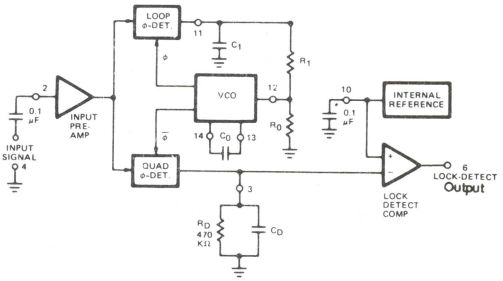


Figure 4. External Circuit Connections for XR-2211 for Sinewave Converter Application

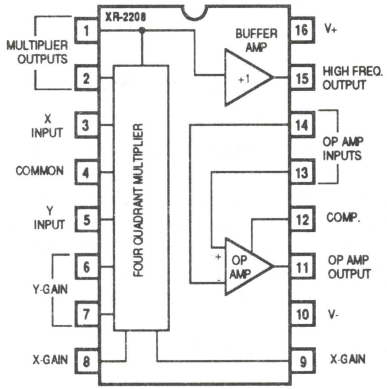


Figure 5. Diagram of XR-2208 Operational Multiplier

Figure 7 shows the recommended circuit connection of the XR-2211 and the XR-2208 to form a universal sine wave converter circuit. In this figure, a non-critical zener diode ($V_Z \approx 6V$ to $7V$) is used to reduce the supply voltage applied to XR-2211, to facilitate DC coupling between the two chips. The frequency of the VCO section of the XR-2211 is set by the timing components R_o and C_o. In this application, a fixed value of $R_o = 10K\Omega$ is recommended, giving a center frequency, f_o value of:

$$f_o = \frac{100}{C_o\ (\mu F)}\ Hz$$

If a R_O value greater than $10K\Omega$ is used, the VCO may not oscillate.

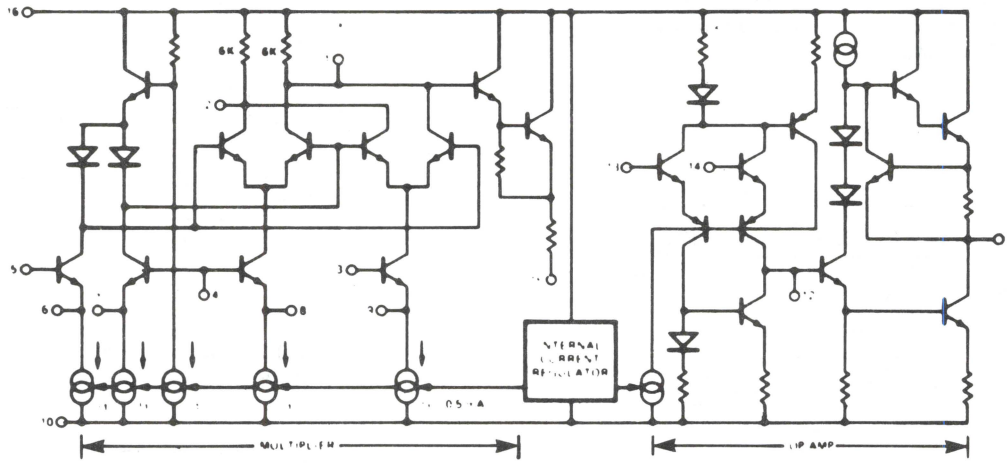


Figure 6. Simplified Circuit Schematic of the XR-2208 Operational Multiplier

The triangle wave oscillator output of the XR-2211 PLL is attenuated through a resistive divider made up of two 10KΩ resistors, and a variable 100KΩ potentiometer, R_x. The attenuated triangle wave across R_x is then applied differentially to the X-input (pins 4 and 5) of the XR- 2208. The 100Ω external resistor across Y-gain setting terminals (pins 6 and 7) causes the Y-input of the multiplier to be slightly overdriven, and thus causes the peaks of the triangle input to be rounded into a low-distortion sine wave.

The distortion of the sinewave is minimized by adjusting R_x, which sets the triangle wave amplitude. The output is available at the unity-gain buffer terminal (pin 15) of the XR-2208. This output is then level-shifted toward ground, through two 10KΩ resistors, and is AC coupled to the inverting input of the op amp section of XR-2208. The gain of the op amp is externally adjusted by means of the 500KΩ Potentiometer, R_F. The DC voltage level of the op amp output is set at the reduced supply voltage (i.e., $V_{CC} - V_Z$).

The lock-detect output of the XR-2211 (pin 6) is shorted to the mid-point of the resistive divider at pin 15 of the XR-2208. With no input signal present at the input within the lock range of the XR-2211, pin 6 is at a "low" state. Thus it acts as a shorting switch to ground and disables the op amp section of the XR-2208. When a periodic input signal appears at the circuit input and the XR-2211 establishes lock with the signal; the lock-detect output at pin 6 goes to a "high" or nonconducting state and enables the output op amp of the XR- 2208; and a low-distortion sine wave output is obtained at the output (pin 11 of XR-2208).

The circuit of Figure 7 can operate as a sine wave converter, over a frequency band between two frequencies f_H and f_L corresponding to the upper and lower lock ranges of the PLL, With the components shown in the figure, this corresponds to approximately 130% bandwidth around the center frequency, f_o, for inputs with close to 50% duty cycle. For periodic inputs with less than 50% duty cycle, this lock range is reduced further. For example, for inputs with 20% duty cycle, this bandwidth drops to about 110% of center frequency. The operation of the circuit with input signals having less than 10% (or more than 90%) duty cycle is not practical. The minimum input level required for circuit operation is 10mV rms. The circuit can generate a nearly sinusoidal output with input signals from very low frequencies up to 100kHz. Typical distortion characteristics of the output are shown in Figure 8, as a function of frequency of operation. Figure 9 shows a typical example of input and output waveforms for sine converter circuit of Figure 7, operating at 1kHz input repetition rate, with a noisy input signal.

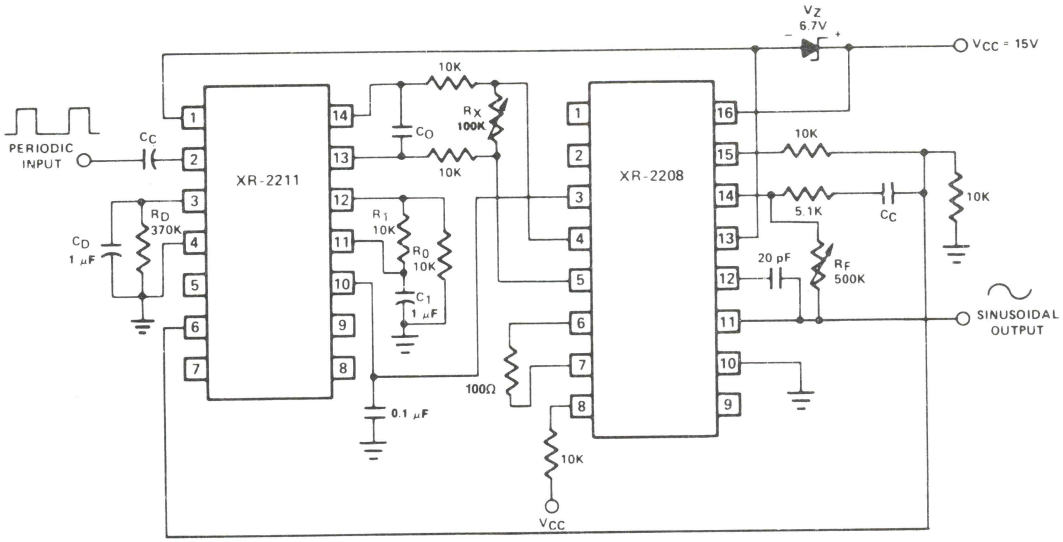


Figure 7. Recommended Circuit Connection for the Regenerative Sinewave Converter

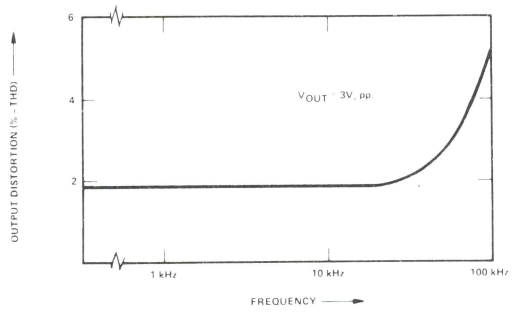


Figure 8. Output Distortion vs Frequency

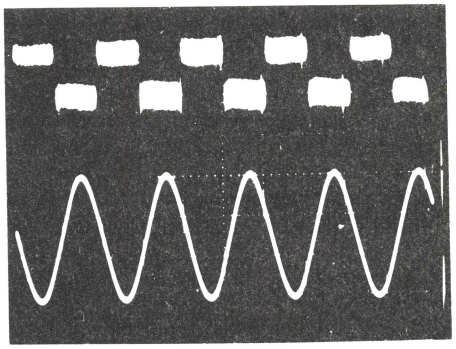


Figure 9. Typical Input-Output Waveforms

(Top: Noisy Input Signal; Bottom: Sinusoidal Output.)
Scale: Vertical: 1 Volt/Div.
Horizontal: 1 m Sec./Div.

Designing High-Frequency Phase-Locked Loop Carrier-Detector Circuits

Application Note

INTRODUCTION

The phase-locked loop (PLL) system can be converted to a frequency-selective tone- or carrier-detection system by the addition of a quadrature detector section to the basic PLL. Such a carrier-detect system serves as a lock indicator for the PLL and produces a logic signal at its output when there is a tone or a carrier signal present within the lock range of the phase-locked loop.

A number of monolithic tone-decoder ICs have been developed which implement the quadrature-detection technique for detection of low frequency tones, such as those used for telephone dialing or ultrasonic remote control. However, because of the particular PLL designs used in these monolithic detectors, their applications are limited to frequencies below 100 kHz. This application note describes a circuit approach, using the XR-210 or the XR-215 high frequency PLLs, along with the XR-2228 monolithic multiplier/detector, which extends phase-locked loop tone detection capabilities to frequencies up to 20MHz.

PRINCIPLES OF OPERATION

The basic block diagram of a phase-locked loop tone detector system is shown in Figure 1. Such a detector system produces a logic-level signal at its output, when the PLL is locked on an input signal. It is made up of two main sections:

1. A PLL section which synchronizes or locks on the input signal.

2. A quadrature detector section made up of a phase-detector, a low-pass filter and a voltage-comparator.

The principle of operation can be briefly described as follows: When the PLL is locked on an input signal, its voltage-controlled oscillator (VCO) section produces a set of input signals, ϕ_1 and ϕ_1, which are 90° apart in phase, but have the same frequency as the input signal to be detected. One of these signals, ϕ_1, is used to drive the PLL phase detector; the other output, which is called the "quadrature output" is used to drive a quadrature phase-detector, as shown in Figure 1. If the PLL is locked on the input signal, then the input signal and the VCO signal applied to the quadrature phase-detector are coherent in phase and frequency. This causes a DC level shift at the low-pass filtered output of the quadrature phase-detector and makes the voltage comparator output change its output logic state. Thus, an output logic signal is produced indicating the lock condition of the PLL.

This type of tone detection technique is a special case of the synchronous AM detection principle, discussed in detail in Exar's Application Note AN-13. The key difference between the tone detection and the synchronous AM detection application is that, in the case of the tone detection, a binary logic output is produced, corresponding to the presence or the absence of the desired input tone, rather than an analog demodulated signal.

XR-210 AND XR-215 HIGH FREQUENCY PLL CIRCUITS

The XR-210 and the XR-215 are high frequency phase-locked loop detector and demodulator circuits. Their functional block diagrams are shown in Figures 2 and 3. Both circuits are packaged in 16-pin dual-in-line packages and contain high frequency VCO and phase- detector sections. The XR-215 chip also contains an operational amplifier. In the case of the XR-210, this op amp section is replaced by a high-gain voltage comparator which drives an open-collector type logic output. The XR-210 is particularly intended for FSK demodulation and can operate up to 20MHz. The XR-215 is designed for linear FM detection and is suitable for frequencies up to 35MHz. Except for the frequency capability of the VCO, the oscillator and the phase-comparator sections of both circuits are quite similar.

The VCO section of the XR-210 or the XR-215 does not provide a separate quadrature output, which is 90° phase-shifted with respect to the basic VCO output (Pin 15). However, the triangular output available across the VCO timing capacitor terminals (Pins 13 and 14) can serve as a quadrature output if it is amplified and "sliced" externally, as shown in the timing diagram of Figure 4.

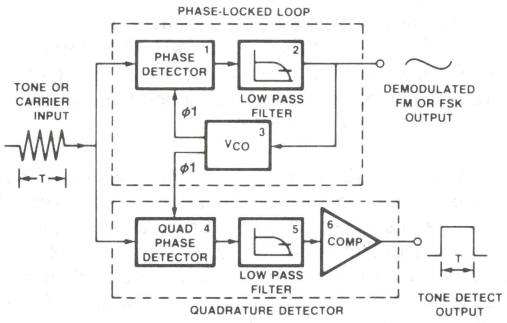


Figure 1. Functional Block Diagram of a PLL Tone- or Carrier-Detector System

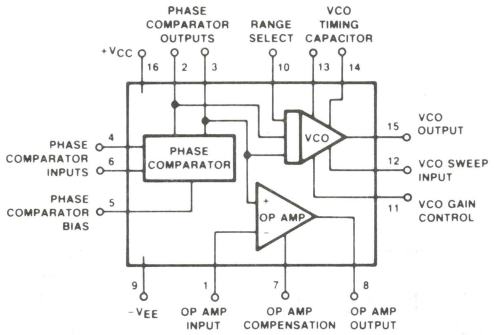


Figure 2. Functional Block Diagram of XR-210 High-Frequency FSK Modulator/Demodulator

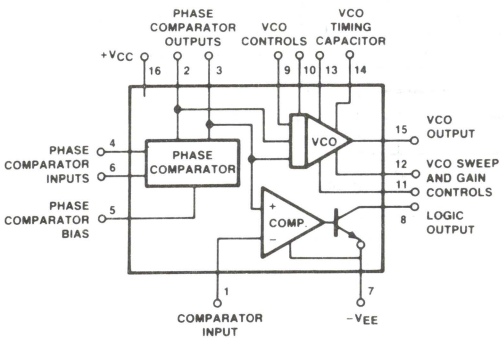


Figure 3. Functional Block Diagram of XR-215 High-Frequency Phase-Locked Loop

XR-2228 MULTIPLIER/DETECTOR CIRCUIT

The XR-2228 is comprised of a four-quadrant multiplier and a high-gain op amp on a single monolithic chip. It is packaged in a 16-pin dual-in-line package and has the functional block diagram shown in Figure 5. It contains independent and fully differential X- and Y-inputs which makes it easy to interface with the XR-210 or the XR-215 type PLL circuit for carrier-detection applications. In the tone- or carrier-detect application, the multiplier section of the XR-2228 is used as the quadrature phase-detector section of the block diagram of Figure 1. The op amp is used as a high-gain voltage comparator which converts the differential voltage level changes at the multiplier outputs into logic level output signals.

CIRCUIT OPERATION

Figure 6 shows the generalized circuit connection of the XR-2228, along with either the XR-210 or the XR-215 high frequency PLL IC, for tone- or carrier-detection application. Since the external connections for the XR-210 or the XR-215 are the same as those given in their respective data sheets, only the external circuitry associated with the XR-2228 is shown in the figure. The circuit, as shown, can operate with a single power supply, from 10V to 20V, or with split supplies in the range of ±5V to ±10V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 6 to ground.

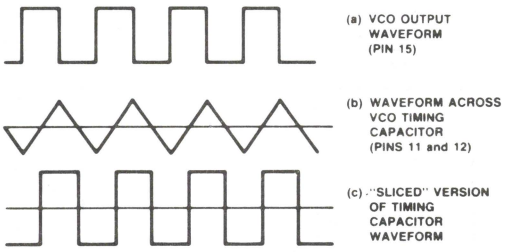


Figure 4. Timing Diagram of VCO Output Waveforms Available from XR-210 or XR-215 High-Frequency PLL Circuits

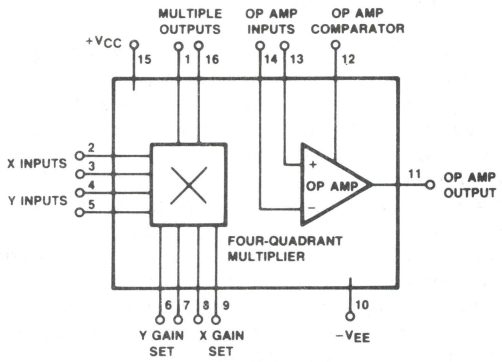


Figure 5. Functional Block Diagram of XR-2228 Multiplier/Detector

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used, and to the X-input terminal (Pin 2) of the XR-2228.

The Y-inputs (Pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at Pins 13 and 14 of the PLL IC) which is AC coupled to Pins 4 and 5 of the XR-2228 multiplier input. The multiplier input stage "slices" this signal to produce the quadrature frequency waveform shown in Figure 4(c).

The differential DC voltage level at the multiplier output terminals (Pins 1 and 6) is offset by means of an external resistor, R_A, as shown in Figure 6. This initial offset causes the op amp output of the XR-2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 6, the op amp output (Pin 11) would be at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (near $+V_{CC}$) when the PLL circuit is locked on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

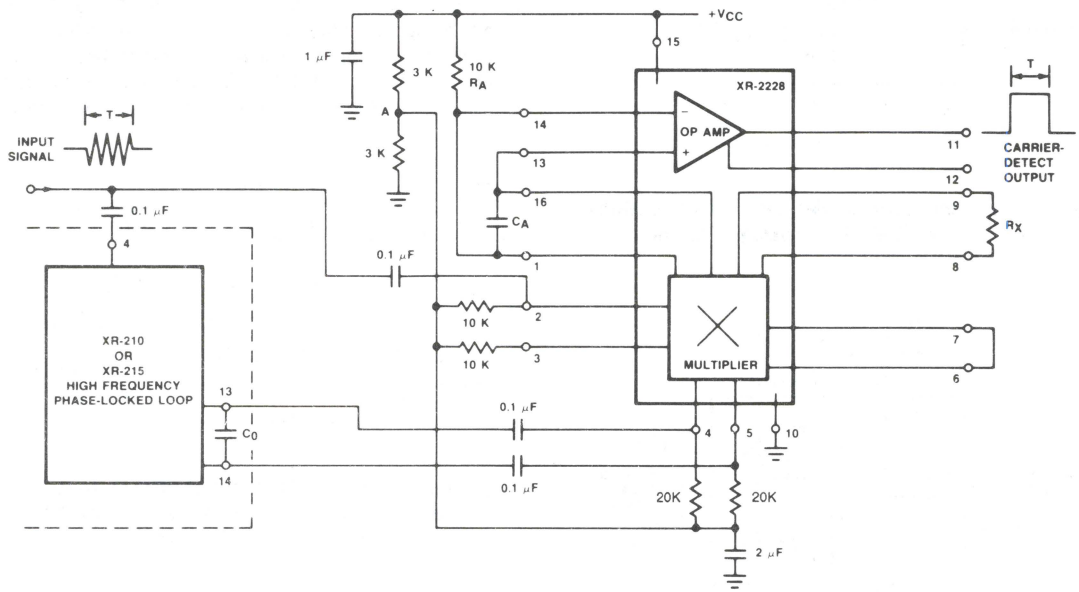


Figure 6. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone- or Carrier-Detector Application

The filter capacitor, C_A, connected across Pins 1 and 16 of the multiplier outputs, serves as the post- detection low-pass filter (Block 5 of Figure 1). The time constant of this filter is equal to (C_A R_B where R_B ($\approx$ 8KΩ is the internal resistance of the IC at Pins 1 and 16. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

If chatter or oscillation is seen on the output of the XR-2228 op amp, a compensation capacitor of 200pF from pin 12 to 11 should be added.

The detection threshold (minimum detectable input signal amplitude) varies inversely with the multiplier gain-setting resistor R_X. Figure 7 shows the typical detectable signal level, as a function of R_X, with the output offset resistor, R_A, equal to 10KΩ. Note that the minimum detectable input signal, with R_X = 0, is approximately 100mV, rms.

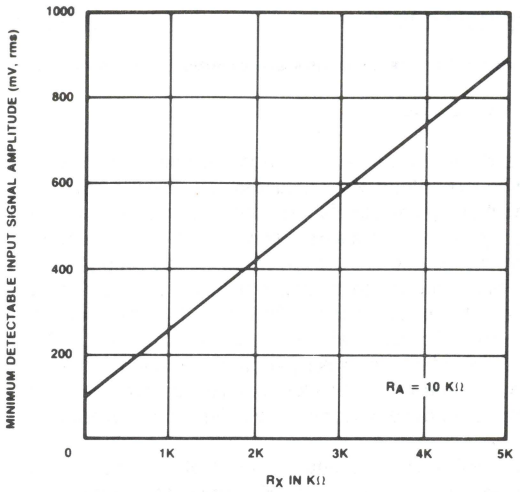


Figure 7. Minimum Detectable Input Carrier Level, as a Function of Multiplier Gain Setting Resistor, R_X

Frequency-Selective AM Detection Using Monolithic Phase-Locked Loops

Application Note

INTRODUCTION

This application note describes the use of monolithic phase-locked loop (PLL) circuits in detection of amplitude-modulated (AM) signals. The detection capabilities of a PLL system, which is a frequency-selective FM demodulator, can be extended to cover AM signals simply by the addition of an analog multiplier (or mixer) and a low-pass filter to the basic phase-locked loop. This technique of AM demodulation, which is called synchronous AM detection, offers significant performance advantages over conventional peak-detector type AM demodulators, in terms of its dynamic range and noise characteristics.

This application note outlines some of the fundamental principles of synchronous AM detectors, and gives design examples using the XR-2228 multiplier/detector IC in conjunction with the XR-215 and the XR-2212 monolithic PLL circuits.

PRINCIPLES OF OPERATION

The phase-locked loop AM detector circuits operate on the so-called "coherent AM detection" principle, where the amplitude modulated input signal is mixed with an unmodulated "coherent" carrier signal, and then low-pass filtered to produce the desired demodulated output signal. Figure 1 gives a simplified block diagram of such a detector system.

The amplitude-modulated input signal can be described by an expression of the form:

$$\text{Input Signal} = V_m(t) \cos \omega_o t$$

where $V_m(t)$ is the modulated amplitude of the input signal and ω_o is the input signal frequency expressed in radians/seconds. If this signal is linearly multiplied with an unmodulated signal which has the same frequency and phase as the input signal then the output of the multiplier, $V_0(t)$, is a composite signal of the form:

$$V_0(t) = K_0 V_m(t) [1 + \cos (2 \omega_o t)]$$

where K_0 is the gain of the multiplier circuit. If the above signal is then passed through a low-pass filter, to eliminate the double-frequency term, the resulting output signal is:

$$V_{out} = \text{Output Signal} = K_0 V_m(t)$$

which corresponds to the detected AM information.

The phase-locked loop AM detectors also operate on a similar principle: the PLL is made to "lock" on the carrier frequency of the input AM signal; then the VCO output of the PLL will regenerate the unmodulated coherent carrier signal necessary for detection. When this signal is mixed with the input AM signal and the resulting composite signal is passed through a low pass filter, one obtains the demodulated output. Figure 2 gives a block diagram of such an AM detector system. Compared to the basic synchronous AM detector system of Figure 1, the phase-locked loop AM detector of Figure 2 also has one added feature: the output of the PLL control voltage (i.e., output of the PLL low-pass filter) can be used as an FM detector or a frequency discriminator. Thus, such a system is capable of simultaneous AM and FM detection. In other words, the frequency and the amplitude modulation information present on the input signal can be separately and simultaneously demodulated. The particular design and application examples given in this application note fall into this category.

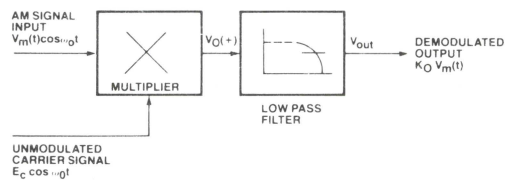


Figure 1. Block Diagram of a Synchronous AM Detector

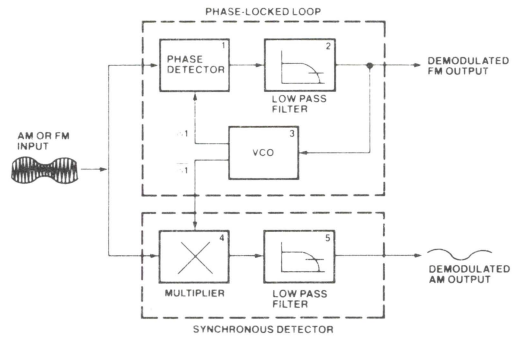


Figure 2. The Basic Phase-Locked Loop AM Detector

XR-2212 AND XR-2228 MONOLITHIC CIRCUITS

The XR-2212 monolithic PLL is made up of an input preamplifier, a phase-detector, a high-gain differential amplifier and a stable voltage-controlled oscillator (VCO) as shown in Figure 3. The key feature of the XR-2212 PLL is the temperature stability and the frequency accuracy of its VCO section; it offers 20 ppm/°C typical temperature stability and a frequency accuracy of ±1% for an external RC setting. The oscillator section of the XR-2212 contains a separate "quadrature output" terminal (Pin 15) which is particularly intended for interfacing with a synchronous AM detector such as the XR- 2228.

The XR-2228 multiplier/detector IC is specifically intended as a basic building block for synchronous AM detection. It contains a four-quadrant analog multiplier and a high-gain op amp on the same chip, as shown in the functional block diagram of Figure 4.

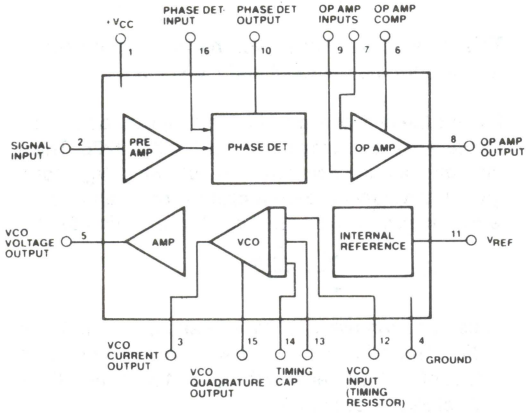


Figure 3. Functional Block Diagram of XR-2212 Precision Phase-Locked Loop

XR-215 HIGH FREQUENCY PHASE-LOCKED LOOP

The XR-215 is a high frequency phase-locked loop circuit capable operating with input signal frequencies up to 35MHz. It is comprised of a high frequency VCO, a phase-detector and an op amp section, as shown in the block diagram of Figure 5.

Unlike the XR-2212 PLL, the VCO section of the XR-215 does not have a separate quadrature output terminal. However, such a quadrature oscillator signal can be obtained by amplifying and "slicing" the triangle wave-form available across the timing capacitor (Pins 13 and 14) of the XR-215 oscillator section. Figure 6 shows the relative phase relationship of these oscillator wave-forms available from the circuit. The desired quadrature output signal (curve C of Figure 6) can be obtained by directly connecting one pair of the differential inputs of the XR-2228 directly across the timing capacitor terminals of the XR-215.

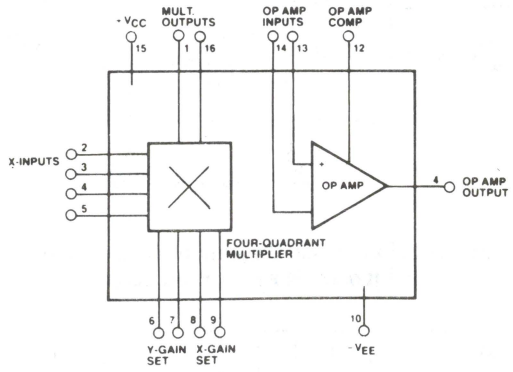


Figure 4. Functional Block Diagram of XR-2228 Multiplier/Detector IC

AM/FM DETECTION USING THE XR-2212 PLL

Figure 7 shows a generalized circuit connection diagram for a two-chip AM and FM detection system, utilizing the XR-2212 PLL and the XR-2228 multiplier/ detector. The XR-2212 section serves as the basic FM detector. The quadrature output of its VCO (Pin 15) is AC coupled to the Y input of the XR-2228.

The Y input of the XR-2228 is operated in its switching mode, with the Y gain terminals (Pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; and all the mutliplier inputs are DC biased from the internal reference output of the XR-2212 (Pin 11). The output of the multiplier, at Pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal.

The circuit configuration shown in Figure 7 can operate with a single power supply, over the supply voltage range, of 10V to 20V. Its operation or performance can be tailored for any particular AM and FM detection application by the choice external components shown in the figure, over a carrier frequency band of 1kHz to 300kHz. The functions of these external components are as follows:

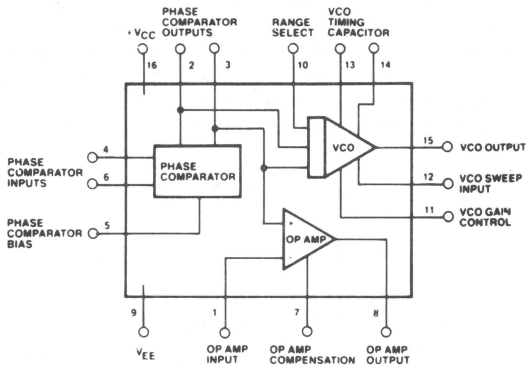


Figure 5. Functional Diagram of XR-215 High-Frequency Phase-Locked Loop

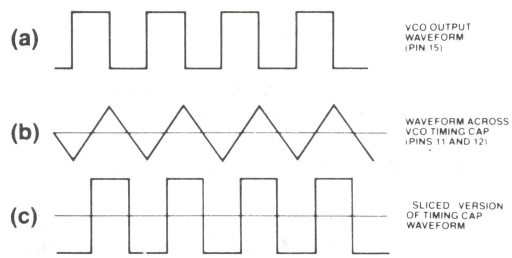


Figure 6. Timing Diagrams of VCO Output Waveforms from XR-215 Monolithic Phase-Locked Loop

a) R_0 and C_0 set the VCO center frequency for the XR-2212 PLL circuit. The center frequency, f_o, is given as:

$$f_0 = \frac{1}{R_0 C_0}$$

The VCO frequency f_0 is chosen to be equal to the carrier frequency of the input signal. R_0 is normally chosen to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. For most applications $R_0 \approx 20k\Omega$ is recommended. Once f_0 is given and R_0 is chosen, the C_0 can be calculated from the above equation.

b) R_1 determines the tracking bandwidth of the PLL. For a required tracking bandwidth, Δf (see Figure 9 of XR-2212 data sheet) and f_o, R_1 can be calculated as:

$$R_1 = R_0 \frac{f_0}{\Delta f}$$

This tracking bandwidth, Δf, is the band of frequencies in the vicinity of f_o, over which the PLL can maintain lock.

c) C_1 sets the loop-damping factor for the PLL. For most applications, C_1 is chosen to be equal to one-half of C_o.

d) R_2 and C_2 form a low-pass filter for the detected FM signal. The 3dB frequencing, f_2, of this low-pass filter is:

$$f_2 = \frac{1}{2\tau R_2 C_2}$$

Normally, f_2 is chosen to be equal to the demodulated FM information bandwidth.

e) R_C and R_{F1} set the gain of the op amp section of the XR-2212 as:

$$A_V = 1 + \frac{R_{F1}}{R_C}$$

This op amp section serves as the post-detection amplifier for the demodulated FM signals.

f) R_X sets the multiplier gain for the X input and R_{F2} sets the gain of the op amp section of the XR-2228. Thus, the demodulated AM signal output swing, V_{out}, for a given input signal of peak amplitude of V_M and modulation index of m ($0 \le m \le 1$) can be approximated as:

$$V_{out} = \frac{(V_M)m}{4} \frac{R_{F2}}{R_X}$$

Thus, for example, a 100mV peak input signal with 30% AM modulation (m = 0.3) will give a demodulated output of 150mV peak, with R_{F2} = 100kΩ and R_X = 5kΩ, at Pin 11 of the XR-2228.

g) C_3, in conjunction with the 5kΩ internal impedance of the multiplier output (Pin 16) serves as the low-pass post-detection filter for the demodulated AM signal.

For further explanation and description for the system design equations, the reader is referred to the XR-2212 and the XR-2228 data sheets.

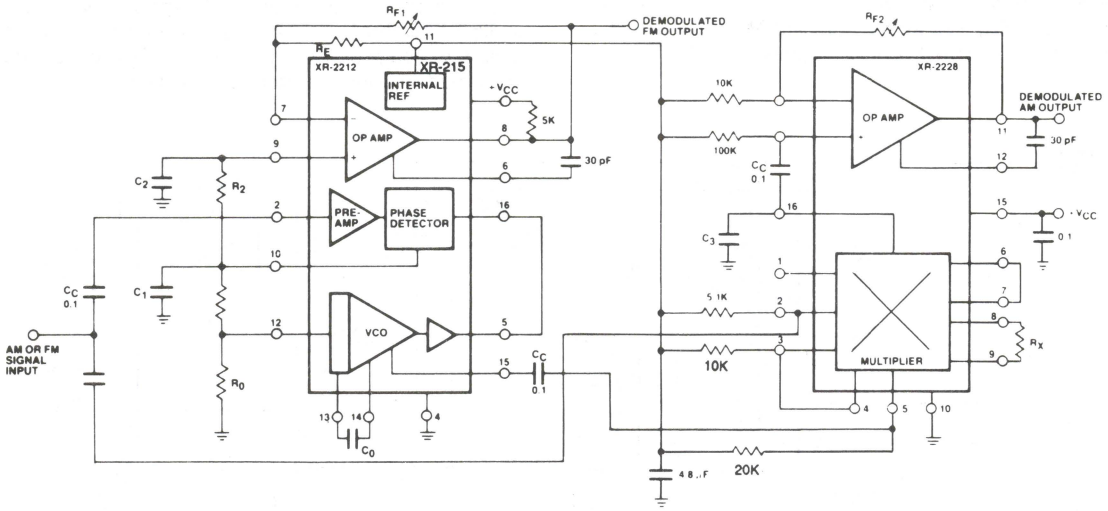


Figure 7. A Two-Chip AM/FM Detector System Using the XR-2212 Phase-Locked Loop and the XR-2228 Multiplier/Detector

Design Example

Design an AM demodulator for 100kHz carrier frequency with a detection (tracking) bandwidth of ±4%. The demodulated information bandwidth is 3kHz and an output level of one volt peak is required for a one volt peak input with 30% modulation.

Using the circuit of Figure 7, one proceeds as follows: Since FM detection is not required in this example, components R_2, C_2, R_C and R_{F1} are not essential to circuit operation. R_2 and R_C can be short-circuited, C_2 and R_{F1} can be left open-circuited. The rest of the component values are calculated as follows:

Step 1) Set f_0 = 100kHz by choosing R_0 = 20kΩ and calculating C_0 from paragraph (a) above.

$$C_0 = \frac{1}{R_0 f_0} = 500pF$$

Step 2) Determine R_1 to set tracking bandwidth to ±4%, from paragraph (b): R_1 = 500kΩ.

Step 3) Calculate C_1: $C_1 - C_0/2 \approx 250pF$.

Step 4) From paragraph (f), calculate the value of R_X and R_{F2}. For a typical choice of R_X = 5kΩ, and m = 0.3 (30% modulation) with one volt input carrier level, the value of R_{F2} to get one volt demodulated output is: R_{F2} = 67kΩ.

Step 5) Calculate C_3 to get 3kHz bandwidth for post-detection filter: $C_3 \approx 0.01\mu F$.

AM DETECTION USING THE XR-215 PLL

Figure 8 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit of Figure 8 is useful as a phase-locked AM detector for carrier frequencies up to 20MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate quadrature output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (Pins 13 and 14) of XR-215. The Y input of the XR-2228 is operated with maximum gain, since the Y gain control terminals (Pins 6 and 7) are shorted together. This causes the triangular waveform across C_0 to be converted to an effective quadrature drive as indicated by the timing diagram of Figure 6. The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X inputs of the XR-2228, are biased at approximately one-half of V_{CC}, by means of an external resistive divider.

In Figure 8, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The mode of operation of the XR-2228 is virtually the same as that described in connection with Figure 7: R_X sets the multiplier demodulation gain; C_3 serves as the low-pass post-detection filter. The values of R_X, R_{F2} and C_3 are calculated as given in paragraphs (f) and (g).

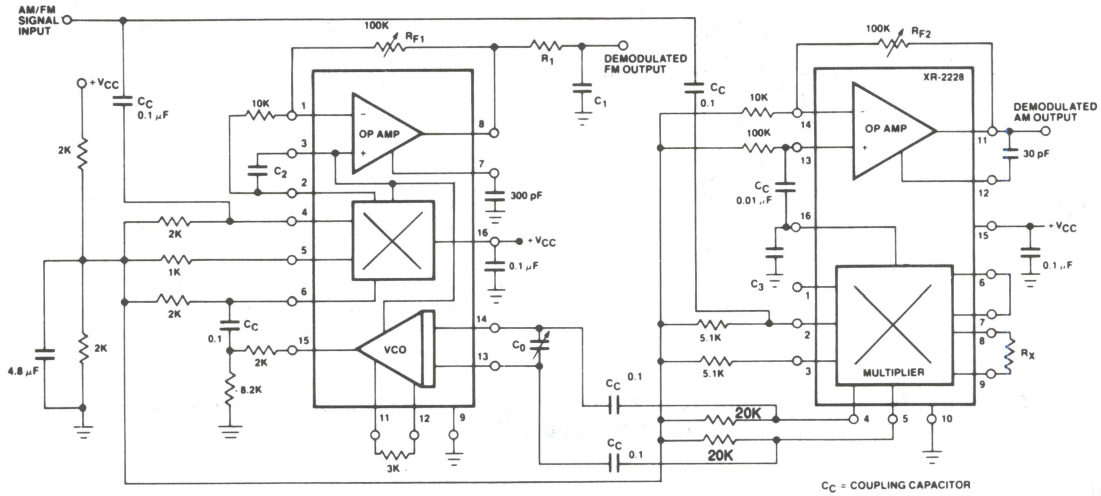


Figure 8. Circuit Connection tor a High-Frequency AM and FM Detector Using the XR-215 and XR-2228

High-Quality Function Generator System with the XR-2206

Application Note

INTRODUCTION

Waveform or function generators capable of producing AM/FM modulated sine wave outputs find a wide range of applications in electrical measurement and laboratory instrumentation. This application note describes the design, construction and the performance of such a complete function generator system suitable for laboratory usage or hobbyist applications. The entire function generator is comprised of a single XR-2206 monolithic IC and a limited number of passive circuit components. It provides the engineer, student, or hobbyist with a highly versatile laboratory instrument for waveform generation at a very small fraction of the cost of conventional function generators available today.

GENERAL DESCRIPTION

The basic circuit configuration and the external components necessary for the high-quality function generator system is shown in Figure 1. The circuit shown is designed to operate with either a 12V single power supply, or with 16V split supplies. For most applications, split-supply operation is preferred since it results in an output dc level which is nearly at ground potential.

The circuit configuration of Figure 1 provides three basic waveforms: sine, triangle and square wave. There are four overlapping frequency ranges which give an overall frequency range of 1Hz to 100kHz. In each range, the frequency may be varied over a 100:1 tuning range.

The sine or triangle output can be varied from 0 to over 6V (peak to peak) from a 600Ω source at the output terminal.

A squarewave output is available at the sync output terminal for oscilloscope synchronizing or driving logic circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

The performance characteristics listed below are not guaranteed or warranted by Exar. However, they represent the typical performance characteristics measured by Exar's application engineers during the laboratory evaluation of the function generator system shown in Figure 1. The typical performance specifications listed below apply only when all of the recommended assembly instructions and adjustment procedures are followed:

(a) **Frequency Ranges:** The function generator system is designed to operate over four overlapping frequency ranges:

1 Hz to 100Hz
10 Hz to 1kHz
100 Hz to 10kHz
1 kHz to 100kHz

The range selection is made by switching in different timing capacitors.

(b) **Frequency Setting:** At any range setting, frequency can be varied over a 100:1 tuning range with a potentiometer (see R_{13} of Figure 1).

(c) **Frequency Accuracy:** Frequency accuracy of the XR-2206 is set by the timing resistor R and the timing capacitor C, and is given as:

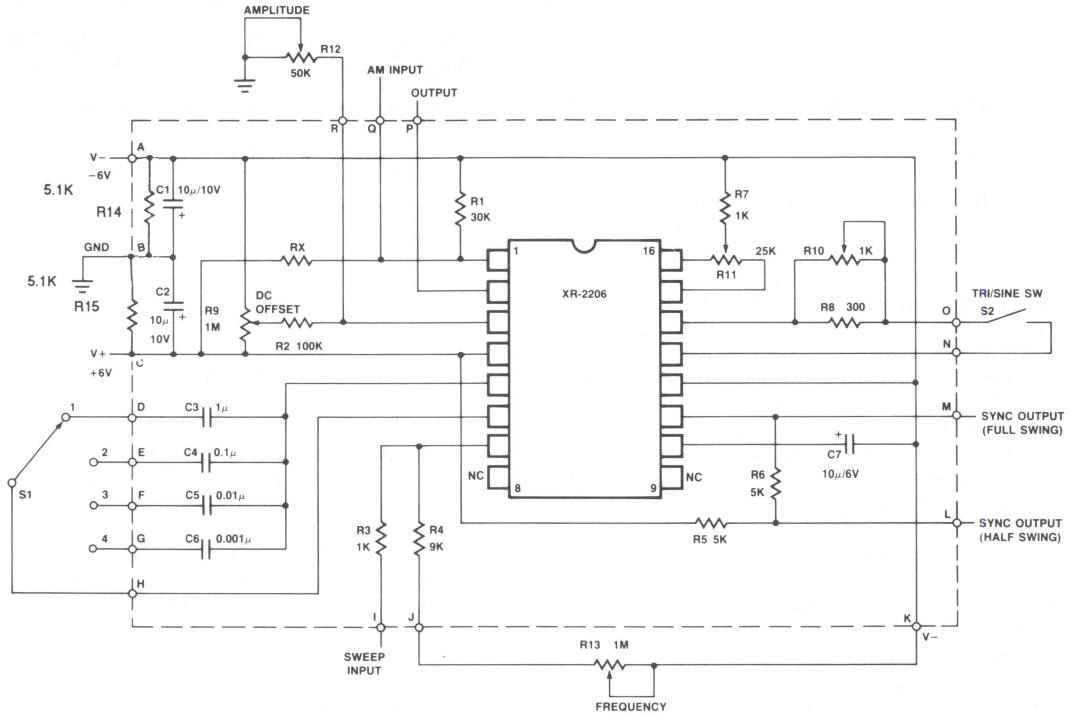
$$f = 1/RC$$

The above expression is accurate to within 15% at any range setting. The timing resistor R is the series combination of resistors R_4 and R_{13} of Figure 1. The timing capacitor C is any one of the capacitors C_3 through C_6, shown in the figure.

(d) **Sine and Triangle Output:** The sine and triangle output amplitudes are variable from 0V to $6V_{pp}$. The amplitude is set by an external potentiometer, R_{12} of Figure 1. At any given amplitude setting, the triangle output amplitude is approximately twice as high as the sinewave output. The internal impedance of the output is 600Ω.

(e) **Sinewave Distortion:** The total harmonic distortion of sinewave is less than 1% from 10Hz to 10kHz and less than 3% over the entire frequency range. The selection of a waveform is made by the triangle/sine selector switch, S_2.

(f) **Sync Output:** The sync output provides a 50% duty cycle pulse output with either full swing or upper half swing of the supply voltage depending on the choice of sync output terminals on the printed circuit board (see Figure 1).



NOTE:

1. For Single Supply Operation Lift GND Connection Keeping R12 Across Terminals R and B Intact, and Connect Terminal A to GND.

2. For Maximum Output, R_X may be open. R_X = 68 KΩ is Recommended for External Amplitude Modulation.

Figure 1. Circuit Connection Diagram for Function Generator. (See Note 1 for Single Supply Operation)

(g) **Frequency Modulation (External Sweep):** Frequency can be modulated or swept by applying an external control voltage to sweep terminal (Terminal I of Figure 1). When not used, this terminal should be left open circuited. The open circuit voltage at this terminal is approximately 3V above the negative supply voltage and its impedance is approximately 1000Ω.

(h) **Amplitude Modulation:** The output amplitude varies linearly with modulation voltage applied to AM input (terminal Q of Figure 1). The output amplitude reaches its minimum as the AM control voltage approaches the half of the total power supply voltage. The phase of the output signal reverses as the amplitude goes through its minimum value. The total dynamic range is approximately 55dB, with AM control voltage range of 4V referenced to the half of the total supply voltage. When not used, AM terminal should be left open-circuited.

(i) **Power Source:** Split supplies: 16V, or single supply: +12V. Supply Current 15mA (see Figure 2). For single supply operation bias resistors, R_{14} and R_{15} should be added, the GND point left floating and V^- tied to ground.

EXPLANATION OF CIRCUIT CONTROLS

Switches

Range Select Switch, S1: Selects the frequency range of operation for the function generator. The frequency is inversely proportional to the timing capacitor connected across Pins 5 and 6 of the XR-2206 circuit. Nominal capacitance values and frequency ranges corresponding to switch positions of S1 are as follows:

Position	Nominal Range	Timing Capacitance
1	1Hz to 100Hz	1μF
2	10Hz to 1kHz	0.1μF
3	100Hz to 10kHz	0.01μF
4	1Hz to 100kHz	0.001μF

If additional frequency ranges are needed, they can be added by introducing additional switch positions.

Triangle/Sine Waveform Switch, S2: Selects the triangle or sine output waveform.

Trimmers and Potentiometers

DC Offset Adjustment, R9: The potentiometer used for adjusting the dc offset level of the triangle or sine output waveform.

Sinewave Distortion Adjustment, R10: Adjusted to minimize the harmonic content of sinewave output.

Sinewave Symmetry Adjustment, R11: Adjusted to optimize the symmetry of the sinewave output.

Amplitude Control, R12: Sets the amplitude of the triangle or sinewave output.

Frequency Adjust, R13: Sets the oscillator frequency for any range setting of S1. Thus, R13 serves as a frequency dial on a conventional waveform generator and varies the frequency of the oscillator over an approximate 100 to 1 range.

Terminals

A. Negative Supply -6V
B. Ground
C. Positive Supply +6V
D. Range 1, timing capacitor terminal
E. Range 2, timing capacitor terminal
F. Range 3. timing capacitor terminal
G. Range 4, timing capacitor terminal
H. Timing capacitor common terminal
I. Sweep Input
J. Frequency adjust potentiometer terminal
K. Frequency adjust potentiometer negative supply terminal
L. Sync output (1/2 swing)
M. Sync output (full swing)
N. Triangle/sine waveform switch terminals
O. Triangle/sine waveform switch terminals
P. Triangle or sinewave output
Q. AM input
R. Amplitude control terminal

PARTS LIST

The following is a list of external circuit components necessary to provide the circuit interconnections shown in Figure 1.

Capacitors:

C1, C2, C7	Electrolytic, 10μF, 10V
C3	Mylar, 1μF, nonpolar, 10%
C4	Mylar, 0.1μF, 10%
C5	Mylar, 0.01μF, 10%
C6	Mylar, 1000pF, 10%

Resistors.

R1	30KΩ, 1/4 W, 10%
R2	100KΩ, 1/4 W, 10%
R3, R7	1KΩ, 1/4 W, 10%
R4	9KΩ, 1/4 W, 10%
R5, R6	5KΩ, 1/4 W. 10%
R8	300KΩ,1/4 W, 10%
RX	62KΩ, 1/4 W, 10% (RX can be eliminated for maximum output)

The following two resistors are used in single supply applications:

R14, R15	5.1KΩ, 1/4 W 10%

Potentiometers:

R9	Trim, 1MΩ, 1/4 W
R10	Trim, 1KΩ, 1/4 W
R11	Trim, 25KΩ, 1/4 W

The following additional items are recommended to convert the circuit of Figure 1 to a complete laboratory instrument:

Potentiometers:

R12	Amplitude control, linear, 50KΩ
R13	Frequency control, audio taper, 1MΩ

Switches:

S1	Rotary switch, 1-pole, 4 positions
S2	Toggle or slide, SPST

7" x 4" x 4" (approx.) Metal or Plastic
(See Figure 4(b).)

Power Supply:

Dual supplies 16V or single +12V
Batteries or power supply unit
(See Figures 3(a) and 3(b).)

Miscellaneous:

Knobs, solder, wires, terminals, etc.

BOARD LAYOUT

Care should be given to the layout of the board, to prevent noise from the supplies from affecting the XR-2206 performance.

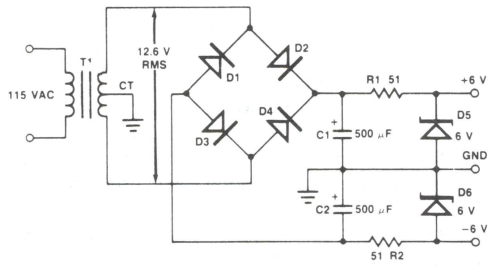
Any simple power supply having reasonable regulation may be used. Figure 2 gives some recommended power supply configurations.

Precaution: Keep the lead lengths small for the range selector switch. This will reduce stray capacitance.

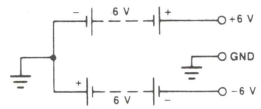
ADJUSTMENT PROCEDURE

When assembly is completed and you are ready to put the function generator into operation, make sure that the polarity of power supply and the orientation of the IC unit are correct Then apply the dc power to the unit.

To adjust for minimum distortion, connect the scope probe to the trianglelsine output. Close S2 and adjust the amplitude control to give non-clipping maximum swing. Then adjust R10 and R11 alternately for minimum distortion by observing the sinusoidal waveform. If a distortion meter is available, you may use it as a final check on the setting of sine-shaping trimmers. The minimum distortion obtained in this manner is typically less than 1% from 1Hz to 10kHz and less than 3% over the entire frequency range.



(a) Zener Regulated Supply



(b) Battery Power Supply

T1: Filament Transformer
Primary 115V Secondary 12.6 VCT, 0.5A
D1 — D4: IN4001 or Similar
D5, D6: IN4735 or similar
R1, R2: 51Ω, 1.2W, 10%

Figure 2. Recommended Power Supply Configurations

Designing Wide-Tracking Phase-Locked Loop Systems

Application Note

INTRODUCTION

Phase locked-loops with their excellent frequency tracking characteristics have found their way into many applications where synchronizing or synthesizing of signals is required. Although they do have the ability to track an incoming signal very well, the actual tracking range is quite limited by the nature of PLL's to less than 2:1. This range of less than 2:1 must be observed if harmonic locking, a plague to the designer, is to be avoided.

This application note describes the design of tracking PLL with a tracking range of greater than 100:1, with no harmonic locking problems. This design uses the XR-2212 Precision Phase-Locked Loop in conjunction with the XR-320 Monolithic Timer and an XR-084 Quad BiFet Operational Amplifier to form a wide range PLL with automatic tuning.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the tracking PLL. The circuit is comprised of three blocks: the PLL, the Frequency to Voltage Converter, and Precision Clamping Circuit. The blocks operate as follows. The PLL locks onto the incoming frequency and produces an output frequency identical to that of the input, but phase shifted. The center of the lock range is controlled by V_1. V_1 is derived from the F/N converter, which produces a voltage proportional to the incoming frequency. This voltage, V_1, thus provides an automatic PLL center frequency tuning signal. The swing of the phase detectors filtered voltage, V_2, controls the amount the VCO can be moved about its center frequency. The precision clamp fixes the swing on V_2 to a fixed percentage of V_1, keeping the tracking range of the PLL constant as its center frequency is varied.

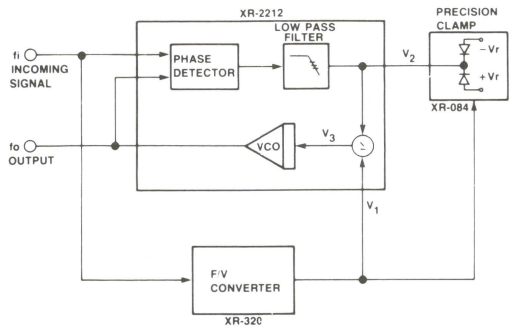


Figure 1. Tracking PLL Block Diagram

The actual driving voltage for the VCO is now a voltage proportional to fi which can be varied a fixed percentage by the phase detector.

CIRCUIT DESIGN

The heart of the circuit is the XR-2212 Precision Phase-Locked Loop. Figure 2 shows the XR-2212's internal blocks and necessary external components. The VCO in the XR-2212 is actually a current controlled oscillator.

Pin 12 is fixed at the reference voltage, $V_r = \frac{V+}{2}$, and the the current drawn from this terminal controls the frequency of oscillation of the VCO, f_0. With R_0 grounded, as shown, the VCO's free running or center frequency is:

$$f_0 = \frac{1}{R_0 C_0}$$

R_0 and C_0 are calculated using this relationship at f_0 maximum. With the PLL locked on its center frequency, the phase detector's dc output, Pin 10, is also at V_r and the current flowing in R_0 is proportional to f_0. If the bottom end of R_0 is now raised above ground, the current in R_0 will change linearly with the voltage, as will to thus providing the voltage control input for the VCO. If R_0 is left at zero volts and fi is moved, the dc voltage at Pin 10 will inversely follow fi, increasing fi decreases the voltage at Pin 10, modulating the current from Pin 10 and thus f_0. The maximum swing of Pin 10 is $\simeq \pm V_r$, giving the following relationship:

$$\pm \frac{\Delta f}{f_o} = \frac{\frac{\pm V_r}{R_1}}{\frac{V_r}{R_0}} = \frac{R_0}{R_1} \pm \frac{(V_r R_0)}{V_r R_1} = \pm \frac{R_0}{R_1}$$

Δf being the PLL's tracking range.

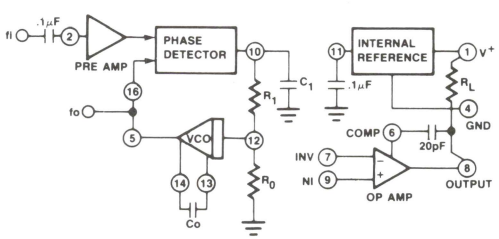


Figure 2. XR-2212 Internal Blocks with External Components

In our application a constant $\frac{\Delta f}{f_0}$ is desired, so if the output of the phase detector, Pin 10, is clamped to ~ V_{R0}, the voltage across R_0, a constant tracking range will be maintained. C_1 serves as the loop, low pass filter, and is made to equal $\frac{C_0}{4}$ for a damping of 1/2.

The voltage driving R_0 comes from the F/V converter which is formed by the XR-320 Monolithic Timer. The internal blocks and external components of the XR-320 are shown in Figure 3. The input to the F/V is brought to the trigger input, Pin 6, which, when driven above the threshold, triggers the F/F and opens the internal switch transistor, S_1. The voltage on C_T will linearly rise, at a rate set by R_T until V_r is reached at which time the comparator resets the F/F and closes S_1, waiting now for the next rising edge on Pin 6. Once triggered the output (Pin 12) will go low for the timing period defined by the relationship:

$$T_{low} = 2R_TC_T$$

Since Pin 12 will now have a constant low time and a repetition rate equal to that of the incoming signal, fi, it can be filtered to provide a voltage proportional to fi. Figure 4 shows the complete tracking PLL circuit. The precision clamp is formed by A_1–A_3 which samples the voltage across R_0 and clamps the XR-2212's phase detectors output to $\pm V_{R0}$. With the given values, the tracking range of the circuit is one 1kHz to 100kHz, with the XR-2212's tracking range set at approximately ±0.33 f_0. The input frequency voltage range is 10mV RMS to 3V RMS with the output producing a $10V_{P-P}$ square wave. Calibration is done by first applying 100kHz to the input and adjusting P_1 for f_0 equal to fi in frequency but shifted in phase by approximately 90°, then with fi = 1kHz P_2 is adjusted again for equal frequencies with 90° of phase shift.

WIDE RANGE SYNTHESIZER USING XR-2212 PLL

This same technique of automatic tuning can be used to form a wide range synthesizer as shown in the block diagram of Figure 5. Here a programmable frequency divider has been put into the loop between the VCO output and the phase detector input. Since the PLL will drive the VCO until its two inputs are at the same frequency, the VCO will be at:

$f_{VCO} = Nf_r$ where N in the binary number applied to the programmable divider ($N \geq 1$)

The F/V converter used in the previous application, R_0, which was used to tune the PLL, is now replaced with a digital-to-analog converter (DAC). Its digital inputs come from the same lines which control N. The DAC's output voltage, which drives R_0, will now vary proportionally with N, or retuning the PLL with each new N. The same clamping network is used on the phase detectors output as discussed earlier.

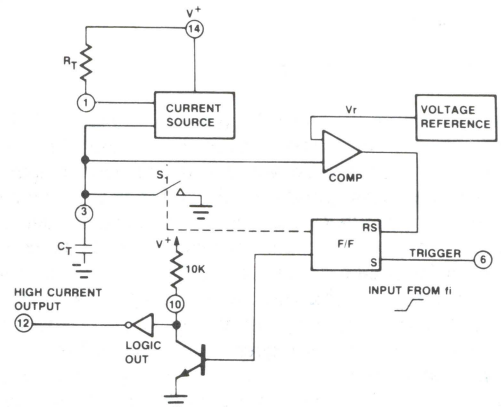


Figure 3. XR-320 Internal Blocks with External Components

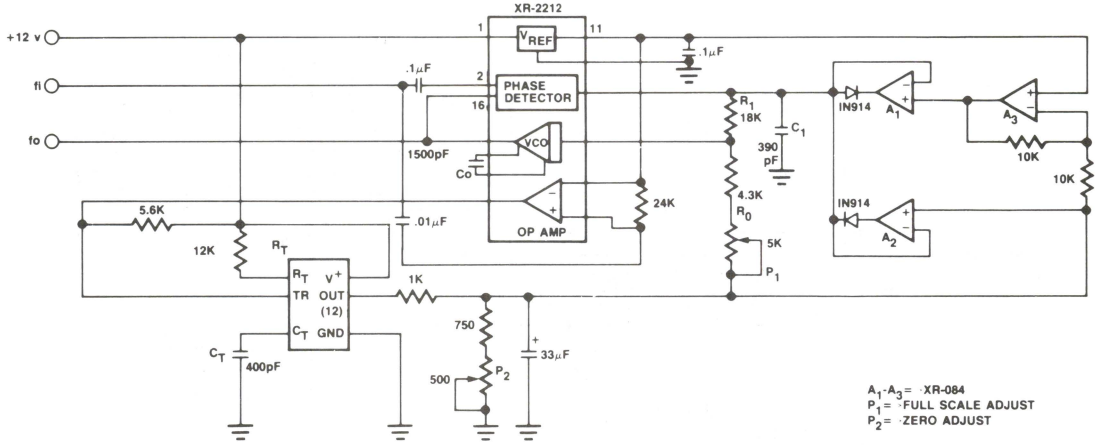


Figure 4. Wide Range Tracking PLL

Figure 6 shows the complete wide range synthesizer circuit. The two 4-bit binary counters, 74161, and magnitude comparator, 8130, form the programmable divider. The output of the divider is a variable duty cycle pulse so that the flip-flop, 7474, was added so that phase detector was always presented with a square wave. Since the flip-flop also divides by two, the minimum value for the divider will be 2 or the actual N of the overall divider will be the binary input times two, 2N. The DAC uses the reference voltage of the XR-2212 as its reference with amplifier A_4 used to scale the voltage to R_0 correctly. C_1 provides loop compensation and its value will determine not only the response of the circuit but the short term frequency stability of f_0. A trade off must be made here as decreasing C_1 will provide for a faster responding loop but decrease the short term stability of f_0. It is probably most desirable to have a highly stable output frequency and slower responding loop.

With the values shown, f_o will be 1 kHz to 100kHz with f_{ref} = 500Hz and N = 1 to 100. The reference input voltage range is 10mV RMS to 3V RMS with the output providing a T^2L compatible square wave.

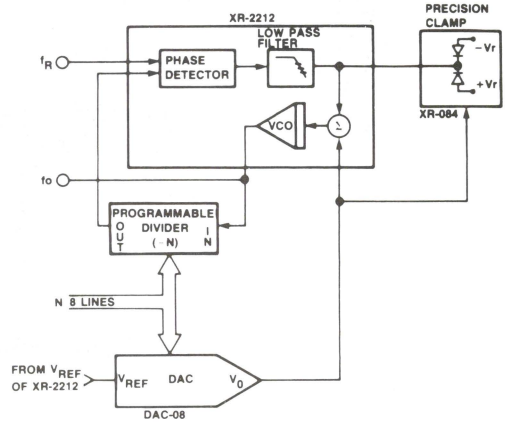


Figure 5. Wide Range Synthesizer Block Diagram

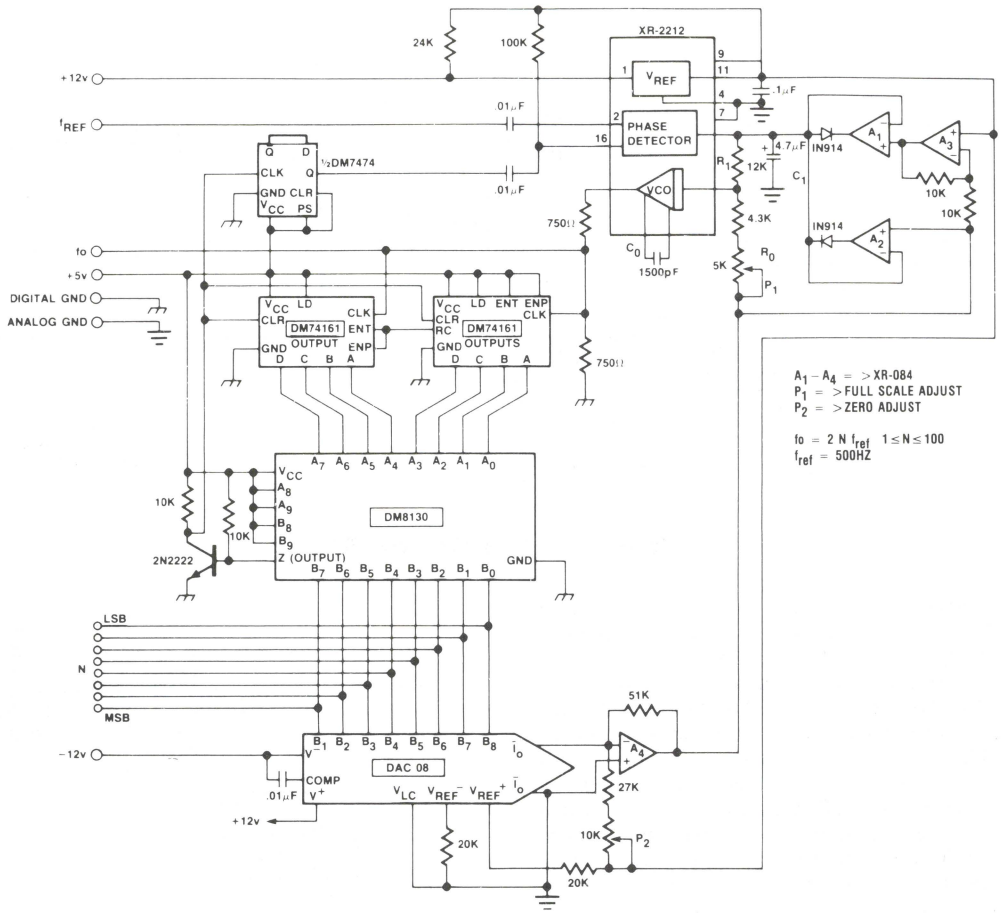


Figure 6. Wide Range Synthesizer

Calibration is done by first adjusting P_1 for a 100kHz output with N = 100 and then adjusting P_2 for a one kHz output with N = 1.

Typical input and output waveforms for r_{ref} = 500Hz, top trace, and f_o, bottom trace, with N switching from 40 to 8 are shown in Figure 7.

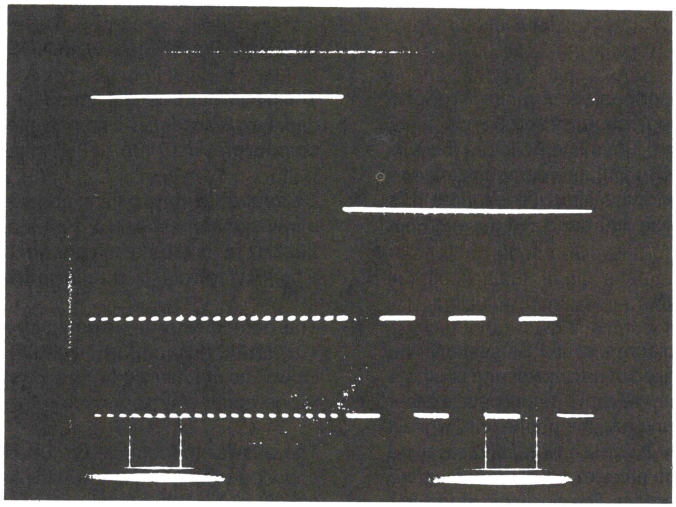


Figure 7. Typical Input and Output Waveform

Building a Complete FSK Modem Using XR-2211 and XR-2206

Application Note

INTRODUCTION

The application note describes the construction of a simple modem system using frequency shift keying, FSK, for serial data transmission. The system utilizes the XR-2206 as a modulator, the XR-2211 as a demodulator, and an XR-4136 amp as a bandpass filter. These three IC's make up a complete working 300 baud, full duplex, FSK modem.

GENERAL DESCRIPTION

Figure 1 shows the block diagram of an FSK system. The complete system is comprised of an answer and originate modem. The answer modem will convert input data to either 1070Hz or 1270Hz and send it to the phone line, while it will decode to "1's" and "0's" 2025Hz and 2225Hz received from the line. The originate modem simply reverses the frequencies for send and receive. The sinewave modulator will produce two discrete frequencies at its output corresponding to a "1" or a "0" at its data input. The line hybrid will steer these frequencies to the phone line while causing received frequencies to go to the bandpass filter and demodulator. This block will therefore provide isolation between modulator and demodulator at each end. The bandpass filter is used to remove unwanted signals and noise received from the phone line before they reach the demodulator.

The PLL demodulator will lock onto incoming frequencies at its input and produce "1's" or "0's" at its output. The carrier detect output will produce a low, "0" signal out when valid data is being received.

OPERATION AND CALIBRATION

The circuit has been designed for +12 volt operation. The data inputs accept TTL compatible signal levels, while the outputs provide 0V to +12V signal levels.

Calibration is done by first adjusting the modulator. With a low signal on its input, R_{21} is adjusted for 1270Hz or 2225Hz for originate and answer respectively. Then with a high signal in, R_{22} is adjusted for 1070Hz or 2025.

The demodulator is adjusted by feeding an alternating 1070Hz/1270Hz or 2025Hz/2225Hz signal to the modem input. The modulating frequency should be 150Hz, which is one-half the system baud rate of 300.

The answer modem can be used to drive the originate and vice-versa. R_{19} is then adjusted for a square-wave of 50% duty cycle on the data received output.

R_{20} is used to set the modulator output level. With the modulator output set at –6dBm, the system will operate with an input signal range of +10dBm to –48dBm.

CIRCUIT CONSTRUCTION

Figures 2 and 3 show the circuit schematic and component layout. One PC board is used for answer or originate and should use the appropriate components as listed in Table 1.

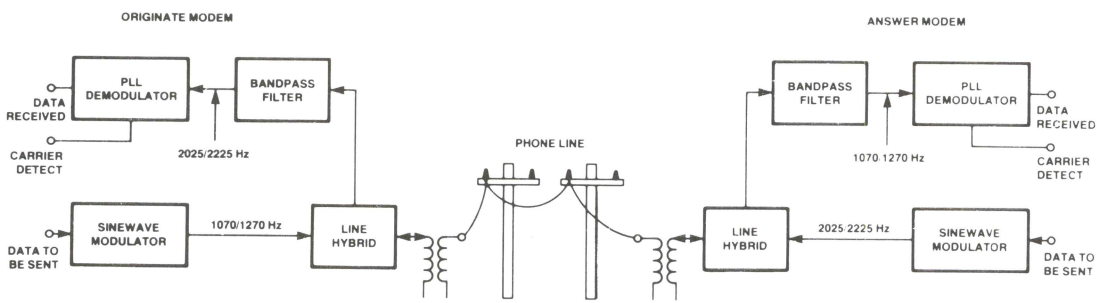


Figure 1. Block Diagram of FSK Modem System

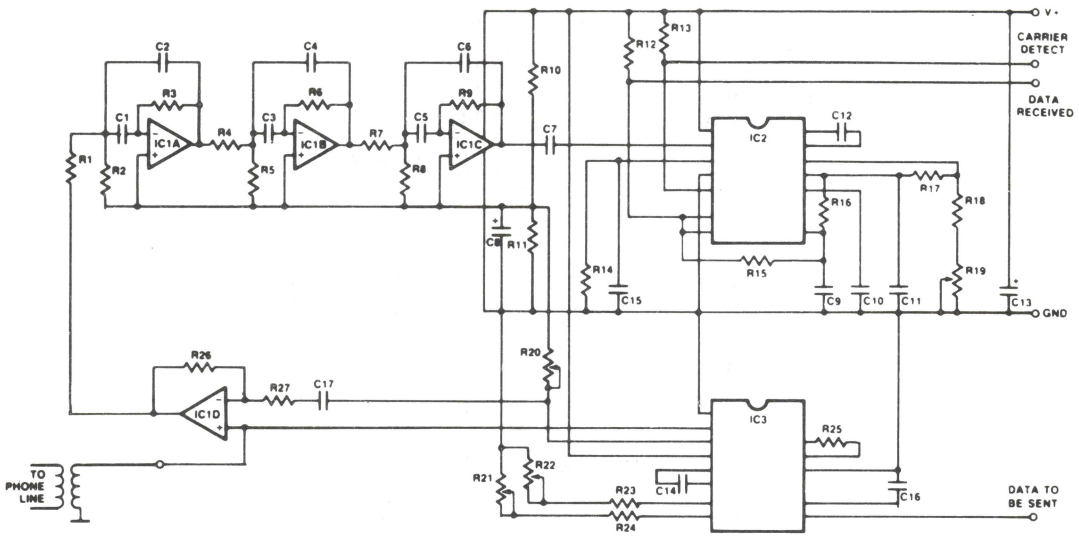


Figure 2. Complete FSK Modem Using XR-2211 and XR-2206

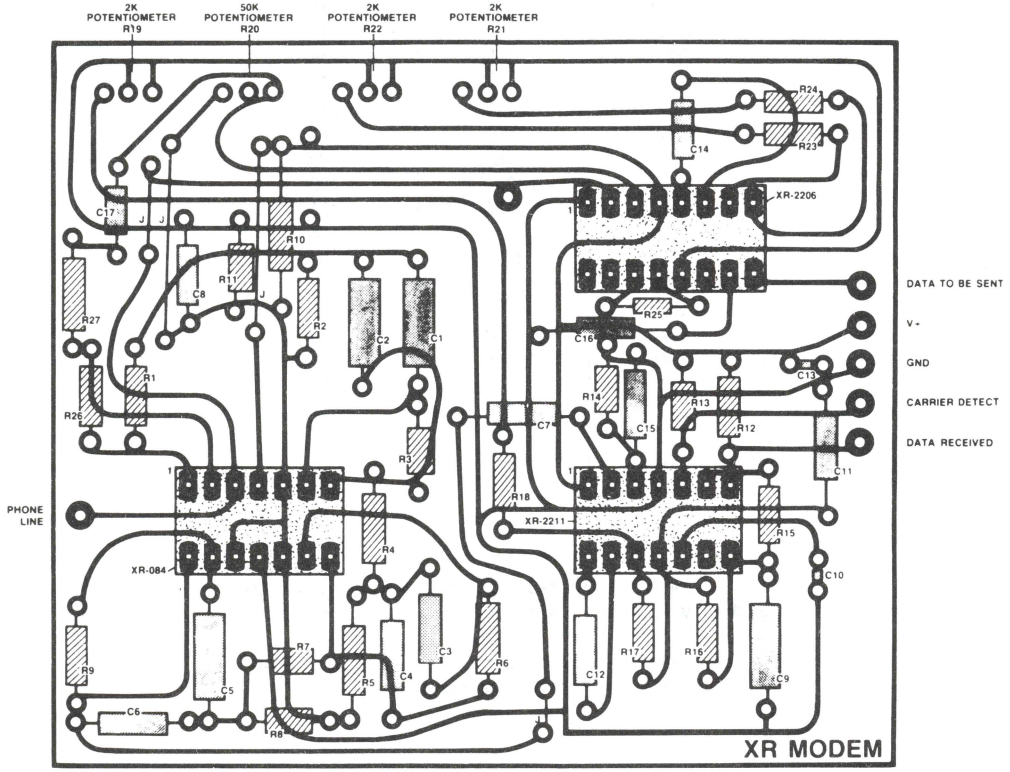


Figure 3. XR Modem Foil Side Shown (Not to Scale)

Table 1. Modem Parts List

IC1A-D IC2 IC3	XR-4136 XR-2211 XR-2206	
	ANSWER	**ORIGINATE**
R1*	40.2K	47.5K
R2*	499	191
R3*	270K	357K
R4*	60.4K	39.4K
R5*	680	160
R6*	383K	270K
R7*	24.9K	20K
R8*	1.21K	360
R9*	160K	160K
R10	1K	1K
R11	1K	1K
R12	5.1K	5.1K
R13	5.1K	5.1K
R14	510K	510K
R15	510K	510K
R16	100K	100K
R17	47K	100K
R18	7.5K	9.1K
R19	2K	2K
R20	50K	50K
R21	2K	2K
R22	2K	2K
R23	3.9K	8.2K
R24	3.6K	6.8K
R25	200	200
R26	1M	1M
R27	1M	1M
C_1–C_6*	0.01	0.01
C7	0.1	0.1
C8	22	22
C9	0.01	0.01
C10	0.1	0.1
C11	0.022	0.01
C12	0.1	0.047
C13	1	1
C14	0.1	0.1
C15	0.1	0.1
C16	1	1
C17	1	1

All resistors are 1/4 watt –5% tolerance, except as marked with (*) which are 1% tolerance. Values given in (Ω).

All capacitors are 5% tolerance, except as marked with (*) which are 1% tolerance. Values given in μF.

High-Performance Frequency-to-Voltage Converter Using the XR-2211

Application Note

INTRODUCTION

A stable highly linear f/v converter can be easily designed using the XR-2211 phase locked loop. The f/v can be used for a dynamic range from ±1% to ±80% over a frequency range of .01Hz to 1MHz.

The block diagram of the f/v is shown in Figure 1. The circuit will perform f/v conversion according to the relationship

$$f_{IN} = -K_1 V_0 + K_2$$

where K_1 and K_2 are set by the designer.

The transfer function relating V_O to f_{IN} is shown in Figure 2. The carrier detect output, Q, (Pin 6) which goes high over the tracking range is shown in Figure 3.

The basic circuit diagram is shown in Figure 4. The slope K_1 is determined by the relationship

$$K_1 = \frac{-1}{V_R C_O R_1}$$

where $V_R = V_{CC}/2 - 650mV$
V_{BE} = 650mV 1.3V typically under absolute maximum conditions.

The x intercept or upper frequency, K_2 is determined by the relationship

$$K_2 = \frac{R_0 + R_1}{R_0 R_1 C_0} = f_{MAX}$$

DESIGN EXAMPLE

Design a f/v converter for the frequency range 100Hz to 600Hz.

The first step is to calculate the center frequency f_o, (Figure 2) in

$$f_o = \frac{f_L + f_H}{2} = \frac{100 + 600}{2} = 350Hz$$

Supply voltage is directly proportional to the degree of resolution obtainable.

In order to obtain a greater resolution a higher supply voltage is used. For this design an 18V supply is used giving us a resolution of approximately

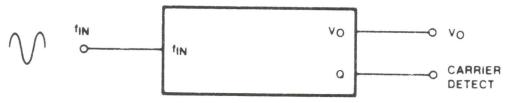


Figure 1. F/V Block Diagram

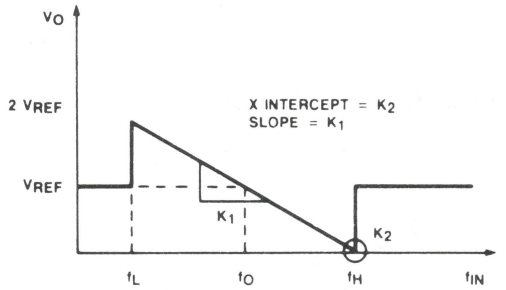


Figure 2. F/V Transfer Function

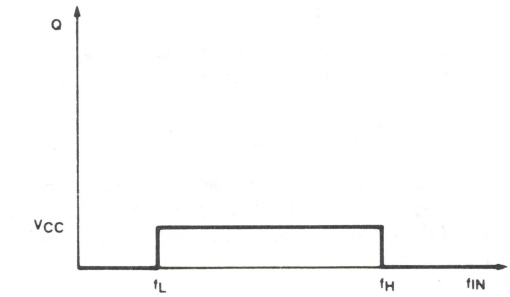


Figure 3. F/V Carrier Detect Output

$$\text{resolution} \approx \frac{V_{CC} - V_{BE}}{f_H - f_L} = \frac{18 - 1.3}{600 - 100} = \frac{33.4mV}{Hz}$$

for V_{CC} = 18V

We can now calculate V_{REF}

$$V_{REF} = V_{CC}/2 - V_{BE} = 9V - .65V = 8.35V$$

The center frequency is given by

$$f_o = \frac{1}{R_O C_O}$$

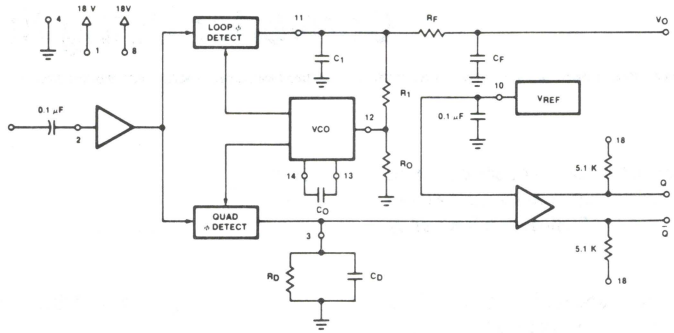


Figure 4. F/V Circuit Diagram

choosing $R_0 = 20K$ and rearranging

$$C_0 = \frac{1}{R_0 F_0} = \frac{1}{(20K\Omega)\,(350Hz)}$$
$$= .143\mu F$$

Since $$\frac{R_0}{R_1} = \frac{(f_H - f_L)}{2\,f_o}$$

$$R_1 = \frac{2\,f_0\,R_0}{(f_H - f_L)} = \frac{2\,(350Hz)\,(20K)}{(600 - 100)\,Hz}$$
$$= 28K$$

The selection of C_1, the loop filter capacitor has a degree of flexibility in its value. For a damping coefficient of 1/2

$$C_1 \approx \frac{C_0}{4} = \frac{.143\mu F}{4} = .035\mu F$$

It should be noted that an increased value of C_1 will increase response time but reduce ripple, while a decreased value of C_1 will reduce response time, increase capture range, but increase ripple.

The slope K_1 can now be calculated

$$K_1 = \frac{1}{V_R C_0 R_1} = \frac{1}{(8.35)\,(.143\mu F)\,(28K)}$$
$$= 29.91\ \frac{Hz}{V}$$

and since $K_2 = f_{MAX} = 600Hz$

The transfer function is then given by

$$f_{IN} = -29.91\ V_0 + 600$$

The filter $R_F\,C_F$ forms a one-pole post detection filter, with a time constant

$$\tau = R_F\,C_F$$

and a cut-off frequency

$$f_C = \frac{1}{2\mu R_F C_F}$$

Selecting $R_F = 100K$, C_F is then given by

$$C_F \approx \frac{3}{\Delta f/\Delta t}\ \mu F$$

where $\frac{\Delta f}{\Delta t}$ = maximum expected rate of change of input frequency

for $$\frac{\Delta f}{\Delta t} = 300\ cycles/sec$$

$$C_F = \frac{3}{300}\ \mu F = .01\mu F$$

giving $\tau = 1\ \mu secs$ $F_C = 160Hz$

A carrier detect output is available at Pins 5 and 6 (Q and $\overline{Q}$). The components C_D and R_D comprise the lock-detect filter. For $R_D = 470K$, and a capture range approaching the lock range, a minimum value of C_D is given by

$$C_D(\mu F) \geq \frac{16}{f_H - f_L} = \frac{16}{500} = .032\mu F$$

$R_D = 470K$

TEMPERATURE STABILITY

The XR-2211 is characterized by excellent temperature stability, in the order of 50ppm/°C. The output voltage temperature coefficient can be calculated by

$$\frac{V}{°C} \times \frac{1}{K_1} \times \frac{50ppm}{°C} \times (f_H - f_L)$$

substituting

$$= \frac{3.4mV}{Hz} \times 50ppm \times (600 - 100)\,Hz$$

$$= \frac{.8mV}{°C}$$

Digitally Programmable Phase-Locked Loop

Application Note

INTRODUCTION

Most phase-locked loops require manual potentiometer adjustment if the center frequency of the circuit is critical. Also, once adjusted, if ambient temperature changes cause the PLL's VCO or center frequency to shift, the potentiometer would have to be readjusted if the accurate center frequency was to be maintained. Readjustments are, of course, an impractical solution.

This application note describes the design of a digitally programmable PLL. Being digitally controlled, a microprocessor or other digital circuitry could easily tune or retune the VCO when necessary. The design uses the XR-215 monolithic PLL together with the BA-9201 D/A converter, which provides the tuning function.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the digitally programmable PLL. The circuit is comprised of two blocks: the PLL and the D/A converter. The PLL is used for FM demodulation, synchronzing signals, or frequency synthesis. These signals, are centered around its free-running frequency, f_o, which is set by the internal voltage-controlled oscillator. The VCO within the XR-215 is really a current-controlled oscillator, (ICO), the frequency of oscillation of the ICO proportional to the timing current, I_T. I_T is made up of two components: an internal fixed current and an externally programmable current, $I_{PIN\ 10}$. This $I_{PIN\ 10}$ control current is provided by a D/A converter with a current output. Since the D/A provides an output current that is directly set by an input digital code, this code will actually control the center frequency of the PLL's ICO, f_o.

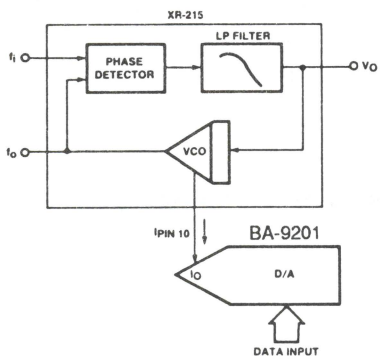


Figure 1. Programmable PLL Block Diagram

CIRCUIT DESIGN

Figure 2 shows the XR-215 internal blocks and necessary external components. The VCO center frequency, f_o, is calculated by the formula:

$$f_o = \frac{200}{C_O}\left(1 + \frac{0.6}{R_X}\right)\begin{matrix} C_O \text{ in } \mu F \\ R_X \text{ in } K\Omega \end{matrix} \qquad (1)$$

In this application it is desirable to have a variable current drawn from Pin 10, and R_X omitted. Equation 1 is then modified to equation 2 where a current issued instead of a resistor.

$$f_o = \frac{200}{C_O}\left(1 + I_{PIN\ 10}\right)\begin{matrix} C_O \text{ in } \mu F \\ I_{PIN\ 10} \text{ in mA} \end{matrix} \qquad (2)$$

Equation 2 can now be used to determine $I_{PIN\ 10}$ for a given f_o adjustment range. Once the center frequency has been set, R_O can be calculated to adjust the tracking range using the relationship:

$$\pm\Delta W_L = 2\pi\Delta f_L = \frac{1565}{R_O C_O}\ \frac{\text{rad}}{\text{sec}}\ \begin{matrix} R_O \text{ in } K\Omega \\ C_O \text{ in } \mu F \end{matrix} \qquad (3)$$

or

$$R_O = \frac{1565}{2\pi\Delta f_L C_O}\quad R_O \text{ in } K\Omega,\ C_O \text{ in } \mu F \qquad (4)$$

Now with R_O calculated for Δf_L, the capture range, Δf_C is set using the loop time constant capacitors C_1:

$$\pm\Delta W_C = \sqrt{\frac{K_O K\phi}{\tau_1}} = 2\pi\Delta F_C \qquad (5)$$

τ_1 = Loop Time Constant
K_O = VCO Conversion Gain
$K\phi$ = Phase Detector Conversion Gain

Substituting the values for $K_O K\phi$ and solving for F_C:

$$\Delta F_C = \frac{1}{2\pi}\sqrt{\frac{0.684}{R_O C_O C_1}} \qquad (6)$$

or

$$C_1 = \frac{0.017}{\Delta f_C^2 R_O C_O}\quad R_O \text{ in } K\Omega,\ C_O \text{ in } \mu F \qquad (7)$$

The resistors R_I and R_F are used to set the gain of the op amp when used for FM demodulation. C_C is op amp compensation and is in the range of 300pF for unity gain to 50pF for a gain of 10 and up. The resistors going to Pins 4, 5, and 6 are used to dc-bias the phase detector inputs to half the supply voltages. The capacitors C_2 and C_1 are used for capacitive coupling.

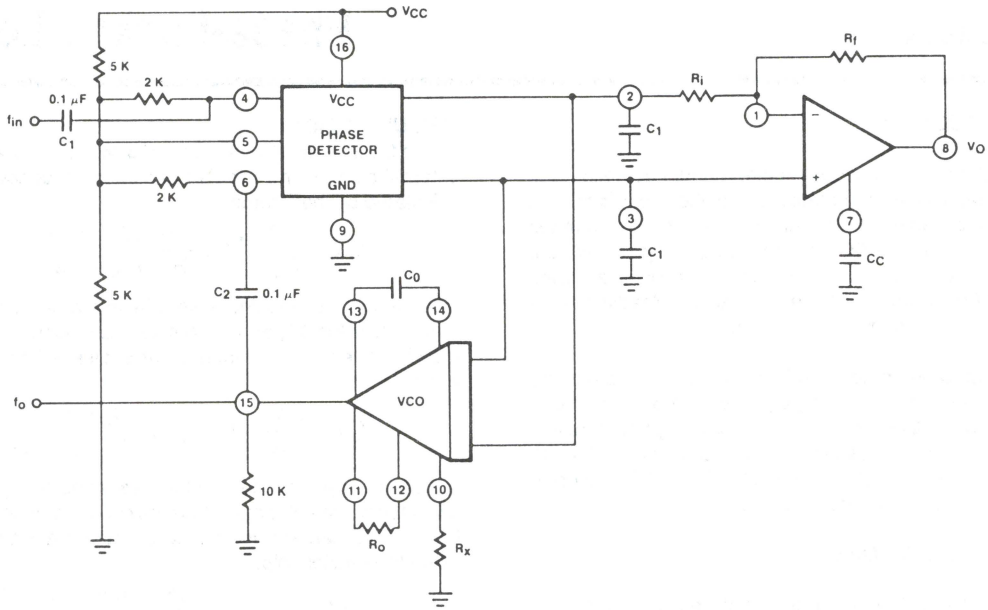


Figure 2. XR-215 with External Components

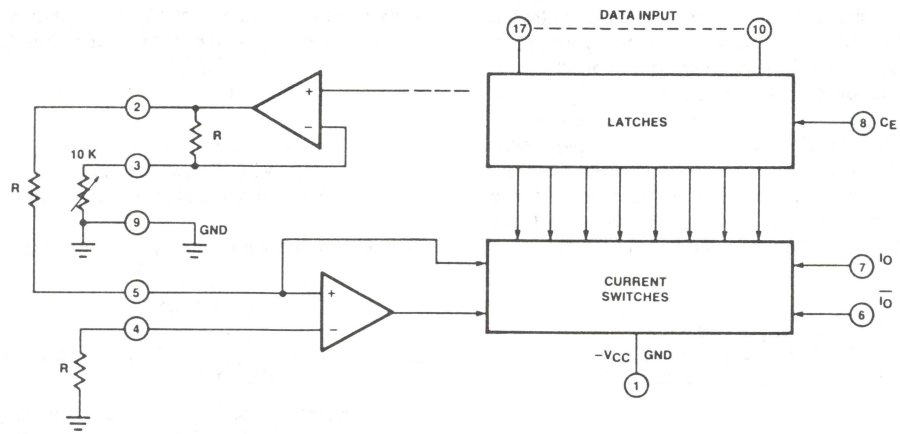


Figure 3. BA-9201 D/A with External Components (ROHM Corporation 714-855-2131)

related to the digital inputs by:

$$I_O = 2I_{REF}\left[\frac{B_7}{2}+\frac{B_6}{4}+\frac{B_5}{8}+\frac{B_4}{16}+\frac{B_3}{32}+\frac{B_2}{64}+\frac{B_1}{128}+\frac{B_0}{256}\right] \quad (8)$$

where $B_N = 1$ if bit N is high
$B_N = 0$ if bit N is low
B_7 = MSB
B_0 = LSB

Also: $I_O + \bar{I}_O = I_{FS}$ = Full-scale Current (9)

$$I_{FS} = 2\, I_{REF}\left(\frac{255}{256}\right) \quad (10)$$

The full-scale current is set using R by the relationship:

$$R = \frac{V_{REF}}{I_{REF}} \quad V_{REF} \simeq 2V \quad (11)$$

The 10KΩ potentiometer from Pin 3 to ground is used to fine-adjust the internal reference to exactly 2.00V.

DESIGN EXAMPLE

Design a digitally programmable PLL with a center frequency, f_o, equal to 20kHz. Provide for a 10% digital tuning range. The circuit shall also have the following lock and capture ranges:

$$\pm\Delta f_L = 5kHz, \pm\Delta f_C = 4kHz$$

1. Using equation 2, first with $I_{PIN\ 10} = 0$ (digital inputs all zeros) C_O can be determined.

$$f_o = \frac{200}{C_O} \qquad C_O = 0.01\mu F$$

2. This same equation is used to determine the maximum value of $I_{PIN\ 10}$ for a 10% change in f_o. Rearranging equation 2 yields:

$$I_{PIN\ 10}\ (max) = \frac{f_o C_O}{200} - 1 = \frac{22K\ (0.01)}{200} - 1 = 0.1mA$$

f_o = 20K + 2K Adjustment Range

3. R_O is now calculated from equation 4:

$$R_O = \frac{1565}{(2\pi)(5K)(0.01)} \simeq 5\ K\Omega$$

4. C_1 is determined by equation 7:

$$C_1 = \frac{0.017}{(4K)^2\ (5)\ (0.01)} \simeq 0.022\mu F$$

5. The D/A components can now by specified, first using equation 10 and the previously calculated $I_{PIN\ 10}$ maximum current:

$$I_{PIN\ 10}\ (max) = I_{FS}^2\, I_{REF}\left(\frac{255}{256}\right)$$

$I_{REF} \simeq 50\mu A$

6. The reference current setting resistor, R, is now determined using equation 11:

$$R = \frac{2.00}{50\mu A} = 40K\Omega$$

7. Calibration of the system is accomplished by adjusting potentiometer R_3 for V_{REF} on the BA-9201 to exactly 2.00V.

Figure 4 shows the completed design example.

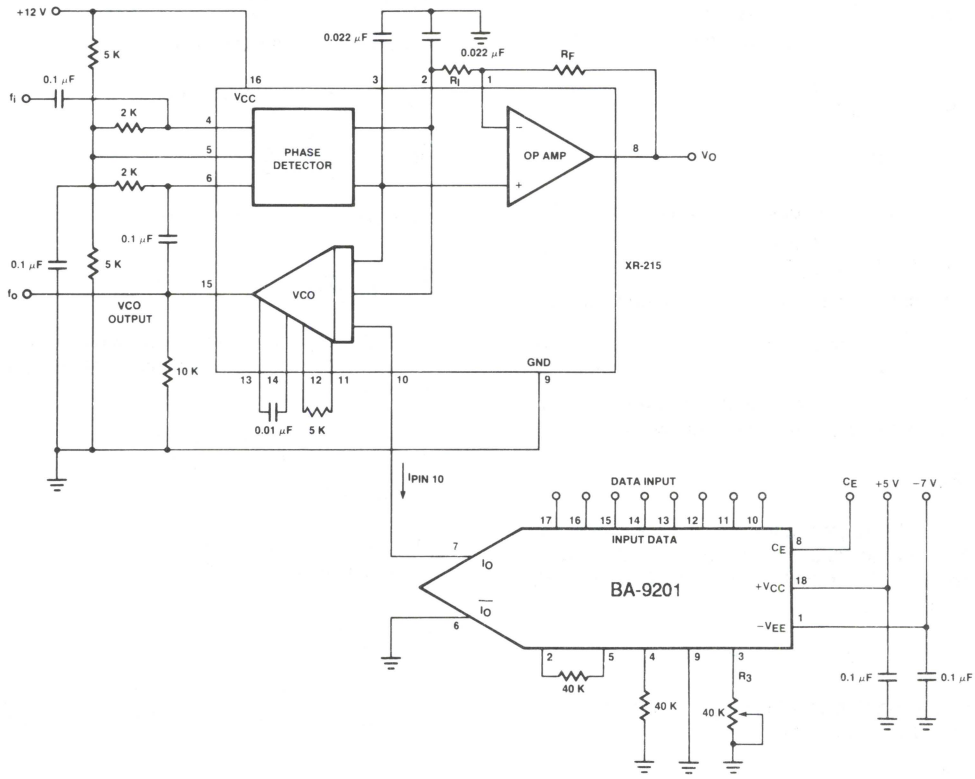


Figure 4. Digitally Programmable PLL

Application Note

High-Speed FSK Modem Design

INTRODUCTION

As the need for transmitting data increases, some applications require data to be sent faster than the conventional telephone line modems. This application note describes the design and construction of a high speed full-duplex, FSK modem using XR-2206 as a modulator and XR-210 as the demodulator transmitting data at the rate of 100 Kilobaud.

PRINCIPLES OF OPERATION

The block diagram in Figure 1 describes the basic building block in any FSK modem system. The major difference is that in high speed applications, data is transmitted over a twisted pair wire or coaxial cable instead of the telephone line with its limited bandwidth. The complete system is comprised of an answer and originate modem. Simply stated, the modulator converts the input data to two discrete frequencies corresponding to its 1's and 0's and is then sent over a line or cable. The line hybrid steers these frequencies to the bandpass filter, where it will remove any unwanted signals that might have gotten through due to the line or cable before reaching the demodulator, The demodulator, which is a phase locked loop, will lock onto the incoming frequencies and produce 1's and 0's on its output. A detailed description on FSK techniques is given in AN-28.

DESIGN EQUATIONS — Refer to Figure 6

1. The frequency of oscillation of the XR-2206 when used as a modulator, with the FSK input (Pin 9) is high is:

$$\frac{1}{R7A + R7B\ C_3}$$

When the FSK input (Pin 9) is low the frequency equals

$$\frac{1}{R8A + R8B + C_3}$$

2. The filter best suited for modem applications is the butterworth filter due to its linear phase response within the passband. Table 1 shows the normalized capacitor values for butterworth filters up to fifth order.

Table 1

ORDER NO	C1	C2	C3
2	1.414	.7071	
3	3.546	1.392	.2024
4	1.082	.9241	
	2.613	.3825	
5	1.753	1.354	.4214
	3.235	.3090	

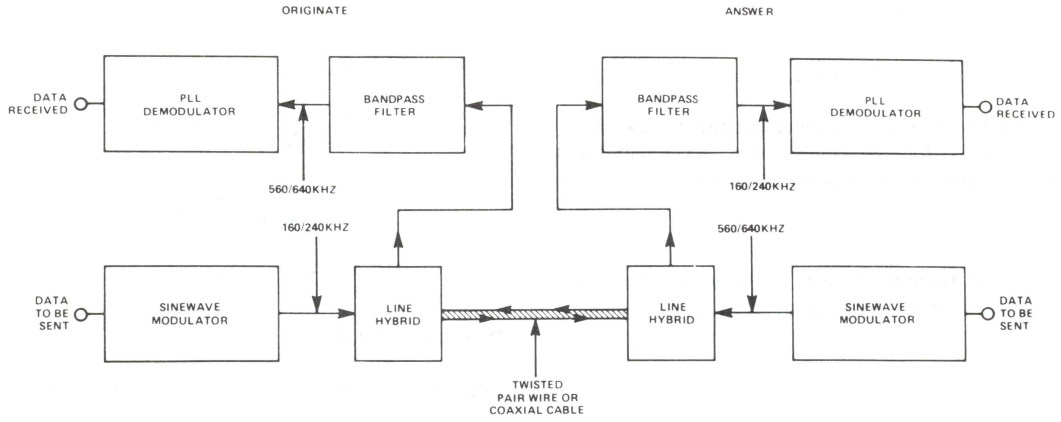


Figure 1. Block Diagram of High Speed FSK Modem System

Figure 3 shows a third order active high pass filter. To solve for the actual resistor values we use the formula:

$$R = \frac{1}{W_c\, CN\, C}$$

Where CN is the normalized capacitor and $W_c = 2\pi F_c$. In this equation, make all capacitors equal.

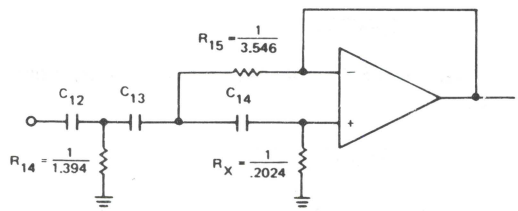


Figure 3.

After calculating R_x remember for single supply operation the op amp must be biased at 1/2 V_{CC}; therefore take twice the calculated value for R_x and configure as shown in Figure 4.

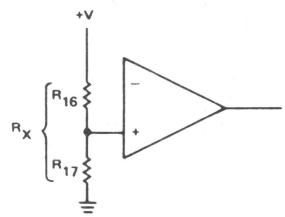


Figure 4.

Figure 5 shows a third order active butterworth low pass filter. To convert from the normalized capacitor values to the actual capacitor values, we use the formula.

$$C = \frac{CN}{W_c R}$$

Where CN is the normalized capacitor value and $W_c = 2\pi F_c$. In this equation, make all resistors equal.

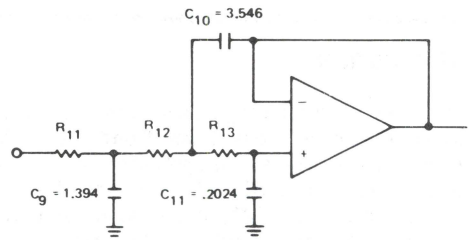


Figure 5.

The equations for using the XR-210 as an FSK demodulator are as follows:

$$\Delta F_L = (2)\Delta F$$

$$\Delta F = F_{mark} - F_{space}$$

$$\Delta F_L = 2(F_{mark} - F_{space})$$

$$F_0 = \frac{F_{mark} + F_{space}}{2}$$

$$F_0 = \frac{234}{C_0}\left(1 + \frac{.1}{R_T}\right) \quad \begin{array}{l} C_0 \text{ is in } \mu F \\ R_T \text{ is in } K\Omega \end{array}$$

$$C_0 = \frac{234}{F_0}$$

$$\Delta W_c = \sqrt{\frac{\Delta W_L}{6KC_1}}$$

$$\Delta W_L = 2\pi\, \Delta F_L$$

$$C_1 = \frac{\Delta W_L}{6K\Delta W_c 2}$$

$$R_0 = \frac{2(1565)}{\Delta W_L C_0} \qquad R_0 \text{ is in } K\Omega$$

$$C18 = \frac{10^{-4}}{2\pi\,(\text{Baud Rate})}$$

$$C19 = \frac{10^{-4}}{3\pi\,(\text{Baud Rate})}$$

DESIGN EXAMPLE

Design a FSK Demodulator with the following specification:

$F_0 = 200kHz$

$\Delta F_L = 160kHz$

Baud Rate = 100 Kilobaud

In this example, we must know the mark and space frequencies. If F_{mark} = 160kHz and F_{space} = 240kHz, the free running frequency is equal to

$$\frac{F_{mark} + F_{space}}{2} = 200kHz$$

In order to calculate the free running frequency, we use the formula:

$$F_0 = \frac{234}{C_0}$$

In this example we will use a variable resistor (R_T) in order to fine tune F_0 to exactly 200kHz, therefore:

$$F_0 = \frac{234}{C_0}\left(1 + \frac{.1}{R_T}\right)$$

The lock range (ΔF_L) is equal to twice the difference of the mark and space frequencies, so

$$\Delta F_L = 2(F_{space} - F_{mark})$$

R_0, which sets the lock range equals:

$$R_0 = \frac{2(1565)}{\Delta W_L C_0}$$

$$\Delta W_L = 2\pi F_L$$
$$6.28\ (160 \times 103) = 1004800$$

$$= \frac{2(1565)}{1004800.0015}$$

Where C_0 is in µF and R_0 is in KΩ

$$= 2.0K\Omega$$

The Capture Range (ΔF_c) is equal to:

$$\Delta W_c = \sqrt{\frac{\Delta W_L}{6K\ C17}} \qquad \Delta W_c = 2\pi\Delta F_c \qquad \Delta W_L = 2\pi\Delta F_L$$

In order to solve for C17 we rearrange the equation to read.

$$C17 = \frac{\Delta W_L}{(6K)\ W_C^2}$$

$$= \frac{1004800}{(6K)7536002} = 300 \times 10^{-12}$$

therefore:

$$\Delta W_c = \frac{1004800}{(6 \times 10^3)\ 300 \times 10^{-12}}$$
$$= 118.97kHz$$

It is important to note C17 and 6K set the loop time constant. When used as an FSK Demodulator, the XR-210 has post detection filtering on the output of the phase detector. In order to calculate the values for C18 and C19 we use the relationships:

$$C18 = \frac{10^{-4}}{2\pi\ (\text{Baud Rate})}$$

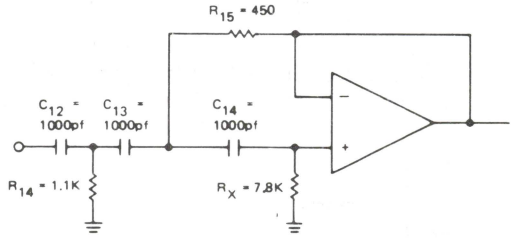
$$= \frac{10^{-4}}{6.28\ (100 \times 10^3)} = 160 \times 10^{-12} \text{ or } 160pF$$

$$C19 = \frac{10^{-4}}{9.42\ (100 \times 10^3)} = 106 \times 10^{-12} \text{ or } 106pF$$

For the filter, 18dB of attenuation should be sufficient; therefore:

Design a third order high pass butterworth filter with f_c = 100kHz.

1) In order to solve for actual resistor values use Table 1 and set all capacitors equal. The design example is shown below:



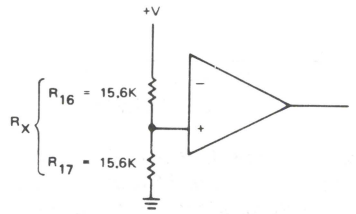
$$R = \frac{1}{W_C C N\ C}$$

$$R15 = \frac{1}{(6.28x100x10^3)3.546(1000x10^{-12})} = 450\Omega$$

$$R14 = \frac{1}{(6.28x100x10^3)1.392(1000x10^{-12})} = 1.1K\Omega$$

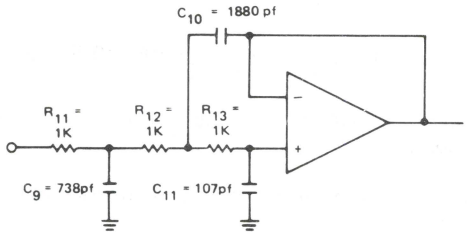
$$R_x = \frac{1}{(6.28x100x10^3).2024(1000x10^{-12})} = 7.8K\Omega$$

After calculating R_x take twice the value and configure as shown below:



Design a third order lowpass butterworth filter with F_c = 300kHz.

2) In order to solve the actual capacitances, use Table 1 and set all resistors equal. The design example is shown below:



$$C = \frac{CN}{W_cR} \qquad W_c = 2\pi F_c$$

$$C = \frac{3.546}{2\pi(300 \times 10^3)\ 1 \times 10^3} = 1880pF$$

$$C10 = \frac{3.546}{1884000000} = 1880pF$$

$$C9 = \frac{1.392}{1884000000} = 738pF$$

$$C11 = \frac{.2024}{1884000000} = 107pF$$

Design an FSK modulator with F_{mark} = 560kHz and F_{space} = 640kHz. The frequency of oscillation with the FSK input (Pin 9) is high is equal to:

$$F_{mark} = \frac{1}{R7A + R7B\ C3}$$

$$= \frac{1}{1K + 785\Omega.001\mu F} = 560 \times 10^3 \text{ or } 560kHz$$

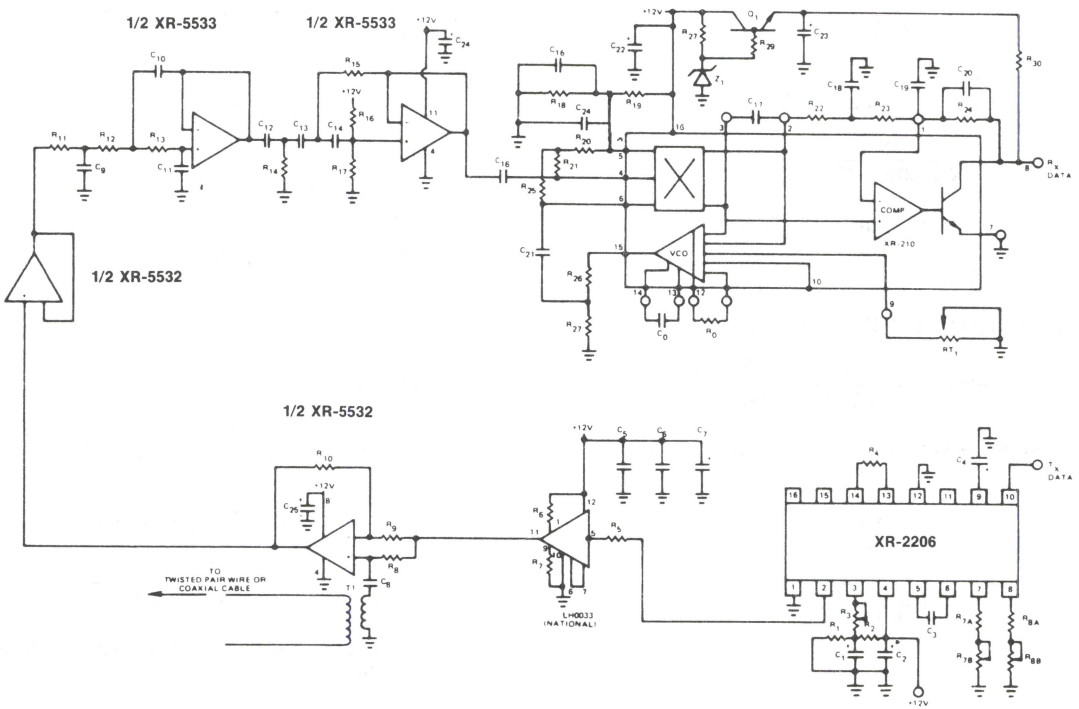


Figure 6. Complete Schematic for 100 Kilobaud FSK Modem

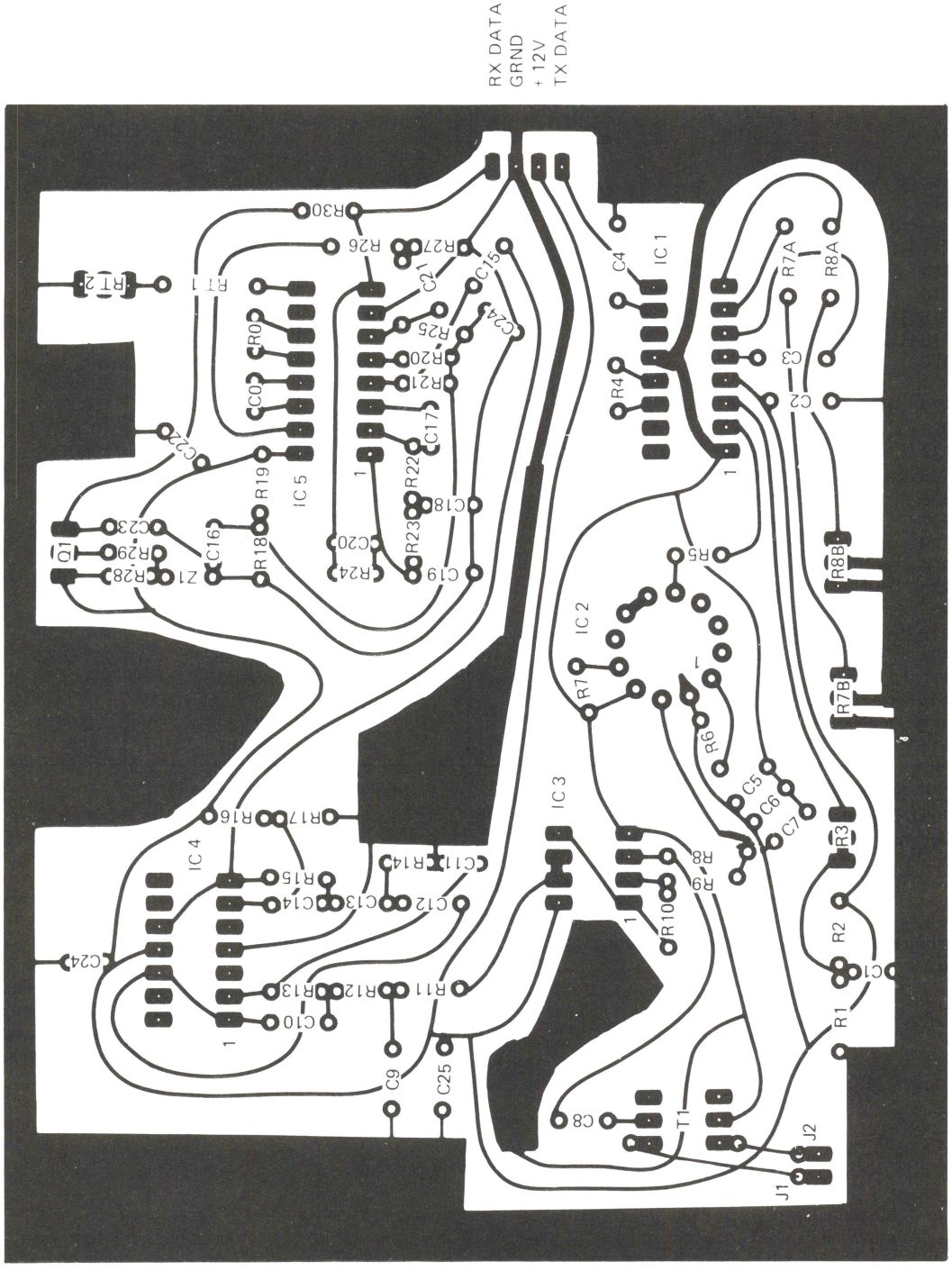


Figure 7. PC Board Layout for 100 Kilobaud FSK Modem-Component Side

PART NO.	ANSWER	ORIGINATE	PART NO.	ANSWER	ORIGINATE
R1-R2	5.1K	5.1K	C1	47µF	47µF
R3	50KΩ Pot	50KΩ Pot	C2	4.7µF	4.7µF
R4	200Ω	200Ω	C3	.001µF	.001µF
R5	51Ω	51Ω	C4	4.7µF	4.7µF
R6-R7	100Ω	100Ω	C5-C6	.1µF	.1µF
*R8	75Ω, 1W	75Ω, 1W	C7	4.7µF	4.7µF
R9-R10	10KΩ	10KΩ	C8	1µF	1µF
R11-R13	1KΩ	1KΩ	C9	738pF	317pF
R14	1.1KΩ	228Ω	C10	1800pF	807pF
R15	450Ω	90Ω	C11	107pF	46pF
R16-R17	16KΩ	3KΩ	C12-C14	1000pF	1000pF
R18-R19	5KΩ	5KΩ	C15	.22µF	.22µF
R20	2KΩ	2KΩ	C16	1µF	1µF
R21	4KΩ	4KΩ	C17	300pF	300pF
R22	10KΩ	10KΩ	C18	150pF	150pF
R23	5KΩ	5KΩ	C19	106pF	106pF
R24	249KΩ	249KΩ	C20	10pF	10pF
R25	4KΩ	4KΩ	C21	.1µF	.1µF
R26	3KΩ	3KΩ	C22-C25	4.7µF	4.7µF
R27	10KΩ	10KΩ	Q1	2N2222A	2N2222A
R28	5KΩ	5KΩ	T1	PE-576 **	PE-576 **
R29	562Ω	562Ω	Z1	1N5232	1N5232
R30	1.3KΩ	1.3KΩ	IC 1	XR-2206	XR-2206
R0	2.4KΩ	7.4KΩ	IC 2	LH0033†	LH0033†
RT2	1KΩ Pot	1KΩ Pot	IC 3	XR-5532	XR-5532
R7A	1.4KΩ	562Ω	IC 4	XR-5533	XR-5533
R7B	1KΩ Pot	1KΩ Pot	IC 5	XR-210	XR-210
R8A	750Ω	3.3KΩ			
R8B	1KΩ Pot	1KΩ Pot	J1-J2	JUMPER	JUMPER
RT1	50Ω	100Ω		WIRE	WIRE

* Coaxial Wire (75Ω)
** Pulse Engineering (619-268-2400)
† National

Figure 8. Component List for 100 Kilobaud FSK Modem

When FSK input (Pin 9) is low the frequency is equal to:

$$F_{space} = \frac{1}{R8A + R8B\ C3}$$

$$= \frac{1}{1K + 562\Omega.001\mu F} = 640 \times 103 \text{ or } 640kHz$$

Transformer Comments

The Pulse Engineering PE-5766 transformer provides a low inductance, for maximum power transfer and small physical size. Resistor R8, for 75Ω impedance coaxial cable should be 75Ω, 1W. For twisted pair, the resistor should be 150Ω, 1W.

High-Frequency TTL Compatible Output from the XR-210 and XR-215 Monolithic PLL Circuits

Application Note

INTRODUCTION

With digital circuitry as common as it is, it is necessary to be able to interface analog signals to digital systems. This can be done by using the XR-215, a monolithic PLL circuit, and an additional buffer circuit.

When an input signal is present within the capture range of the PLL system, the XR-215 will lock on the input signal and the VCO section of the PLL will synchronize with the input frequency, The VCO output can then be buffered in order to produce a TTL compatible output.

PRINCIPLES OF OPERATION

Figure 1 shows a functional block diagram of the XR-215 monolithic PLL system. The circuit contains a phase comparator, a voltage controlled oscillator (VCO), and an operational amplifier. A complete phase locked loop system can be made by simple ac coupling the VCO output to either of the phase comparator inputs, and by adding a low pass filter to the phase comparator outputs.

The VCO output can be buffered in order to produce a TTL compatible output at high frequencies by the simple common emitter circuit shown in figure 2. The amplitude of VCO degrades as frequency increases and at 21MHz, the amplitude is reduced from approximately 2.5 Vpp to 50mVpp. The dc outputlevel is 2 volts below V_{CC} so with V_{CC} equal to 15 volts, the dc level is approximately 3 volts. The VCO output is ac coupled in order to block this dc level. The input signal causes Q_1 to be overdriven, where the amplitude is 400 mVpp offsetted at approximately 0.769 Vdc. When Q_1 is in the offstate, the collector voltage will be forced high and when this voltage exceeds 0.7 Vdc, Q_2 will turn on and the collector of Q_1 will be clamped at 0.7 Vdc. The output of the VCO at the TTL buffered output will be in phase.

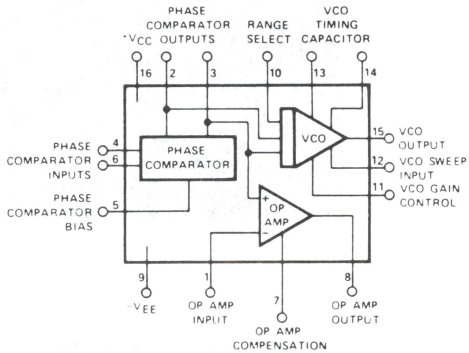


Figure 1. Functional Block Diagram of XR-215 Monolithic PLL Circuit

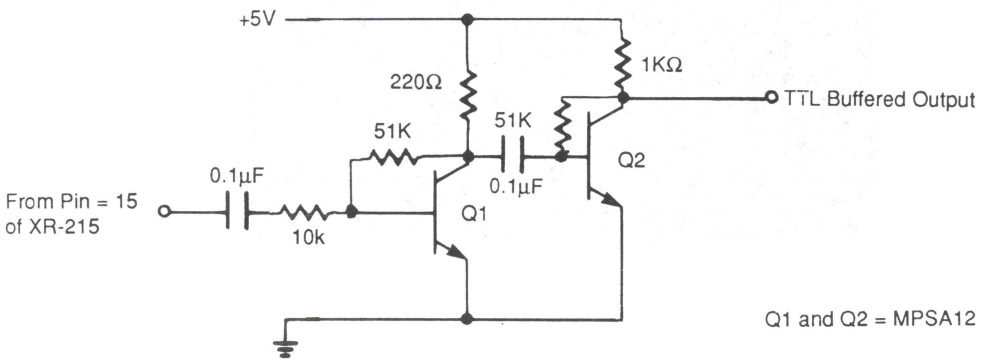
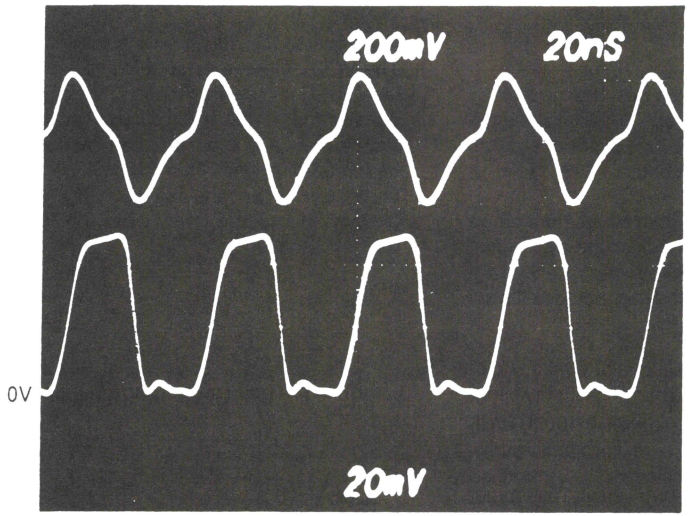
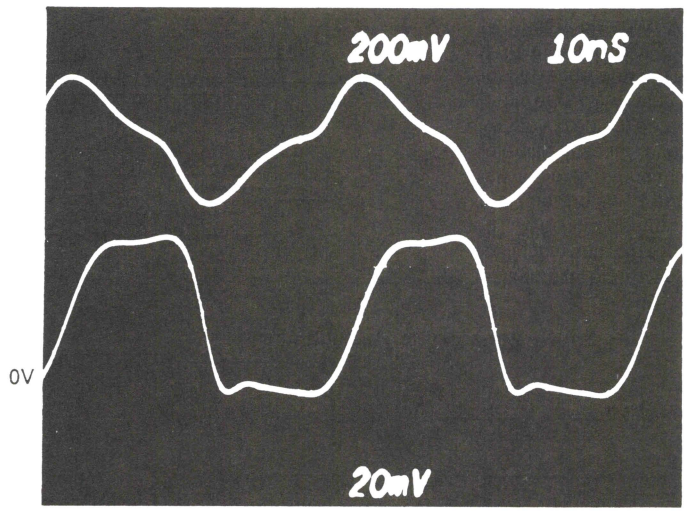


Figure 2. Common Emitter Buffer Circuit



VCO Output (Pin 15) of XR-215 (non-typical)

TTL Buffered Output at 21 MHz measured with X100 probe



Propagation Delay is approximately 5nS.



NOTES



PCM Short Haul Line Interface

Application Note

INTRODUCTION

XR-T5681 is a PCM Transceiver chip consisting of both transmit and receive circuit in a CERDIP 18 pin package. The transceiver is designed primarily for short line (<10dB) PCM transmission applications such as in Digital Private Branch Exchange (PBX) environment, Digital Multiplexed Interface (DMI), and Standard PCM data interface circuit. The maximum frequency of operation is 3Mb/s, so it cover T1, T148, T1C and Europe's CEPT 2.048MBPS data rates. The device is designed to operate over the temperature range of 0°C to +70°C.

PRINCIPLES OF OPERATION

Figure 1 contains a functional block diagram of the XR-T5681. The circuit consists of two separate sections: one is the line receiver and the other is the line transmitter. The receiver accepts incoming bipolar signal and converts it intc TTL D+ and D– data streams. It also produces a clock output from the input data. In the transmit direction, full width, TTL compatible D+ and D– signals at the input, and a 50% duty cycle clock are combined to form the bipolar line signal at the output of a transformer for transmission.

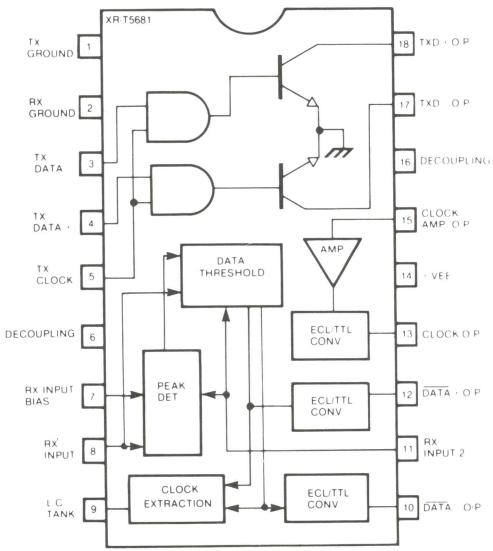


Figure 1. Block Diagram

RECEIVER CIRCUIT DESCRIPTION

The receiver is designed to handle a maximum of 10dB line loss. This means the incoming signal will not suffer from severe attenuation and distortion caused by the cable, and, therefore, it can be reliably retrieved without preamplification circuit and equalizing network placed at the input of the receiver.

The receiver in this design consists of a peak detector which converts the incoming signal amplitude into a variable threshold. The variable threshold is arranged to slice the input signal at 50% level in the data comparator (See Figure 2) for D+ and D– data extraction. This scheme guarantees a maximum tolerance in immunity and ensures a nominal output pulse width change at different input signal level. However, as the data outputs are not regenerated pulses, their width will somewhat depend on the input pattern and cable loss. D+ and D– are active low data and they both go through similar level shifting circuit to be converted into TTL compatible signals.

CLOCK EXTRACTION

Since timing information is extracted from the data and the input spectrum does not carry any frequency component around the transmission rate, input waveform is full wave rectified to obtain all the transition pulses before applied to an external LC resonant circuit. If the input signal is a random data, the tank output looks like a amplitude modulated sine wave. Figure 2 depicts the clock extraction process with a known input pattern. The clock output shown in Figure 2 has the rising edge coincided with the center of the D+ and D– data. This timing relation is essential for the external digital circuit to convert the half-width data into a full width signal when using a positive edge triggered D/FF as that shown in Figure 3. To achieve the 90° phase difference between the data and the clock, the tank output is coupled through a small value capacitor to the input of a common base amplifier (see Figure 4), followed by a zero crossing detector to obtain a square wave with sharp transitions. The emitter of Q10 is a low impedance point, hence, the coupling capacitor C_c forms part of the tank circuit.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0V, operating temperature 0°C to +70°C.

PARAMETERS	PIN NO.	MIN	TYP	MAX	UNITS	CONDITIONS
DC Supply	14	4.75	5.0	5.25	V	
Supply Current	9, 14		35.0	45.0	mA	Transmitter Drivers Open
Tank Drive Current	9	1.7	2.0	2.3	mA	Pin 8 & 11 = 0V, Supply 3.0 V to Pin 6
Clock Output Low	13		0.3	0.8	V	I_{OL} =1.0mA
Clock Output High	13	3.0	4.3		V	I_{OH} = −400µA
D+, D– Output Low	12, 10		0.4	0.8	V	I_{OL} = 1.0mA
D+, D– Output High	12, 10	3.0	4.5		V	I_{OH} = 400µA
Driver Low Voltage	17, 18	0.6		0.05	V	I_{OL} = 40mA
Driver Sinking Current	17, 18			40	mA	V_{OL} = 0.95V
Driver Output Rise Time	17, 18		20	30	nS	With 150Ω Pull-Up to +5.0V, C_L = 15pF
Driver Output Fall Time	17, 18		20		nS	With 150Ω Pull-up to +5.0V, C_L = 15pF
Pulse Width a 2 048MHz	17, 18	219	244	269	nS	With 150Ω Pull-Up to +5.0V
Pulse Width Imbalance at 2.048MHz	17, 18		5	10	nS	At 50%
Clock Duty Cycle at 2.048MHz	13	40	50	60	nS	%
Clock Rise Time	13		25		nS	10-90%

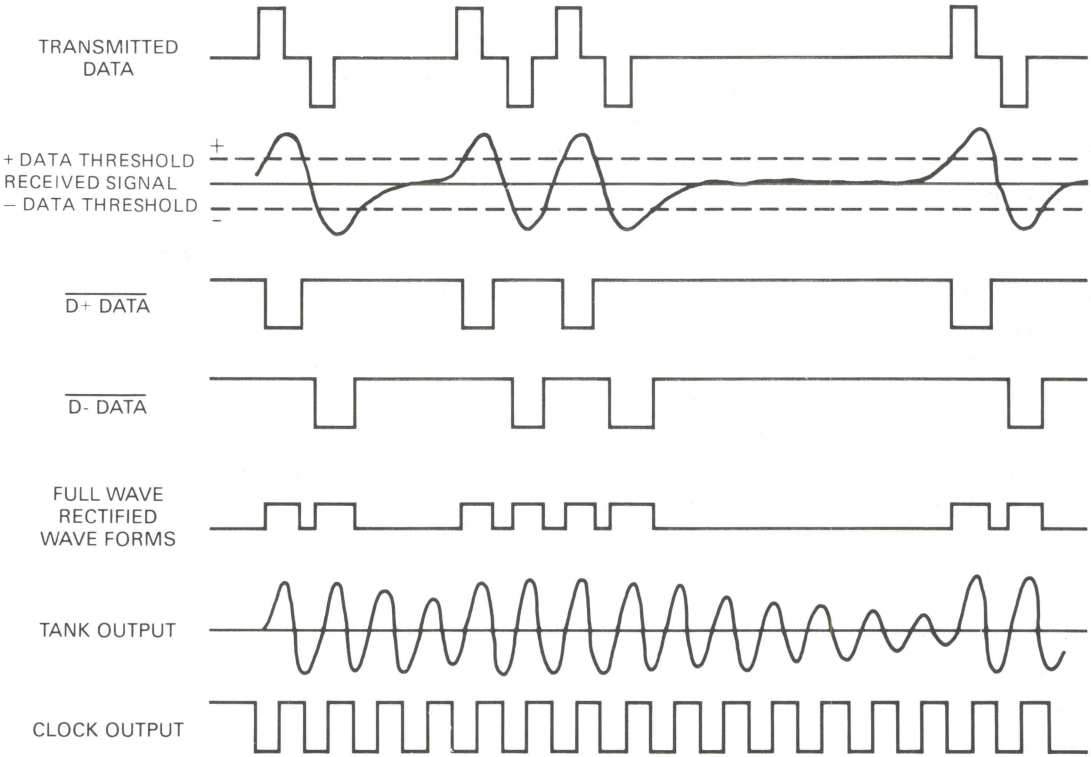


Figure 2. XR-T5681 Clock Extraction Timing Waveforms

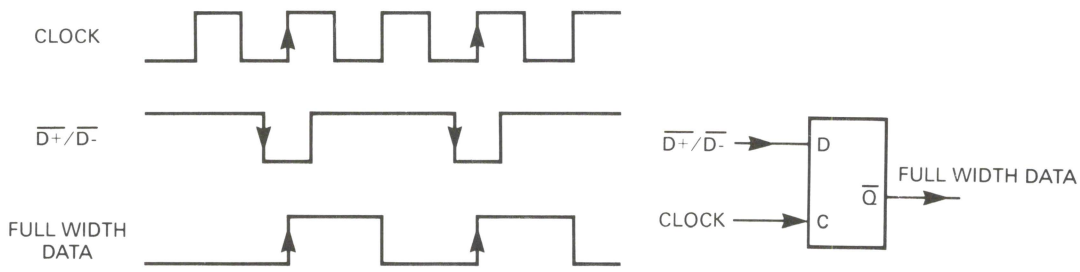


Figure 3. To Convert Half-Width Data into a Full-Width Data, a Positive Edge Triggered D/FF is Commonly Used

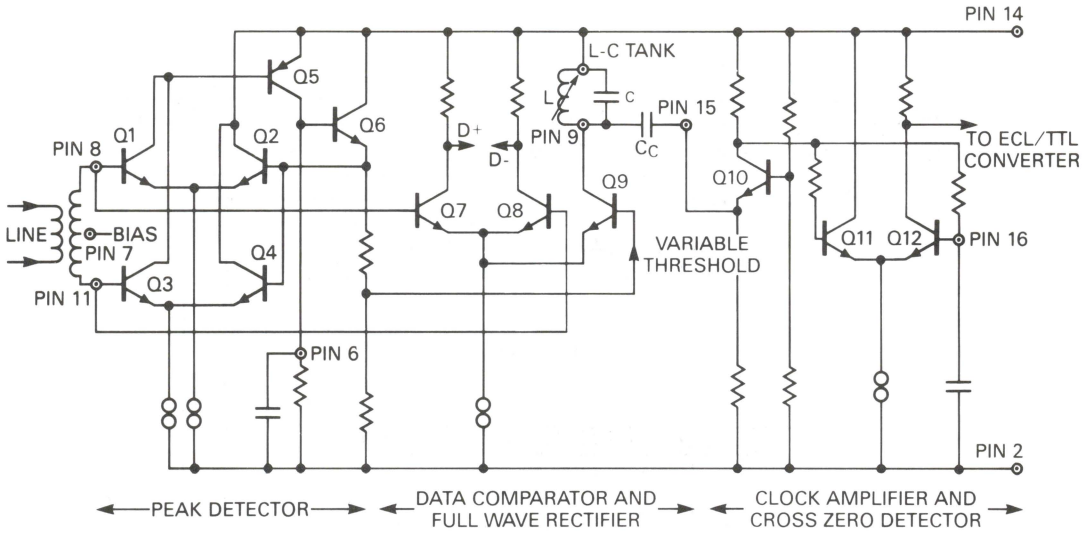


Figure 4. Simplified Schematic of XR-T5681 Receiver

TRANSMITTER

The transmitter consists of two identical TTL input open collector NAND gates. The output driver has a non-saturating stage and can handle a maximum current of 40mA. If the inputs are half width signals, Pin 5 should be returned to $+V_{CC}$ via a 1KΩ resistor. If the input data are full width signals, a synchronized 50% duty cycle TTL clock is needed at Pin 5 to obtain a bipolar signal at the output of a center tapped transformer (See Figure 5). The output pulse conforms to CCITT G.703 recommendation. A circuit connection diagram for 1.5Mb/s line interface is shown in Figure 6.

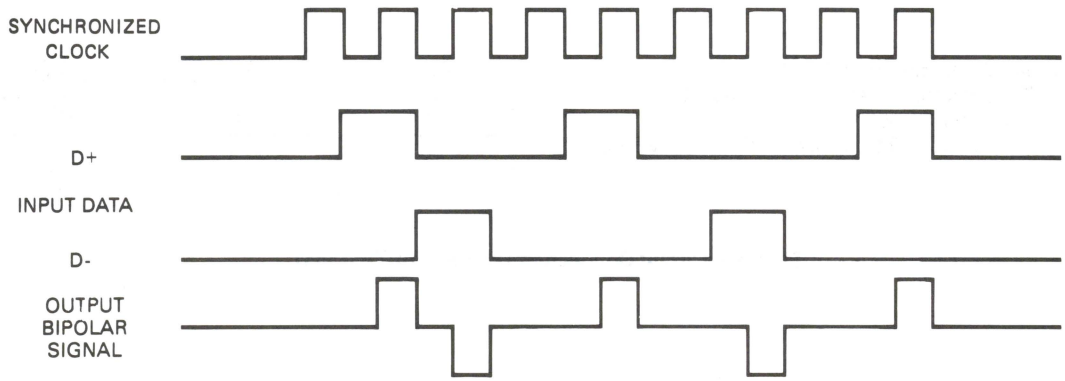
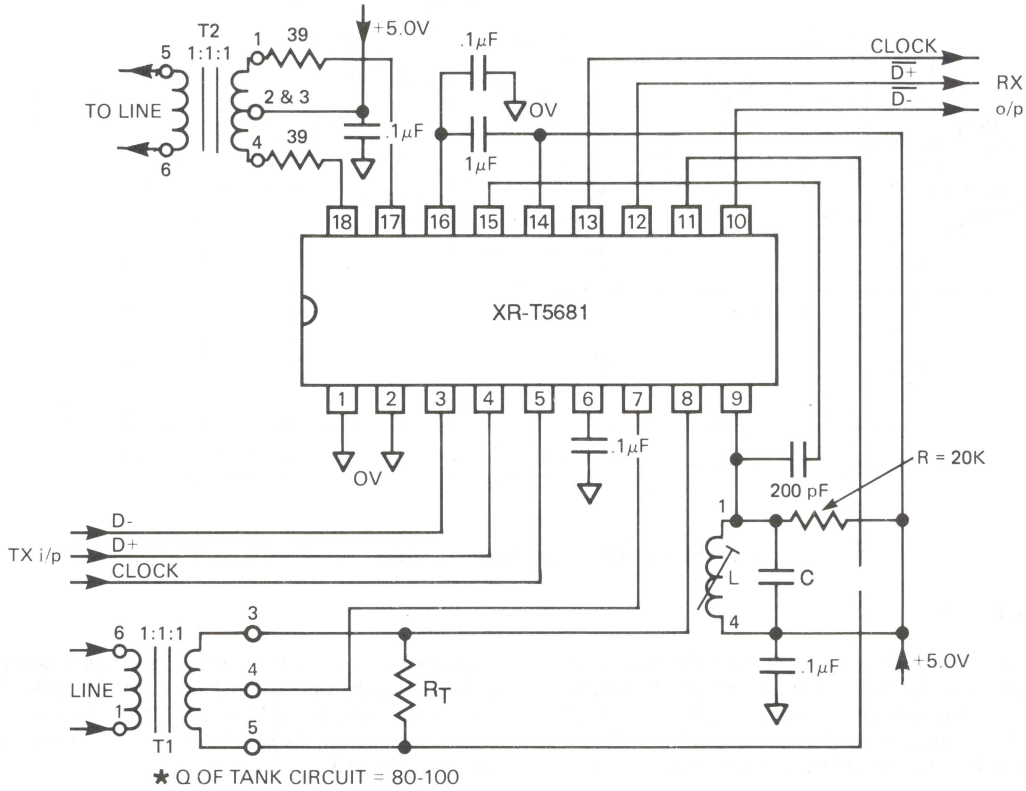


Figure 5. XR-T5681 Transmitter Section Timing Diagram



L = Tank coil AIE part no. 415-0804
T1 = AIE input transformer part no. 315-0765
T2 = AIE part no. 318-0696
Max. input voltage to T1 primary = 6 V_{p-p} at 5.0V supply

Device	1.544 MBPS	2.048 MBPS
L	~60μH	60μH
C	600pF	200pF
R_T	470	390

Figure 6. Circuit Connection Diagram for XR-T5681

Long Haul PCM Line Receiver & Clock Recovery Circuit Using the XR-T5650

Application Note

INTRODUCTION

The XR-T5650 is a monolithic bipolar IC designed for PCM line receiver applications operating at T1, T148, T1C, and 2 Mbits/s data rates It provides all the active circuitry to perform Automatic Line Build Out (ALBO), positive and negative data extract on, and clock recovery. For applications requiring crystal clock extraction, the XR-T5750 is recommended. Some of the features included in this IC are a double matched ALBO, a less than 10ns sampling pulse over the operating range, a 5.1V power supply for easy interfacing with CMOS and TTL circuitry. This device is designed as a general purpose line receiver for bipolar line codes such as HDB3, B8ZS, or AMI formats, and is packaged in a hermetic 18 pin CERDIP.

PRINCIPLES OF OPERATION

Figure 1 illustrates the functional block diagram for the XR- T5650. For ease of analysis, the internal structure of the receiver is divided into the following circuit blocks:

a. Preamplifier
b. Data threshold detector
c. Clock threshold detector
d. ALBO threshold detector
e. Clock amplifier and bias network
f. Limiter and sampling pulse generator
g. Retiming logic and drivers for clock and data outputs

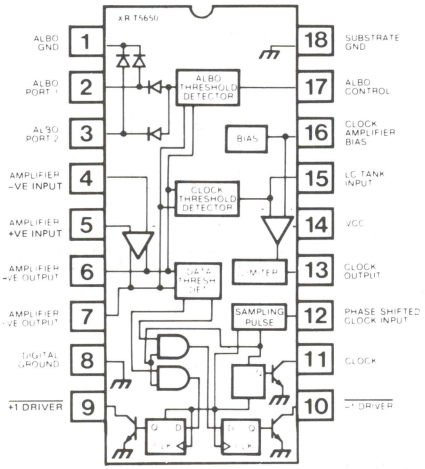


Figure 1. Functional Block Diagram

The basic function of the receiver is to reshape, regenerate, and retime the incoming pulse code modulated signal. The system operates on either pulp or polyethylene insulated paired cable that is either pole mounted or buried. Operation is compatible with a variety of wire gauges, provided that the cable loss at 772KHz is less than 36dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency circuits. It is the function of the amplifier to provide the necessary gain and phase on a pre-equalized signal in order to insure proper recovery of clock and data. The circuit diagram of the preamplifier, as shown in Figure 2, is designed as a two stage differential broadband amplifier with a differential voltage gain of 50dB. The differential outputs of the preamplifier, pin 6 and 7, are internally connected to the peak detector for the ALBO loop and also to the data and clock threshold detectors.

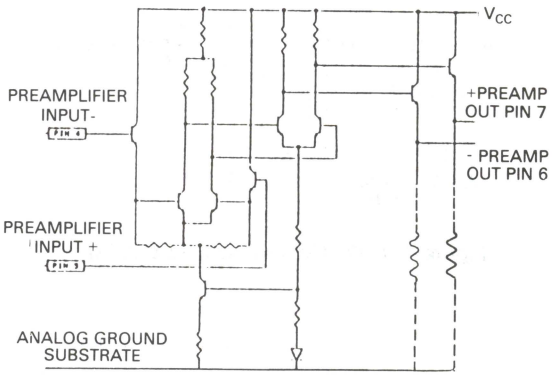


Figure 2. Preamplifier

The data, clock and ALBO threshold detector circuits as shown in Figure 3 are made up of two sets of gain stages which are driven differentially by the preamplifier outputs.

The outputs of the data comparators, D+ and D–, are gated with the sampling pulse to set the data latches. The peak detector output is internally connected to the Automatic Line Build Out section (see Figure 4) of the circuit, whose voltage controls the current through the ALBO diodes. This, in turn, varies the small signal resistance, r (I), which is used to control the attenuation characteristics of the ALBO network to provide shaped loss dependent on the line loss as well as automatic gain control function.

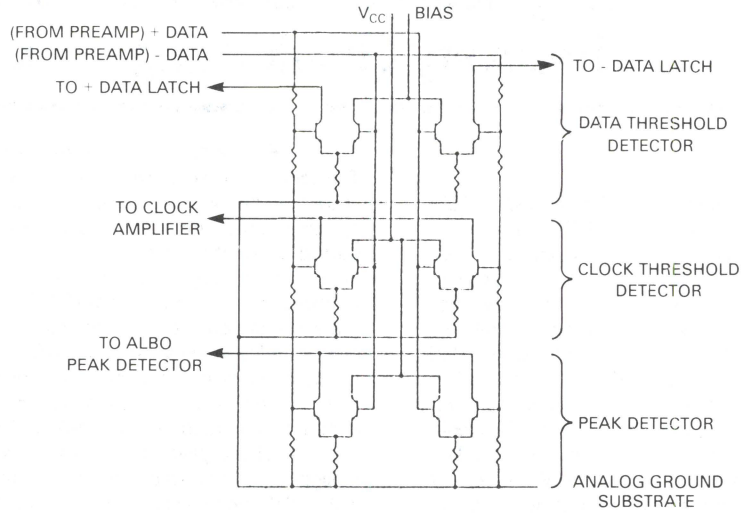


Figure 3. Data, CLock and Peak Threshold Detectors

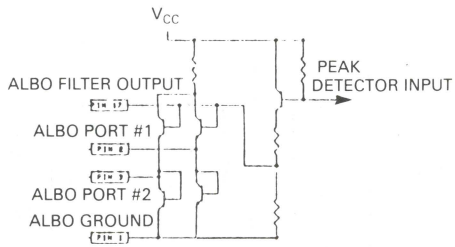


Figure 4. ALBO (Automatic Line Build Out)

The clock recovery section, as shown in Figure 5, consists of an amplifier and an LC tank circuit whose resonant frequency is equal to the incoming data rate. The excitation that comes from the clock threshold detector is applied internally to the input of the clock amplifier and the tank circuit at Pin 15. Pin 16 is used to bias the tank circuit which has a Quality factor (Q) from 60 to 120 to track incoming jitter and to sustain oscillations the zeros are transmitted. The spectrum of bipolar signal does not contain any components at the incoming data rate, therefore,the clock threshold detector full wave rectifies the preamplifier output signal to double the equalized spectrum.

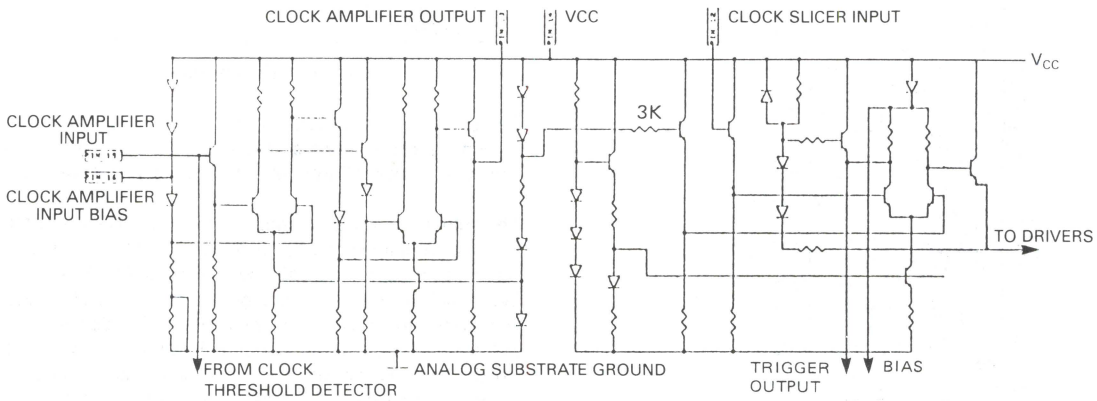


Figure 5. Clock Amplifier and Slicer Circuit

This signal, when applied to the LC resonant circuit generates click at 1.544MHz. The oscillations are applied to the input of the amplifier and sustained for a maximum number of 15 zeroes. It is therefore essential to maintain a sufficient one's density to keep the clock running (Bell Pub 62411 requires a minimum of 12.5% one's density). The clock amplifier (32dB open loop gain and 3dB roll off at 10MHz) regenerates the clock signal and feeds this squarewave through a phase shift network, This network consists of an RLC combination which is located externally and integrates this square waveform into a triangle waveform. The objective in creating this triangle waveform is to generate a 90° phase shift so that the eye can be sampled in the middle. To do so, a sampling pulse is generated on the positive edge of the clock and gated with the data threshold detector outputs to drive the data latches.

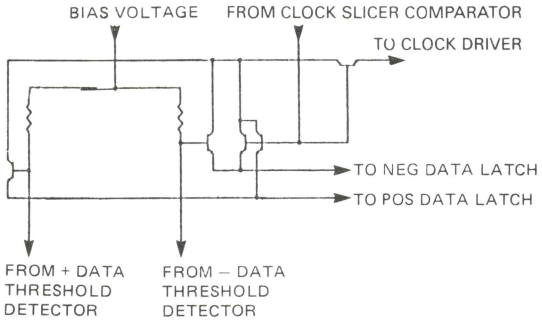


Figure 6. Gates

When D+ is low, the samplinq pulse sets flip-flop 1 on the leading edge of this pulse. Similarly when D– is low, the sampling pulse sets flip-flop 2. The flip-flop outputs are then used to drive the output drivers as shown in Figure 7. The output stage is designed to drive a nominal load of 100Ω, and can handle a peak current of 50mA.

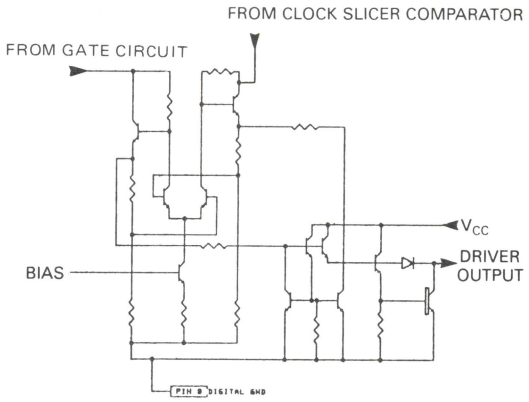


Figure 7. Output Driver & Data Latch Section

WAVEFORM AND TIMING DIAGRAM

A) Input Signal (Pin 4)
B) Oscillator Waveform (Pin 15)
C) Oscillator Output Waveform (Pin 13)
D) Integrated Waveform from Pin 13 (Pin 12)
E) Strobe Pulse
F) Regenerated Clock Output (Pin 11)
G) Data+ (Pin 9)
H) Data– (Pin 10)

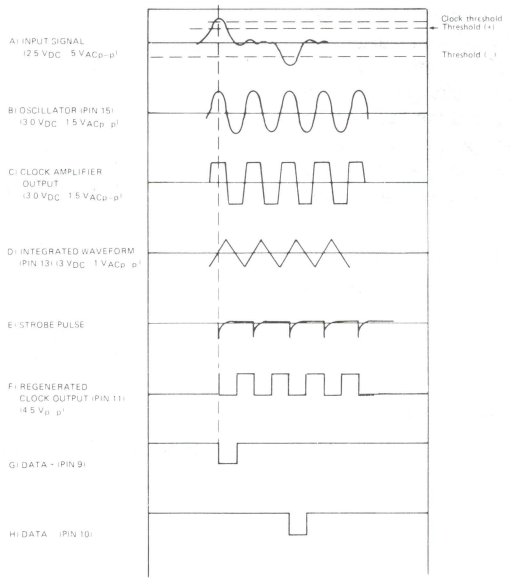
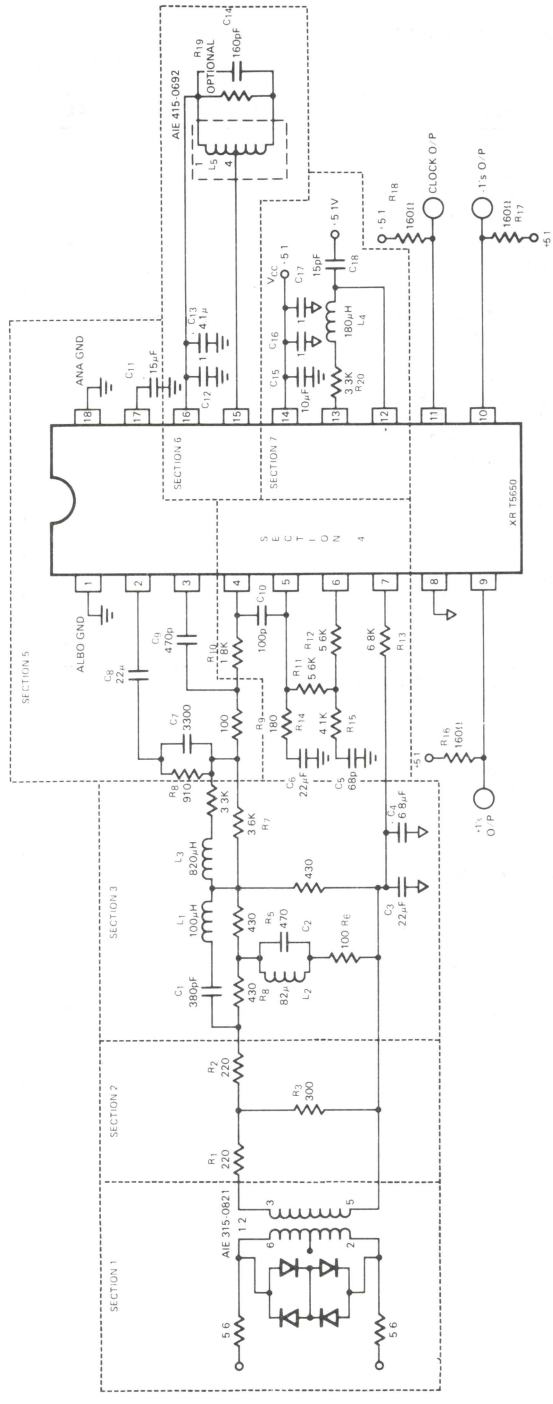


Figure 8. Waveform and Timing Diagram

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1V ± 5%, T_A = 25°C, unless specified otherwise.

	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Supply Current		26	34	mA	ALBO Off
	Clock & Data Output					
	Output Leakeage Current		0	100	µA	$V_{pull\text{-}up}$ = 15V
	Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
	Amplifier Output Offset Voltage	–50	0	50	mV	R_S = 8.2kΩ
	Voltage Swing	2.2			V	Measured Differentially from Pin 7 to Pin 6
	Amplifier Input Bias Current			5	µA	
	ALBO on Current	3			mA	
	Drive Current		1		mA	
	AC CHARACTERISTICS					
	Pre Amplifier AC Gain @ 1MHz		50		dB	
	Input Impedance	20			kΩ	
	Output Impedance			200	Ω	
	Clock Amplifier AC Gain		32		dB	
	–3dB Bandwidth	10			MHz	
	Delay		10		ns	
	Output impedance			200	Ω	
	ALBO					
	Off Impedance	20			kΩ	
	On Impedance			25	Ω	
	CLOCK DATA OUTPUT BUFFERS					
	Rise Time		30		ns	R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1V ± 5%
	Fall Time		30		ns	
	Output Pulse Width		244		ns	
	Sampling Pulse Width		10		ns	
	V_{OL}		0.7		V	
	I_L sink		35		mA	
	THRESHOLDS					
	ALBO	1.4	1.5	1.6	V	
	Clock Drive Current Peak		1.0		mA	At $V_O = V_{ALBO}$ Threshold
	CLOCK THRESHOLD					
	% of ALBO	63	69	75	%	
	DATA THRESHOLD					
	% of ALBO	40	46	52	%	



APPLICATION CIRCUIT PRINCIPLES

For ease for analysis, the application circuit shown in Figure 9 will be broken down into the following sections:

1. Pulse isolation transformer section
2. Impedance matching pad
3. Equalizer
4. Preamplifier
5. ALBO network
6. LC tank
7. Phase shift network

Figure 9. Application Circuit — Data Rate of 1.544 Mbits/s Sec

APPLICATION CIRCUIT PRINCIPLES

The receiver configuration as shown in Figure 9 will accept signals encoded in AMI, B8ZS, HDB3 and other bipolar line codes. Note that T1 transmission is done over balanced twisted pair for each direction of transmission and terminated by characteristic load impedance of 100Ω ± 5%.

1. Given the above constraints, the pulse isolation transformer shown in Figure 10 uses a set of 5.6Ω resistors to limit the current, and a diode clamping configuration to protect the receiver from electrical differential disturbances that could be present on the line. Note that these diodes will clamp the voltage if the line loss is less than 6dB at the primary side of the transformer.

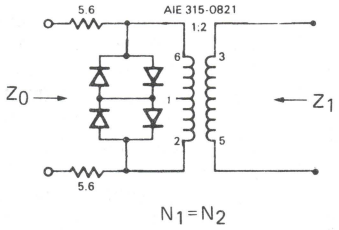


Figure 10. Isolation Transformer

***Note:** The transformer used in this application is an AIE 3150821 which has a 1:2 turns ratio.*

2. Given the characteristic impedance of 100Ω ± 5%, it is first necessary to scale the impedance of the secondary of the transformer

$$\frac{Z0}{Z1} = \left(\frac{N0}{N1}\right)^2$$

Knowing the impedance on the secondary of the transformer, we can use the pad shown in Figure 11 to first match the impedance and also attenuate the incoming signal to an acceptable level.

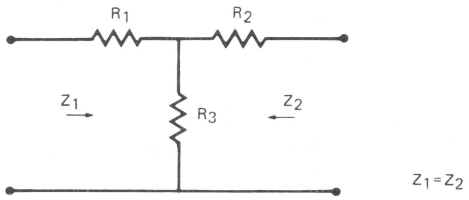


Figure 11. Attenuator Pad

Given a condition where the pad loss needs to be increased or decreased, the following set of formulas can be used:

$$R1 = R2 = \frac{(k-1)Z}{(k+1)}$$

$$R3 = \frac{k2Z}{k^2-1}$$

The "k" factor in this case is the ratio of current, voltage, or power corresponding to a given value of attenuation expressed in decibels. To simplify the calculation of attenuator networks, the following table is helpful in finding the desired resistor values.

n(dB)	$\frac{k-1}{k+1}$	$\frac{k}{k^2-1}$	n(dB)	$\frac{k-1}{k+1}$	$\frac{k}{k^2-1}$	n(dB)	$\frac{k-1}{k+1}$	$\frac{k}{k^2-1}$
0.05	0.0028783	86.8618	8.0	0.43051	0.47309	28.5	0.92755	0.037636
0.1	0.0057562	43.4303	8.5	0.45366	0.43765	29.0	0.93147	0.035526
0.2	0.011512	21.713	9.0	0.47622	0.40592	29.5	0.43518	0.033534
0.3	0.017268	14.473	9.5	0.49817	0.37730	30.0	0.93869	0.031655
0.4	0.023022	10.854	10.0	0.51950	0.35137	31.0	0.94518	0.028207
0.5	0.028774	8.6810	10.5	0.54020	0.32775	31.5	0.94817	0.026627
0.6	0.34525	7.2327	11.0	0.56026	0.30616	32.0	0.95099	0.025135
0 7	0.040274	6.1974	11.5	0.57969	0.28635	33.0	0.95621	0.022398
0.8	0.046019	5.4209	12.0	0.59848	0.26811	34.0	0.96088	0.019961
0.9	0.051763	4.8268	12.5	0.61664	0.25127	34.5	0.96302	0.018843
1.0	0.057502	4.3335	13.0	0.63416	0.23568	35.0	0.96506	0.017788
1.1	0.063237	3.9376	13.5	0.65105	0.22123	36.0	0.96880	0.015853
1.2	0.068968	3.6076	14.0	0.66733	0.20780	37.0	0.97214	0.014128
1.3	0.074695	3.3283	14.5	0.68298	0.19529	37.5	0.97368	0.013338
1.4	0.080418	3.0888	15.0	0.69804	0.18363	38.0	0.97513	0.012591
1.5	0.086132	2.8809	15.5	0.72250	0.17275	39.0	0.97781	0.0112216
1.6	0.091846	2.6991	16.0	0.72639	0 16257	40.0	0.98020	0.0100010
1.7	0.097551	2.5384	16.5	0.73970	0.15305	40.5	0.98130	0.0094414
1.8	0.103249	2.3956	17.0	0.75246	0.14413	41.0	0.98233	0.0089134
1.9	0.108939	2.2676	17.5	0.76468	0.13577	42.0	0.98424	0.0079436
2.0	0.11463	2.1523	18 0	0.77637	0.12792	43.0	0.98594	0.0070795
2.2	0.12597	1.9531	18.5	0.78755	0.12055	43.5	0.98672	0.0066834
2.4	0.13728	1.7867	19.0	0.79823	0.11363	44.0	0.98746	0.0063096
2.5	0.14293	1.7133	19.5	0.80844	0 10713	45.0	0.98887	0.0056234
2.6	0.14856	1,6457	20.0	0.81818	0.10101	46.0	0.99003	0.0050119
2.8	0.15980	1.5245	20.5	0.82747	0.095255	46.5	0.99058	0.0047315
3.0	0.17100	1.4192	21.0	0.83634	0.089841	47.0	0.99111	0.0044668
3.2	0.18215	1.3269	21.5	0.84478	0.084739	48.0	0.99207	0.0039811
3.4	0.19326	1.2453	22.0	0.85282	0.079935	49.0	0.99293	0.0035481
3.5	0.19879	1.2079	22.5	0.86048	0.075411	50.0	0.99370	0.0031623
3.6	0.20432	1.1725	23.0	0.86777	0.071148	51.0	0.99438	0.0028184
3.8	0.21532	1.1072	23.5	0.87470	0.067133	52.0	0.99499	0.0025119
4.0	0.22627	1.0483	24.0	0.88130	0 063348	54.0	0.99602	0.0019953
4.5	0.25340	0.92323	24.5	0.88756	0.059778	55.0	0.99645	0.0017783
5.0	0.28013	0.82241	25.0	0.89352	0.056413	56.0	0.99684	0.0015849
5.5	0.30643	0.73922	25.5	0.89917	0.053238	57.0	0.99718	0.0014125
6.0	0.33228	0.66932	26.0	0.90455	0.050246	58 0	0.99749	0.0012589
6.5	0.35764	0.60964	26.5	0.90965	0.047422	60.0	0.99800	0.0010000
7.0	0.38246	0.55801	27.0	0.91448	0.044757	65.0	0.99888	0.00056234
7.5	0.40677	0.51291	27.5	0.91907	0.042245	70.0	0.99937	0.00031623
			28.0	0.92343	0.039874			

3. The equalizer exhibits shaped attentuation characteristics to compensate for the line loss which varies with, cable size, cable length and applied frequencies. Spectrum components attenuated by the line cannot be recovered. However, a flat (or equialized) response can be obtained by attenuating predominant spectrum components with an equalizer having inverse line loss characteristics. For the equalizer shown below in Figure 12, the two resistors, R4 and R5, are equal to the circuit impedance (400Ω). Resistor R6 is varied in order to obtain different values of loss. As the frequency is increased, the reactance of C1 and C2 decreases and the reactance of L1 and L2 increases. At resonance given by the formula:

$fr = 1/2\pi\sqrt{LC}$ $f1 = f2$ $f1 = 1/2\pi\sqrt{L1C1}$ $f2 = 1/2\pi\sqrt{L2C2}$

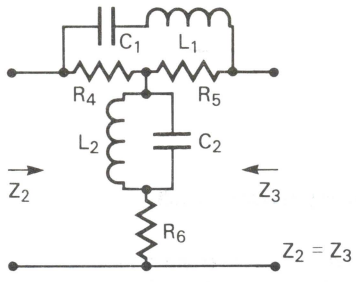


Figure 12. Equalizer Network

R4 and R5 are for all intent and purposes shorted and R6 is opened up. Thus, the pad loss is theoretically zero. The response of the equalizer needs to be shaped to the line loss characteristic of the cable in order to obtain as flat a response as possible at the output of the equalizer. Twenty dB of equalization is about all that can be obtained with a single equalizer of this configuration. If a greater amount of equalization is required two or more equalizers may be connected in tandem. The typical response of this network is shown in Figure 13. It is important to note about this circuit is the characteristic impulse response which may cause a ringing effect on the incoming data waveform.

If the shape of the equalizer response needs to be adjusted for a steeper response (going from 2 to 1), choose a higher inductance and a lower capacitance for the series resonant circuit and a lower inductance, higher capacitance for the parallel resonant circuit.

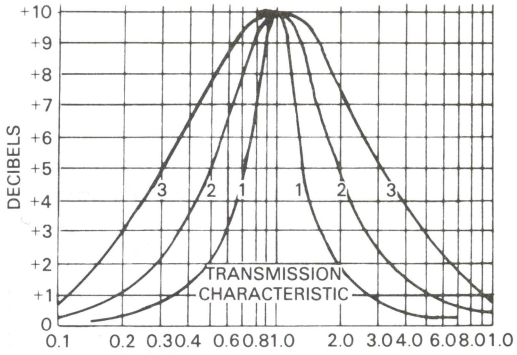


Figure 13. Transmission Characteristics of Equalizer Network

4. For ease of analysis concerning the preamplifier section, the following characteristics should be noted

   a. The input impedance of the preamplifier at 1.544MHz (pins 4 and 5) is approximately 10kΩ.

   b. The preamplifier closed loop AC gain is approximately equal to the ratio of (R11 + R12) over R14 as shown in Figure 15. For the application circuit shown in Figure 9, this value is calculated to be approximately 36dB. Capacitor C6 is an isolation capacitor and will be in the order of 1μF or higher.

   c. In order to minimize the noise at the input of the preamplifier, a small RC low pass filter is placed between pins 4 and 5 (R10 C10). Notice that the dynamic range and stability of the preamplifier is very susceptible to the capacitance between 4 and 5.

   d. R13 is chosen in order to minimize the offset of the preamplifier outputs. Its value is dependent on the resistor values used for the preamplifier gain adjust and the total series resistance between pin 7 and 4. C4 is a decoupling capacitor and forms a low pass filter together with R13.

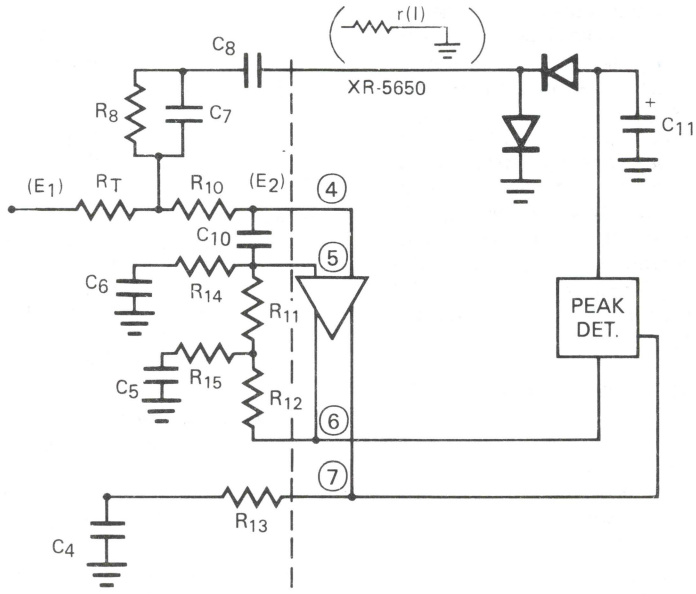


Figure 15. Preamplifier and ALBO Network Equivalent Circuit

5. The ALBO section usually preceeds the preamplifier and acts as a variable cable length simulator so that overall loss introduced by the cable and ALBO network equals to the loss of 6000 ft. long 22 AWG cable. The circuit implementation is based on the following characteristics:

   a. The energy of the pulse generated is constant.

   b. The gain phase characteristics of the preamplifier are fixed as shown in the application circuit.

Automatic equalizer adjusts its amplitude characteristics based on the peak value of the input signal. Figure 16 shows typical loss characteristics for 22 AWG cable for different lengths. It is important to notice that the location of the single pole and the low frequency loss are both a function of cable length.

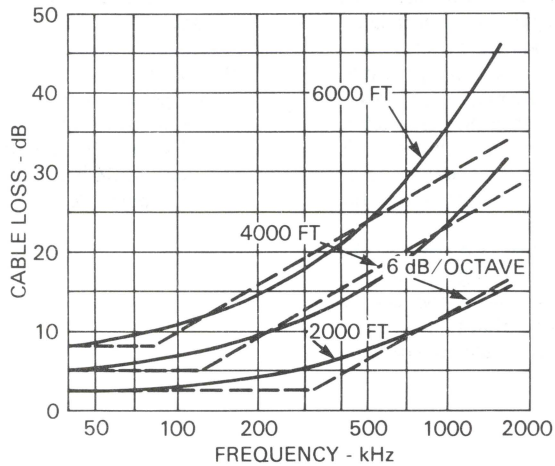


Figure 16. Loss of 22 Gauge Cable vs. Frequency

To obtain these characteristics it is necessary to generate an adjustable single zero and an adjustable flat gain for varying cable lengths.

The combination of the ALBO equalizer network and the cable loss will give a first order approximation, to produce a flat gain and linear phase below 772KHz. The feedback amplifier has an unbalanced input, a balanced output and contains fixed equalization in the feedback network. It also provides a fixed real zero below 772kHz and one beginning about at 800 kHz to optimize the immunity of the receiver for nearend crosstalk (NEXT) produced by other systems operating within the same cable sheath. The output of the prearmpifier is fed to a peak detector whose output voltage generates a control current (I), which in turn varies the small signal resistance, r(I). When diodes are fully on r(I) is guaranteed to be less than or equal to 25Ω. See Figure 15.

The capacitor C8 is used to block the DC from the input to the amplifier. Capacitor C11 is part of the ALBO filter circuit and together with R_{INT} sets ALBO time constant and AGC droop rate. It also smooths out the on current of the variolosser diodes. Assuming that the input impedance to the amplifier is sufficiently large so that it does not load down the output of the ALBO, we get the following transfer function:

$$(1) \qquad \frac{E2}{E1} = \frac{+r(I)}{RT+r(I)} \cdot \frac{s+\dfrac{r(I)+R8}{r(I)\ R8\ C7}}{s+\dfrac{1}{R8\ C7}}$$

where r(I) = ≈25Ω when fully on

this transfer function has a fixed pole at

$$s = -\frac{1}{R8\ C7}$$

and adjustable zero at

$$(3) \qquad s = \frac{r(I)+R8}{r(I)\ R8\ C7}$$

and a variable flat loss at

$$(4) \qquad \frac{R8 + r(I)}{RT + r(I)}$$

Notice that the feedback network as shown in Figure 15 has also a fixed real zero at S = 1/R15C5 that cancels out the pole of the ALBO and is equal to S = 1/R8C7.

6. An LC resonator is used to recover the clock from the incomming PCM pulse stream, Since the spectrum of bipolar signal passes through zero at the clock frequency, the spectrum is doubled by full wave rectifying the signal above the clock threshold. This brings the peak of the rectified spectrum on top of the clock frequency. The resonator is then driven by the output of the full wave rectifier to produce a stable clock signal.

   Frequency of resonance is given by

$$fo = \frac{1}{2\pi\sqrt{LC}}$$

   The 3dB bandwidth of the tank is related to the resonant frequency by the following expression:

$$B = \frac{fo}{Q}$$

   and the Q is related to circuit components as follows

$$Q = \frac{R}{Wo}$$

   Two important criteria need to be taken into account when receiving PCM signals. First, the tank has to have enough bandwidth so that the jitter in the recovered clock follows the jitter in the data in order not to cause any errors in the reception process. Second, the tank has to have enough Q to sustain the clock signal when 15 successive zeros are received. These two factors are in contradiction with each other, however, in practice, Qs in the range of 60-120 are used to meet the jitter and clock recovery requirements.

7. To achieve a minimum bit error rate, the eye pattern needs to be sampled in the middle where it has the largest opening. Since sampling is performed on the positive edge of the internal clock, this edge needs to be aligned with the peak of the eye pattern. To achieve this, an external RLC network is used to phase shift the clock signal by 90 degrees, R is chosen as 3.3k to cancel out the offset caused by an internal resistor. An RC combination could be used for phase shifting purposes as well. However, use of inductor L improves and emphasizes the clock transitions. In practice, the driver outputs are observed to turn , on roughly 30–40ns after the peak of the eye pattern. This is due to the delay of the clock signal through the slicer and output driver circuits.

   Output drivers are designed with open collector outputs which can handle 50mA peak currents to drive lines with characteristic impedance of 100Ω. The data output pulses are 50 percent duty cycle.

Short Haul PCM Line Interface Using the XR-T5683/L85

Application Note

INTRODUCTION

The XR-T5683/L85 Monolithic PCM Transceivers are designed primarily for short line (<10dB) PCM transmission applications such as in digital Private Branch Exchange's (PBXs), Digital Multiplexed Interfaces (DMI) and standard PCM data interface circuits. Both of these devices are identical in pinout but intended to operate in slightly different applications. The XR-T5683 is a higher frequency device (10MBPS), capable of extracting and transmitting data and clock from the AMI encoded data stream. The XR-T56L85 is capable of performing the same function up to 2.048MBPS and only consume one forth the power. Also, because of a different preamplifier input stage, the XR-T56L85 is capable of accepting either single coaxial, a twisted pair capacitive coupled or a balanced transformer input.

Both of these devices are packaged in a hermetirc 18 pin CERDIP and designed such that there is no phase difference between the extracted clock and data outputs.

PRINCIPLES OF OPERATION

Figure 1 contains a Functional Block Diagram of the XR-T5683 and XR-T56L85. The Circuit consists of two separate sections: one is the line receiver, and the other is the line transmitter. The receiver accepts incoming bipolar signals and converts them into TTL D+ and D– data streams. The main difference between the XR-T5683 and the XR-T56L85 preamplifier is that the XR-T56L85 is capable of accepting a single ended capacitive coupled AMI signal as well as a balanced transformer coupled signal. In order to successfully recover the data from the capacitive coupled signal, the receiver relies on the peak detector, which converts the positive signal amplitude into a DC variable threshold. This variable threshold is then mirrored around 2.5V (Voltage Reference) in order to be able to detect the negative coupled pulses. It also produces a clock output from the input data. In the transmit direction, full width, TTL compatible D+ and D– signals at the inputs and a 50% duty cycle clock are combined to form the bipolar line signal at the outputs of a transfomer. The power supplies for the two sections of the circuit are internally isolated to avoid crosstalk problems.

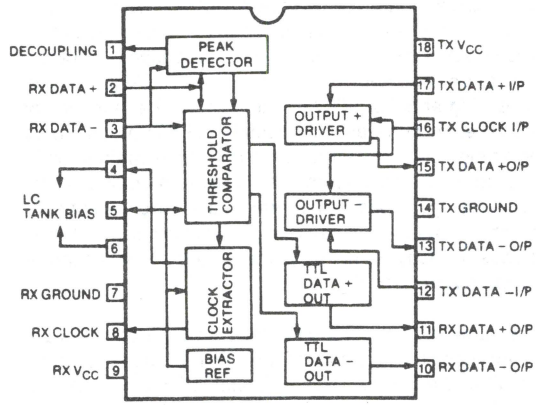


Figure 1. Functional Block Diagram for the XR-T5683 or XR-T56L85

Receiver Circuit Description:

The receiver is designed to handle a maximium of 10dB line attenuation. This condition allows the design to adopt a relatively simple approach as compared with long transmission line receivers which usually require ALBO circuits and equalization networks to function properly.

The operation of the XR-T5683 receiver relies on the peak detector which converts the incoming signal amplitude into a DC variable threshold. The variable threshold is arranged to slice the input signal at half amplitude point of the peak voltage (see figure 3), so that D+ and D– data can be accurately extracted under the worst expected condition. It also ensures a constant output pulse width, over the nominal 10dB of line attenuation. The D+ and D– data pulses go through similar level shifting circuits to be converted into TTL compatible output signals.

Clock Extraction and Timing

Since the input does not carry any frequency components around the transmission rate, the input waveform is full wave rectified and applied to an extenal L-C resonant circuit for clock extraction. The amplitude modulated sine wave at the resonant circuit is coupled through a capacitor to a zero crossing detector before being applied to the input of an ECL/TTL converter as shown in Figure 2.

To convert the half-width data at the receiver outputs into full width signals for digital processing, it is common practice to use positive edge triggered D/FFS. This requires the mid-point of the data to be aligned with the rising edge of the clock so that no error will result. Should the data be jittered with a max. amplitude of ±0.25 UI relative to the clock (see Figure 5). The disadvantage of this scheme is additional hardware that is needed to ensure the two signals have the correct timing relationship.

It is possible by means of an alternative retiming circuit as shown in Figure 6 to perform the same function while still keeping the data and the clock in the same phase. This circuit has twice the jitter tolerance under the same condition as compared with a single D-type counterpart and is recommended to be used with the XR-T5683/L85. It is anticipated that no glitches due to crosstalk, etc., should exist at the receiver data output terminals under the intended applications.

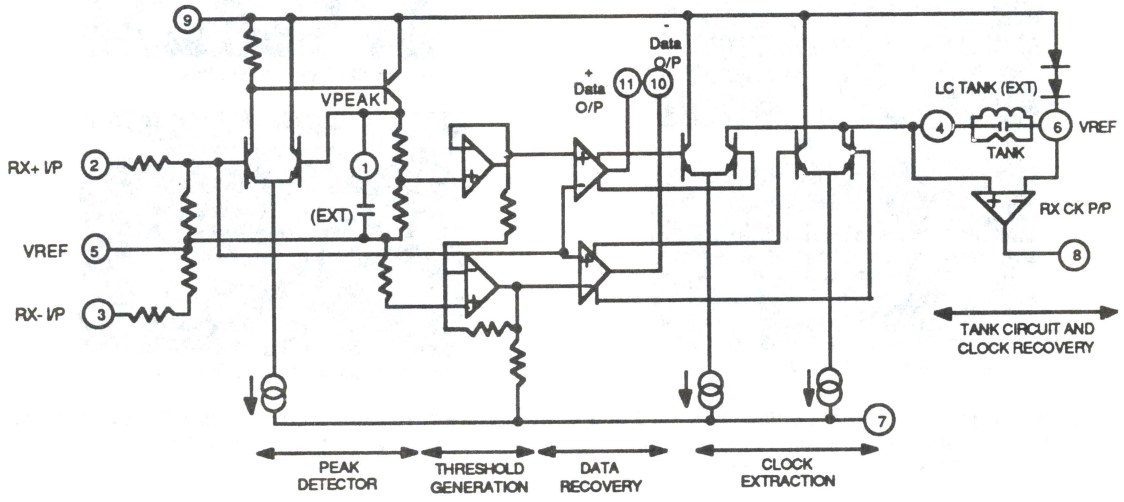


Figure 2. Simplifield Circuit of XR-T56L85 Circuit

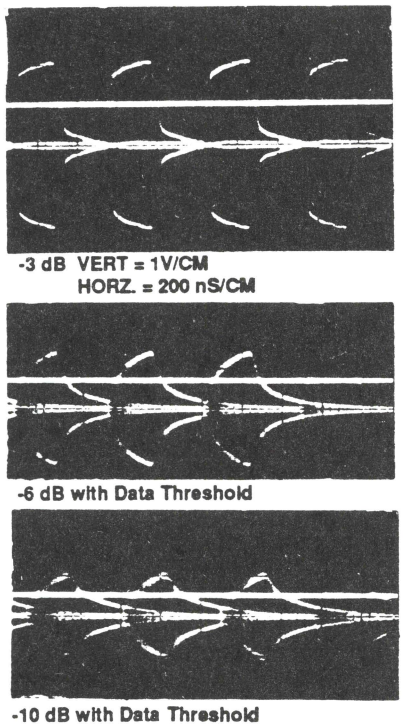


Figure 3. Typical Eye Pattern obtained at Pin 2 or 3 for Coaxial Cable at Various Line Length. Bit Rate = 2.048 KBits/s

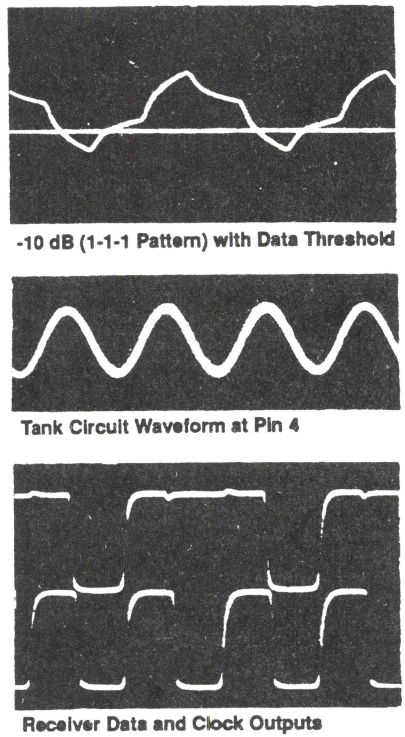


Figure 4. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern

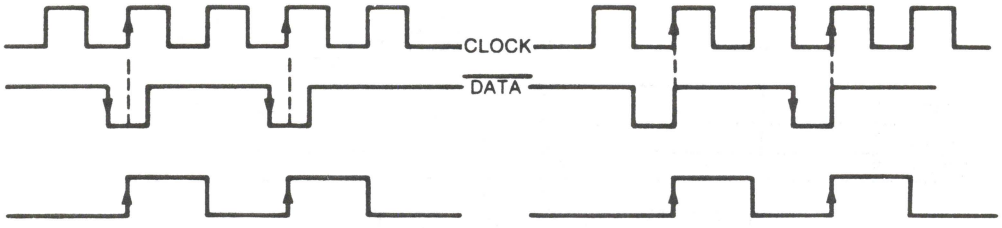


Figure 5. Retiming Circuit Requires Clock to be phase advanced by 90°C relative to data for optimum operations

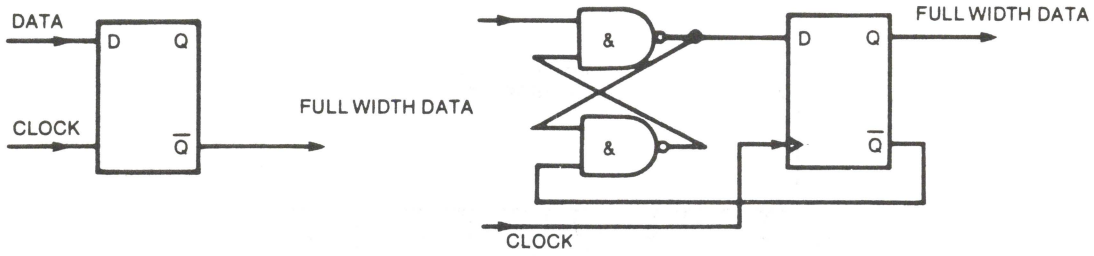


Figure 6. Retiming Circuit to be used with XR-T5683/L85

Transmitter:

The transmitter consists of two identical TTL input open-collector NAND gates. The output drivers are capable of handling a maximum current of 40mA for the XR-T5683 and 80mA for the XR-T56L85. If the input D+ and D– are half width signals, Pin 16 should be returned to $+V_{CC}$ via a 1K resistor. If the input data are full width signals, a synchronized 50% duty cycle TTL clock is needed at Pin 16 to obtain a bipolar signal at the output of a centre-tapped line transformer (see Figure 7). The output signal conforms to CCITT G.703 recommendation.

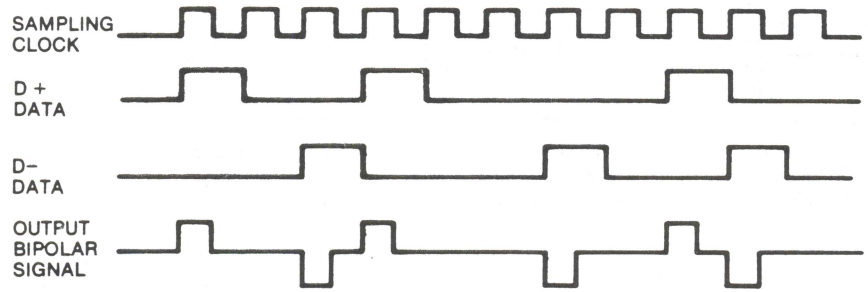
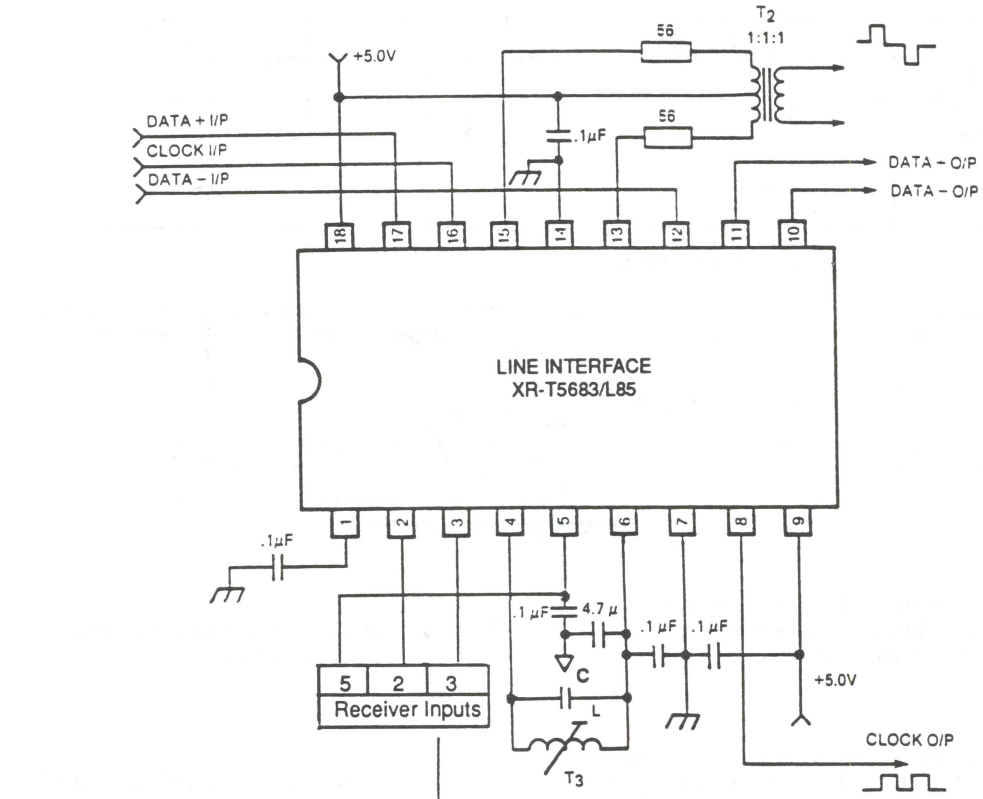
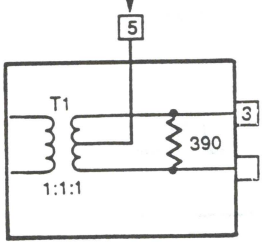
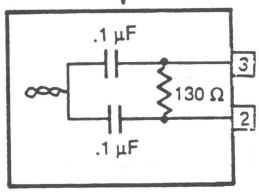


Figure 7. Input Timing Diagram for Transmitter

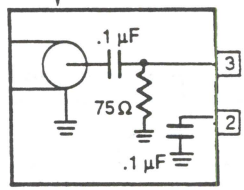




Transformer Coupling
(XR-T5683 &
XR-T56L85 only)



Capacitively Coupled
(Twisted Pair)
(XR-T56L85 only)



Coaxial Single Ended
Coupling
(XR-T56L85 only)

	1.544MPBS	2.048MPBS
Tank	AIE4150804	AIE4150804
C	175pF	100pF
T1	AIE3150765	AIE3150765
T2	AIE3180696	AIE3180696

Figure 8. Recommended Circuit for XR-T5683/L85

Application Note

Introduction to Phase-Locked Loop

INTRODUCTION

The phase locked loop provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 1, the PLL in its most basic form is a feedback system comprised of three basic functional blocks: a phase comparator, low-pass filter and voltage controlled oscillator (VCO).

The basic principle of operation of a PLL can briefly be explained as follows: With no input signal applied to the system, the error voltage $V_e(t)$ equal to zero. The VCO operates at a set frequency, f_o, which is known as the free- running frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to sychronize, or lock, with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a PLL system are its lock and capture ranges. They can be defined as follows:

Lock range: The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the tracking or holding range. Lock range increases as the overall gain of the PLL is increased.

Capture range: The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It decreases as the filter bandwidth is reduced.

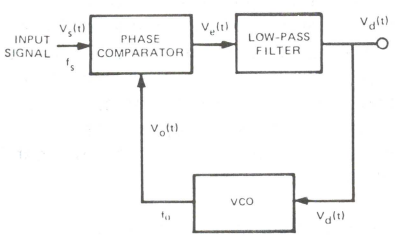


Figure 1. The basic phase locked loop consists of three functional blocks: a phase comparator, a low pass filter and a voltage-controlled oscillator

The lock and the capture ranges of a PLL can be illustrated with reference to Figure 2, which shows the typical frequency-to-voltage characteristics of a PLL. In the figure, the input is assumed to be swept slowly over a broad frequency range. The vertical scale corresponds to the loop error voltage.

In the upper part of Figure 2, the loop frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency f_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input, causing a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of the VCO voltage-to-frequency conversion gain, and goes through zero as $f_s = f_o$. The loop tracks the input until the input frequency reaches f_2, corresponding to the upper edge of the lock range. The PLL then loses lock, and the error voltage drops to zero.

If the input frequency is now swept slowly back, the cycle repeals itself as shown in the lower part of Figure 2. The loop recaptures the signal at f_3 and traces it down to f_4 The frequency spread between (f_1, f_3) and (f_2, f_4) corresponds to the total capture and lock ranges of the system. that is, $f_3 - f_1$ = capture range and $f_2 - f_4$ = lock range. The PLL responds only to those input signals sufficiently close to the VCO frequency, f_o, to fall within the "lock" or "capture" range of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered around f_o.

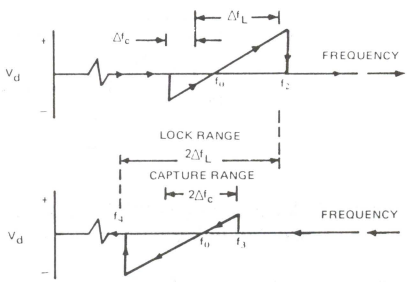


Figure 2. Typical PLL frequency-to-voltage transfer characteristics are shown for increasing (upper diagram) and decreasing (lower diagram) input frequencies

EXAMPLES OF APPLICATIONS

As a versatile building block, the PLL covers a wide range of applications. Some of the more important applications are the following:

FM demodulation: In this application, the PLL is locked on the input FM signal, and the loop-error voltage, $V_d(t)$ in Figure 1 (see Box), which keeps the VCO in lock with the input signal, represents the demodulated output. Since the system responds only to input signals within the capture range of the PLL, it also provides a high degree of frequency selectivity. In most applications the quality of the demodulated output (i.e., its linearity and signal/noise ratio) obtained from a PLL is superior to that of a conventional discriminator.

FSK demodulation: Frequency-shift keyed (FSK) signals are commonly used to transmit digital information over telephone lines, In this type of modulation, the carrier signal is shifted between two discrete frequencies to encode the binary data. When the PLL is locked on the input signal, tracking the shifts in the input frequency, the error voltage in the loop, $V_d(t)$, converts the frequency shifts back to binary logic pulses.

Signal conditioning: When the PLL is locked on a noisy input signal, the VCO output duplicates the frequency of the desired input but greatly attenuates the noise, undesired sidebands and interference present at the input. It is also a tracking filter since it can track a slowly varying input frequency.

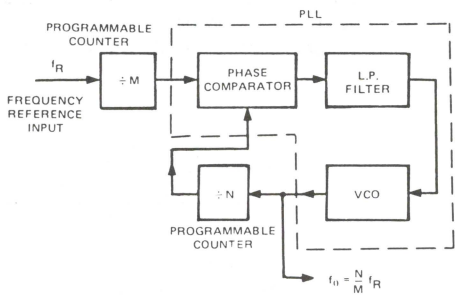


Figure 3. A frequency multiplier/divider can be constructed using a phase locked loop

Frequency synthesis: The PLL can be used to generate new frequencies from a stable reference source by either frequency multiplication and division, or by frequency translation. Figure 3 shows a typical frequency multiplication and division circuit, using a PLL and two programmable counters. In this application, one of the counters is inserted between the VCO and phase comparator and effectively divides the VCO frequency by the counter's modulus N. When the system is in lock, the VCO output is related to the reference frequency, f_R, by the counter moduli M and N as:

$$f_o = \left(\frac{N}{M}\right) f_R$$

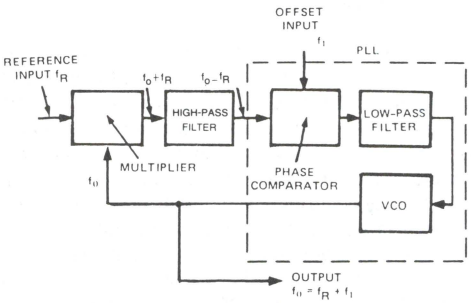


Figure 4. Frequency translation can be accomplished with a phase locked loop by adding a multiplier and an additional low-pass filter to the basic PLL

By adding a multiplier and an additional low-pass filter to a PLL (Figure 4), one can form a frequency translation loop. In this application, the VCO output is shifted from the reference frequency, f_R, by an amount equal to the offset frequency, f_1, i.e., $f_o = (f_R + f_1)$.

Data synchronization: The PLL can be used to extract synchronization from a composite signal, or can be used to synchronize two data streams or system clocks to the same frequency reference. Such applications are useful in PCM data transmission, regenerative repeaters, CRT scanning and or drum memory read-write synchronization.

At the onset of his design, the user of monolithic PLL products is faced with the key question of choosing the phase-locked loop IC best suited to his application. The broad line of PLL products offered by Exar cover a wide range of applications. It is often difficult to determine a a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question, "What is the best PLL product for the job?"

Table 2 gives a brief listing of some of the major classes of PLL applications, and lists the recommended circuits for each. A further discussion of the key performance parameters associated with each application is listed below.

FM demodulation: Essentially all the PLL circuits listed in Table 1 can be used for FM demodulation. However, it is often possible to narrow the choice down to 2 or 3 circuits, based on the particular performance criteria. In general, there are three key performance parameters which should be examined:

- Quality of demodulated output: This is normally measured in terms of the output level, distortion, and signal/noise ratio for a given FM deviation.
- VCO frequency range and frequency stability: For reliable operation, VCO upper frequency limit (see Table 1) should be at least 20% above the FM carrier frequency. VCO frequency stability is important, especially if a narrow-band filter is used in front of the PLL, or multiple input channels are present. If the VCO exhibits excessive drift, the PLL can drift out of the input signal band as the ambient temperature varies.
- Detection threshold: This parameter determines minimum signal level necessary for the PLL to lock and demodulate an FM signal of given deviation.

In most FM demodulation applications, it is also desirable to control the amplitude of the demodulated output. This feature is provided in some of the PLL circuits (such as the XR-215 and the XR-2212) by means of a variable-gain amplifier contained on the chip.

For low-frequency FM detection (below 300kHz carrier frequency) the XR-2212 is recommended because of its versatility and temperature stability. For FM demodulation at frequencies above 300kHz, the XR-215 offers the best performance because of its high frequency capability.

FSK decoding: Frequency-shift keying used in digital communications is very similar to analog FM modulation. Therefore, any PLL IC can be used for FSK decoding, provided that its input sensitivity and the tracking range are sufficient for a given FSK signal deviation. Some of the basic requirements and desirable features for a PLL used in FSK decoding are:

- Center frequency stability.
- Logic compatible output.
- Control of VCO conversion gain.

Center frequency stability is essential to insure that the VCO frequency range stays within the signal band over the operating temperature range. A logic compatible output is desirable to avoid the need for an external voltage comparator (slicer) to square the output pulses. It is particularly convenient if the output conforms to RS-232C standard, thereby eliminating the need for a separate line-driver circuit. Control of the VCO's conversion gain allows the circuit to be used for both large deviation FSK signals (such as 1200 baud operation) as well as for small deviation (75 baud) FSK signals.

For FSK decoding at low frequencies (i.e., below 300kHz) the XR-2211 is by far the optimum circuit to use because of its frequency stability and carrier-detect capability. For FSK delection at higher frequencies (up to 10MHz) the XR-210 is the recommended circuit.

Frequency synthesis: This application requires a PLL circuit with the loop opened between the VCO output and the phase comparator input, so that an external frequency divider can be inserted into the feedback loop of the PLL. This requirement is satisfied by the XR-S200, XR-210, XR-215 and the XR-2212 PLL circuits.

For frequency synthesis at low frequencies (i.e., with maximum output frequency less than 300kHz) the XR-2212 is by far the best suited circuit since it has the best VCO stability and interfaces easily with all logic families. For operation above 300kHz, either the XR-210 or the XR-215 PLL IC's can be used for frequency synthesis; however the XR-215 offers the highest frequency capability.

Signal conditioning: Most signal conditioning applications require very narrow-band operation of the PLL. This in turn may require the use of active filters within the loop (between the phase detector and the VCO). The PLL circuits which allow active filers to be inserted into the loop are the XR-S200 and the XR-2212. Both of these circuits already contain an op. amp. on the chip for active filtering. For low frequencies (i.e. below 300kHz) the XR-2212 is the best suited circuit because of its adjustable tracking bandwidth and excellent frequency stability. For higher frequencies the XR-S200 is the recommended circuit.

Tone decoding: The PLL circuits especially designed for this application are the XR-567, the XR-L567, the XR-2567 and the XR-2211. The XR-2211 offers the highest frequency stability among the three circuits and independent control of system bandwidth and response time. The XR-567 has a relatively high input threshold (≈ 20mV, rms) and may require input preamplification; however it requires fewer external components than the XR-2211. The XR-2567, which contains two independent 567-type tone decoders on the same chip may be more economical to use in multiple-tone detection systems.

AM detection: The PLL can be converted to a synchronous AM detector with the addition of a non-critical phase-shift network, an analog multiplier and a low-pass filter. The system block diagram for this application is shown in Figure 5.

In this application, as the PLL tracks the carrier of the input signal, the VCO regenerates the unmodulated carrier and feeds it to the reference input of the multiplier section. In this manner, the system functions as a synchronous demodulator with the filtered output of the multiplier representing the demodulated audio information.

Tone detection: In this application, the PLL is again connected as shown in Figure 5. When a signal tone is present at the input, within a frequency band corresponding to the capture range of the PLL, the output dc voltage is shifted from its tone-absent level. This shifts easily converted to a logic signal by adding a threshold detector with logic-compatible output levels.

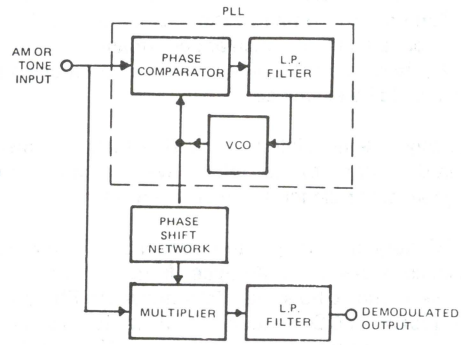


Figure 5. AM and tone detection are possible by adding three functional blocks to the basic phase locked loop

Motor speed control: Many electromechanical systems, such as magnetic tape drives and disc or drum head drivers, require precise speed control. This can be achieved using a PLL system, as shown in Figure 6. The VCO section of the monolithic PLL is separated from the phase-comparator and used to generate a voltage controlled reference frequency, f_R. The motor shaft and the tachometer output provide the second signal, frequency f_M, which is compared to the reference frequency. The controller is a power amplifier which drives the speed-control windings of the motor. Thus, the motor and tachometer combination essentially functions as a VCO which is phase locked to the voltage controlled reference frequency, f_R.

Stereo decoding: In commercial FM broadcasting, suppressed carrier AM modulation is used to superimpose the stereo information on the FM signal. To demodulate the complex stereo signal, low-level pilot tone is transmitted at 19kHz (1/2 of actual carrier frequency). The PLL can be used to lock onto this pilot tone, and regenerate a coherent 38kHz carrier which is then used to demodulate the complete stereo signal. A number of highly specialized monolithic circuits have been developed for this application.

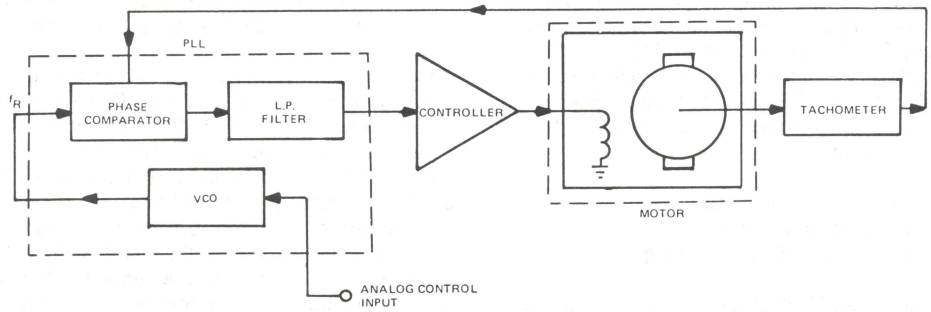


Figure 6. Very precise motor speed control is possible with a phase locked loop system of this type

Table 1. Major Applications for Exar's PLL Circuits

Table 1. Major Applications for Exar's PLL Circuits

Major Application	Part Number							
	XR-S200	XR-210	XR-215	XR-2211	XR-2212	XR-567	XR-L567	XR-2567
FM Demodulation High Frequency Low Frequency	√	√	√ √ √		 √ √			
Frequency Synthesis High Frequency Low Frequency	√	 √ √	 √ √		 √			
FSK Demodulation		√		√				
Signal Conditioning	√				√			
Tone Detection				√		√	√	√
Motor Speed Control	√				√			
Data Synchronization			√		√			
Low Power Operation							√	

Table 2. A Summary of Exar's PLL Circuits

Product Designation	Package	Operating Supply Range	High Frequency Limit	VCO Stability		Primary Applications
				Power Supply	Temp. (ppm/°C)	
XR-S200	24 Pin DIP	6V to 30V ±3V to ±15V	30MHz	0.08 (typ) 0.5 (max)	300 (typ) 650 (max)	Multi-function building block for FM/FSK detection, frequency systhesis
XR-210	16 Pin DIP	5V to 26V	20MHz	0.05 (typ) 0.5 (max)	200 (typ) 550 (max)	FSK modem, frequency synthesis, data synchronization
XR-215	16 Pin DIP	5V to 26V	35MHz	0.1 (typ) 0.5 (max)	250 (typ) 600 (max)	General purpose PLL. FM detection, tracking filter, frequency synthesis
XR-2211	16 Pin DIP	4.5V to 20V	300kHz	0.05 (typ) 0.5 (max)	±20 (typ) ±50 max)	FSK demodulation tone decoding, carrier detection
XR-2212	16 Pin DIP	4.5V to 20V	300kHz	0.05 (typ) 0.5 (max)	±20 (typ) ±50 (max)	Frequency synthesis, FM detection, data synchronization, tracking filter
XR-567	8 Pin DIP	4.75V to 9V	500kHz	0.5 (typ) 1 (max)	±140 (typ)	Tone detection
XR-L567	8 Pin DIP	4.75V to 9V	50kHz	0.5 (typ) 2 (max)	–150 ppm (typ)	Tone detection low-power equivalent of XR-567
XR-2567	16 Pin DIP	4.75V to 15V	600kHz	0.05 (typ) 0.2 (max)	±100 (typ)	Dual tone decoder (Dual tone equivalent)

Fundamentals of Monolithic Waveform Generation and Shaping

Application Note

INTRODUCTION

Waveform or function generators find a wide range of applications in communications and telemetry equipment, as well as for testing and calibration in the laboratory. In most of these applications, commercially-available monolithic IC oscillators and function generators provide the system designer with a low-cost alternative to conventional, non-integrated units costing several hundred dollars or more.

The fundamental techniques of waveform generation and shaping are well suited to monolithic IC technology. In fact, monolithic integrated circuits offer some inherent advantages to the circuit designer, such as the availability of a large number of active devices and close matching and thermal tracking of component values. By making efficient use of the capabilities of integrated components and the batch-processing advantages of monolithic circuits, it is now possible to design integrated waveform generator circuits that can provide a performance comparable to that of complex discrete generators, at a very small fraction of the cost. This article provides a brief review of the fundamental principles of monolithic waveform generation and wave- shaping methods.

Basics of IC Waveform Generation

Essentially a waveform generator is a stable oscillator circuit that outputs well-defined waveforms; and, these can be externally modulated or swept over a frequency range. A waveform generator usually consists of four sections: (1) an oscillator to generate the basic periodic waveform; (2) a wave-shaper; (3) an optional modulator section to provide AM capability, and (4) an output buffer amplifier to provide the necessary load drive. Figure 1 shows a simplified generator using the four functional blocks. Each block can be built readily in monolithic form with established linear IC technology. Hence fabrication of all four blocks on a single monolithic chip has evolved as a natural extension of earlier circuits.

The oscillator, usually a relaxation type, can generate linear, triangle or ramp waveforms. The usual technique involves constant-current charging and discharging of an external timing capacitor. Figure 2 shows a typical, though simplified, example: an emitter-coupled multivibrator circuit, which can generate a square wave as well as a triangle or a linear ramp output.

The circuit's operation is as follows: At any given time, either Q_1 and D_1 or Q_2 and D_2 are conducting such that capacitor C_o is alternately charged and discharged by constant-current I_1. The output across D_1 and D_2 corresponds to a symmetrical square wave, having a pk-pk amplitude of $2V_{BE}$, or twice the transistor base-emitter voltage drop. Output V_A, constant when Q_1 is on, becomes a linear ramp with a slope equal to $-I_1/C_o$ goes off. Except for a half cycle delay, output $V_B(t)$ is the same as $V_A(t)$.

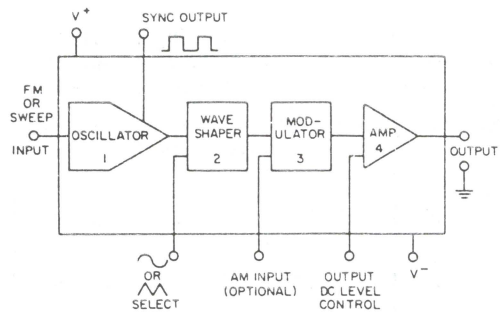


Figure 1. Basically, a waveform generator consists of four sections. Each section can be built readily in monolithic form with established IC technology

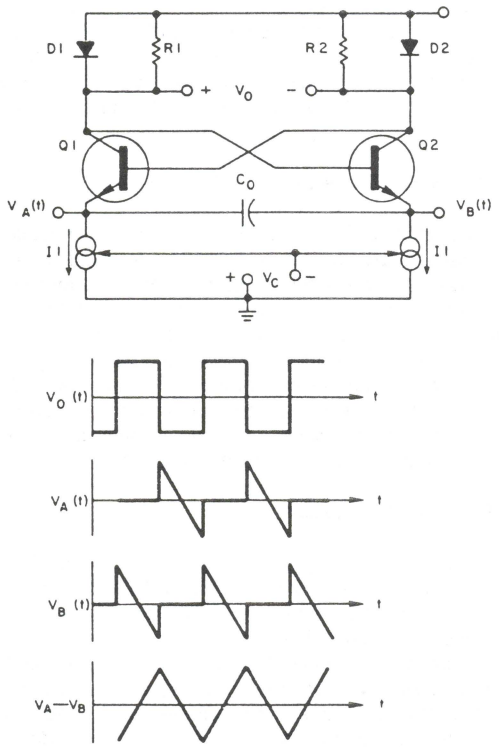


Figure 2. A simple oscillator circuit can be used to generate square, ramp and triangle waveforms

Both linear ramp waveforms have pk-pk amplitudes of $2V_{BE}$. Their frequency of oscillation, f_o, can be determined from the formula

$$f_o = \frac{I_1}{4V_{BE}C_o}$$

And f_o can be controlled by variation of charging-current I_1 via control voltage V_C. A subtraction of one output ramp voltage from the other, by use of a simple differential amplifier, obtains the linear triangular wave-form.

Symmetry of triangle and square-wave outputs may be adjusted by replacement of one of the two current sources in Figure 2 by I_2, where $I_2 \neq I_1$. Then the duty cycle of the output waveforms becomes the following:

$$\text{Duty Cycle} = 50 \frac{I_1}{I_2} \%.$$

The duty cycle of the output may be varied over a wide range by varying the ratio of the currents I_1 and I_2.

Wave-Shaping Techniques

The most useful waveform in signal processing applications is the sine wave. In the design of function generators, sinusoidal output is normally obtained by passing a triangular wave through a wave shaping circuit. In most discrete-component generators, wave-shaping involves a diode-resistor or a transistor-resistor ladder network. Introduction of a finite number of "break points" on the triangle wave changes it to a lower distortion sine wave.

Although this method can also be adapted to monolithic circuits, it is not as practical because it requires extremely tight control of resistor values and diode characleristics. A simpler, and more practical, sine shaper for monolithic circuits employs the "gradual cutoff" characteristics of a basic differential gain stage, as in Figure 3.

Reduction of the emitter = degeneration resistance, R_E, allows either transistor Q_3 or Q_4 to be brought near their cutoff point when the input triangle waveform reaches its peaks. For the proper choice of the input amplitude and bias-current levels, the transfer characteristics at the peaks of the input triangle waveform become logarithmic rather than linear. Thus, the peaks of the triangle become rounded, and the output appears as a low distortion sine wave.

Use of this technique permits output harmonics to be reduced to less than 0.5% with only a single adjustment. The low distortion is possible because the technique relies on component matching rather than their absolute values. Since monolithic ICs can be designed readily for close matching, this wave-shaping is ideally suited to monolithic design.

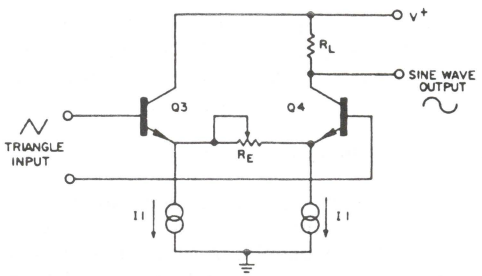


Figure 3. Conversion of triangle to sine wave employs a differential gain stage, which avoids dependence on absolute values of components

Phase-Locked Loop Design

The current-controlled or voltage-controlled oscillator (VCO) is one of the essential components of a phase-locked loop (PLL) system. The key requirement for this application is that the oscillator should have a high degree of frequency stability and linear voltage or current-to-frequency conversion characteristics. Sinusoidal output, although often useful, is generally not required in this application.

Although all of Exar's IC oscillators can be used as a VCO in designing PLL systems, the XR-2207 or its low-cost and simplified version, the XR-2209, are often the best suited devices for this application. For additional information refer to Application Note AN-06, entitled "Precision PLL System Using the XR-2207 and the XR- 2208" included in this Data Book.

Sweep Oscillator

A sweep oscillator is required to have a large linear sweep range. Among Exar's function generators, the XR-2207 and the XR-2206 have the widest linear sweep range (over 1000:1), and are best suited for such an application.

By using a linear ramp output from the XR-2207 to sweep the frequency of the XR-2206, one can build a two-chip sweep oscillator system which has a 2000:1 sweep range and sinusoidal output.

Low-Cost General Purpose Oscillator

In many digital design applications, one needs a stable, low-cost oscillator IC to serve as the system clock. For such applications, the XR-2209 precision oscillator is a logical design choice since it is a simple, low-cost oscillator circuit and offers 20ppm/°C frequency stability.

The monolithic timer circuits, such as 555 types or the micropower version, the XR-L555, can also be used as low-cost, general purpose oscillators by operating them in their free-running, i.e., self-triggering mode.

Ultra-Low Frequency Oscillator

In certain applications such as interval-timing or sequencing, stable, ultra-low frequency oscillators which can operate at frequencies of 0.01Hz or lower are required. Among Exar's oscillator circuits, the IC most suited to such an application is the XR-8038 since it can operate with a polarized electrolytic capacitor as its timing component. All other oscillator circuits described in this book require non-polar timing capacitors, and therefore are not practical for ultra-low frequency operation.

An alternate approach to obtaining stable ultra-low frequency oscillators is to use the XR-2242 counter/timer as an oscillator in its free-running mode. Such a circuit generates a square wave output with a frequency of 1/256 RC where R and C are the external timing component value.

CHOOSING THE RIGHT IC OSCILLATOR

At the onset of his/her design, the user of monolithic oscillator products is faced with the key question of choosing the oscillator or the function generator best suited to his application. The broad line of function generator products offered by Exar covers a wide range of applications. It is often difficult to determine at a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question. "What is the best IC oscillator for the job?

Sine Wave Generation

In evaluating the output characteristics of sinusoidal IC oscillators, total harmonic distortion (THD) of the output waveform is usually the key performance criteria. In a number of voice-grade telecommunication or laboratory applications, sine wave distortion of 2% to 3% may be tolerable. However, for audio-quality signals, distortion level of 1% or less is required. Furthermore, it is desirable that the output distortion should be relatively independent of the output amplitude, frequency or temperature changes; and that the distortion level be minimized with a minimum amount of external adjustments.

Exar manufactures three separate families of IC oscillators which provide sinusoidal output waveforms. These are the XR-205, XR-2206 and the XR-8038. All of these circuits require external trimming to minimize the output distortion. In the case of XR-205, the untrimmed distortion is about 5%; in the case of the XR-2206 and the XR-8038, untrimmed distortion is typically less than 2%, and can be reduced to 0.5% with additional trimming.

For low frequency sine wave generation (below 100kHz), the XR-2206 and the XR-8038 are the recommended circuits. The XR-8038 has a fixed output level, whereas the XR-2206 offers separate output dc level and amplitude adjustment capability.

AM Generation

Linear modulation of output amplitude by means of an analog control signal is a desirable feature for telemetry and data transmission applications. In monolithic IC oscillators, this capability is normally obtained by including a four-quadrant transconductance multiplier on the IC chip. Both the XR-205 and the XR-2206 circuits have such a feature included on the chip and can be used for generating sinusoidal AM signals. They can operate both in suppressed-carrier or conventional double-sideband AM generator mode. For operation with frequencies below 100kHz, the XR-2206 has superior performance characteristics over the XR-205.

FM Generation

Essentially all of Exar's IC oscillator circuits can be used for generating frequency-modulated waveforms. For small frequency deviations (i.e., 15% or less) about the center frequency, all of these oscillators have FM nonlinearity of 0.1% or less. However, if wider FM deviations are required the XR-2209, XR-2207 and the XR-2206 offer the best FM linearity.

FSK Generation

Frequency-shift keying (FSK) is widely used in data communications, particularly in data-interface or MODEM systems. In monolithic IC oscillators, FSK capability is obtained by using a current-controlled oscillator and keying its control current between two or more programmed levels which are set by external resistors. This results in output waveforms which are phase-continuous during the frequency transitions between the "mark" and "space" frequencies.

The XR-2207 can produce four discrete frequencies, set by one external capacitor and four setting resistors. Frequency keying between these four frequencies is achieved by a two-bit binary logic input. The circuit produces both triangle and square wave outputs. The XR-2206 produces two discrete frequencies, f_1 and f_2, and has a one-bit keying logic input. The key advantage of XR-2206 over the XR-2207 in FSK MODEM design is the availability of a sinusoidal output waveform.

Exar has compiled a comprehensive application note describing the use of both of these IC products in the design of FSK MODEM systems. This application note (AN- 01) entitled "Stable FSK MODEMs Featuring the XR-2207, XR-2206 and the XR-2211" is also included in this Data Book.

Laboratory Function Generator

One of the main applications for oscillators is for laboratory or test instrumentation or calibration where a variety of different output waveforms are required. Such applications require both AM/FM modulation capability, linear frequency sweep and sinusoidal output. The circuit fitting this application the best is the XR-2206. It has all the fundamental features of a complete function generator system.

A comprehensive description of building a self-contained laboratory-quality function generator system using the XR-2206, Application Note AN-14, is included in this Data Book.

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DATA COMMUNICATION PRODUCTS

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Application Notes
AN-34 Using the XR-88C681 CMOS DUART 3-389

Modem Product Selection Guide

Part Number	Description	Standards		Supply Voltages	Package		
		CCITT	Bell		DIP	PLCC	QFP
XR-2900	Fax/Data Modem	V.29 V.27ter V.22bis V.22 V.21 ch 2	212A 103	+5V XR-2901 ±5V XR-2902	40 48	44 52	44 52
XR-2400	V.22bis Modem	V.22bis V.22	212A 103	+5V XR-2401 ±5V XR-2402	40 48	44 52	
XR 2402A	Enhanced AFE	V.22bis V.22	212A 103	±5V	48	52	
XR-2403B	MNP5 Microcontroller		MNP 2-5	+5V	40	44	
XR-2321	V.23/V.21 Modem	V.23 V.21		±5V	20	20	24 JEDEC SO
XR-2100	V.21 Modem	V.21		±5V	20	20	
XR-2135A	Bell/CCITT Data Buffer			+5V	14		
XR-2442	V.42/MNP5 Microcontroller	V.42	MNP5	+5V	40	44	44
XR-2443	V.42bis/MNP5 Microcontroller	V.42 V.42bis	MNP5	+5V	40	44	44
XR-2942	Fax/Data Microcontroller	V.29 V.27ter V.22bis V.21ch2 V.42	212A 103	±5V XR-2901 ±5V XR-2902	40	44	44
XR-2943	Fax/Data Microcontroller	Same as XR-2942 V.42bis	212A 103	±5V XR-2901 ±5V XR-2902	40	44	44
ADVANCED INFORMATION - CONSULT FACTORY FOR AVAILABILITY							
*XR-2321A	V.23/V.21 Modem	V.23 V.21		±5V	20	20	24 JEDEC SO

** Includes selectable CPM filters and other features for european market*

UART Product Selection Guide

Part Number	Description	Product Features	Technology	Supply Voltages	Package
XR-16C450	Asynchronous Receiver and Transmitter	Pin and Functional Compatible to INS8250 Includes Modem Control Signals Programmable Character Length (5, 6, 7, 8) Odd, Even or No Parity Generation Independent Receive and Transmit Control TTL Compatible Input and Outputs	CMOS	+5V ±5%	28 Pin Plastic PLCC
XR-16C452	Dual Universal Asynchronous Receiver and Transmitter with Parallel Printer Port	Pin-to-pin and functionally compatible to VL16C452 Fully compatible with all New Bidirectional PS/2 Printer Port Registers Modem Control Signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~) Programmable Character Lengths (5, 6, 7, 8) Even, Odd, or no parity bit generation and detection Status Report Register Independent Transmit and Receive Control TTL Compatible Inputs, Outputs Direct Replacement of Logic for PC/XT/AT High Data Transfer Rate 448 kHz Transmit/Receiver Operation with 7.372MHz Crystal or External Clock Source	CMOS	+5V ±10%	PLCC
XR-16C550	Universal Asynchronous Receiver/ Transmitter with FIFOs	Pin-to-pin and Functional Compatible to NS16550, VL16C550, WD16C550 Modem Control Signal (CTS~, RTS~, DSR~,DTR~, RI~, CD~) 16 byte Programmable FIFO for Transmit and Receive Section Programmable Character Lengths (5, 6, 7, 8) Even, Odd, or No Parity bit Genetation and Detection Status Report Register Independent Transmit and Receive Control TTL Compatible In puts, Outputs Software Compatilbe with INS8250, NS16C450 448kHz Transmit/ Receive Operation with 7.372MHz Crystal or External Clock Source	CMOS	5V ±10%	PLCC

Part Number	Description	Product Features	Technology	Supply Voltages	Package
XR-16C552	Dual Universal Asychronous Receiver / Transmitter with FIFOs and Parallel Printer Port	Pin-to-pin and Functionally Compatible to VL16C552 Fully Compatible with all New Bidirectional PS/2 Printer Port Modem Control Signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~) Programmable Character Lengths (5, 6, 7, 8) Even, Odd or No Parity bit generation and Detection Status Report Register Independent Transmit and Receive Control TTL Compatible Inputs, Outputs Direct Replacment of Logic for PC/XT/ATHigh Data Transfe Rate	CMOS	5V +10%	PLCC
XR-88C681	Dual Asynchronous Receiver and Transmitter	Fully Independent Operation Buffered Receiver and Transmitter Programmable Stop Bits (1/16 Increments) Internal Bit Rate Generator	CMOS	+5V ±5%	28 & 40 Pin Ceramic LCC Plastic PLCC
XR-68C681	Dual Asynchronous Receiver and Transmitter	Bit Rate Selection (Receiver or Transmitter) Max Bit Rate (1 XCLK=1MBPS,16XCLK=125kBPS) Normal, Autoecho, Local and Remote Loopback Multifunction 16 Bit Counter/ Timer Eight Maskable Interrupt Conditions Interrupt Vector Output on Acknowledge Programmable Interrupt Daisy Chain 15 I/O Pins Depending on Package Multidrop Mode (8051 Nine Bit Mode) Stand By Mode for Reduced Power	CMOS	+5V ±5%	40 Pin Ceramic LCC Plastic PLCC
XR-82C684	Quad Asynchronous Receiver and Transmitter	Quadruple Receive and Transmit Buffer Programmable Stop Bits in 1/16 Increments Pin Selectable 88 or 68 Mode Four Bit Rate Generators (33 Baud Rates) External Clock Capability Normal, Autoecho, Local and Remote Loopbacks Two Multifunction 16 Bit Counter/Timer Interrupt Output with 16 Interrupt Condition Interrupt Vector Output on Acknowledge Programmable Interrupt Daisy Chain 16 I/O Pins Depending on Package Multidrop Mode Depending on Package Stand By Mode For Reduced Power Debounced Reset Input (20ns) Operates with 3.68 or 7.38MHz Crystals	CMOS	+5V ±5%	44 Pin PLCC 68 Pin PLCC

V.21 Modem

GENERAL DESCRIPTION

The XR-2100 is designed to provide the CCITT V.21 modem function. Complete circuitry is included for this 300 BPS FSK full duplex operation.

The XR-2100 can be used as a stand-alone modem under control of a standard microcontroller such as the 8031. Bus structured control interfaces have been implemented for direct microcontroller connection. The XR-2100 may also be programmed for serial control.

The XR-2100 can also be used to provide V.21 operation for other higher speed Exar modem chips such as the XR-2400and XR-2900 chip sets for V.29/V.27ter/V.22 bis/V.22/212A applications. The XR-2100 ties directly to the same control bus and line interface circuitry as the XR-2400 chip set.

The XR-2100 is constructed in silicon gate CMOS technology for low power operation. Available in a 20 pin dip (0.3" width) and PLCC package, the XR-2100 operates from ±5 volt power supplies.

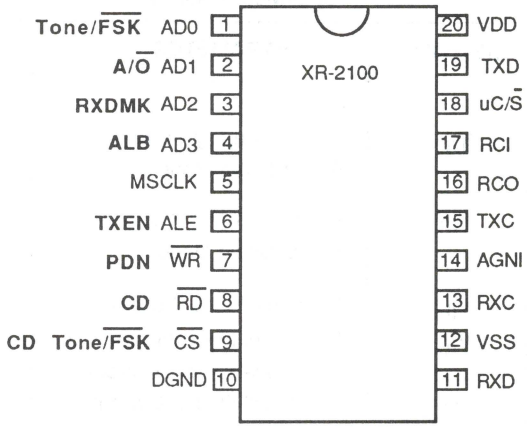
FEATURES

CCITT V.21 operation
300 BPS FSK, full duplex
Universal microcontroller or serial interface
Direct connection to:
XR-2900/XR-2400, V.29/V.27ter/V.22bis/V.22/212A
Low power CMOS(100 mW TYP)
Analog loopback
Generator and detector for answer and calling tones
Power down mode

ABSOLUTE MAXIMUM RATINGS

Power Supply	
VDD	-0.3 to 7V
VSS	0.3 to -7V
InputVoltage	VSS -0.3V to VDD +0.3V
DC Input Current	+10mA
Power Dissipation (Package Limitation)	
Plastic Dip	1W
Derate Above 25°C	
Plastc Dip	5mW/°C
Storage Temperature Range	-65°C to +150°C

PIN ASSIGNMENT



Bold type indicates uC/$\overline{STD}$ = 0

(For other pin assignments refer to the end of this datasheet)

ORDERING INFORMATION

Part umber	Package	Operating Temperature
XR-2100CP	Plastic	0°C to 70°C
XR-2100CJ	PLCC	0°C to 70°C

APPLICATIONS

Stand-alone V.21 Modem
V.21 Mode for 1200/2400 BPS Systems
Internal Type Modem

SYSTEM DESCRIPTION

The XR-2100, when connected to a microcontroller and line interface circuit, forms a complete CCITT V.21 300 BPS modem. Utilizing a universal bus interface, the XR-2100 can be used as a stand-alone modem or for providing the V.21 to existing modem chip sets such as the XR-2400 and XR-2900 modems.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^{\circ}C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $MS_{CLK} = 11.0592$ MHz $\pm$ 0.05% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	Positive Supply Current		11		mA	
	Power Down Mode		7		mA	Guaranteed but not tested.
I_{SS}	Negative Supply Current		11		mA	
	Power Down Mode		7		mA	Guaranteed but not tested.
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4$ V
I_{OL}	Low Level Output Current			2	mA	
I_I	Input Current			50	µA	V1 = 0 to V_{DD}
VO_{CAR}	Transmit Carrier Output	+6.5	7	8.2	dBm	FSK Carrier calling or
		+5.7	7	8.2		ANS Tone, calling tone
$V_{CAR\ RNG}$	Input Carrier Range	-43		-10	dBm	ANS, ORIG mode.
CD off		-49	-48	-47	dBm	FSK
CD on		-43	-43	-41	dBm	FSK
CD_{HYS}	Carrier Detect Hysteresis	2	6	20	dB	FSK,
S/N	Signal-to-noise Ratio		7		dB	ANS/ORIG $R_{XC} = -40$ dBM $T_{XC} = -10$ dBM C0, C2, or B/B line conditions BER≤1/10-5
BIAS DIST	Bias Distortion		4		%	ORIG mode
			5		%	ANS mode
f_{AMARK}	Mark Frequency Answer		1650		Hz	
f_{ASPACE}	Space Frequency Answer		1850		Hz	
fo_{MARK}	Mark Frequency Originate		980		Hz	
foSPACE	Space Frequency Originate		1180		Hz	
fANS	Answer Tone Frequency		2100		Hz	

Carrier Frequencies fMSCLK - 11.0592 MHz

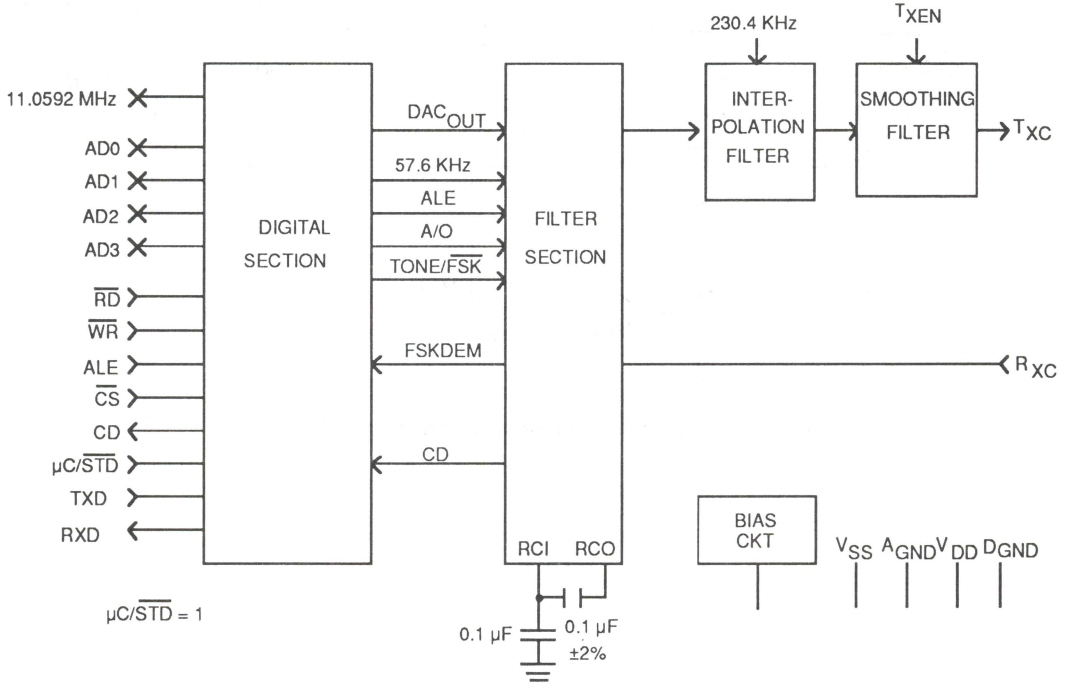
Desired (Hz)	Actual (Hz)	Error (Hz)
980	978.34	-1.66
1180	1181.54	+1.54
1650	1651.61	+1.61
1850	1850.60	+0.60
1300	1301.69	+1.69
2100	2104.11	+4.11

Table 1. Frequency Accuracy

Mode	Transmit Frequency (Hz)		Receive Frequency (Hz)	
	Mark	Space	Mark	Space
Originate	980	1180	1650	1850
Answer	1650	1850	980	1180

Table 2. CCITT V.21 Frequency Parameters

CCITT V.25 Answer
Tone: 2100 Hz



System Block Diagram For XR-2100

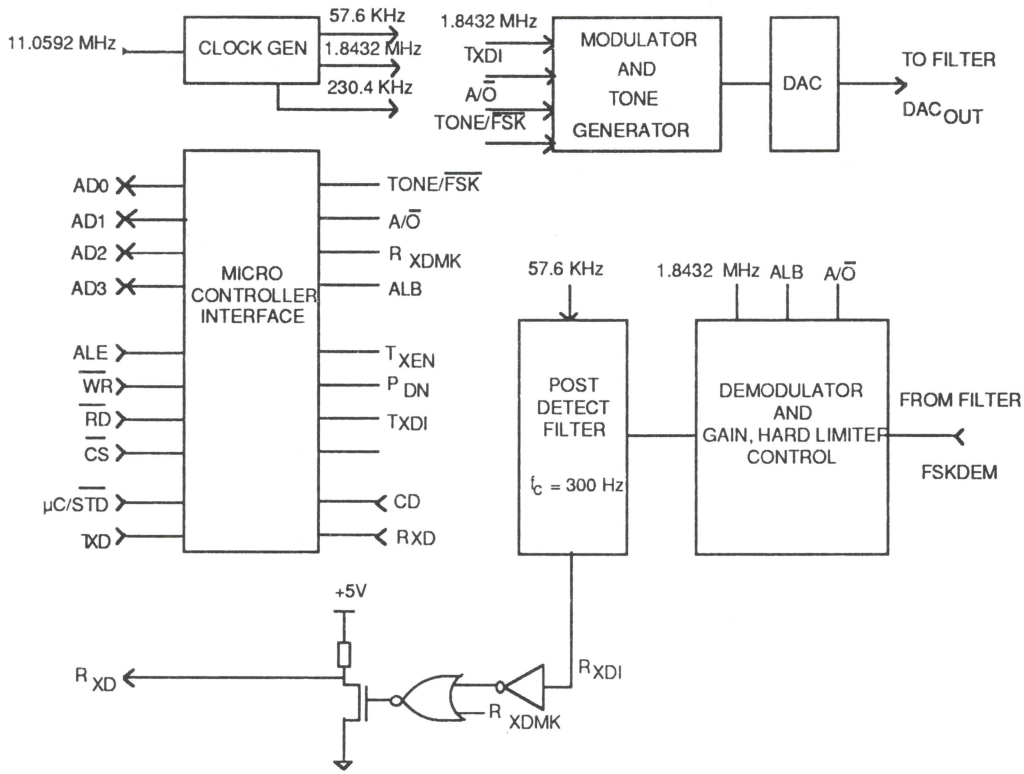


Figure 1. Digital Section Block Diagram For XR-2100

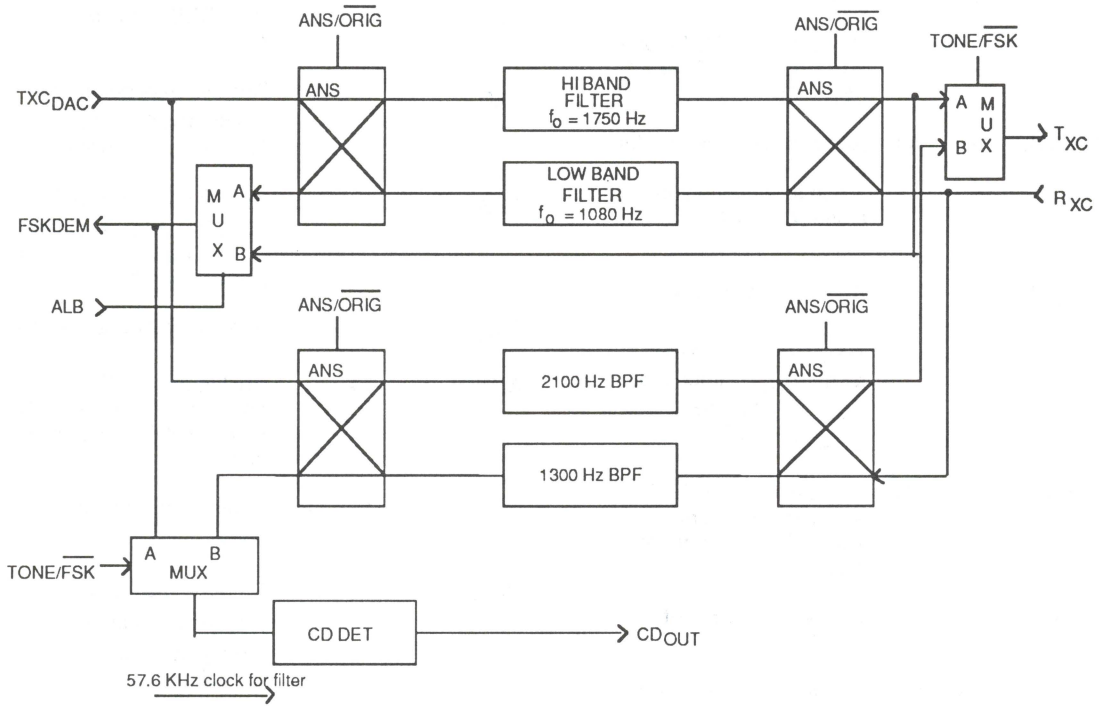


Figure 2. Block Diagram of XR-2100 Filter Section

PIN DESCRIPTIONS

Name	Pin #	I/O	Description
AD0 (Tone/$\overline{FSK}$)	1	I/O	Address/data bus bit 0 for µC. Select tone or FSK mode for stand-alone (Tone = 1, FSK = 0).
AD1 (A/$\overline{O}$)	2	I/O	Address/data bus bit 1 for µC. Mode select for stand-alone (ANS = 1, Orig = 0).
AD2 (RX_{DMK})	3	I/O	Address/data bus bit 2 for µC. R_{XD} control for stand-alone (R_{XD} clamped to mark = 1, R_{XD} from DEMOD = 0).
AD3 (ALB)	4	I/O	Address/data bus bit 3 for ALB control for stand-alone (ALB = 1, normal receive = 0).
MSCLK	5	I	Master clock input of 11.0592 MHz.
ALE (T_{XEN})	6	I	Address latch enable for µC. Transmit carrier control for stand-alone (1 = enable0 = disable).
$\overline{WR}$ (P_{DN})	7	I	Write enable 'or" for µC. Power down control for stand-alone (1 = power down, 0 = normal operation).
$\overline{RD}$ (CD)	8	I/O	Read enable 'not' for µC. Carrier detect status for stand-alone.
$\overline{CS}$ (CD Tone/$\overline{FSK}$) stand-	9	I	Chip select 'not' for µC. Energy output control alone. (1 = Tone Energy, 0 = FSK Energy)
DGND	10	I	Digital ground. This pin should be routed separate to the AGND to the power supply.
R_{XD}	11	O	Receive data output from the demodulator output (1 = mark, 0 = space).
V_{SS}	12	I	Negative power supply, -5V ±5%. A 0.1uF ceramic bypass capacitor should be placed near the device.
R_{XC}	13	I	Analog recieve carrier input.
AGND	14	I	Analog ground. This pin should be routed separate to the DGND to the power supply.
T_{XC}	15	O	Analog transmit carrier output.
R_{CO}	16	O	Receive filter output. Connected to the R_{CI} through a 0.1 µF capacitor.
R_{CI}	17	I	Demod input. Connected to R_{CO} through a 0.1 µF capacitor
µC/$\overline{STD}$	18	I	Control input for selecting µC or stand-alone interface. (1 = µC, 0 = stand-alone).
T_{XD}	19	I	Transmit data input (1 = mark, 0 = space).
V_{DD}	20	I	Positive power supply voltage, +5V±5%. A 0.1 µF bypass capacitor should be placed near this pin.

CONTROL REGISTERS
With µC/$\overline{STD}$ = 1 (µC interface selected)

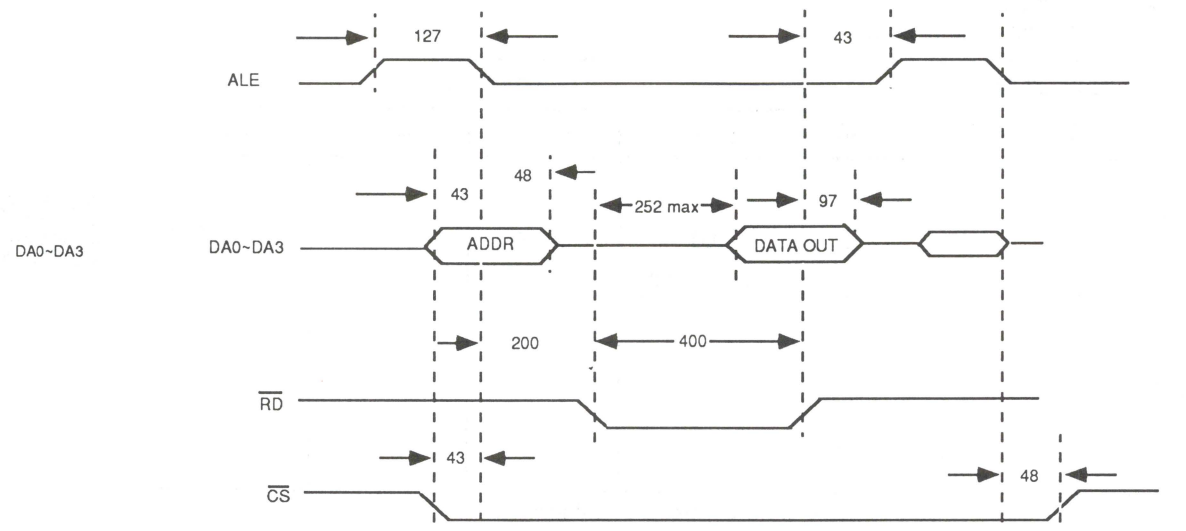
ADDRESS BITS				DATA BITS			
AD3	AD2	AD1	AD0	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{WR}$ =0							
1	0	0	0	ALB	RXDMK	A/$\overline{O}$	Tone/$\overline{FSK}$
1	0	0	1	CD Tone/$\overline{FSK}$	-	PDN	TXEN
$\overline{RD}$ = 0							
1	0	0	0	-	-	CD	RXD

Table 3. µC Control Bit Assignments

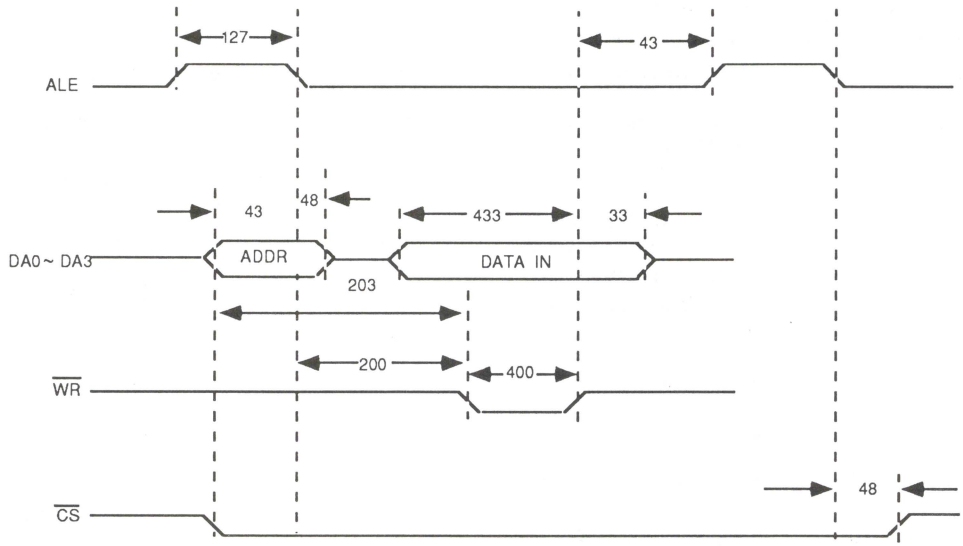
STAND-ALONE MODE SELECTIONS
With µC/$\overline{STD}$ = 0 (Stand-alone mode selected).

Mode	I/O State	Mode Descriptions
Tone/$\overline{FSK}$	1	Answer or calling tone, 2100 Hz for A/$\overline{O}$ = 1 and 1300 Hz for A/$\overline{O}$ = 0.
	0	FSK mode, 980 Hz/ 1180 HZ for mark/space in ORIG and 1650 Hz/ 1850 Hz for mark/space in ANS.
A/$\overline{O}$	1	Answer mode.
	0	Originate mode.
RXDMK	1	R_{XD} is clamped to mark.
	0	R_{XD} is demod output.
ALB	1	ALB

Mode	I/O State	Mode Descriptions
T_{XEN}	1	T_{XC} is enabled.
	0	T_{XC} is disabled.
P_{DN}	1	Power down mode
	0	Normal operation.
CD	1	CD is on.
	0	CD is off.
		CD depends on the mode selected, it can be: . Normal receive HI band: FSK Orig. . Normal receive LO band: FSK Ans. . Ans Tone Detect: Tone Orig. . Calling Tone Detect: Tone Ans.



Read Cycle



Write Cycle

Note: 12 MHz Oscillator
All units in nanoseconds (minimum), unless otherwise specified.

Figure 3. Read/Write Timing Waveforms for XR-2100 Using 8031/51 Controller

APPLICATIONS INFORMATION

Figures 4 and 5 illustrate the XR-2100 used in various applications. In each, several precautions should be followed in order to ensure optimum performance.

1) Analog (AGND) and digital (DGND) grounds should be routed separately to the power supply. They should be single point connected at the supply. This will minimize higher digital currents from interfering with more sensitive analog sections.

2) The power supply pins should be bypassed with 0.1 μF ceramic capacitors close to the IC.

Figure 4 shows the XR-2100 used in a stand-alone configuration as selected by μC/$\overline{STD}$ = 0. The various modes of operation are selected by switches S1-S7.

The XR-2100 is shown in the XR-2400 schematic to provide the V.21 operation for a V.22 bis (2400BPS) modem. Here the XR-2401/XR-2402 chips support V.22 bis, V.22 and Bell 212A modes. The control for both the XR-2100 and XR-2401/XR-2402 come from the XR-2403B microcontroller. User-specified firmware can be added to drive the XR-2100.

Should your future application require combined V.21 and V.23 communications, the design shown in Figure 5 can be easily retrofitted with the pin-compatible XR-2321. By a simple drop-in replacement and one jumper modification, the resulting solution will support all four CCITT Standards (V.22bis, V.22, V.23 and V.21) providing "Quad" modem capabilities.

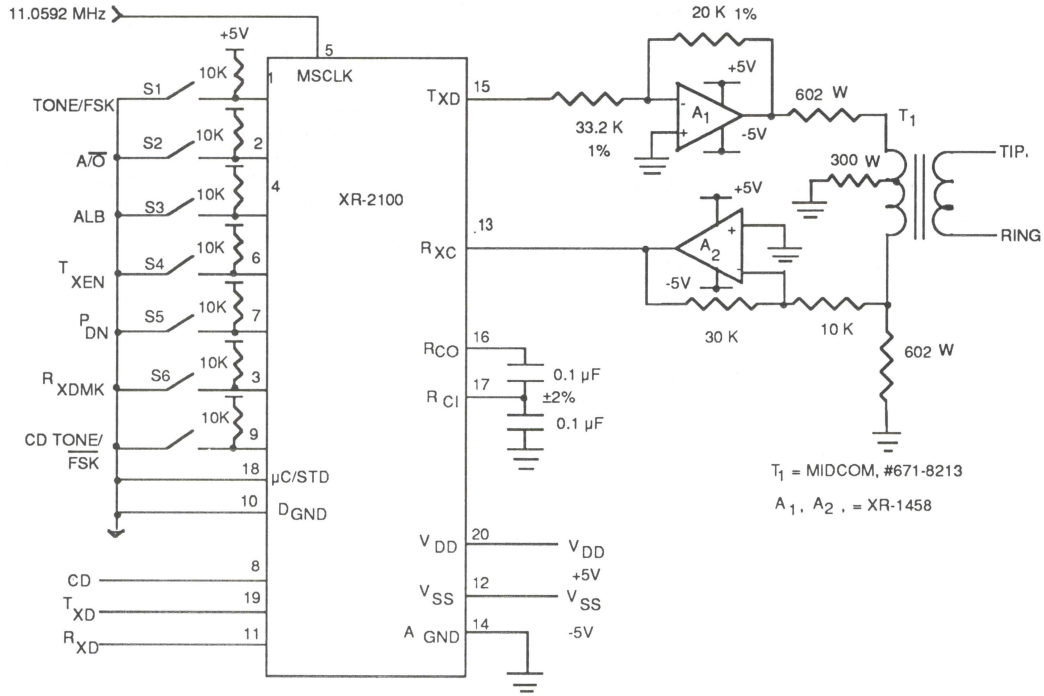
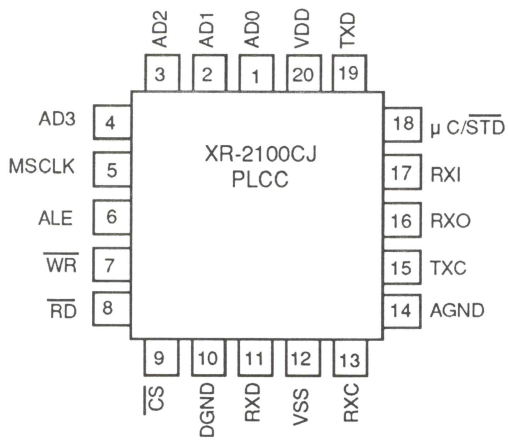


Figure 4. Standalone V.21 Modem With Serial Control



XR-2135A CCITT Data Buffer

GENERAL DESCRIPTION

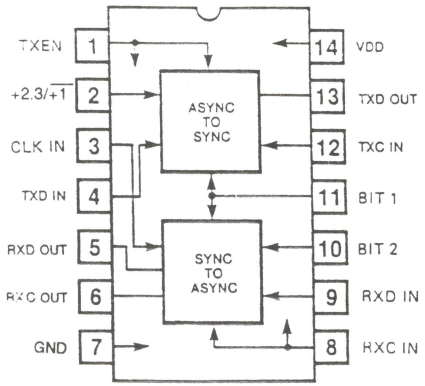
The XR-2135A is a digital circuit designed to perform the function of data buffering for various serial data systems, including modems. Both the asynchronous- to-synchronous conversion and the synchronous-to- asynchronous conversion are performed at data rates up to 19.2 kBPS. The XR-2135A is selectable for character lengths of 8, 9, 10 and 11 bits. A combined enable/disable input is supplied for the synchronous-to- synchronous and asynchronous-to-synchronous converter sections. This input allows the same data lines to be used for synchronous or asynchronous modes of operation.

The receive data buffer section (synchronous-to-asynchronous) accepts input synchronous data along with a receive clock and converts this to an asynchronous format. The transmit data buffer (asynchronous-to-synchronous) accepts on the input asynchronous data and will synchronize the data to a transmit clock. The transmit data input can accept data from -2.5% underspeed up to +2.3% overspeed in 8, 9,10 bit and 11 bit word modes. The +2.,3/+1* pin selects the overspeed capability. Automatic break extension is included in case of a break being received. The XR-2135A is constructed using polysilicon gate CMOS technology for low power and high speed operation. The master clock (CLK IN) can be clocked at speed up to 4.9152 MHz (19.2 kBPS data rate). The XR-2135A, available in a 14 pin package, is designed to operate with a single 5V supply.

FEATURES

Data Rates up to 19.2 kBPS
Asynchronous-to-Synchronous Conversion
Synchronous-to-Asynchronous Conversion
Independent Disable Inputs for Receiver and Transmitter Sections
Single 5 Volt Supply Operation
Underspeed and Overspeed capability of -2.5% to +1%or + 2.5% to +2.3%
Missing Stop bit detector
Break extended for transmitted data
Programmable Character Lengths of 8, 9,10 or 11 bits

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2135ACN	Ceramic	0°C to 70°C
XR-2135ACP	Plastic	0°C to 70°C

APPLICATIONS

Modem Data Buffers
Terminals
Data Communication Test Equipment

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3 to +7.0 V
Input Voltage	-0.3toVDD+0.3V
DC Input Current (any input)	±10 mA
Power Dissipation (Package Limitation)	250 mW
Storage Temperature Range	65°C to +125C

ELECTRICAL CHARACTERISTICS

Test Conditions: VDD = 5VDC ±5%, TA= 25°C, CLK IN = 307.2 KHz ± 0.01%,
Data Rate - 1200 BPS f_{TXC} IN = 1200 Hz f_{RXC} IN= 1200 Hz ±0.01%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
V_{OL}	Output Low Voltage			0.05	V	I_{OL}= 20 uA
V_{OH}	Output High Voltage	4.8	5.0		V	I_{OH}= -20 uA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
I_{OL}	Output Low Current	2	7		mA	
I_{OH}	Output High Current		-9	-400	uA	
I_{IN}	Input Leakage Current	-10	0	10	uA	
I_{DD}	Supply Current Quiescent		100	250	uA	CLK IN, TXCIN, RXC IN At 5VDC
AC CHARACTERISTICS						
t_{wstr}	Start Bit Width	819	821		uS	B1 = 1 B2 = 0 (10 bit)
BPS RANGE	Receiver Transmit	1170	1200	1212	BPS	8, 9, and 10 Bit Mode
f_{RXCO}	RXC OUTfrequency Multiplier	1.015			Hz/Hz	RXC OUT=1219 Hz

SYSTEM DESCRIPTION

The XR-2135A provides the complete interface between synchronous and character asynchronous formatted data systems. The synchronous side consists of two data lines TXD IN and RXD IN each with their respective clocks, TXC and RXC. Received data should change on the falling edge of RXC and be stable on the rising edge of RXC. The asynchronous-to-synchronous conversion handies data that is formatted so that the data bits or data and parity bits are bracketed by start and stop bits. Acceptable character lengths are 8, 9, 10 and 11 bits. The word length is pin selectable.

The XR-2135A is optimized for applications where a single clock is the source for the master clock (CLK IN), the TXDIN IN and RXC IN. The master clock (CLK IN) is 256 times the data rate. In modem applications, the RXC IN should be in lock with the received data, and jitter should be less than $\pm$30 ns. The asynchronous transmit data being clock in by an asynchronous clock at the data rate (CLK IN/256). The asynchrorious-to- synchronous converter when receiving overspeed data will shave on the stop bit. The break signal extended will detect a missing stop bit and extend this an additional character length and 3 bits.

PRINCIPLES OF OPERATION

The XR-2135A data buffer can be separated into three blocks: the asynchronous-to-synchronous converter for the transmitted data, the synchronous-to-asynchronous converter for the received data and the master dock divider.

The asynchronous-to-synchronous converter uses a two bit shift register to allow resetting of the stop bit to compensate for underspeed conditions.

A counter circuit, synchronized to the location of the stop start bit occurrence is used to control when the stop bit needs to be adjusted. An 11 bit shift register is used to monitor the data for the occurrence of a break signal.

The break extended is activated by the continuous reception of a series of logic 0s for one entire word's time (8, 9, 10 or 11 bits depending upon the setting of BIT 2 and BIT 1). When this oocurs, the synchronized register is reset, and 2 words + 3 bits of logic 0s are shifted out and appear at TXD OUT.

If 1% overspeed data is received, and the modem is selected for 8, 9, 10 or 11 bit word operation, the stop bit in the word will be increased in width. In the case of underspeed, the stop bit will be truncated, when the one bit shift register is reset. When the +2.3% mode is selected the operation remains the same, only a different timer is used to determine the location of the stop bit.

The enable pin, Pin 1, controls the bypassing of the asynchronous-to-synchronous converter and the synchronous-to-asynchronous converter. The bypass mode is buffered and the delay through the buffer is less than 30 ns.

The synchronous to asynchronous converter contains a 21 bit synchronous shift register and a 8,9, 10 or 11 bit programmable parallel loading asynchronous shift register also uses a stop-start bit detector. The difference is that a missing stop bit detector is needed for synchronous data that is received without a stop bit. When this occurs, the last stage of the asynchronous shift register is set, and a stop bit re-inserted. The asynchronous shift register is clocked at a rate that is 1.015 times the nominal data rate. For 1200 BPS, this is 1219. For 9600 BPS, the rate would be 9744 BPS.

The master clock divider takes the CLK IN and divides by 256 to provide the internal data clocks as well as producing various reset pulses to perform the functions described above.

PIN DESCRIPTIONS

PIN#	SYMBOL	DESCRIPTION
1	TXEN	Enable Input: This input when tied to a logic high permits the TXD IN to be clocked through the asynchronous-to-synchronous converter. When this input is tied to a logic low, the shift registers of the asynchronous-to-synchronous converter and synchronous-to-asynchronous converters are bypassed and both TXEN and RXD IN are buffered and connected.
2	+2.3/+1	Overspeed Enable Input: This input when tied to a logic high enables the asynchronus-to-synchronous converter to accept data at a rate from-2.5% to +1%. When disabled,

PIN#	SYMBOL	DESCRIPTION
3	CLK IN	Master Clock Input: This clock provides the asynchronous clocks and reset pulses used by the XR-2135 to perform the asynchronous-to-synchronous conversion as well as the synchronous to asynchronous conversion. The formula to use for determining the datarate is CLK IN / 256-data rate in BPS.
4	TXD IN	Transmit Data Input: The serial data should be applied to this pin. When 8, 9, or 10 bits are selected, the range for the data rate is -2.5% to +1%. This input has a high input impedance.
5	RXD OUT	Received Data Output: This is the asynchronous received data output (when TXEN is tied high). The data rate of this output is 1.5 times the synchronous data rate.
6	RXC OUT	Received Clock Output: This clock is synchronized with the RXD OUT. It should be noted that when stop bits are being inserted or deleted, the clock will produce a pulse at the time of the stop bit.being shifted out at RXD OUT.
7	GND	This pin should be tied to the digital ground of theXR-2135.
8	RXC IN	Receive Clock Input: The received clock synchronous with the received data should be tied to this pin. The acceptable litter is only $\pm$30ns relative to the data. The data should be stable on the rising edge of this clock and change on the failing edge. If the received data is bit asynhronous (no clock relative to the data) this pin does not have to be clock for the data to appear at RXD OUT if TXEN is at a logic low.
9	RXD IN	Received Data input: The synchronous data is applied to this pin.
10	BIT 2	Character Length Select:
11	BIT 1	These two digital inputs control the length of the word that will be applied to the XR-2135. Refer to Table 2 for the truth table of the function.
12	TXC IN	Transmit Clock Input: The system clock that the transmit data is to be synchronized to be tied to this pin. Note that this clock must be locked to the master clock CLK IN. Acceptatble variation is +0.01%. In many modem applications this is not a problem.
13	TXDOUT	Transnmit Data Output: This output provides the serial data synchronous to the clock applied to TXCIN if TXEN is at a logic high. In an underspeed situation, all bits will be shortened. In an over- speed situation, all bits will be widened. If TXEN is at a logic low this output will provide a buffered version the data at TXD IN. The amount of delay is 30 ns.
14	V_{DD}	Positive Supply: This input should be tied to 5 V $\pm$ 5%. A 0.1 µF decoupling capacitor should be adequate for decoupling any system noise to ground.

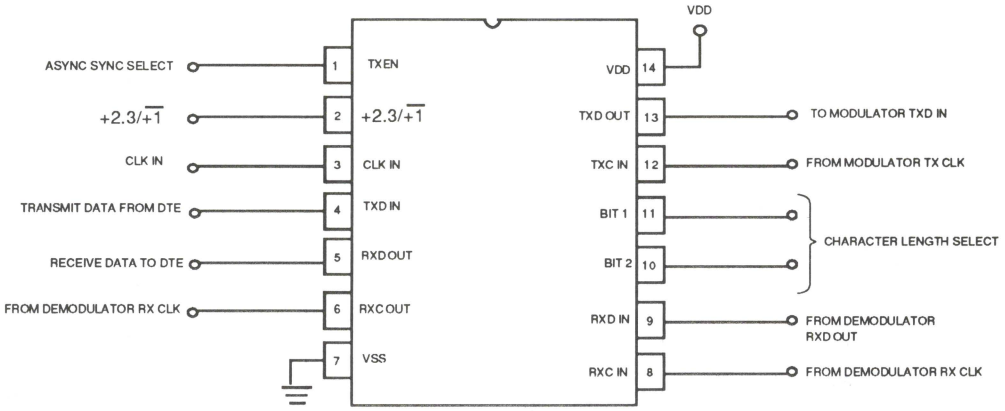
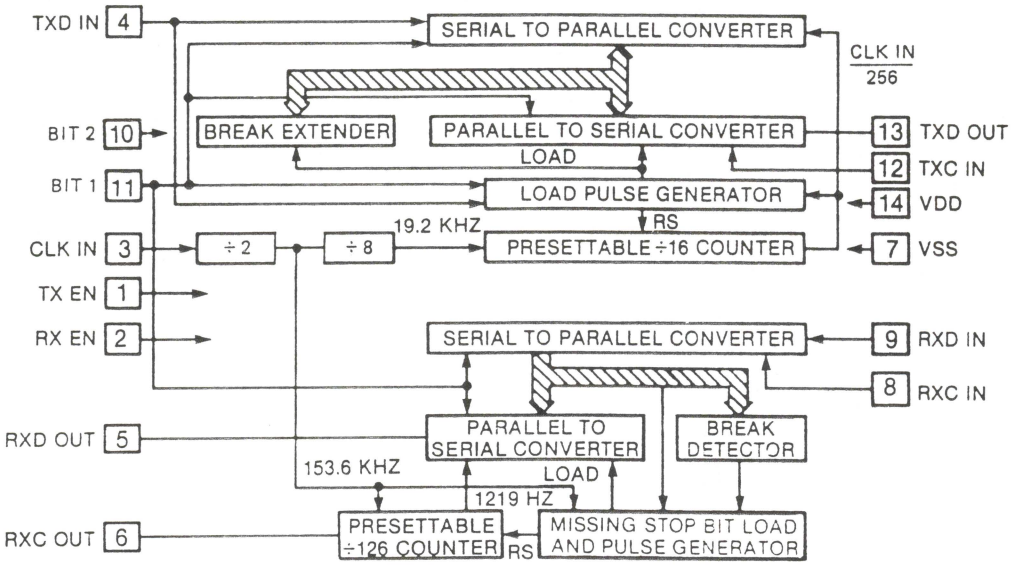


Figure 1. Test Circuit

BIT 1 (11)	BIT 2 (10)	CHARACTER LENGTH
0	0	8 Bit
0	1	9 Bit
1	0	10 Biit
1	1	11 Bit

Table 2. Character Length Selection



FREQUENCIES SHOWN ARE FOR 1200 BPS OPERATION,
CLK IN EQUALS 307.2 KHZ

Figure 2. Equivalent Schematic Diagram

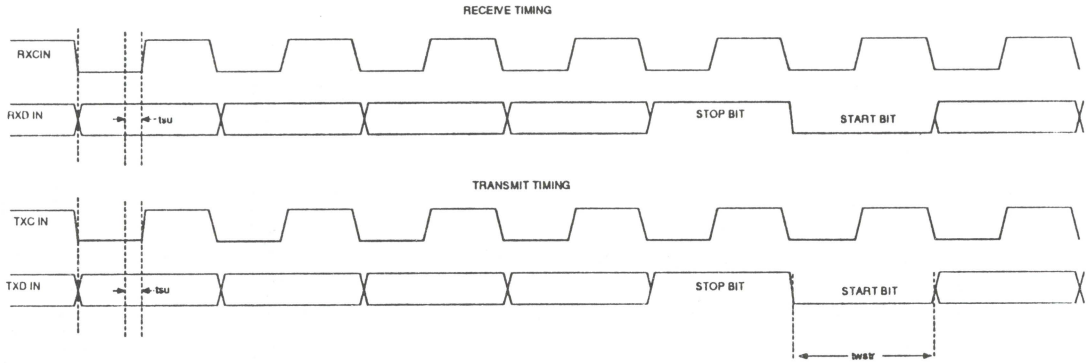


Figure 3. Transmit Receive Timing Characteristics

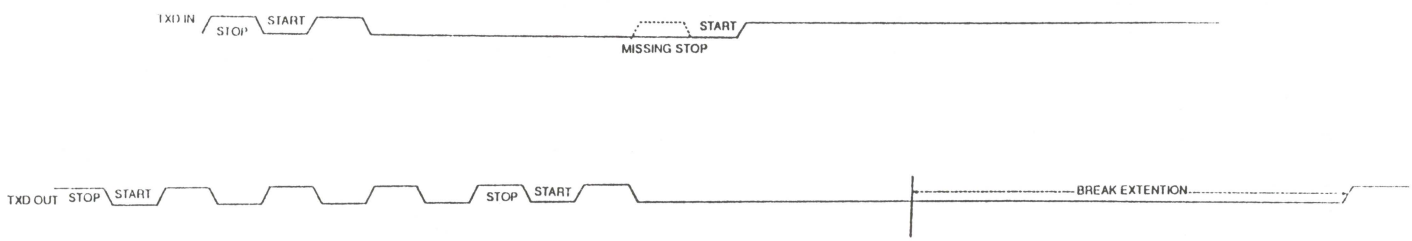


Figure 4. Break Extention and Data Delay Example at 8 Bit Word Length

V.23/V.21 Single Chip Modem

GENERAL DESCRIPTION

The XR-2321 is a single-chip asynchronous continuous phase FSK (Frequency Shift Keying) mode modem. Half or full duplex operation is possible over general switched network or leased line conditions. Modem functions and modes are selected through micro-controller bus structured interfaces. It is compatible with the CCITT recommended standards for V.21 and V.23 type modems.

The XR-2321 can be used with other higher speed Exar modem chips, such as the XR-2400 and XR-2900 chip sets in V.29/V.27ter/V.22bis/V.22/212A multi-modem application.

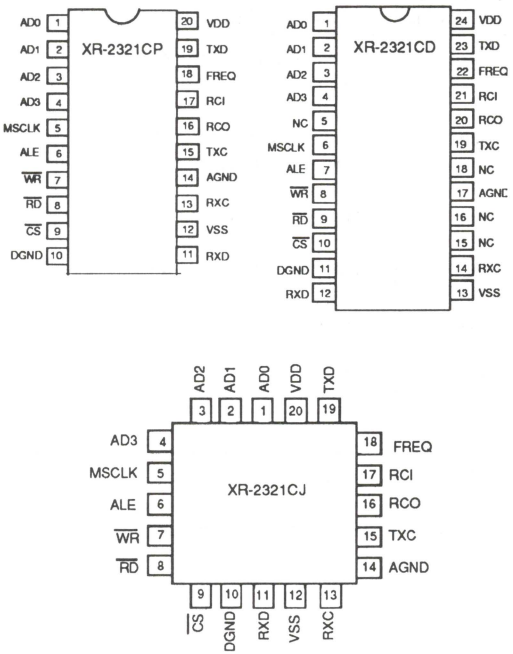
Switched capacitor techniques and CMOS technology are employed in the XR-2321 to perform all major filtering functions and modulation/ demodulation respectively. The 75 BPS back channel is also provided when it is selected in V.23 mode.

The XR-2321 is available in a 20 pin DIP or PLCC package. All the digital input and output signals are TTL compatible. Power supply requirements are +/-5 volts.

FEATURES

Dual FSK Modem Chip in a 20-Pin Package
CCITT V.21 (300 BPS Full Duplex) Compatible
CCITT V.23 (1200 BPS Half Duplex Mode 2)
Compatible, also with 75 BPS FSK Back Channel
No External Filtering Required
Analog Loop Back Test Mode
2 Wire Full Duplex for 300 BPS
2 Wire Half Duplex for 1200 BPS
Universal Microcontroller Interface
Low Power CMOS
Generator & Detector for Answer & Calling Tones
Power Down Mode
Line Equalizer Enable or Disable (Selectable)
XR-2100 Pin-to-Pin Compatible

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Power Supply	
VDD	-0.3 to 7V
VSS	0.3 to -7V
Input Voltage	VSS -0.3V to VDD +0.3V
DC Input Current	±10mA
Power Dissipation (Package Limitation)	
Plastic Dip	1W
Derate Above 25°C	
Plastic Dip	5mW/°C
Storage Temperature Range	-65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2321CP	Plastic	0°C to 70°C
XR-2321CJ	PLCC	0°C to 70°C
XR-2321CD	JEDEC SO	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^{\circ}C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $MS_{CLK} = 11.0592$ MHz $\pm 0.05\%$ unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	Positive Supply Current Power Down Mode		11 5		mA mA	
I_{SS}	Negative Supply Current Power Down Mode		12 5		mA mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4$ V
I_{OL}	Low Level Output Current			2	mA	
I_I	Input Current			50	µA	V1 = 0 to V_{DD}
TXC	Transmit Carrier Output	-2	0	+2	dBM	FSK Carrier
RXC	Receiver Dynamic Range	-43		-9	dBM	V.23 option with 1200 baud receive, and the back channel enabled for TX.
		-40		-9	dBM	V.23 option, with 1200 baud transmit and the back channel enabled for RX.
		-43		+10	dBM	V.21 option
CD Off	Carrier Detect Off Level		-48		dBM	FSK
CD On	Carrier Detect On Level		-43		dBM	FSK
CD_{HYS}	Carrier Detect Hysteresis	2	6		dB	FSK,1300 Hz,2100 Hz

SYSTEM PERFORMANCE Transmit Level = -10dBm*, Receive Level = -40dBM*
Conditions: Noise BW = 5KHz, C2, 3002, B/B Line Conditions, 511 PRBP

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V.21 MODE						
S/N	Signal-to-Noise Ratio		7		dB	BER < 10^{-5}
BIAS DIST	Bias Distortion		6 6		% %	ORIG Mode ANS Mode
V.23 MODE						
S/N	Signal-to-Noise Ratio		15		dB	BER <10^{-6} Primary Channel Receive Reverse Channel Transmit.
BIAS DIST	Bias Distortion		 7 7		 % %	Primary Channel ORIG Mode ANS Mode
S/N	Signal-to-Noise Ratio		7		dB	BER <10^{-5} Reverse Channel Receive Primary Channel Transmit
BIAS DIST	Bias Distortion		 5 5		 % %	Reverse Channel ORIG Mode ANS Mode

FREQUENCY PARAMETERS

Mode	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		FREQ Accuracy (Hz)
			Space (Hz)	Mark (Hz)	Space (Hz)	Mark (Hz)	
CCITT V.21 ORIG.	300	FULL	1180	980	1850	1650	+/-2
CCITT V.21 ANS	300	FULL	1850	1650	1180	980	+/-2
CCITT V.23 Primary	1200	HALF	2100	1300	2100	1300	+/-6
CCITT V.23 Reverse	75	HALF	450	390	450	390	+/-2

Answer Tone Frequency: 2100 Hz +/- 6Hz
** The level is measured at Tip and Ring with 600Ω load.*

PIN DESCRIPTIONS

Name	Pin #	I/O	Description
AD0 - AD3	1,2,3,4	I/O	Address/Data bus for microcontroller.
MSCLK	5	I	External master clock input of 11.0592MHz +/- .01%.
ALE	6	I	Address latch enable from microcontroller
$\overline{WR}$	7	I	Write Enable for microcontroller. Active Low.
$\overline{RD}$	8	I	Read Enable for microcontroller. Active Low.
$\overline{CS}$	9	I	Chip select. This enables the 4-bit parallel bus on the XR-2321.
DGND	10	I	Digital Ground. This pin should be routed separately from the AGND trace to the power supply.
RXD	11	O	Demodulated receive data output for V.21, V.23 main or reverse channel.
VSS	12	I	Negative power supply -5V +/- 5%. A 0.1µF ceramic bypass capacitor should be placed near the device.
RXC	13	I	Analog receive carrier input for V.21, V.23 or backward channel signal.
AGND	14	I	Analog Ground. This pin should be routed separate from DGND to the power supply.
TXC	15	O	Analog transmit carrier output for V.21, V.23 main or backward channel signal.
RCO, RCI	16,17	O/I	Receive filter output and demodulator input require 0.1µF +/- 10% ceramic capacitor connected between them.
FREQ	18	O	This pin provides a TTL compatible output of the signal received.
TXD	19	I	Transmit data input for V.21, V.23 main or reverse channel.
VDD	20	I	Positive power supply, +5V. A 0.1 µF ceramic bypass capacitor should be used for this pin.

PIN DESCRIPTION - for "CD" package

AD0-AD3	1,2,3,4	I/O	Address/Data bus for microcontroller.
NC	5,15,16,18	-	
MSCLK	6	I	External master clock input of 11.0592MHz ±0.01%.
ALE	7	I	Address latch enable from microcontroller.
$\overline{WR}$	8	I	Write Enable for microcontroller. Active Low.
$\overline{RD}$	9	I	Read Enable for microcontroller. Active Low.

Name	Pin#	I/O	Description
$\overline{CS}$	10	I	Chip Select. This enables the 4-bit parallel bus on the XR-2321.
DGND	11	I	Digital Ground. This pin should be routed separately from the AGND trace to the power supply.
RXD	12	O	Demodulated receive data output for V.21, V.23 main or reverse channel.
VSS	13	I	Negative power supply.
RXC	14	I	Analog receive carrier input for V.21, V.23 or backward channel signal.
AGND	17	I	Analog Ground. This pin should be routed separate from DGND to the power supply.
TXC	19	O	Analog transmit carrier output for V.21, V.23 main or backward channel signal.
RCO, RCI	20,21	O/I	Receive filter output and demodulator input require 0.1µF ±10% ceramic capacitor connected between them.
FREQ	22	O	This pin provides a TTL compatible limited output of the signal received.
TXD	23	I	Transmit data input for V.21, V.23 main or reverse channel.
VDD	24	I	Positive power supply, +5V. A 0.1µF ceramic bypass capacitor should be used for this pin.

FUNCTIONAL DESCRIPTION

As outlined in Figure 1, the XR-2321 consists of three main sections which perform the functions of transmitter, receiver and logic control.

Transmitter

The transmitter section consists of a Frequency Shift Keying (FSK) modulator, a Digital-to-Analog (D/A) converter, transmit filter, and an output gain stage. Its primary function is to convert binary digital data into a corresponding analog signal suitable for transmission on the telephone line system.

The binary data appears at the input of the FSK modulator at the TRANSMIT DATA (TXD) pin. The modulator creates a digitally synthesized sine wave at a given frequency depending on whether a logic 1 or logic 0 is present at the TXD pin. Following a digital filtering stage in the FSK modulator, this digital representation is converted into an analog signal by the DAC. The signal is then filtered by the transmit filter which is implemented using switched capacitor techniques. The resulting signal is finally smoothed using a continuous time low-pass filter and amplified by a programmable gain stage. The FSK-modulated carrier is then brought to the output TRANSMIT CARRIER (TXC) pin, and normally applied to the phone line through a Data Access Arrangement (DAA) interface or an acoustic coupler.

Receiver

The receiver consists of an anti-aliasing filter, a receive filter, a tone conditioner, a slicer, a FSK demodulator, a carrier detector, and a post-detection filter. Its function is to recover the binary digital information from the received analog signal.

The FSK-modulated carrier is received through a DAA or acoustic coupler and fed to the RECEIVE CARRIER (RXC) input pin. The signal is first presented to a simple low-pass anti-aliasing filter and then routed to both the receive band-pass filter and the tone conditioning section. This latter section provides a TTL compatible limited output of the received analog signal at the FREQUENCY OUTPUT (FREQ) output pin. Along the other route, the receive filter band limits the signal and passes it to the slicer section which creates a digital bit stream. This bit stream is processed by the FSK demodulator and passed through a post-detection filter. The resulting signal is squared off by the output comparator section whose output now represents the recovered data pattern. This is made available at the RECEIVE DATA (RXD) output.

A CARRIER DETECT (CD) signal is also generated from the received line carrier after the receive filter. The CD signal, which is used to indicate the presence of valid data, is read via the data bus by addressing the READ register of the XR-2321. Control programming information is discussed in the following section.

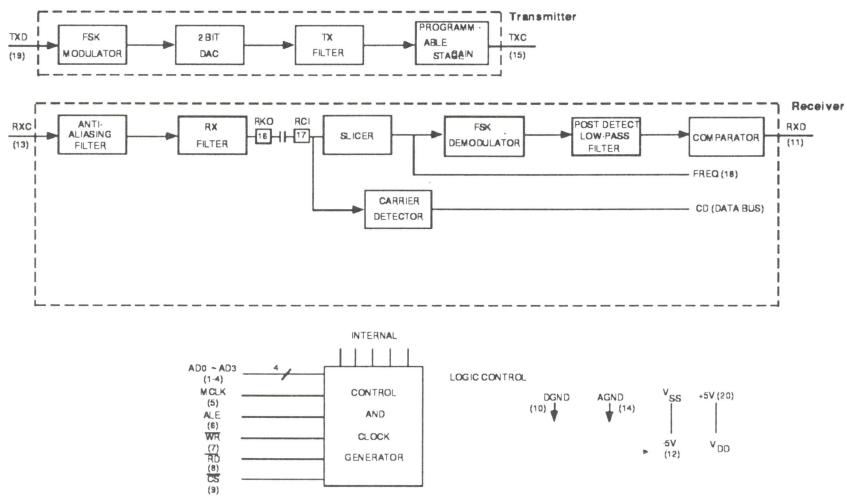


Figure 1. Functional Block Diagram

CONTROL PROGRAMMING INFORMATION

Operation of the XR-2321 is programmed via the read and write registers which are accessed by the AD0-AD3 pins. Control and mode configuration is acheived by writing control words into the appropriate write register, while status and data information can be read from the read register. Read/write register address locations are given in Table 1.

Register bit formats are shown in Table 2. By following the READ/WRITE cycle procedure outlined in Figure 2, the individual bits can be accessed. Figure 2 outlines the timing applicable to interfacing the XR-2321 with the 8031 or alike modem controllers.

Write Register Bit Description

ALB - Analog Loop Back

This bit will activate analog loop-back mode for diagnostic testing purposes.

RXDMK - Receive Data Mark

By setting this bit high, the user can force the RXD output pin high continuously. This is useful when performing functions such as handshaking protocol and/or CD is off.

A/O - Answer/Originate Mode

In the low state, this bit will configure the modem in originate mode and conversely, when set high, the modem will be in answer mode.

TONE/FSK - Transmit Tone or Transmit FSK Modulated Carrier

This bit controls the TXC output pin to transmit the 2100 Hz answer/ 1300 Hz calling tone when the bit is set high. When low, TXC will be the standard FSK-modulated carrier. (Note: TONE/DTMF = 1 for tone operation.)

TXD - Transmit Data

This bit is the data bit to be transmitted and is loaded via the data bus.

PDN - Power Down Mode
When selected, all sections of the device are powered off except for the control section. This mode allows for reduced power consumption when the modem is not receiving or transmitting.

TXEN - Transmitter Enable

When set low the transmitter output is disabled.

CPM - Call Progress Mode

This bit is set high when the modem is attempting call establishment in originate mode by monitoring dial tone, ring back tone or busy tone.

TONE/DTMF

With this bit set high, the transmitter will operate at tone frequencies corresponding to the given configuration. When set low, the transmitter is set to DTMF mode and follows the configuration programmed in the DTMF Bit Select register.

V.23/V.21

This configuration bit is to set the modem in V.23 or V.21 communications mode. V.23 is selected with this bit high, while V.21 is set with this bit low.

PTXD - Parallel Transmit Data

This bit allows the user to select whether data to be transmitted is loaded from the parallel data bus, or if it is to be loaded serially from the TXD pin. With PTXD set low, data is taken from pin 19 (TXD).

DTH3 - DTH2/DTL1 - DTL0 - DTMF Bit Select

These bits are used to set the DTMF frequencies to be transmitted. The bits are programmed according to Table 4 - DTMF Bit Selectable Table.

TX3 - TX0 - Transmit Gain Bit Select. Refer to Table 5 for gain selection.

Read Register Bit Descriptions

FREQ - Frequency Output

Reading from this bit is equivalent to pin 18 FREQ output. It provides a TTL version of the received analog signal.

CD - Carrier Detect

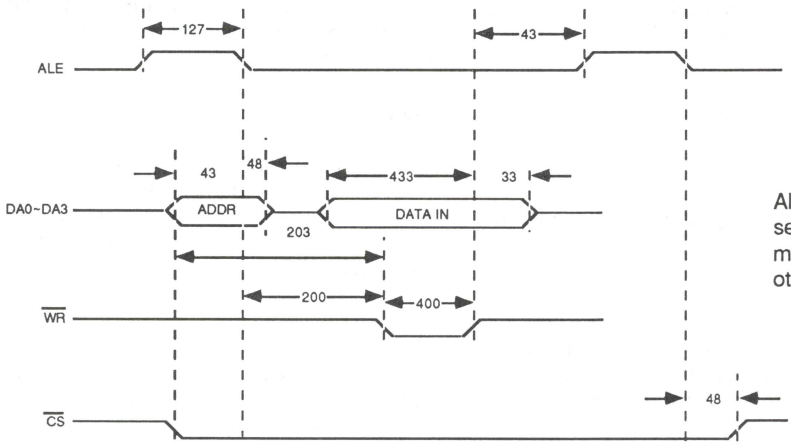
If this bit is high, it indicates the presence of a valid signal in the receive band.

RXD - Receive Data

Demodulated digital data is read from this bit. When data is read from this register, the RXD pin can be ignored.

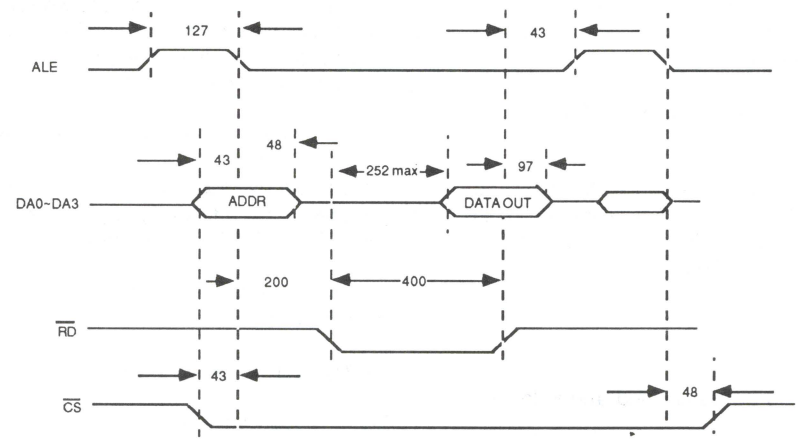
Mode Configuration Programming

Tables 3 to 5 detail the necessary bit register programming steps for each configuration mode, DTMF select and transmit carrier gain select levels respectively.



All units are in nano-seconds and are minimum values, unless otherwise specified.

Write Cycle



Read Cycle

Figure 2. Read/Write Timing Waveforms (12MHz Clock)

CONTROL REGISTERS FOR XR-2321

	ADDRESS BITS				
	AD3	AD2	AD1	AD0	HEX
$\overline{WR}$=0	1	0	0	0	(8)
	1	0	0	1	(9)
	1	0	1	0	(A)
	1	0	1	1	(B)
	1	1	0	0	(C)
$\overline{RD}$=0	1	0	0	0	(8)

Table 1. Read/Write Register Address Locations

	DATA BITS				
	BIT 3	BIT 2	BIT 1	BIT 0	ADDR
$\overline{WR}$=0	ALB	RXDMK	A/$\overline{O}$	TONE/$\overline{FSK}$	(8)
	$\overline{V.23}$ EQ	TXD	PDN	TXEN	(9)
	CPM	TONE/$\overline{DTMF}$	V23/$\overline{V21}$	PTXD	(A)
	DTH3	DTH2	DTL1	DTL0	(B)
	TX3	TX2	TX1	TX0	(C)
$\overline{RD}$=0	***	FREQ	CD	RXD	(8)

Table 2. Read/Write Register Bit Assignments

CONFIGURATION MODE BIT PROGRAMMING

D = Databit

FUNCTION	WRITE ADDRESS (HEX)	DATA BITS BIT 3	BIT 2	BIT 1	BIT 0
V.21 ORG mode, Transmit low and and receive high band.	8	0	0	0	0
	9	X	D	0	1
	A	0	X	0	0/1
V.21 ANS mode, Transmit high band and receive low band.	8	0	0	1	0
	9	X	D	0	1
	A	0	X	0	0/1
V.23 mode, Primary channel transmit and reverse channel receive.	8	0	0	0	0
	9	0/1	D	0	1
	A	0	X	1	0/1
V.23 mode, Reverse channel transmit and primary channel receive.	8	0	0	1	0
	9	0/1	D	0	1
	A	0	X	1	0/1
Transmit calling tone and prepare to detect calling tone energy.	8	0	X	0	1
	9	X	X	0	1
	A	0	1	X	X
Transmit answer tone and prepare to detect calling tone energy.	8	0	X	1	1
	9	X	X	0	1
	A	0	1	X	X
Transmit calling tone and receive CPM.	8	0	X	0	1
	9	1	X	0	1
	A	1	1	X	X
V.21 Analog loop back in originate mode.	8	1	0	0	0
	9	X	D	0	1
	A	0	X	0	0/1
V.21 Analog loop back in answer mode.	8	1	0	1	0
	9	0	D	0	1
	A	0	X	0	0/1
V.23 Primary channel analog loop back.	8	1	0	0	0
	9	0/1	D	0	1
	A	0	X	1	0/1

Table 3. Configuration Mode Programming

V.23 Reverse channel analog loop back.	8 9 A	1 X 0	0 D X	1 0 1	0 1 0/1
Read register. Pin 11 is clamped to "Mark" in V.21 mode.	8 9 A	X X 0	1 X X	X 0 0	X X X
Read register. Pin 11 is clamped to "Mark" in V.23 mode.	8 9 A	X X 0	1 X X	X 0 1	X X X
Power down mode.	8 9 A	X X X	X X X	X 1 X	X X X

Table 3 (Cont'd) - Configuration Mode Programming

DTMF BIT PROGRAMMING

WRITE ADDRESS	DATA BITS				TONE FREQUENCY		
	BIT3	BIT 2	BIT 1	BIT0	LOW	HIGH	
8 9 A	0 1 0	0 X 0	0 0 X	1 1 X			
B	0	1	1	1	941	1336	(0)
B	0	0	0	0	697	1209	(1)
B	0	1	0	0	697	1336	(2)
B	1	0	0	0	697	1477	(3)
B	0	0	0	1	770	1209	(4)
B	0	1	0	1	770	1336	(5)
B	1	0	0	1	770	1477	(6)
B	0	0	1	0	852	1209	(7)
B	0	1	1	0	852	1336	(8)
B	1	0	1	0	852	1477	(9)
B	0	0	1	1	941	1209	(*)
B	1	0	1	1	941	1477	(#)
B	1	1	0	0	697	1633	(A)
B	1	1	0	1	770	1633	(B)
B	1	1	1	0	852	1633	(C)
B	1	1	1	1	941	1633	(D)

Table 4. DTMF Programming

TRANSMIT GAIN BIT PROGRAMMING

WRITE ADDRESS	DATA BITS BIT 3	BIT 2	BIT1	BIT 0	OUTPUT TRANSMIT LEVEL (dBm)
C	0	0	0	0	-18.0
C	0	0	0	1	-16.8
C	0	0	1	0	-15.6
C	0	0	1	1	-14.4
C	0	1	0	0	-13.2
C	0	1	0	1	-12.0
C	0	1	1	0	-10.8
C	0	1	1	1	-9.6
C	1	0	0	0	-8.4
C	1	0	0	1	-7.2
C	1	0	1	0	-6.0
C	1	0	1	1	-4.8
C	1	1	0	0	-3.6
C	1	1	0	1	-2.4
C	1	1	1	0	-1.2
C	1	1	1	1	0

Table 5. Transmit Gain Programming

APPLICATIONS INFORMATION

1) Analog (AGND) and digital (DGND) grounds should be routed separately to the power supply. They should be single-point connected at the supply in order to minimize higher digital currents from interfering with the more sensitive analog sections.

2) Power supply pins should bypass as close as possible to the IC with a 0.1 µF ceramic capacitor.

In the XR-2400 modem schematic, the XR-2321 is shown integrated into a V.22bis/V.22 modem with the XR-2400 chip set.(For schematic, call the factory). The XR-2321 provides the V.23 and V.21 functions resulting in a quad modem solution. If the user is upgrading from a XR-2100 (V.21 single-chip modem) design, the circuit can be retrofitted with the pin-for-pin compatible XR-2321 by replacing the XR-2100 and removing the jumper on pin 18 (FREQ out).



NOTES



V.23/V.21 Single Chip Modem

GENERAL DESCRIPTION

The XR-2321A is a single-chip asynchronous continuous phase FSK (Frequency Shift Keying) mode modem. Half or full duplex operation is possible over general switched network or leased line conditions. Modem functions and modes are selected through micro-controller bus structured interfaces. It is compatible with the CCITT recommended standards for V.21 and V.23 type modems.

The XR-2321A can be used with other higher speed Exar modem chips, such as the XR-2400 and XR-2900 chip sets in V.29/V.27ter/V.22bis/V.22/212A multi-modem application.

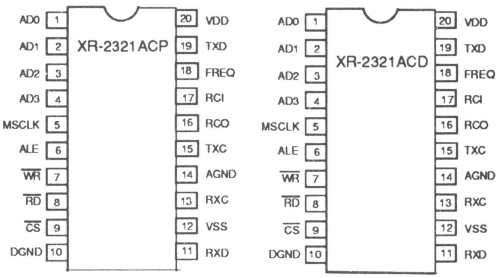
Switched capacitor techniques and CMOS technology are employed in the XR-2321A to perform all major filtering functions and modulation/ demodulation respectively. The 75 BPS back channel is also provided when it is selected in V.23 mode.

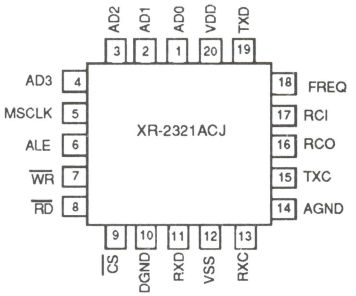
The XR-2321A is available in a 20 pin DIP or PLCC package. All the digital input and output signals are TTL compatible. Power supply requirements are +/-5 volts.

FEATURES

Dual FSK Modem Chip in a 20-Pin Package
CCITT V.21 (300 BPS Full Duplex) Compatible
CCITT V.23 (1200 BPS Half Duplex Mode 2) Compatible, also with 75 BPS FSK Back Channel
No External Filtering Required
Analog Loop Back Test Mode
2 Wire Full Duplex for 300 BPS
2 Wire Half Duplex for 1200 BPS
Universal Microcontroller Interface
Low Power CMOS
Generator & Detector for Answer & Calling Tones
Power Down Mode
Line Equalizer Enable or Disable (Selectable)
XR-2100 Pin-to-Pin Compatible
Carrier Detect Gain Control
DTMF High / Low Tone Difference Programmable
Call Progress Filter Selection
Adjustable Review Gain Control

PIN ASSIGNMENT





ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2321ACP	Plastic	0°C to 70°C
XR-2321ACJ	PLCC	0°C to 70°C
XR-2321ACD	JEDEC SO	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	
VDD	-0.3 to 7V
VSS	0.3 to -7V
Input Voltage	VSS -0.3V to VDD +0.3V
DC Input Current	±10mA
Power Dissipation (Package Limitation)	
Plastic Dip	1W
Derate Above 25°C	
Plastic Dip	5mW/°C
Storage Temperature Range	-65°C to +150°C



NOTES



V.22 bis Modem

GENERAL DESCRIPTION

The XR-2400 Chip Set is designed to provide the complete modem function for V.22 bis (2400 BPS) type modems. The chip set consists of the XR-2401 DSP Modem Signal Processor and the XR-2402A Analog Front End (AFE) with microcontroller interface. The XR-2400 set also supports Bell 212A (1200/300 BPS) and CCITT V.22 (1200 BPS) modes for a Bell/CCITT compatible system.

The XR-2401 is the heart of the system. It is a digital signal processor (DSP) based chip providing 300 BPS FSK, 1200 BPS DPSK, and 2400 QAM modulation and demodulation for the system. Other functions included are scrambler/descrambler, adaptive equalizer, carrier detection, DTMF tone generator, and AGC control.

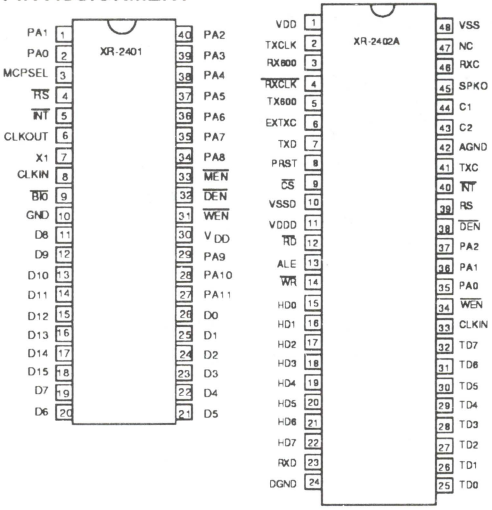
The XR-2402A provides the interface functions for the XR-2401, such as A/D and D/A converters for accessing the DSP chip inputs and outputs. Also provided are band splitting filters (SCF type), a programmable gain amplifier (PGA), asynchronous to synchronous and synchronous to asynchronous conversion, guard tone generation for CCITT applications, and a timing recovery.

Both the XR-2401 and XR-2402A are constructed with the Si-gate CMOS technology for low power operation. The XR-2401 is available in a 40 pin and the XR-2402A in a 48 pin package. The XR-2401 operates from a single +5 volt and XR-2402A from ±5 volt power supply.

FEATURES

2400 BPS (QAM), 1200 BPS (DPSK), 300 BPS (FSK) Operation
V.22 bis, V.22, 212A, 103 Compatible
DSP Based (XR-2401)
Bus Structured Control
No Adjustments
DTMF Dialing
Low Power CMOS (450 mw max.)
Adaptive Equalization
Asynchronous/Synchronous Operation
550 Hz/1800 Hz Guard Generation
Automatic Call Progress Monitoring
Upgradeable to MNP 5 Operation With the XR-2403B 5 microcontroller or V.42bis with the XR-2443 microcontroller

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2401CP	Plastic	0°C to 70°C
XR-2402ACP	Plastic	0°C to 70°C
XR-2401CJ	PLCC	0°C to 70°C
XR-2402ACJ	PLCC	0°C to 70°C
XR-2401CQ	QFP	0°C to 70°C
XR-2402ACQ	QFP	0°C to 70°C

For other pin assignments, refer to the end of this datasheet

APPLICATIONS

Stand Alone Modems
Internal Modems
Smart Modems
Laptop Applications

ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-2401	-0.3 to +7 V
XR-2402A	-7 to +7 V
Input Voltage	-0.7 to VDD + 0.3 V
DC Input Current (Any Input)	± 10mA
Power Dissipation (package limitation)	1 Watt
Storage Temperature Range	-65°C to +125°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
XR-2401 $f_{CLKIN} = 19.6608$ MHz ± 0.01%						
I_{DD}	Positive Supply Current	33	50	mA		
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	High Level Input Voltage	2.0			V	Except CLKIN
V_{IHC}	CLK High Level Input Voltage	0.56 V_{DD}			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			20	µA	$V_{OH} = V_{DD} - .4V$
				300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High Level Output Voltage	$V_{DD} - .4$			V	$I_{OH} = 20$ µA
		2.4			V	$I_{OH} = 300$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
XR-2402A $f_{CLKIN} = 4.9152$ MHz ± 0.01%						
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
VSS	Negative Supply Voltage	-5.5	-5.0	-4.5	V	
I_{DD}	Positive Supply Current		15	20	mA	
I_{DDS}	Positive Supply Current, Standby Mode		3	5	mA	
I_{SS}	Negative Supply Current			20	mA	
I_{SSS}	Negative Supply Current, Standby Mode			5	mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High level Output Voltage	2.4			V	$I_{OH} = 700$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
R_{XC}	Receive Carrier Range	-6		-45	dBm	(Using 6/16 dB RCVG feature)

SYSTEM DESCRIPTION

The XR-2401 / XR-2402A Modem Chip Set is designed to interface directly to popular microcontrollers, such as 8031. The microcontroller provides such functions as handshake control, smart functions such as "AT" commands, and dialing control. Exar provides a complete "AT" command set which can be used as is or modified.

The only other circuitry necessary is a line interface circuit (DAA) and RS-232 interface.

TRANSMITTER SPECIFICATIONS

All values are measured at TXC (Pin 41) of the XR-2402A with Bit 0-2 = 1 of CNTRL 0.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER POWER						
T_{XC} QAM	QAM/PSK Transmitter Power	-.6		+3.4	dBm	
T_{XC}550	CCITT Guard Tone Power	-1.7		-.4	dBm	
T_{XC}1800		-5.2		-3.4	dBm	
T_{XC} QAM/PSK 550	QAM/PSK Transmitter Power With Guard Tone	1.9			dBm	
T_{XC} QAM/PSK 1800		.8			dBm	
T_{XC} FSK	FSK Transmitter Power	-.16		+2.5	dBm	
T_{XC} AT	Answer Tone Power	1.6		2.9	dBm	
T_{XC} DTMF C	DTMF Tone Power Column	-4.9		-3.1	dBm	
T_{XC} DTMF R	DTMF Tone Power Row	-6.2		-4.4	dBm	
ΔT_{XC} DTMF	DTMF Amplitude Difference	-2		+2	dB	
SPEAKER						
AV SPKR	Gain - RXC to SPKO	4	6	8	dB	AV SPKR = 20 Log $\frac{V_{SPKO}}{V_{RXC}}$

SYSTEM PERFORMANCE

V_{RXC} = -40dBm 40, Originate Mode, 3002 Line Conditions, T_{XC} = -10dBm.

SYSTEM	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
S/N	Signal-to-Noise Ratio		16		dB	2400 BPS
			9		dB	1200 BPS
			12		dB	300 BPS
F_{OFF}	Frequency Offset		±10		Hz	2400/1200 BPS

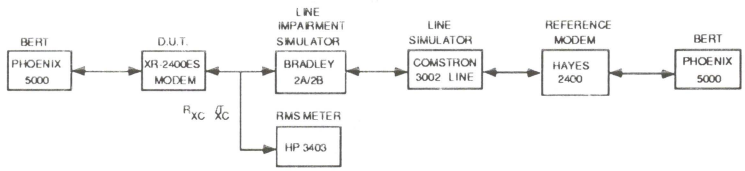
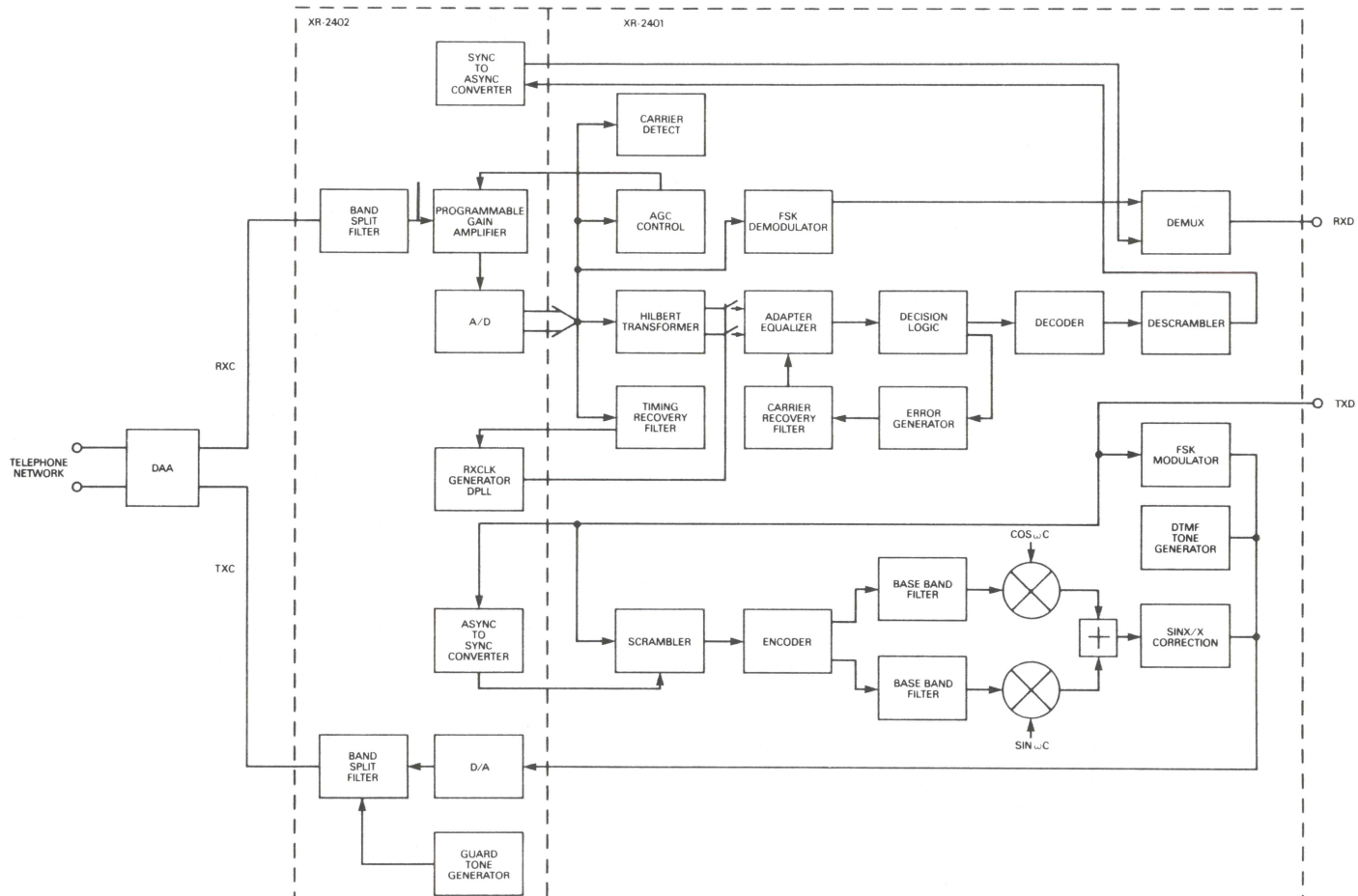
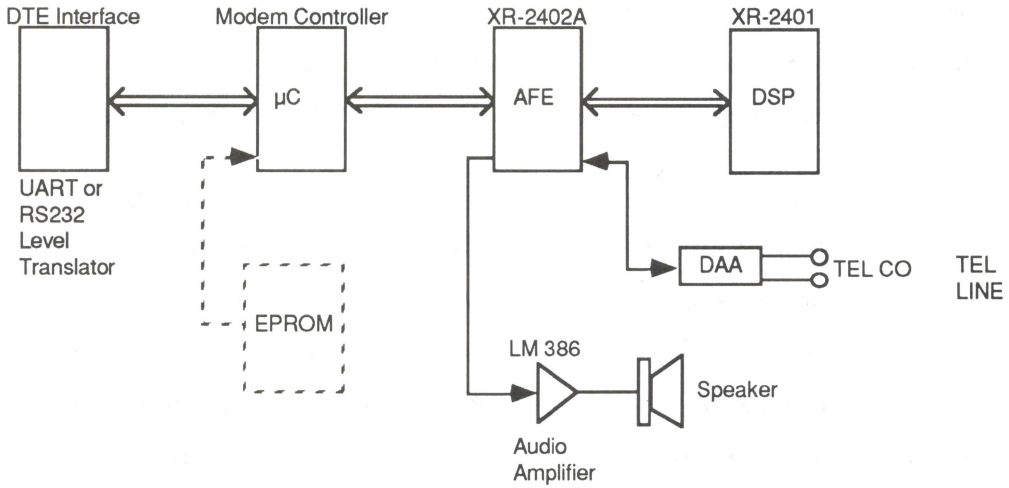


Figure 1. Performance Test Set-Up



XR-2400 Functional Block Diagram



XR-2400 Typical System Connection

PIN DESCRIPTIONS/FUNCTIONS

The XR-2401 and XR-2402A provide the heart of a V.22 bis modem system and when connected to a microcontroller such as the 8031 type, a complete system is formed. The XR-2402A provides the analog front end (AFE) function as well as the bridge, or interface, between the XR-2401 digital signal processor (DSP) and microcontroller.

The pin functions of the XR-2401 are as follows:

Symbol	I/O	Pin#	Description
V_{DD}	I	30	Positive supply Voltage +5V ±5%
GND	I	10	Ground connection - digital
$\overline{RS}$	I	4	Reset to initialize chip
X1	I	7	Crystal input 19.6608 MHz ±0.01%
CLK IN	I	8	Crystal input or external clock
CLK OUT	O	6	1/4 crystal/CLK IN frequency
PA0-PA11	O	1,2 27,29, 34-40	External address bus. I/O port address multiplexed over PA0-PA2
$\overline{BIO}$	I	9	External polling input for bit test and jump operations.
D0-D15	I/O	11-26	16 bit data bus
$\overline{DEN}$	O	32	Data enable indicates the XR-2401 accepting input data on D0-D15.
$\overline{INT}$	I	5	Interrupt input
MCPSEL	I	3	Mode select. 1 = microcomputer mode, 0 = microprocessor mode.
$\overline{MEN}$	O	33	Memory enable indicates that D0-D15 will accept memory instruction.
$\overline{WEN}$	O	31	Write enable indicates valid data on D0-D15.

The pin functions of the XR-2402A are as follows:

Symbol	I/O	Pin#	Description
VDD	I	1	Positive analog supply +5V ±5%
VSS	I	48	Negative analog supply -5V ±5%
VDDD	I	11	Logic positive supply +5V ±5%
VSSD	I	10	Logic negative supply -5V ±5%
DGND	I	24	Logic ground
AGND	I	42	Analog ground
PRST	I	8	Power on reset input
Microprocessor Interface			
ALE	I	13	Address latch enable
HD0	I/O	15	Address/data bus bit 0
HD1	I/O	16	Address/data bus bit 1
HD2	I/O	17	Address/data bus bit 2
HD3	I/O	18	Address/data bus bit 3
HD4	I/O	19	Address/data bus bit 4
HD5	I/O	20	Address/data bus bit 5
HD6	I/O	21	Address/data bus bit 6
HD7	I/O	22	Address/data bus bit 7
$\overline{CS}$	I	9	Chip select
$\overline{WR}$	I	14	Write strobe
$\overline{RD}$	I	12	Read strobe

XR-2401 Interface			
Symbol	**I/O**	**Pin#**	**Description**
CLK IN	I	33	4.9152MHz input from XR-2401
$\overline{INT}$	O	40	Interrupt flag for XR-2401
$\overline{RS}$	O	39	Reset output for XR-2401
PA0	I	35	I/O port address bus bit 0
PA1	I	36	I/O port address bus bit 1
PA2	I	37	I/O port address bus bit 2
$\overline{DEN}$	I	38	Read enable strobe
$\overline{WEN}$	I	34	Write enable strobe
TD0	I/O	25	Data bus bit 0
TD1	I/O	26	Data bus bit 1
TD2	I/O	27	Data bus bit 2
TD3	I/O	28	Data bus bit 3
TD4	I/O	29	Data bus bit 4
TD5	I/O	30	Data bus bit 5
TD6	I/O	31	Data bus bit 6
TD7	I/O	32	Data bus bit 7
RS232C Interface			
EXTXC	I	6	External transmit clock
TXCLK	O	2	Transmit clock output
TXD	I	7	Transmit data input
$\overline{RXCLK}$	O	4	Receive clock output
RXD	O	23	Receive data output, with pull-up resistor

Special Functions

TX600	O	5	Transmit 600 Hz output
RX600	O	3	Receive 600 Hz output
SPKO	O	45	Audio output to speaker

Analog Interface

TXC	O	41	Transmit carrier output
RXC	I	46	Receive carrier input
C1	O	44	Programmable gain stage output
C2	I	43	A/D input

SYSTEM OPERATION

The XR-2400 (XR-2401/2402A) is designed to interface with a host controller by both hardware and software. The XR-2400 looks like a memory mapped peripheral to the host controller. The XR-2402A acts as a bridge or interface between the XR-2401 DSP and host controller and thus, all control/status information will pass through it. Figure 2 shows the general data/address bus connection of the XR-2400 to the host controller.

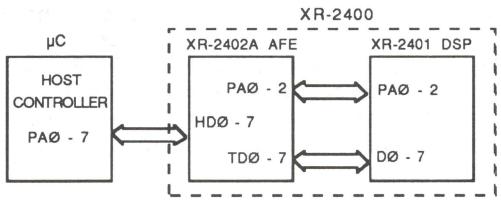


Figure 2. General Data/Address Bus Connection

The XR-2401 DSP performs all of the modem signal processing functions. While, the controller functions are left to the host microcontroller for system flexibility.

There are two kinds of control/status registers for the host microcontroller to access; one in the XR-2402A and one in the XR-2401 via the XR-2402A interface buffer. To the µc, the XR-2402A register looks just like an external data memory. The XR-2401 data memory must be accessed through the XR-2402A. The handshake procedure to access the memory map is shown in Table I.

Read	Write	XR-2402A
	0	Address register (8 bit latch)
	1	Write data register (8 bit latch)
2		Read data register (8 bit latch)
3		Status register in XR-2402A
	3	Control register in XR-2402A

Table 1. Memory Map for Host

GENERAL MODE SETTING READING INFORMATION FROM XR-2400

A handshake procedure is necessary for communication between the host microcontroller and XR-2400. All data (address, write data, read data) passes through a register in the XR-2402A with the procedure for controlling this register as follows:

Read Cycle

First, the host microcontroller will write a target address to the XR-2402A address register. Simultaneously, the XR-2402A will generate an interrupt for the XR-2401, which will branch to interrupt service routine and send data out to the XR-2402A reading register. This procedure takes 3 microseconds, thus, the host microcontroller needs to ensure it waits at least 3 microseconds from target address and reading data. (Refer to Figure 12)

Write Cycle

The write cycle is used for the host microcontroller to write to the XR-2400. Data is written first to the XR-2402A then the target address to the address register. It will generate interrupt for the XR-2401 and after a 6 microseconds delay, the XR-2401 will take the data from the write register. (Refer to Figure 12)

Read/Write Data Directly From the XR-2402A

There are two data memory locations which the host microcontroller can access immediately.

1. Status Register - Address 3

   Bit 3 - Bit 0 are copied from Control Register 7 in the XR-2401. Bit 6 - bit 4 are generated in the XR-2402A.

   Bit 0 R_{XDATA}
   Bit 1 Unscrambled R_{XDATA}
   Bit 2 Energy Detect
   Bit 3 Signal Quality Indicator
   Bit 4 S1 Signal Detector. With and S1 pattern coming in, Bit 4 will be continuously high allowing the user to access the coming S1 signal information.
   Bit 5 Dotting Pattern Detect Indicator. With an incoming dotting pattern (alternating etc.), this indicator will be high allowing the user to detect digital loopback.
   Bit 6 R_{XD} after Buffer. The user may access parallel R_{XD} through the data bus.

The following is an instruction example for the status register:

```
MOV     RO,#3 ;     Put #03 in RO
MOVX    A, @ RO;    Move external memory #03 to ACC.
```

2. Control Register

   Bit 0 Parallel TXD Input - This allows the user to input TXD through the parallel data bus.

   Bit 1 Software Reset for XR-2401 - Reset = "0" ; Normal Operation = "1". For prop er reset operation, a low must be present for at least 2 µs.

The following is an example of writing to the control register:

```
MOV     RO, #3   ; Put #03 in RO
MOVX @ RO, A     ; Move data from ACC
                   to external memory.
```

Modem Mode Selection Control

The XR-2401 data memory location #69 is used for mode selection as follows:

0	Idle Mode
1	FSK Mode
2	PSK Mode
3	DTMF Mode

Handshake Sequences

The XR-2400 chip set provides operating modes of 2400 BPS, 1200 BPS and 300 BPS to cover CCITT standards of V.22 bis and V.22 as well as Bell 212A and 103. The following figures illustrated the handshake sequences for automatic rate speed selection. Figure 3 shows the sequence for 2400 BPS (V.22 bis) with V.25 automatic answering. The following figures, 4 through 7, show the remaining handshake sequences needed to support other CCITT/Bell operating modes.

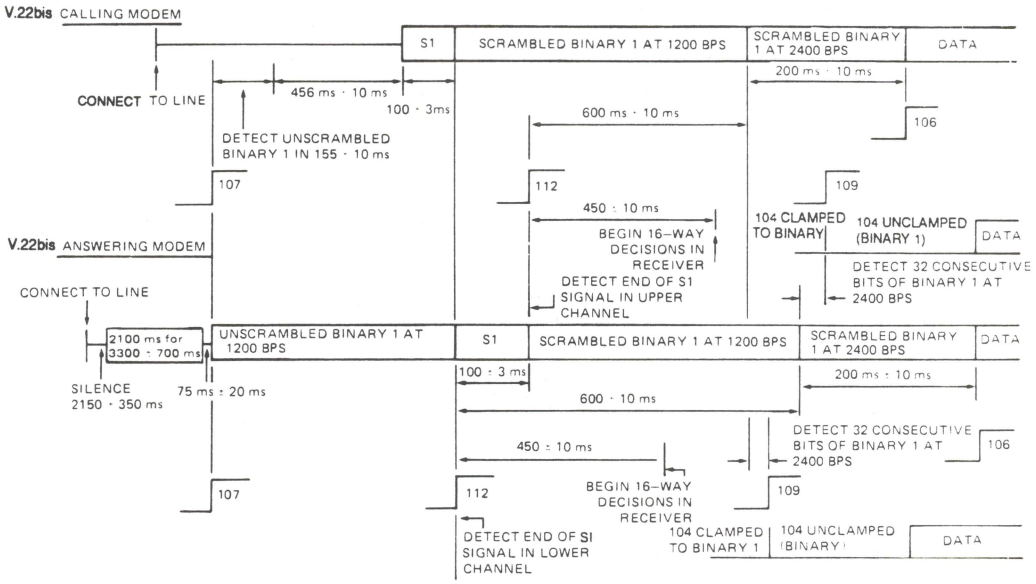


Figure 3. V.22 bis Handshake Sequence at 2400 BPS (with V.25 Auto Ans.)

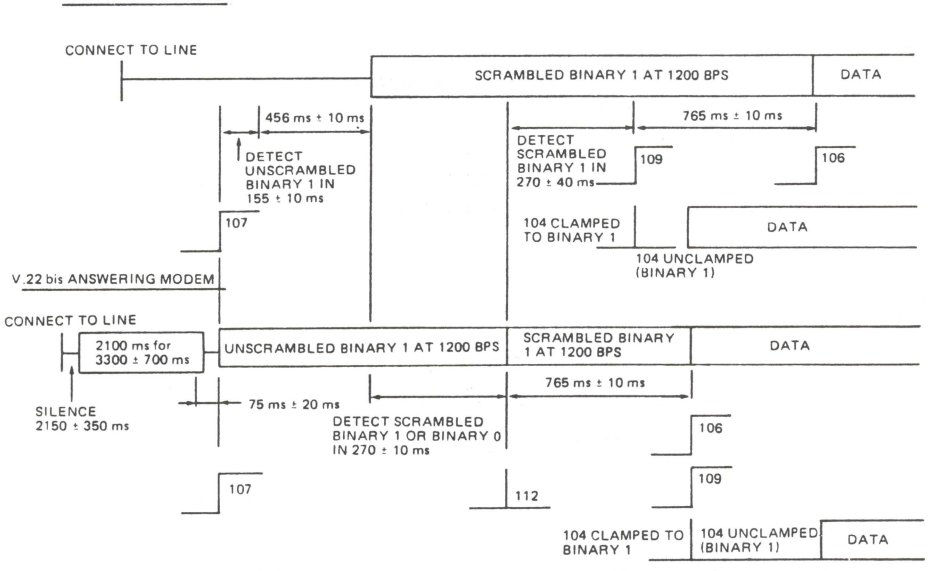


Figure 4. V.22 bis Handshake Sequence at 1200 BPS with V.22 Calling Modem (with V.25 Auto Ans.)

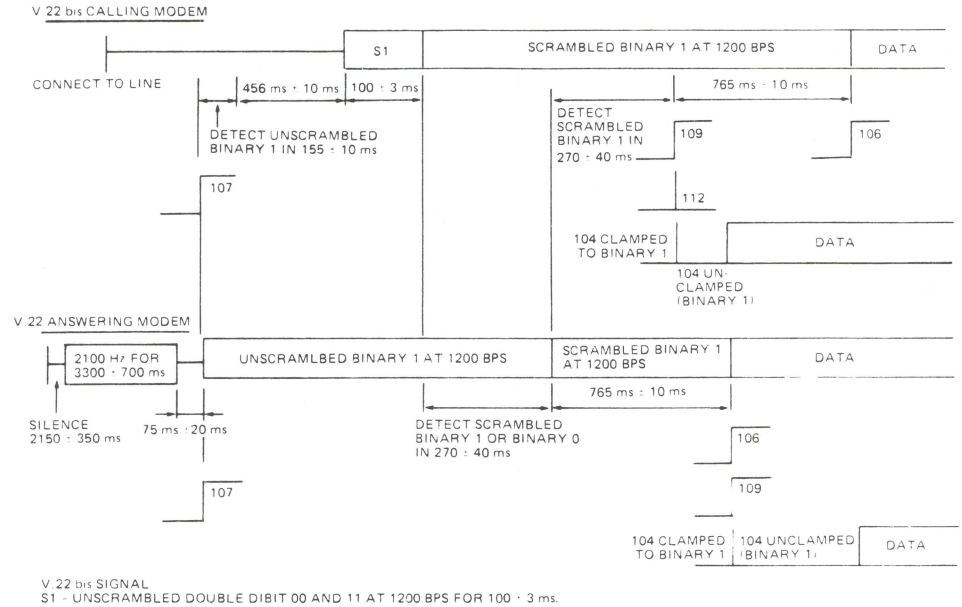


Figure 5. V.22 bis Handshake Sequence at 1200 BPS with V.22 Answering Modem (with V.25 Auto Ans.)

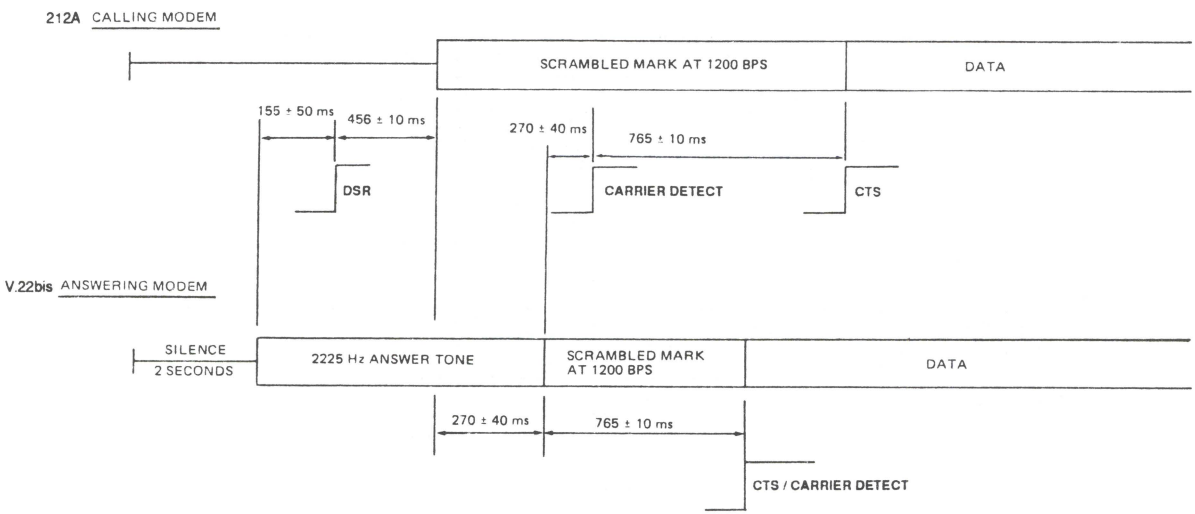


Figure 6. 212A Handshake Sequence at 1200 BPS with 212A Modem

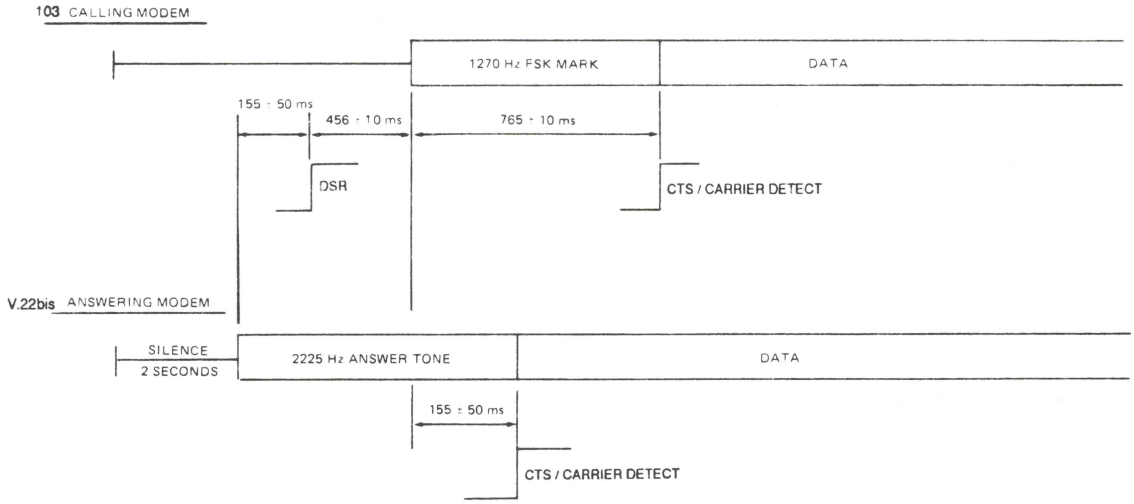
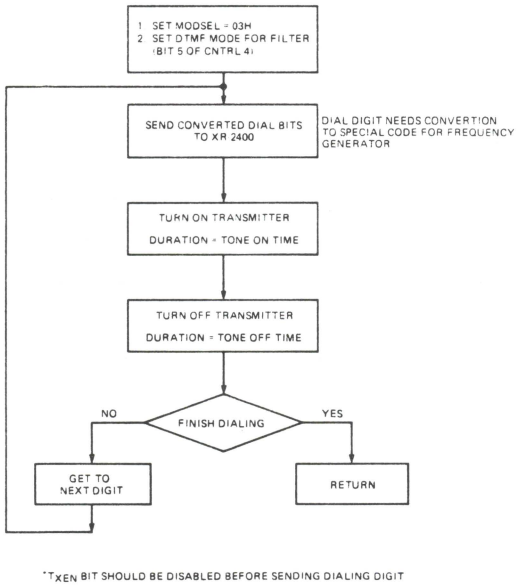


Figure 7. 103 Handshake Sequence at 300 BPS with 103 Modem

DTMF Generation

The XR-2400 provides an onboard DTMF generator which is controlled by the host microcontroller. The flow chart in Figure 8 illustrates the procedure for DTMF tone generation.



*T_{XEN} BIT SHOULD BE DISABLED BEFORE SENDING DIALING DIGIT

Figure 8. DTMF Generation Flow

Table 2 shows the digit/tone pairs for the DTMF generator.

Dial Digit	Encode D4	D3	D2	D1	Tone Pairs (Hz) Tone 1	Tone 2
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	770	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477
(B)	1	1	0	0	697	1633
(C)	1	1	0	1	770	1633
(D)	1	1	1	0	852	1633
(F)	1	1	1	1	941	1633

Table 2. DTMF Tone Pairs / Dial Digits

Call Progress Tone Monitor Operation

The host microcontroller uses the XR-2402A as a filter for call progress detection mode. When CPM = HIGH (enabled), the XR-2402A low band will be scaled down by a factor of 2.5 or 300-660 Hz. The ALB control bit provides the input for band connection to the carrier detect as shown in Table 3.

CPM = 1

ALB	Carrier Detect (CD) Connected to
0	High Band (2400 Hz)
1	Low Band (Scaled low band 300-660 Hz)

Table 3. CPM Frequency Band Assignments

The output of the CD circuit is monitored by the host microcontroller for duration and repetition rate to determine line status. The CD information is available by reading Bit 2 of CNTRL 7. The CD status is as follows:

CD = Energy Detect (direct access locations)
1 = Energy Detected
0 = No Energy

The MODSEL is set to FSK mode. After CPM mode, the microcontroller needs to send a reset signal to the XR-2401.
Table 4 indicates the various CD selections.

CPM	ALB	A/O	CD
1	0	0	Received high band; monitor answer tone.
1	1	0	Received low band filter scaled down by 2.5; monitoring dial tone, busy tone, and ring back tone.
0	0	0	Normal high band energy detect.
0	0	1	Normal low band energy detect.

Table 4. CD Frequency Band Assignments

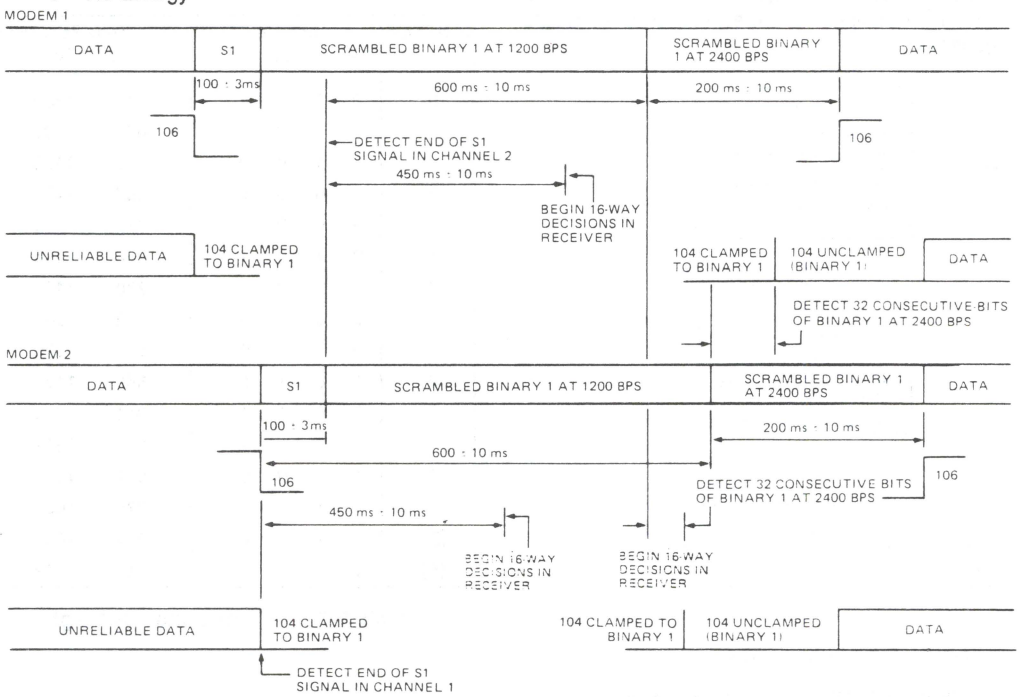


Figure 9. 2400 BPS Retrain Sequence

Signal Quality Indicator

The XR-2400 provides a signal quality indicator, SGQ, to indicate the quality of the received demodulated data. The state of this output is as follows:

SGQ Output:	
0	Good Signal
1	Bad Signal

The XR-2401 signal quality detector utilizes least mean square error method for error detection.

The XR-2400 provides the SGQ indicator for the host microcontroller. A counter is set up in the microcontroller, and if the value in it exceeds a preset value in a predetermined time, a request for retrain requirement will be given. The retrain sequence is shown in Figure 9.

Test Modes

ALB, Analog Loopback, is a test mode which is used for complete testing of the local modem. Figure 10 illustrates the basic signal flow.

The transmit carrier is looped back to the demodulator input, bypassing the receive filter. The demodulator is set to the transmit carrier frequency. Table 5 illustrates ALB selection for answer and originate.

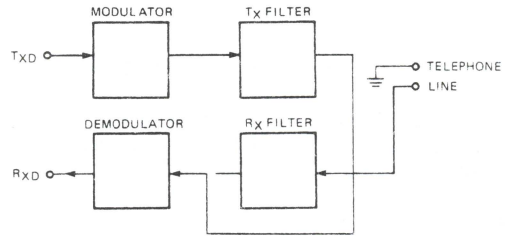


Figure 10. ALB Signal Flow

ALB = 1

MODE	T_X	R_X
ANS	Low Band	Low Band
ORIG	High Band	High Band

Table 5. ALB Frequency Assignments

RDLT, Remote Digital Loopback, is used to test the far-end or remote modem. The start of this type of loopback is automatically initiated by sending an unscrambled mark pattern, as seen in Figure 11. Also shown in Figure 11 is the carrier pattern for termination of RDLB.

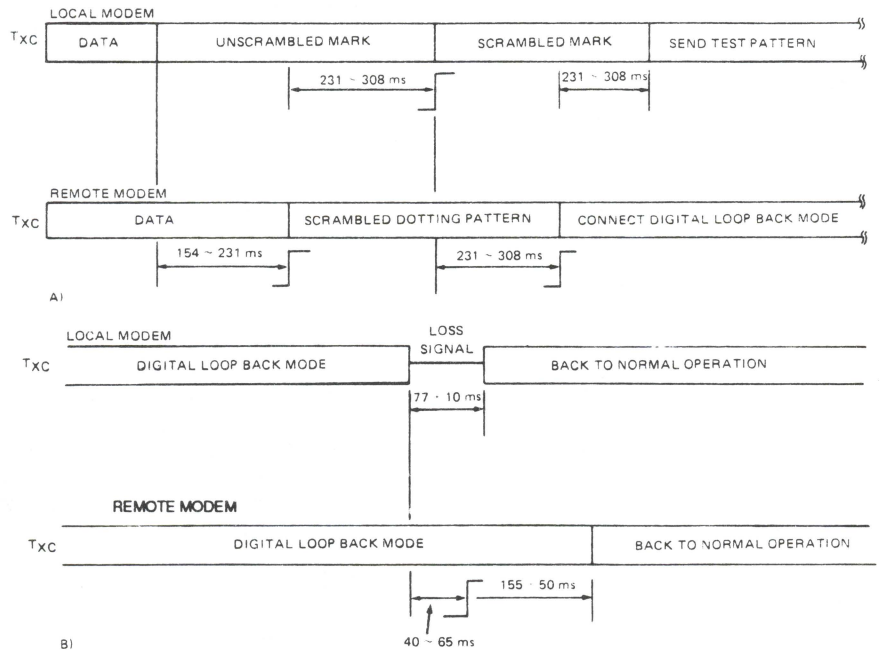


Figure 11. RDLB Initiation (A) and Termination (B)

XR-2400 / MICROCONTROLLER INTERFACING

The XR-2400 looks as a memory peripheral to a host microcontroller. The following indicates the address locations with bit functions of XR-2401 registers.

Location 60H - CNTRL 0

Bit	Description
0	TXL1
1	TXL2
2	TXL3
3	SPKR On / Off (O = Off)
4	TST1 (EXAR Special Test Mode)
5	TST2 (EXAR Special Test Mode)
6	SPKR1 Speaker Control LSB
7	SPKR2 Speaker Control MSB

Location 61H - CNTRL 1

0	OPTD
1	SP1
2	SP2
3	ETE
4	DLB
5	BC1
6	BC2
7	ASY

Bit 2	Bit 1	Bit 0	Transmit Level (±1 dB)
0	0	0	-10.5 dB
0	0	1	-9.0 dB
0	1	0	-7.5 dB
0	1	1	-6.0 dB
1	0	0	-4.5 dB
1	0	1	-3.0 dB
1	1	0	-1.5 dB
1	1	1	0

Bit 3	Speaker
0	OFF
1	ON

Bit 0	Async Data Rate
0	+1% to -2.5%
1	+2.3% to -2.5%

Bit 2	Bit 1	Receiver Speed
1	1	2400 BPS
0	1	1200 BPS
1	0	300 BPS

Bit 3	Transmit Clock
0	Internal
1	External

Bit 4	Bit Status	
0	Normal Data Mode	
1	Digital Loopback	TXCLK connect to RXCLK TXDATA connect to TXDATA

Bit 6	Bit 5	ASY Character Length
0	0	8 bit
1	0	9 bit
0	1	10 bit
1	1	11 bit

Bit 7	Mode
0	Synchronous
1	Asynchronous

Location 62H - CNTRL 2

0	TEN	Transmitter Enable (EN = 1)
1	SCR	Scrambler Enable (EN = 1)
2	64B	64 Bit Mark Sensor (EN = 1)
3	EQO	Adaptive Equalizer ON/OFF Control (ON @ 1)
4	EQT	Adaptive Equalizer T or T/2 Select (T/2 = 1)
5	VBS	Transmitter Shaping Select. 1 = CCITT 75% square root raised cosine 0 = Bell shaping
6	ANT	Answer Tone Selection (0=2225 Hz / 1 = 2100 Hz)
7	REQ	Equalizer Reset Control (RS = 0)

Location 63H - CNTRL 3

0	FL	Fast Locking Control (FL = 1). At the beginning of communication FL is set to 1 for fast DPLL response to the incoming signal.
1	CRD	RXD Clamp Control (RXD = 1 when CRD = 1)
2	TSP	Transmit Clock Select (2400 BPS = 1 / 1200 BPS = 0)
3	TST4	EXAR SPECIAL TEST MODE, set to 0 for normal operation.
4	PTD	Parallel TXD Input Selection (Parallel = 1). TXD will be taken from the µc data bus.
5	NTD	Normal Data Mode TXD from RS232 when (NTD = 1). 0: TXDATA will be taken from the selection of TC1, TC2.
6	TC1	
7	TC2	

Bit 7	Bit 6	TXC (NTD = 0)
1	1	Dotting Pattern used for DLB/Self Test
0	1	300 Hz, used to Generate S1 Pattern
1	0	Mark (ones)
0	0	Space (zeros)

Location 64H - CNTRL 4

0	PDM	Power Down Mode (PD=1). During power down mode, only the analog portion of the XR-2402A is disabled. The digital portion will still be active waiting for a control signal from the µc.
1	MOD	Answer/Originate Mode (Ans = 1)
2	GTE	Guard Tone Enable (GT=1)
3	GTS	Guard Tone Selection (1800 Hz = 1 / 550 Hz = 0)
4	RCVG	Receive Filter Gain (6dB = 1, 16 dB = 0)
5	DMFM	DTMF Mode Control (DTMF=1)
6	CPD	Call Progress Tone Detect Mode (CPT = 1)
7	ALB	Analog Loopback Enable (ALB = 1)

Location 65H - CNTRL 5

0	D1	Dial Digit 1
1	D2	Dial Digit 2
2	D3	Dial Digit 3
3	D4	Dial Digit 4
4	-	
5	-	
6	-	
7	-	

Location 66H - CNTRL 6 AGC Word

0	AG0	7 bits AGC control, each step is 0.375 dB
1	AG1	
2	AG2	
3	AG3	
4	AG4	
5	AG5	
6	AG6	
7	-	

Location 67H - CNTRL 7 Status Word

0	RXD	Receive Data
1	USD	Unscrambled Received Data
2	CD	Energy Detect
3	SGQ	Signal Quality Indicator

Location 69H - MODSEL

0	IDLE MODE
1	FSK MODE
2	PSK MODE
3	DTMF TONE MODE

A summary of control locations is given below in Table 6.

CNTRL	BIT 7	BIT 6	BIT5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CNTRL 0	-	TST3	TST2	TST1	SPC	TXL3	TLX2	TLX1
CNTRL 1	ASY	BC2	BC1	DLB	ETE	SP2	SP1	OPTD
CNTRL 2	REQ	ANT	VBS	EQT	EQO	64B	SCR	TEN
CNTRL 3	TC2	TC1	NTD	PTD	TST4	TSP	CRD	FL
CNTRL 4	ALB	CPDQ	DMFM	RCVG	GTS	GTE	MOD	PDM
CNTRL 5	-	-	-	-	DIAL DIGIT	DIAL DIGIT	DIAL DIGIT	DIAL DIGIT
CNTRL 6	-	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0
CNTRL 7	-	-	-	-	SGQ	CD	URXD	RXD

Table 6. Control / Status Locations

The following describes the read/write ports of the XR-2401 which is selected by PA0 ~PA2

Write Ports (WEN)

Port 0 Write to XR-2402A DAC D0-D7

Port 3 Write RXD to XR-2402A D0-RXD
D1 - Underscrambled RXD
D2 - CD
D3 - Equalizer Crash Indicator

Port 4 Write AGC Gain to XR-2402A/
Reset RX600 FLAG 6 D0 - D6

Port 5 Write PLL Information to XR 2402
D0 -Late/Early (L/E) Information

Port 6 Write Eye Pattern Information D0 - D15

Port 7 Write Data to XR-2402A D0 - D7

Read Ports (DEN)

Port 0 Read Status from XR-2401 and XR-2402A
D0 - RX9600 Hz Ready
D1 - TX9600 Hz Ready
D2 - RX600 Hz Ready
D3 - TXD Ready
D4 - RXD Ready
D5 - TX600 Hz Ready
D6 -
D7 - Write Register Ready

Port 1 Read Serial TXD from XR-2402A

Port 3 Read Converted Signal from A/D on XR-2402A D0 - D7

Port 4 Read Address Information from XR-2402A D0 - D7

Port 5 Read "Write Register" Data from XR-2402A D0 - D7

Port 6 Output Dummy to Reset TX600 Flag

The following illustrates the 8031 type microcontroller read/write of the XR-2401.

1. Read Target Address #60H in XR-2401:

```
MOV  A,#60H  ; Set up target address for XR-2401
MOV RO,#00   ; Set up RO for external memory
                 read
MOVX@RO,A ;  Move target address to address
                 register
             ; After this instruction will poll the
             ; interrupt for XR-2401
NOP          ; These NOP ensure there is 3 μs
NOP          ; for data setting
MOV RO,#02   ; Put #02 in RO
MOVX A,@RO;  Move data read data register
```

2. Write Data #AA to target Address #60H in XR-2401:

```
MOV A,#AA    ; Put desired data in accumulator
MOV RO,#01   ; Put #01 in RO
MOVX @RO,A ; Move #AA to write data register
MOV A,#60H   ; Move target address #60 to
               accumulator
MOV RO,#00   ; Put #00 in RO
MOVX @RO,A ; Move target address to address
               register
```

After 6 microseconds, the XR-2401 will take data from the XR-2402A to finish the write cycle.

Note: In order to maintain proper operation, there are some limitations on read/write access for the XR-2401. In normal operation (excluding idle mode), more than one access within 100 microseconds is not allowed.

Figure 12 illustrates the read/write data timing to the XR-2400.

APPLICATIONS INFORMATION

Figure 17 shows the XR-2401/XR-2402A in a complete stand alone V.22 bis modem. In this system, an 8031 type μC is used for providing the handshake and command set control. The 2764 EPROM would hold the command set, with the 373 necessary to interface the 8031 to the 2764.

Special attention should be followed in system grounding. The analog and digital grounds should be single point connected at the power supply.

Figure 18 shows XR-2401/XR-2402A in a complete internal V.22bis modem.

Signal Constellation Monitor Circuit

For system testing and evaluation, it is often instructive to evaluate the signal constellation of the modem. During design and testing, the constellation provides useful information on demodulation quality. The circuit in Figure 13 provides an output which can be displayed on an oscilliscope. The general characteristics of the signal constellation is illustrated in Figure 14.

SYSTEM PERFORMANCE

Test set-up conditions shown on page 3, Figure 1.

Data quality is illustrated in figures 15 and 16 for 2400 BPS and 1200 BPS operation.

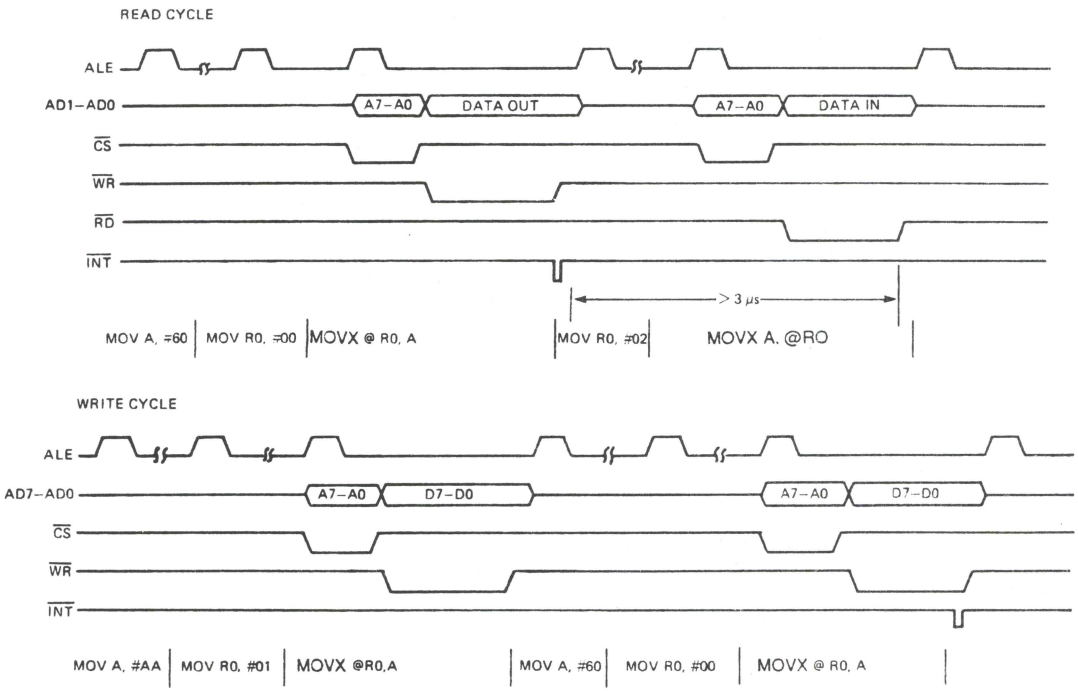


Figure 12. Timing for XR-2400 Read/Write Data

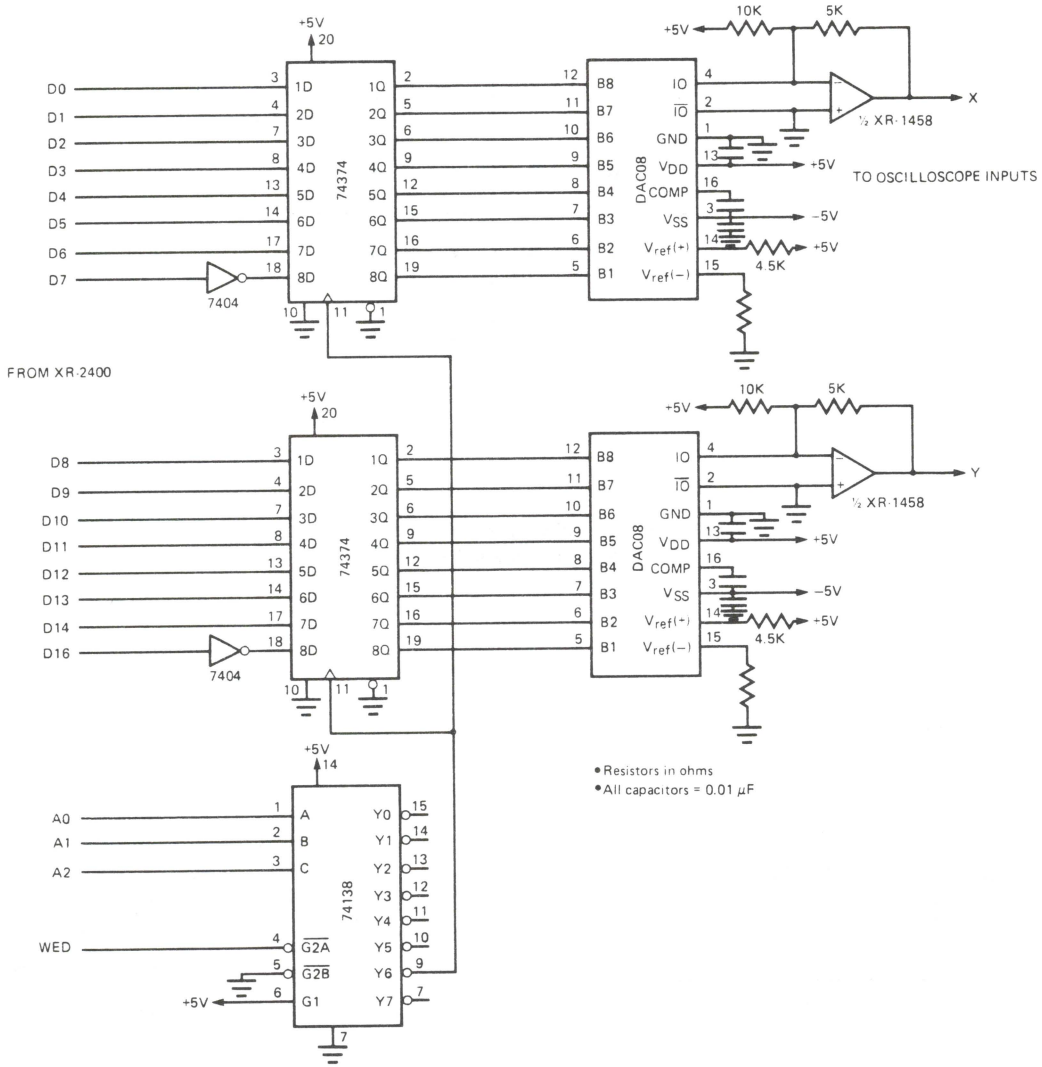


Figure 13. Signal Constellation Monitor

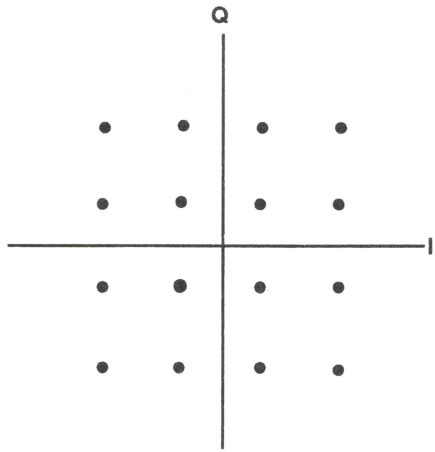


Figure 14. General Characteristics of 16 Point Constellation at 2400 BPS Q I

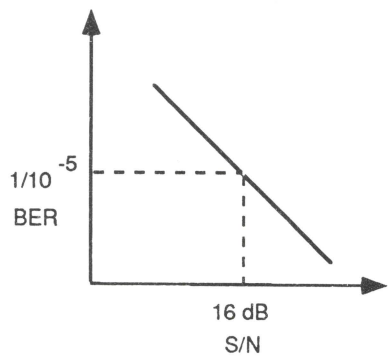


Figure 15. 2400 BPS BER vs. S/N

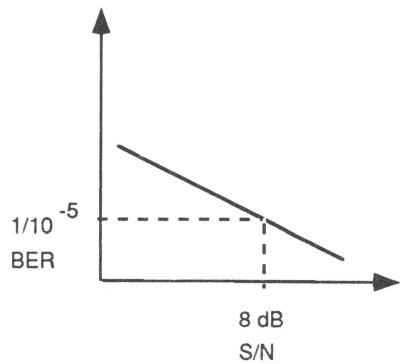
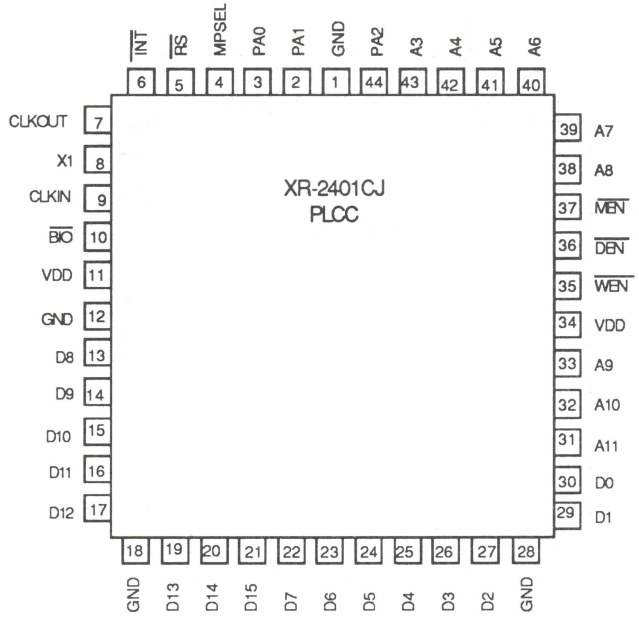
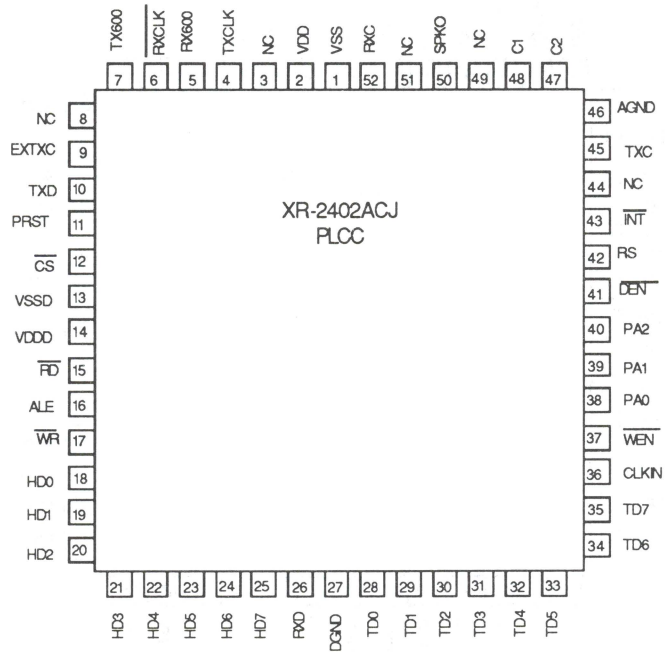
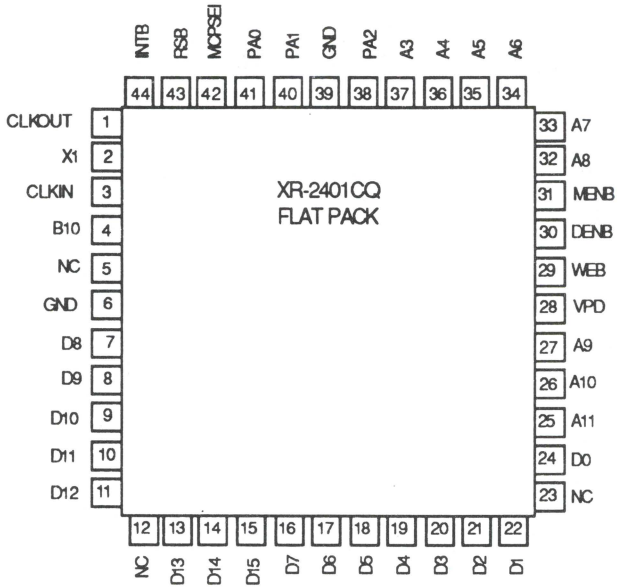
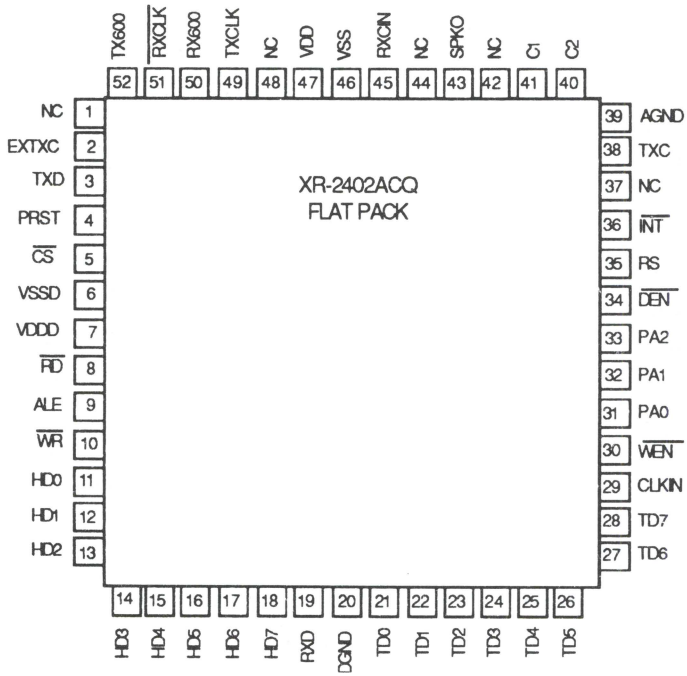


Figure 16. 1200 BPS BER vs. S/N


XR-2401CJ
PLCC
INT 6
RS 5
MPSEL 4
PA0 3
PA1 2
GND 1
PA2 44
A3 43
A4 42
A5 41
A6 40
CLKOUT 7
X1 8
CLKIN 9
BIO 10
VDD 11
GND 12
D8 13
D9 14
D10 15
D11 16
D12 17
39 A7
38 A8
37 MEN
36 DEN
35 WEN
34 VDD
33 A9
32 A10
31 A11
30 D0
29 D1
18 GND
19 D13
20 D14
21 D15
22 D7
23 D6
24 D5
25 D4
26 D3
27 D2
28 GND


XR-2402ACJ
PLCC
TX600 7
RXCLK 6
RX600 5
TXCLK 4
NC 3
VDD 2
VSS 1
RXC 52
NC 51
SPKO 50
NC 49
C1 48
C2 47
NC 8
EXTXC 9
TXD 10
PRST 11
CS 12
VSSD 13
VDDD 14
RD 15
ALE 16
WR 17
HD0 18
HD1 19
HD2 20
46 AGND
45 TXC
44 NC
43 INT
42 RS
41 DEN
40 PA2
39 PA1
38 PA0
37 WEN
36 CLKIN
35 TD7
34 TD6
21 HD3
22 HD4
23 HD5
24 HD6
25 HD7
26 RXD
27 DGND
28 TD0
29 TD1
30 TD2
31 TD3
32 TD4
33 TD5


XR-2401CQ
FLAT PACK
1 CLKOUT
2 X1
3 CLKIN
4 B10
5 NC
6 GND
7 D8
8 D9
9 D10
10 D11
11 D12
12 NC
13 D13
14 D14
15 D15
16 D7
17 D6
18 D5
19 D4
20 D3
21 D2
22 D1
23 NC
24 D0
25 A11
26 A10
27 A9
28 VPD
29 WEB
30 DENB
31 MENB
32 A8
33 A7
34 A6
35 A5
36 A4
37 A3
38 PA2
39 GND
40 PA1
41 PA0
42 MCPSEI
43 RSB
44 INTB


XR-2402ACQ
FLAT PACK
1 NC
2 EXTXC
3 TXD
4 PRST
5 CS
6 VSSD
7 VDDD
8 RD
9 ALE
10 WR
11 HD0
12 HD1
13 HD2
14 HD3
15 HD4
16 HD5
17 HD6
18 HD7
19 RXD
20 DGND
21 TD0
22 TD1
23 TD2
24 TD3
25 TD4
26 TD5
27 TD6
28 TD7
29 CLKIN
30 WEN
31 PA0
32 PA1
33 PA2
34 DEN
35 RS
36 INT
37 NC
38 TXC
39 AGND
40 C2
41 C1
42 NC
43 SPKO
44 NC
45 RXDIN
46 VSS
47 VDD
48 NC
49 TXCLK
50 RX600
51 RXCLK
52 TX600

V.22bis High Performance AFE

GENERAL DESCRIPTION

The XR-2402A High Performance AFE (Analog Front End) is designed to directly interface to the XR-2401 DSP Modem Signal Processor to provide the complete V.22bis 2400 BPS modem function. The XR-2401 is described in detail on the XR-2400 datasheet.

The XR-2402A is a redesigned, enhanced version of the XR-2402. While maintaining pin-to-pin compatibility with the XR-2402, the XR-2402A offers improved low signal level performance. Circuitry has also been added for speaker volume (during CPM) control under 'AT' command set control (ATL 0,1,2,3).

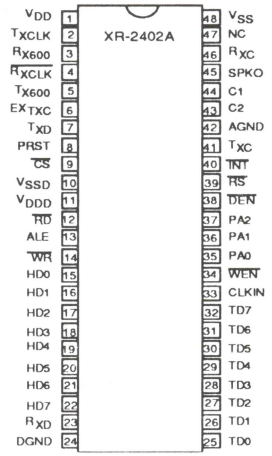
The XR-2402A provides analog interface functions to support the XR-2401 DSP such as, 8 bit D/A and A/D converters allow analog signals to get into and out of the digital XR-2401 DSP chip. Also included are band splitting filters (SCF type), a programmable gain amplifier (PGA), synchronous to asynchronous and asynchronous to synchronous conversion, guard tone generation (CCITT Operation), and timing recovery circuitry.

The XR-2402A is constructed with Si-Gate CMOS technology for low power operation. The XR-2402A is available in a 48 pin DIP or 52 pin PLCC package, and operates from ±5 Volt power supplies.

FEATURES

(When used with the XR-2401 DSP)
Pin-to-Pin Compatible with XR-2402
Improved Low Level Performance (Compared to XR-2402)
2400 BPS (QAM), 1200 BPS (PSK), 300 BPS (FSK) Operation
V.22bis, V.22, 212A, 103 Compatible
Bus Structure Control
DTMF Control
Low Power CMOS (110 mw typ)
Power - Down Mode
Asynchronous / Synchronous Operation
Speaker Volume Control Via Control Register
MNP 5 Operation with XR-2403/B
V.42 Upgradeable with XR-2442
V.42bis Upgradeable with XR-2443

PIN ASSIGNMENT



(Please see last page for PLCC and QFP packages)

APPLICATIONS

Stand-alone Modems
Internal Modems
Laptop Applications
Low Power Applications

ABSOLUTE MAXIMUM RATING

Power Supply	
VDD	-0.3 to +7V
VSS	+0.3 to -7V
Input Voltage	VSS -0.3V to VDD +0.3V
DC Input Current (Any Input)	±10 mA
Power Dissipation **(Package Limitation)**	1 Watt
Storage Temperature Range	-65°C to +125°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2402ACP	40 Pin Plastic Dip	0°C to 70°C
XR-2402ACJ	52 Pin Plastic PLCC	0°C to 70°C
XR-2402A	52 Pin QFP	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = -5V \pm 5\%$, $f_{CLKIN} = 4.9152$ MHz ±0.01%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Positive Supply Voltage	4.75	5.0	5.25	V	
V_{SS}	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
I_{DD}	Positive Supply Current		11	20	mA	
I_{DDS}	Positive Supply Current Standby mode		3	5	mA	
I_{SS}	Negative Supply Current		11	20	mA	
I_{SSS}	Negative Supply Current		3	5	mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High Level Output Voltage	2.4			V	$I_{OL} = 700$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
R_{XC}	Receive Carrier Range	-45		-6	dBm	Using 6/16 dB gain feature measured at tip and ring of Figure 2. RCVG feature (Pin 46 is 3 dB higher than tip and ring)
Speaker Controlled by Bits 6 and 7 of Location 60H - CNTRL 0						
AVSPKR	Gain - RXC TO SPKO					$AVSPKR = 20 \text{ Log } \frac{VSPKO}{VRXC}$
						BIT 7 BIT 6
AVSPKR 1		4	6	8	dB	0 0
AVSPKR 2		-5	-3	-1	dB	0 1
AVSPKR 2		-5	-3	-1	dB	1 0
AVSPKR 3		-14	-12	-10	dB	1 1

TRANSMITTER SPECIFICATIONS

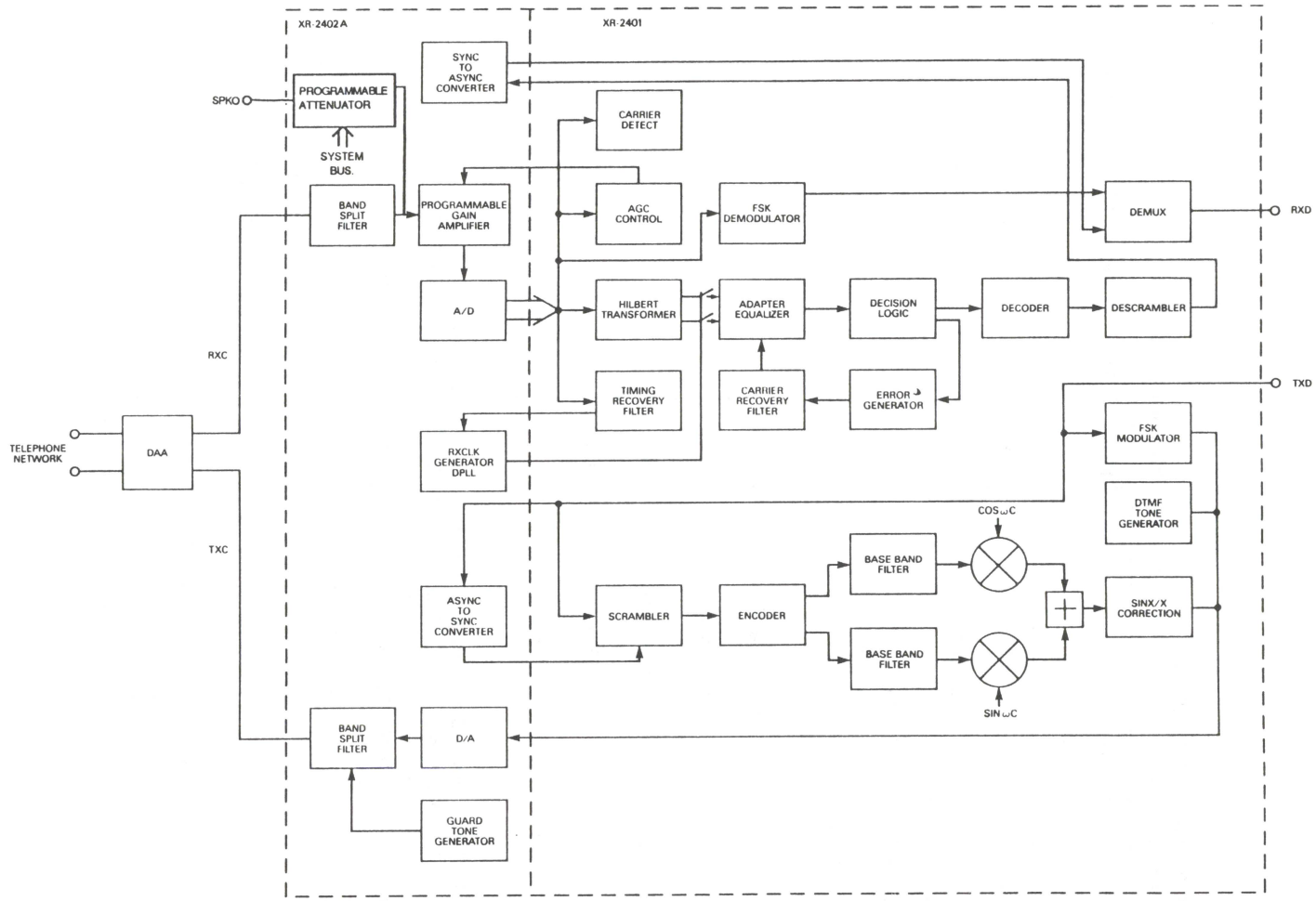
All values are measured at TXC (Pin 41) of the XR-2402A with Bit 0-2 = 1 of CNTRL 0.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER POWER						
T_{XC} QAM/PSK	QAM/PSK Transmitter Power	-.6			dBm	
T_{XC} 550	CCITT Guard Tone Power	-1.7		-.4	dBm	
T_{XC} 1800		-5.2		-3.4	dBm	
T_{XC} QAM/PSK 550	QAM/PSK Transmitter Power With Guard Tone	1.9			dBm	
T_{XC} QAM/PSK 1800		-.8			dBm	
T_{XC} FSK	FSK Transmitter Power	-.16		2.5	dBm	
T_{XC} AT	Answer Tone Power	1.6		2.9	dBm	
T_{XC} DTMF C	DTMF Tone Power Column	-4.9		-3.1	dBm	
T_{XC} DTMF R	DTMF Tone Power Row	-6.2		-4.4	dBm	
ΔT_{XC} DTMF T	DTMF Tone Power Twist	-2		2	dB	

SYSTEM PERFORMANCES (Performance Test Set-up Shown in Figure 1)

VRXC= -40 dBM, Originate Mode, C2, 3002, or B/B Line Conditions, TXC = -10 dBm.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
S/N	Signal-to-Noise Ratio		16		dB	2400 BPS
			9		dB	1200 BPS
			12		dB	300 BPS
FOFF	Frequency Offset		±10		Hz	2400/1200 BPS
R_{XC} Min	Minimum Receive Carrier Carrier Level For Error Free Operation		-45		dBm	2400 BPS



XR-2400A Functional Block Diagram

SYSTEM DESCRIPTION

The XR-2402A offers additional features and performance enhancements over the original XR-2402, such as those listed below:

	XR-2402A	XR-2402
Speaker Volume Control	Internal	External Latch and 2 transistors
Minimum Receive Level for Error-Free Operation	-45dBm	-43dBm
Typical Power Consumption	110 mw	160 mw

MICROCONTROLLER OPTIONS

The XR-2402A, when used with the XR-2401 modem DSP (See XR-2400 Datasheet for details) forms the complete V.22bis modem data pump function.

The XR-2402A/2401 pair, requires a modem controller for supporting intelligent functions such as Hayes 'AT' command control, error correction and data compression.

The XR-2402A has been designed with a very flexible interface to accommodate various common microcontrollers. Exar provides a number of different options and programs to minimize the design cycle. In each case, production worthy, commented source code is provided for use as is or for user customization to individualize each particular design.

Refer to Figure 3 for general connection.

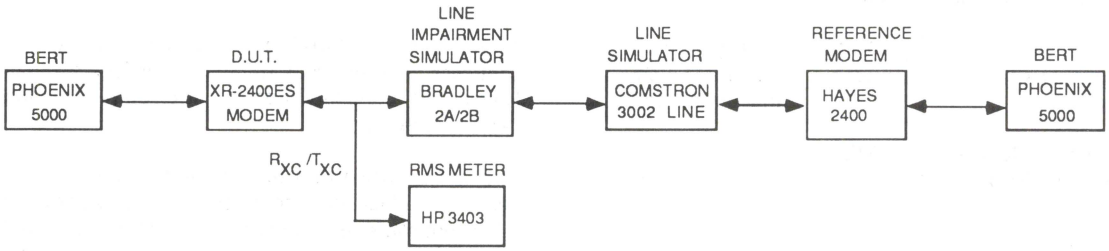


Figure 1. Performance Test Set-up

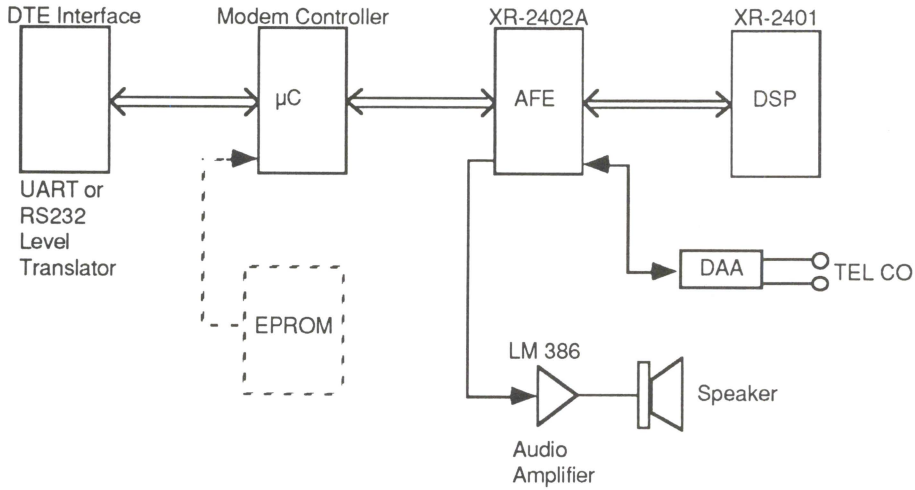


Figure 2. Typical Sytem Connection

APPLICATIONS INFORMATION

Detailed descriptions and operation of the XR-2402A may be found on the XR-2400 datasheet which describes the pin-to-pin and functionally equivalent XR-2402. The information provided here is additional.

Speaker Volume Control

The XR-2402A provides a complete digitally controlled, three level, speaker driver. The control for the driver is located in:

Location 60H - CNTRL 0	
Bit	**Description**
0 TXL1	
1 TXL2	
2 TXL3	
3 SPKR	On/Off (O = Off)
4 TST1	(Exar Special Test Mode)
5 TST 2	(Exar Special Test Mode)
6 SPKR 1	Speaker Control LSB
7 SPKR 2	Speaker Control MSB

The output levels relative to command / logic levels are:

Gain From RXC (P46) to SPK0		Bit 7	Bit 6
6 dB	±3 db	0	0
-3 dB	±3 db	0	1
-3 dB	±3 db	1	0
-12 dB	±3 db	1	1

DESIGN CONSIDERATIONS

A complete V.22bis modem system is shown in XR-2400 ES modem schematic available from EXAR applications department.

Several design considerations must be followed in order to ensure optimum system performance, as follows:

1. System Grounding - The XR-2402A provides both analog and digital grounds. These grounds should be separate up to the actual power supply ground, and single point connected there.

2. Power Supplies - Power supply bypassing should be provided at several points throughout the PCB. At the power input both a high frequency capacitor (0.1μF) and larger type (4.7 μF) for current transients. Particular should be taken to provide bypassing for the XR-2402A, located near the chip.

3. Receive Carrier Input R_{XC} - Care must be taken to route the RXC trace such that it is not near any crystals or logic IC's. in order to keep a clean layout the XR-2402A should be placed on the printed circuit layout near the telephone interface (DAA).

PERFORMANCE

One of the main parameters used as the yardstick to compare modems is the probability of producing errors while subjected to noise, commonly known as bit error rate verses signal-to-noise ratio (BER vs. S/N). The data supplied here was measured by an independent modem test house, Telequality Ass. in Colorado.

Bit error Rate measurement results are shown in Fig 3. This test is purely a measure of the data pump, XR-2402A / XR-2401.

TELEQUALITY BER VS S/N TEST RESULTS

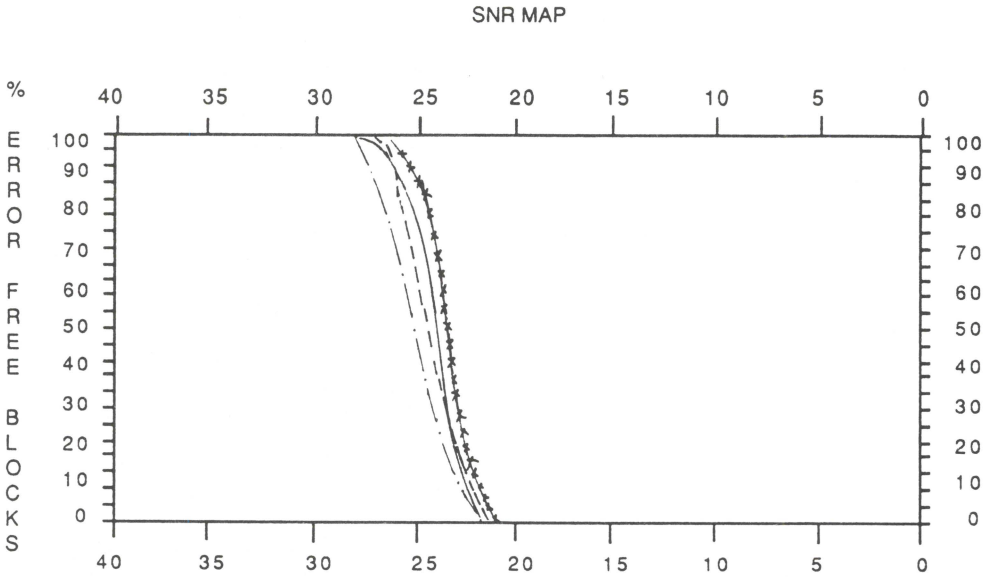
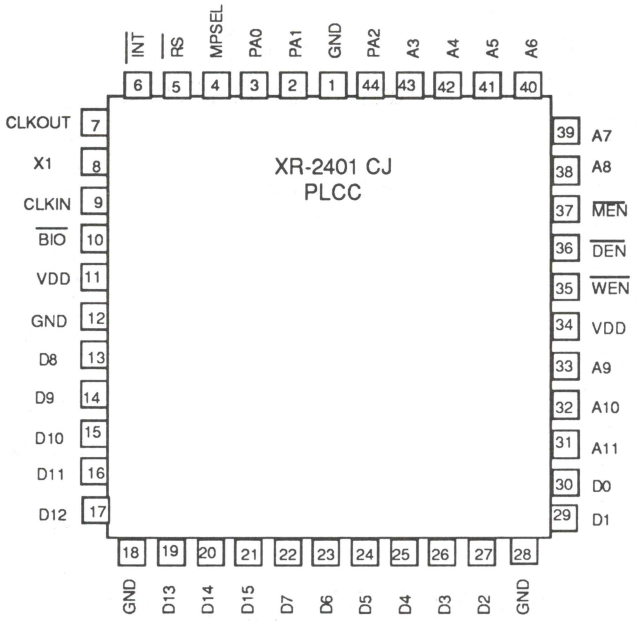
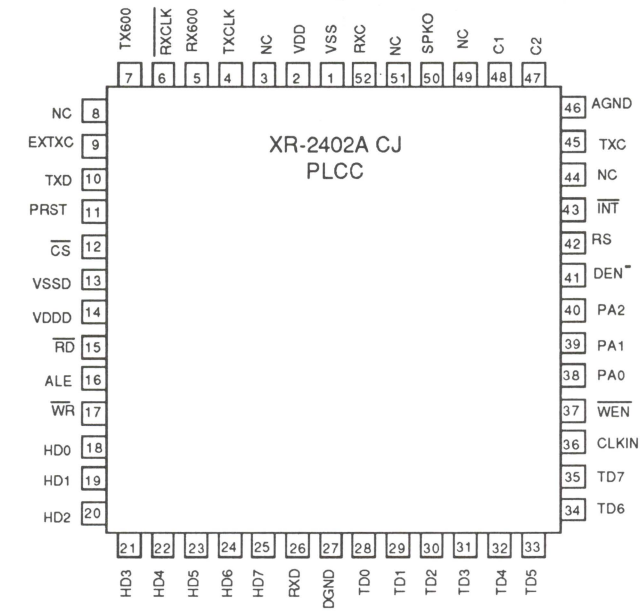


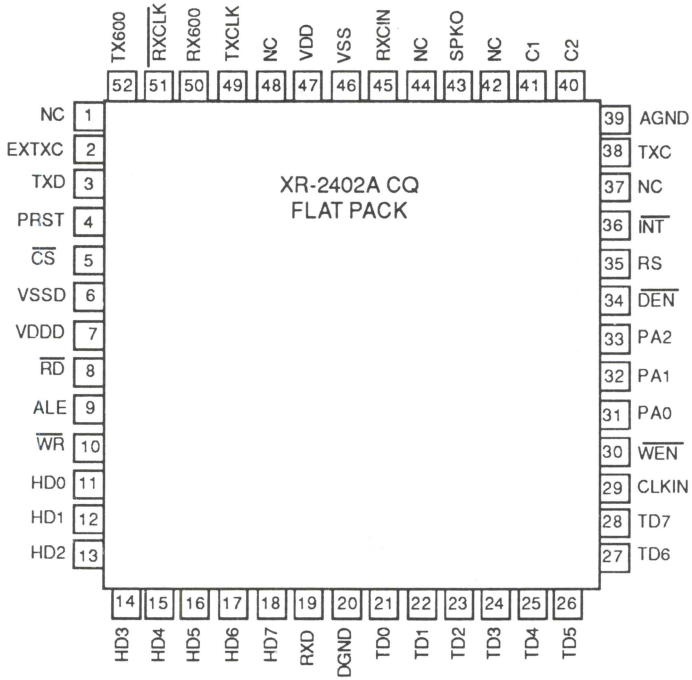
Figure 3. BER vs S/N

EXAR 2400ES
IN ORIGINATE MODE
RECEIVING FROM CONCORD 224
AT 2400 BPS OVER
3002 LINE SIMULATOR

SIGNAL LEVEL (1004 Hz)
12 dBm
-26 dBm
-32 dBm
-35 dBm


XR-2401 CJ
PLCC
INT 6
RS 5
MPSEL 4
PA0 3
PA1 2
GND 1
PA2 44
A3 43
A4 42
A5 41
A6 40
CLKOUT 7
X1 8
CLKIN 9
BIO 10
VDD 11
GND 12
D8 13
D9 14
D10 15
D11 16
D12 17
39 A7
38 A8
37 MEN
36 DEN
35 WEN
34 VDD
33 A9
32 A10
31 A11
30 D0
29 D1
18 GND
19 D13
20 D14
21 D15
22 D7
23 D6
24 D5
25 D4
26 D3
27 D2
28 GND


XR-2402A CJ
PLCC
TX600 7
RXCLK 6
RX600 5
TXCLK 4
NC 3
VDD 2
VSS 1
RXC 52
NC 51
SPKO 50
NC 49
C1 48
C2 47
NC 8
EXTXC 9
TXD 10
PRST 11
CS 12
VSSD 13
VDDD 14
RD 15
ALE 16
WR 17
HD0 18
HD1 19
HD2 20
46 AGND
45 TXC
44 NC
43 INT
42 RS
41 DEN
40 PA2
39 PA1
38 PA0
37 WEN
36 CLKIN
35 TD7
34 TD6
21 HD3
22 HD4
23 HD5
24 HD6
25 HD7
26 RXD
27 DGND
28 TD0
29 TD1
30 TD2
31 TD3
32 TD4
33 TD5


XR-2402A CQ
FLAT PACK
1 NC
2 EXTXC
3 TXD
4 PRST
5 CS
6 VSSD
7 VDDD
8 RD
9 ALE
10 WR
11 HD0
12 HD1
13 HD2
14 HD3
15 HD4
16 HD5
17 HD6
18 HD7
19 RXD
20 DGND
21 TD0
22 TD1
23 TD2
24 TD3
25 TD4
26 TD5
27 TD6
28 TD7
29 CLKIN
30 WEN
31 PA0
32 PA1
33 PA2
34 DEN
35 RS
36 INT
37 NC
38 TXC
39 AGND
40 C2
41 C1
42 NC
43 SPKO
44 NC
45 RXCIN
46 VSS
47 VDD
48 NC
49 TXCLK
50 RX600
51 RXCLK
52 TX600

MNP 5 Microcontroller

GENERAL DESCRIPTION

The XR-2403B is a dedicated microcontroller programmed to provide 'AT' and MNP command control for the XR-2400 V.22bis modem chip set. Coupled with the XR-2400 a modem supporting MNP (Microcom Networking Protocol) class 2-5 operation is easily implemented. The lower classes of MNP (2-4) ensure error free operation, while class 5 adds data compression which basically doubles (4800 BPS) data throughput.

The 8031 based XR-2403B also provides 'AT' command control with the actual command set supported in an external EPROM (16K Bytes) for maximum flexibility. Either use the complete command set supplied by Exar or modify it to meet your specific requirements.

The XR-2403B operates from a single +5 V power supply and offers low power operation with CMOS technology.

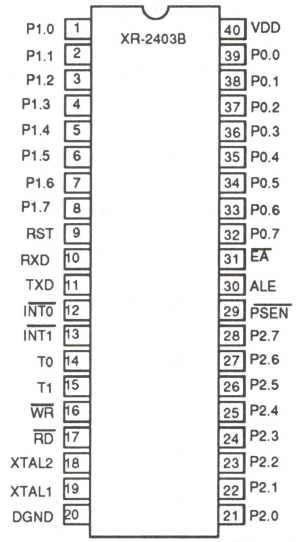
FEATURES

100% Reliable Data Transfer with MNP 2-4
Increased Data Throughput by MNP 5 Data Compression (~200%)
Industry Compatible Commands
Easily Modified/Enhanced Command Set
Offers Minor Chip Change Solution for MNP/Non-MNP Conversion (Same PC Board)
Optimal System Partitioning Provides High Data Throughput for Both Half and Full Duplex Operations
CCITT V.42 Compatible
Future V.42bis Chip Upgrade

APPLICATIONS

Modem Requiring Highly Reliable Data Transfer
Enhanced Throughput Applications - up to 200% (4800 BPS)
Low Power Designs Such as Laptop Applications

PIN ASSIGNMENT



Please see last page for PLCC and QFP packages

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2403BCP	Plastic	0°C to 70°C
XR-2403BCJ	PLCC	0°C to 70°C
XR-2403BCQ	QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7.0V
Input Voltage	-0.7V to (VDD +0.3) V
DC Input Current (any input)	± 10 mA
Power Dissipation (Pkg. Limitation)	1 watt
Storage Temperature Range	-65°C to + 125°C

SYSTEM DESCRIPTION

When coupled with the XR-2400 V.22bis chip set the XR-2403B allows the implementation of an error free, enhanced throughput V.22bis modem.

An Exar supplied 'AT' command set provides:

- Hayes 'AT' Compatibility
- Microcom "\" Commands
- Optional Customized Code by Changing External EPROM Code

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD = 5V ± 10%, fCKLIN = 11.0592 MHz ± 0.05%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{DD}	Power Supply Current		18	22.0	mA	VDD = 5.5V
V_{IH}	Input High Voltage Except XTAL 1 and RST	1.8			V	
V_{IH}	Input High Voltage	3.5			V	XTAL 1 and RST
V_{IL}	Input Low Voltage			1.0	V	
VOH	Output High Voltage Ports 1, 2, 3	2.4			V	IOH = -60µA
V_{OH}	Output High Voltage Port 0 in Ext Bus Mode, ALE, PSEN	2.4			V	IOH = -400µA
V_{OL}	Output Low Voltage Ports 1, 2, 3			0.45	V	IOL = 1.6 MA
V_{OL}	Output Low Voltage Port 0, ALE, $\overline{PSEN}$			0.45	V	IOL = 3.2 MA
I_{IH}	Input High Current (Leakage)			±10	µA	0.45 < Vin < VDD
I_{IL}	Input Low Current			50	µA	Vin = 0.45V

SYSTEM OPERATION

Figure 1 shows the interconnection of the XR-2403B and XR-2400 V.22bis chip set.

The XR-2400 provides the complete modem data pump function for 2400/1200/300 BPS modes. Command control is provided by the XR-2403B, both for MNP and 'AT' functions.

The 'AT' MNP commands reside in the 27128 (or 27256) EPROM. Exar supplies this set to be used as is or modified to provide individuality to the modem. To allow customer modification, the source code is provided for the 'AT' / MNP commands. Also the entry points to the XR-2403B are provided to allow user modification (last section on datasheet).

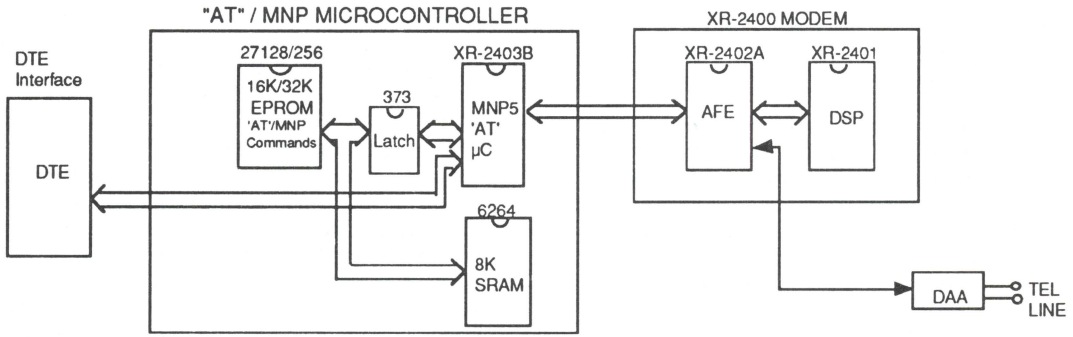


Figure 1. XR-2403B / XR-2400 System Configuration.

MNP OPERATION

To gain a better understanding of the XR-2403B operation and uses, the various modes, flow controls and other aspects of MNP must be understood. The following is provided to help with this understanding and its relation to the XR-2403B.

MNP, an acronym for Microcom Networking Protocol, was developed by Microcom, Inc., a modem manufacturer. Various classes of operation have emerged with class 1-5 operation most popular and being implemented on many 2400 BPS modems.

MNP Classes (Throughput data is based on 2400 BPS line speed).

Class 1 Is a half duplex protocol and not included in many new designs. Throughput was about 70% or 1690 BPS.

Class 2 Synchronous operation with byte orient ed data formatting. Throughput is rough ly 84% of nominal or about 2000 BPS.

Class 3 Conversion to synchronous, bit oriented data handling is transmitted in blocks consisting of 1 to 64 characters. Throughput is about 108% or 2600 BPS. Class 3 was the "industry standard" in 1987.

Class 4 Basic characters are the same as class 3 but block size is dynamic (flexible size is based on data transmission quality). Throughput is 120% or 2900 BPS.

Class 5 Includes class 3 and 4 with data com pression techniques added. The com pression effectiveness is dependent on the type of data, but typical throughput enhancements are up to 200% or 4800 BPS.

ERROR CORRECTION

Error correction is added to modems to ensure 100% perfect data transfer. Software schemes have been most popular until recently, such as X modem and Kermit for async file transfer or SDLC and HDLC Async schemes for mainframe environments. The throughput for these software schemes vary but all reduce data transfer below its nominal rate or typically 91%, which equates to about 2200 BPS for 2400 BPS

Hardware based MNP converts asynchronous data to be transmitted to a synchronous format (strips start and stop bits) for a bit oriented protocol. Typical throughput is about 108% or 2600 BPS.

Actual error correction is accomplished by first attaching a known data pattern to each block of data to be transmitted. Then the receiving side will check each block for the added data pattern and if found to be incorrect, will request the block to be retransmitted.

The data added to each block is based on a 16 bit CRC (Cyclic Redundancy Check) calculation of block of data to be transmitted. The receiving side then calculates each block's CRC value to determine if any errors existed and if retransmission is necessary.

The higher MNP classes 3-5, provide flexible block sizes to decrease the number of retransmitted blocks in poor environments such as noisy line conditions.

DATA COMPRESSION

MNP Class 5 offers data compression techniques to substantially increase a modem's data throughput over its basic line rate. MNP 5 utilizes a scheme which dynamically tabulates redundant characters. These characters are then transmitted in an abbreviated form to increase throughput as much as100% or 4800 BPS for a 2400 BPS modem.

To provide data transmission enhancement the DTE (Data Terminal Equipment) speed must be greater than the line speed. In order to accomplish this a data buffer is included at the transmit data input. The buffer acts as a reservoir to ensure data is not lost when DTE speeds exceed line speed.

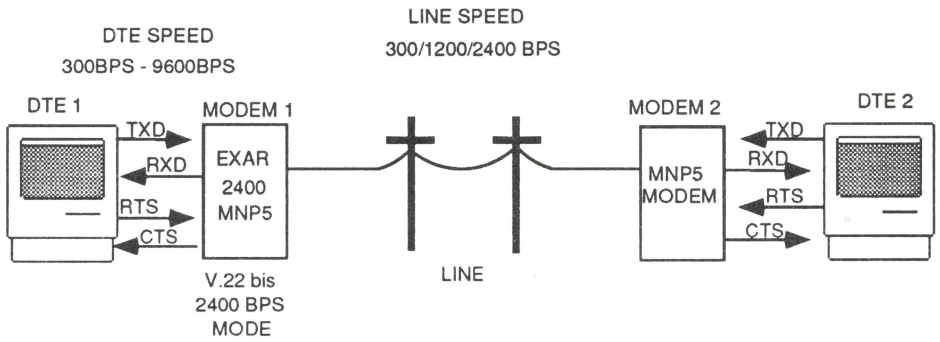


Figure 2. Basic Modem Configuration

The data buffer has a finite size and provision must be supplied to ensure it does not overflow and cause data loss. The method for controlling this condition is known as flow control.

FLOW CONTROL

As previously outlined, a method for regulating the flow of data to be transmitted is necessary when DTE data rates exceed line rates. Figure 2 illustrates a basic modem connection and helps illustrate where flow controls fit in.

Flow control can be under hardware or software control.

HARDWARE FLOW CONTROL

Hardware Flow Control allows the modem to lower or raise its CTS (Clear to Send) line to the DTE. This provides an on/off control of data flow from DTE to modem. If the modem data buffer becomes full it lowers the CTS line to stop transmit data flow to allow the modem to "catch-up".

SOFTWARE FLOW CONTROL

An alternative to hardware flow control is controlled by software, known as Xon/Xoff.This is accomplished by special characters inserted into the data stream to start and stop data flow. Control Q (^Q) is used to start or restart data flow and control S (^S) to stop data flow.

Three different variations of Xon/Xoff control modes are:

- Send Only
- Normal
- Passthrough

XR-2403B MNP FUNCTIONS AND COMMANDS

The XR-2403B with external EPROM (16K x 8) provides control for the following major functions:

FUNCTION	DESCRIPTION
• 'AT' Command Control	Provides 'AT' Command Set Control
• MNP Level 2-4	Provides error correction for 100% perfect data transfer.
• MNP Level 5	Allows roughly a 100% increase (4800BPS for V.22bis mode) in data throughput, through data compression techniques.
• Speed Conversion	Maintain up to 9600 BPS DTE (terminal speed for 300 BPS to 2400 BPS line speeds, both for MNP and non-MNP connections

A complete list of MNP functions and responsive commands are as follows:

*Note: Default values are indicated by **

COMMAND	DESCRIPTION/RANGE - SIZE	FUNCTION
AT \ N0	Normal	Operating Mode
AT\N1	Direct	
AT\N2	Reliable	
AT\N3*	Auto Reliable	
AT \ A0	64 Characters	Transmit Block Size
AT \ A1	128 Characters	
AT \ A2	192 Characters	
AT \ A3*	256 Characters	
AT%An	n = 0-127 ASCII	Auto-Reliable Fallback Character
AT \ L0*	Stream Link	Block MNP Link
AT \ L1	Block Link \L1 = \L0	(Stream Mode)
AT \ O	Initiate Reliable Link After Escape Command Independent of Modem Initial mode (ANS or ORG)	Originate Reliable Link
AT \ U	Accept Reliable Link after Escape Command request from Initiator of LInk	Accept Reliable Link
AT \ Y	Establish Reliable Link after Connecting in Normal Mode	Switch to Reliable Mode
AT \ Z	Switch to Normal Mode After Establishing a Reliable Link	Switch to Normal Mode
AT% C0	MNP 5 Disabled	Compression On/Off Control
AT% C1*	MNP 5 Enabled	

Note: AT & E1 $\triangleq$ AT \ N2 % C0
AT & E2 $\triangleq$ AT \ N2 % C1

COMMAND	DESCRIPTION / RANGE - SIZE	FUNCTION
AT \ V0*	Standard Non-MNP Result Codes	Result Code Form
AT \ V1	Modified MNP Result Codes (As Listed Below)	
AT \ Bn	N = 0 - 9 (100ms Increments) Disable Transmitter Break Default = 0	Transmit Break for Normal Data Mode
AT \ C	Not Functional	Set Auto-Reliable Buffer
AT \ K1	Empty Data Buffers And Immediately Send a Break to the Remote Mode	Break Control for Reliable Data Mode
AT \ K3	Immediately Send a Break to the Remote Terminal or Computer	
AT \ K5	Send a Break to the Remote Modem in Sequence With Any Data Received from the Serial Port	
AT \ K0,2,4	Not Supported (Will be equal to AT \ K5 if selected)	
AT \ Tn	N = 0-90 min N* = 0 (disable)	Inactivity Timer
AT \ I	Not Functional	Interface Protocol
AT \ J0	BPS Rate Adjust Disabled	Speed Conversion Control
AT \ J1*	BPS Rate Adjust Enabled	
AT \ S	Status Display	Read On-Line Status
AT \ G0*	Disables Modem Port Flow Control	Set Modem Port
AT \ G1	Sets Modem Port Flow Control to Xon / Xoff	Flow Control
AT \ X0*	Does Not Pass Xon / Xoff to Remote Modem	Xon / Xoff Pass Through Control
AT \ X1	Passes Xon / Xoff to Remote Modem	
AT \ Q0	Disable Flow Control	Serial Port Flow Control
AT \ Q1	Bidirectional Xon / Xoff Enabled	
AT \ Q2*	Unidirectional Hardware Control by CTS	
AT \ Q3	Bidirectional Hardware Control by RTS / CTS	
AT \ Q4	Unidirectional Xon /Xoff Send Only	
AT % U	Not Functional	Clear Serial Port Speed Serial Port
AT - P0*	Ignores Parity for Special Characters	Check Parity
AT - P1	Processes Special Characters Only if they have Correct Parity	

See Command AT \ V1

STANDARD RESULT CODES		MODIFIED RESULT CODES	
Verbose	Numerical	Verbose	Numerical
Connect	1	Connect 300	20
Connect 1200	5	Connect 1200 / REL 4 or 5	22
Connect 2400	10	Connect 2400 / REL 4 or 5	23

APPLICATIONS INFORMATION

The modem system schematics are also available. Please contact factory.

SYSTEM PERFORMANCE

Performance was measured on a 2400 BPS modem supporting MNP class 2-5 as shown in Figure 3.

Beyond error correction, giving 100% reliable data, data compression operation (class 5) is often the parameter used for comparison purposes.

When measuring data throughput several conditions must be considered. First the speed of data transfer may vary depending on full or half duplex data transfer. This condition will occur if the MNP implementation is processor speed limited. Exar's implementation yields identical throughput for both half or full duplex.

A second consideration is the type of data to be transferred. The efficiency of the MNP 5 data compression is a function of data redundancy. For example a data pattern of "...abab..." would yield an extremely high throughput, roughly 240% of nominal. On the other hand, the standard "quick brown fox" pattern with little redundancy yields a throughput in the 175% area.

Figure 3 shows the effective data throughput for the XR-2400 MNP chip set for various data patterns. The test set-up used is shown in Figure 4.

The modem represented in the modem system schematic was tested for data non-MNP mode. The curve in Figure 5 shows the probability of errors (BER) as a function of input signal-to-noise (S/N) ration. This curve was generated with the set-up as shown in Figure 6. The conditions of the set-up are indicated in Figure 5.

ENTRY POINTS AND MEMORY MAPPING

The XR-2403B MNP 5 Microcontroller when used with the XR-2400 V.22bis chip set, provides a highly compatible MNP 5 / 'AT' 2400 BPS modem function, the architecture as seen in Figure 1, is open with regard to command set modification. This is accomplished by having both MNP and 'AT' commands residing in external EPROM.

To aid in customer modification of 'AT' or MNP commands, the following information is provided.

Entry Point Information

The XR-2403B is a masked 8031 type microcontroller with 8K of internal program memory. The internal program provides control for MNP and 'AT' functions. The MNP portion of the program is Exar proprietary... information and not accessible externally. However, to facilitate modification or enhancement of 'AT' or MNP commands, entry points to the MNP program are provided.

Status / Mode Setting Memory Locations

Status	Location	Description
PASS_B	9D14H	Escape Code Checking Byte in Speed Conversion Mode.
SPEED	9D15H	Speed Indicator For All Modes. 0 - 9600 BPS 1 - 4800 BPS 2 - 2400 BPS 3 - 1200 BPS 4 - 300 BPS
Z_BUF	9D16H	Auto Reliable Fallback Character.
MRCVP2	803BH	Disconnect to Check Auto-Reliable Fallback Mode.

Status	Location	Description
SPD_FLG	20 H.7	Speed Conversion Enable Flag.
MNP_5	9E22H	Reliable Link Indicator
BACK-RAM	9D1AH	Starting Address for Command Buffer Back-up.
BK_PRE	51 H	Break Prescaler Timer
BK_TMR	52 H	Break Timer
OPT_P	9D50H	Output Port Selection Option (F0FF H to 40 FFH). This Parameter is Initialized Immediately After Power On and constantly moni tored by MNP Module.

Function Call Locations - MNP Program Entry Points

Function	Location	Description
EC_MAIN	0080H	Calling Main MNP Program. This is the only location which will initiate the MNP program.
MNP_IN	0066H	MNP Program Immediate Re-Entry Point for modifying MNP Program.
MSG_CPY	0063H	Exar Copyright Calling Subroutine.
MSG_CP	0030H	Exar Copyright Message.
P_ECRAM_1	0060H	After Escape MNP Re-Entry Point.
SPD_INM	0069H	Speed Conversion Program Jump-In Point.
INI_SPDM	006CH	Speed Conversion Initialization Routine.
SCTINT_1	0006H	Interrupt 0 Jump-In Point.
SCRINT_1	0016H	Interrupt 1 Jump-In Point.
SPINT_1	0026H	Serial Port Interrupt Jump-In Point.
V21_IN_1	006FH	300 BPS Speed Conversion Timer Set-Up.

XR-2403B Re-Entry Points

Function	Location	Description
PWR_ONS	C000H	Power On
OUT_SCT	C003H	Interrupt 0
OUT_T0	C006H	Timer 0
OUT_SCR	C009H	Interrupt 1
OUT_T1	C00CH	Timer 1
OUT_SP	C00FH	Serial Port Interrupt
OUT_T2	C0012H	Timer 2
MNP_OUT	C0015H	MNP Program Intermediate Point
CHK070S	C01BH	MNP 'ESC' Jump Out Point
DISCONNECTS	C01EH	MNP Disconnect
ON_LOOPS	C021H	Auto-Reliable Fallback Point.
SPD-OUTS	C024H	Speed Conversion Jump Out Point.
V21_INS	C027H	Call Speed Conversion ASM for 300 BPS.
SPD_TXD	C02AH	Put TXDATA to Modem Chip.
SPD_RXD	C02DH	Get RXDATA From Modem Chip.

RAM Locations

The stack in the 'AT' program starts from 0C0H on page 1 and occupies 64 bytes of space. Internal RAM on page 0 has 23 bytes and page 1 64 bytes of free space.

The external RAM data memory is as follows:

1) Error Control	8000H-8FFFH
2) Data Compression Buffer	9000H-93FFH
3) Break Buffer	9A00H-9AFFH
4) DTE TX Buffer	9B00H-9BFFH
5) DTE RX Buffer	9C00H-9CFFH
6) Misc. Registers	9D00H-9DFFH
7) MNP Program RAM Backup Buffer	9E00H-9EFFH
8) 'AT' Program RAM Backup Buffer	9F00H-9FFFH

Note: For program control, the XR-2403B backs up the entire 256 bytes of internal RAM into external RAM before jumping into or out of the MNP program. The 'AT' program RAM is 9F00H and MNP program RAM is 9E00H-9EFFH.

9) Customer Register 9400H-99FFH

Interrupt Vectors

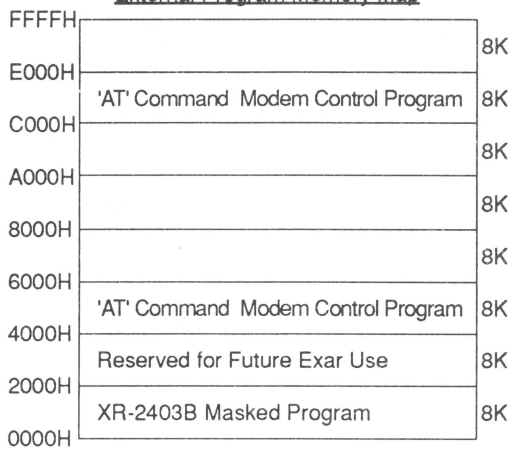
The XR-2403B brings out all interrupt vectors to the external program. This allows easy customer modification of service routines to suit a particular application. The interrupt vectors of the XR-2403B are as follows:

```
            ORG    0
            LJMP   PWR_ONS; Jump to Power
                           On Set Up Routine
            ORG    3H
EXT_INTO:                  ; Interrupt 0 for SCT
            LJMP   OUT_SCT
SCTINT1:
            LJMP   SCTINT
            ORG    OBH
T_INTO:                    ; Timer 0 Interrupt
            LJMP   OUT_TO
            ORG    13H
EXT_INT1:                  ; Interrupt 1 for SCR
            LJMP   OUT_SCR
SCRINT_1:
            LJMP   SCRINT
            ORG    1BH
T_INT1:                     ; Timer 1 Interrupt
            LJMP   OUT_T1
            ORG    23H
INT_SER:                   ; Serial Port Interrupt
            LJMP   OUT_SP
SPINT_1:
            LJMP   SPINT
            ORG    2BH
T_INT2:                    ; Timer 2 Interrupt
            LJMP   OUT_T2
```

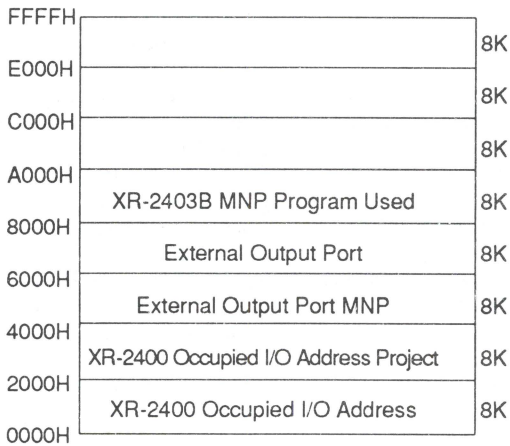
XR-2403B Program Memory Map

The following is a memory map for both external memory and external I/O.

External Program Memory Map



External Data Memory Map (OPT_P=1)



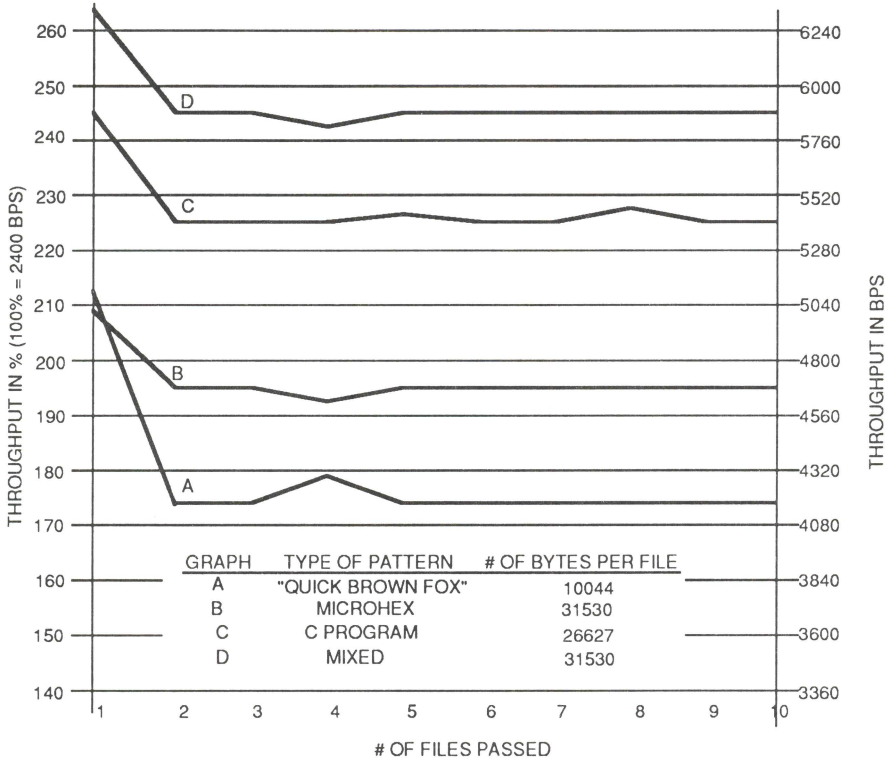


Figure 3. Effective Data Throughput

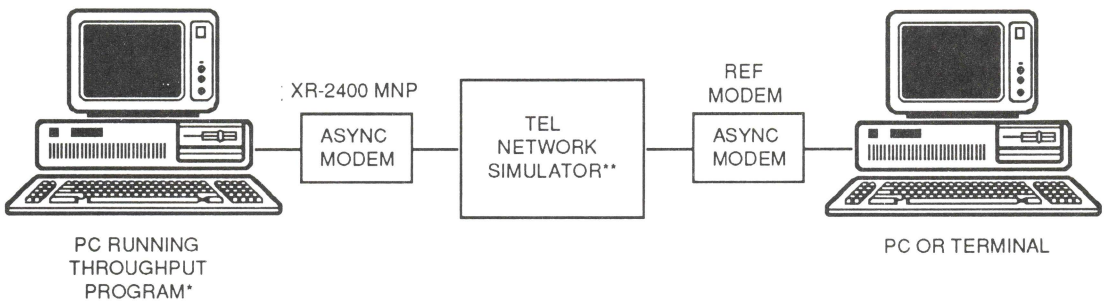


Figure 4. MNP Throughput Measurement Test Set-up

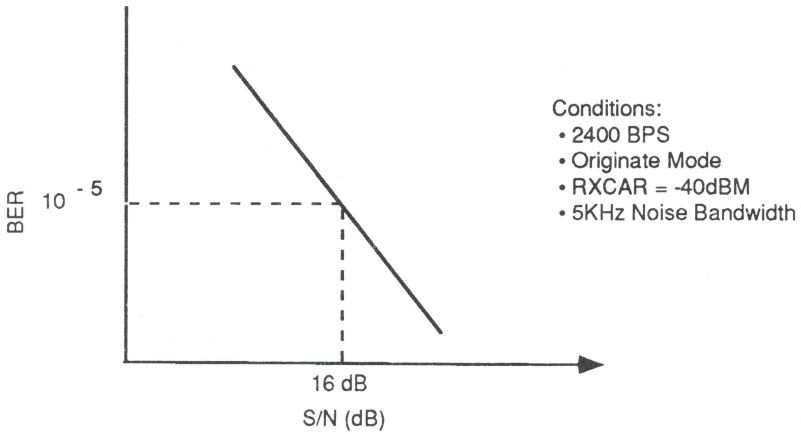


Figure 5. 2400 BPS BER vs S/N (Non-MNP Mode)

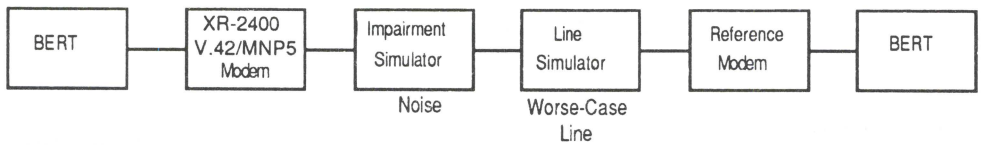
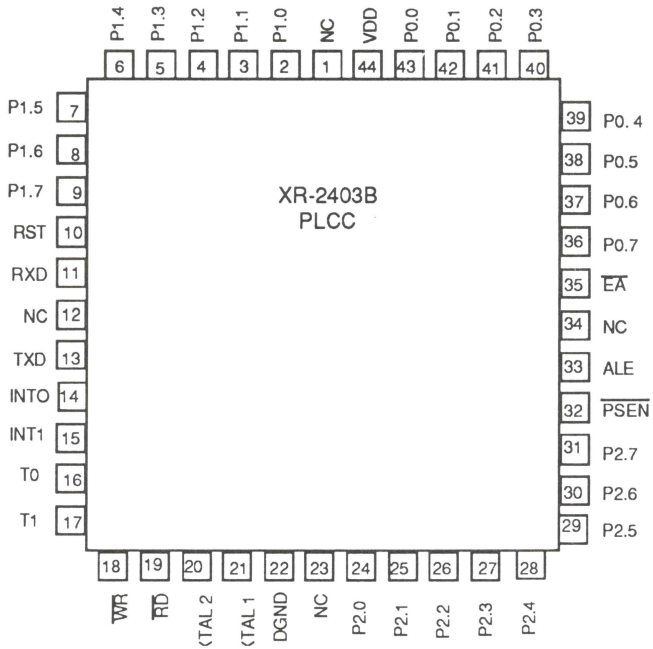
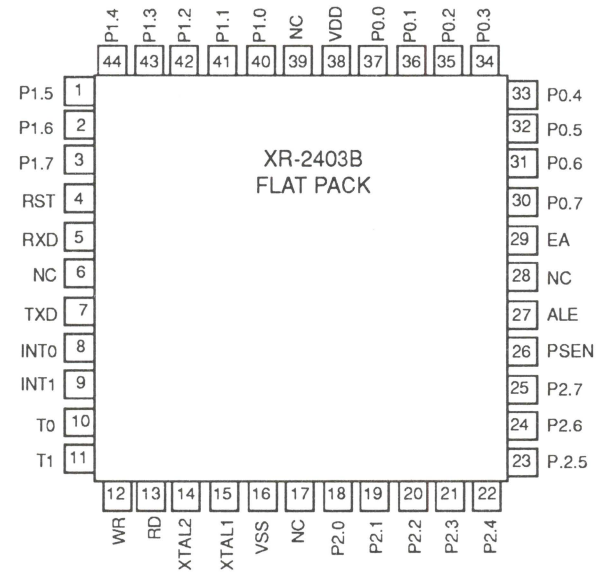


Figure 6. Data Quality Test Set-up


P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0 43
P0.1 42
P0.2 41
P0.3 40
P1.5 7
P1.6 8
P1.7 9
RST 10
RXD 11
NC 12
TXD 13
INTO 14
INT1 15
T0 16
T1 17
39 P0. 4
38 P0.5
37 P0.6
36 P0.7
35 EA
34 NC
33 ALE
32 PSEN
31 P2.7
30 P2.6
29 P2.5
18 WR
19 RD
20 (TAL 2
21 (TAL 1
22 DGND
23 NC
24 P2.0
25 P2.1
26 P2.2
27 P2.3
28 P2.4
XR-2403B
PLCC


P1.4 44
P1.3 43
P1.2 42
P1.1 41
P1.0 40
NC 39
VDD 38
P0.0 37
P0.1 36
P0.2 35
P0.3 34
P1.5 1
P1.6 2
P1.7 3
RST 4
RXD 5
NC 6
TXD 7
INTo 8
INT1 9
To 10
T1 11
33 P0.4
32 P0.5
31 P0.6
30 P0.7
29 EA
28 NC
27 ALE
26 PSEN
25 P2.7
24 P2.6
23 P.2.5
12 WR
13 RD
14 XTAL2
15 XTAL1
16 VSS
17 NC
18 P2.0
19 P2.1
20 P2.2
21 P2.3
22 P2.4
XR-2403B
FLAT PACK



NOTES



V.42 / MNP® 5 Microcontroller

GENERAL DESCRIPTION

The XR-2442 is a dedicated microcontroller that provides command control for the XR-2400 V.22bis modem chip set. The XR-2442 provides control for CCITT recommended V.42 error correction, including LAPM and MNP 2-4 protocols, with MNP class 5 data compression included for greater compatibility. Also supported are the standard 'AT' commands.

The system architecture of the XR-2442 allows the actual command sets for the 'AT', MNP, and LAPM to reside external to the XR-2442, allowing ease of customization. Exar provides these command sets to use as is, or modify to the requirements of your design.

The XR-2442 operates from a single +5 volt power supply, offering low power consumption through CMOS technology.

FEATURES *

V.22bis\V.22\Bell 212A\Bell103 Modem
Error Free Data Transfer
- LAPM
- MNP 2-4

Increased Data Throughput by MNP 5 Data Compression
- 4800 BPS Throughput

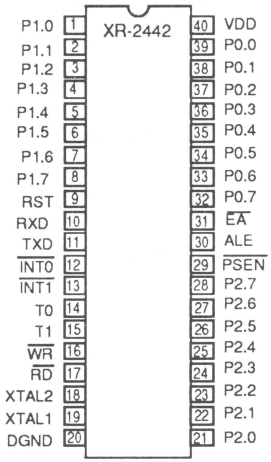
'AT' Command Control
- Easily Modified, Exar Supplied Source Code

**(Apply when used with XR-2400 V.22bis modem chip set)*

APPLICATIONS

Error Free Modem Applications
Stand-Alone Modems
Smart Modems
Laptop Modems

PIN ASSIGNMENT



(For other pin assignment diagrams, refer to the end of this datasheet)

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7V
Input Voltage	-0.7V to (VDD +0.3V)
DC Input Current (any input)	±10mA
Power Dissipation **(Package Limitation)** Derate above 25°C	1W
Storage Temperature Range	-65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2442CP	40 Pin Plastic Dip	0°C to 70°C
XR-2442CJ	44 Pin PLCC	0°C to 70°C
XR-2442CQ	44 Pin QFP	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2442, when coupled to the XR-2400 V.22bis modem chip set, allows the implementation of an error-free, increased throughput V.22bis modem.

The XR-2442 is just one in the family of controller options for the XR-2400 V.22bis modem chip set, including:

FUNCTION	CONTROLLER
'AT'	8031
'AT'/MNP 2- 5	XR-2403B
'AT'/V.42/MNP 5	XR-2442
'AT'/V.42/V.42bis/MNP 5	XR-2443

ELECTRICAL CHARACTERISITCS

Test Conditions: T_A = 25°C, V_{DD} = 5V ±10%, F_{CLK} = 11.0592MHz ±0.05%, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}	Power Supply Voltage	4.5	5	5.5	V	
I_{DD}	Power Supply Current		18	22	mA	
V_{IH}	Input High Voltage	1.8			V	Except XTAL1 and RST
V_{IH}	Input High Voltage	3.5			V	XTAL 1 and RST
V_{OH}	Output High Voltage	2.4			V	Ports 1,2,3 I_{OH} = -60µA
V_{OH}	Output High Voltage	2.4			V	Port 0 (External Bus Mode) ALE, $\overline{PSEN}$ I_{OH} = -800 µA
V_{OL}	Output Low Voltage			0.45	V	Ports 1,2,3, I_{OL} = 1.6 mA
V_{OL}	Output Low Voltage			0.45	V	Port 0, ALE, $\overline{PSEN}$ I_{OL} = 3.2 mA
I_{IH}	Input High Current			±10	µA	0.45V≤VIN ≤V_{DD} (Leakage)
I_{IL}	Input Low Current			-50	µA	V_{IN} = 0.45V

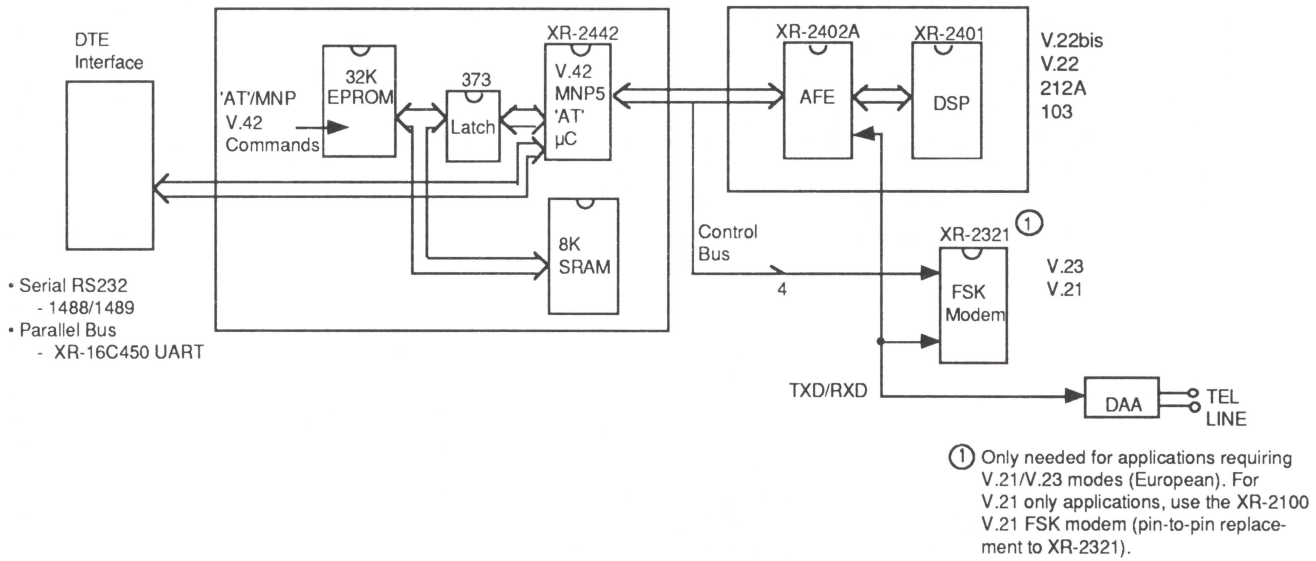


Figure 1. 2400 BPS Modem with V.42 / MNP 5 Block Diagram

SYSTEM OPERATION

A typical application utilizing the XR-2442 to support the XR-2400, V.22bis chip set, is shown in Figure 1. The XR-2400 provides the complete modem data pump function for:

V.22bis	2400 BPS
V.22	1200 BPS
V.23*	1200 BPS/75 BPS
V.21*	300 BPS
212A	1200 BPS
103	300 BPS

** Supported by the XR-2321*

Command control is supported by the XR-2442 for:

MNP 2-4	Microcom Error Correction
MNP 5	Microcom DataCompression
LAPM	CCITT Recommended V.42 Error Correction
'AT'	Industry Standard 'AT'

Although the XR-2442 does provide complete command control, the actual commands for the various modes reside in an external EPROM - 27C256, 32k Byte. With this architecture and an Exar supplied command set, maximum flexibility is offered. The command set can be used as is, or custom tailored to a particular design.

The unique architecture utilized by the XR-2400 and command controller allow the **same** hardware (PCB) to support several different types of 2400 BPS modems. By changing available pin-to-pin microcontrollers, the 2400 BPS modem types listed in Table 1 are all possible with the same printed circuit board. As mode types are changed by the µC, EPROM supported command sets and SRAM size change and/or elimination are also required. In each case Exar provides complete production worthy, command sets which may be used as is, or modified to meet specific application requirements. To aid in software modifications, Table 2, 3 and 4 list the XR-2442 memory mapping, indicating customer usable regions.

External memory modifications requiring µC (XR-2442) support will of course need entry/re-entry point information. This point is important as the XR-2442 contains program memory with EXAR proprietary V.42/MNP 5 functions not accessible externally (fusible link protected) or available to EXAR customers.

2400 BPS Modem Type	Microcontroller Part Number	External Memory Requirements (Bytes)	
		EPROM	SRAM
'AT'	8031 (Generic ROMLESS µP)	16k	NONE
'AT' / MNP 2-5	XR-2403B	16k/32k	8k
'AT' / MNP5/V.42	XR-2442	16k	8k / 32 k
'AT'/MNP5/V.42/ V.42bis	XR-2443	32k	32k

Table 1. 2400 BPS Modem Options / µC, EPROM, RAM Requirements

ENTRY POINTS AND MEMORY MAPPING

Status / Mode Setting Memory Locations

Status	Location	Description
SPD_FLG	20 H.7	Speed Conversion Enable Flag
BK_PRE	51 H	Break Prescaler Timer
BK_TMR	52 H	Break Timer (Only in Normal Mode)
MRCVP2	803BH	Disconnect to Check Auto-Reliable Fallback Mode
PASS_ B	9D14H	Escape Code Checking Byte in Speed Conversion Mode
SPEED	9D15H	Speed Indicator For All Modes 0 - 9600 BPS 1 - 4800 BPS 2 - 2400 BPS 3 - 1200 BPS 4 - 300 BPS
Z_BUF	9D16H	Auto Reliable Fallback Character
BACK_RAM	9D1AH	Starting Address for Command Buffer Backup
OPT_P	9D50H	Output Port Selection Option (F0FF H to 40 FFH) This Parameter is Initialized Immediately After Power On and constantly monitored by MNP Module
MNP_S	9E22H	Reliable Link Indicator

Function Call Locations - V.42/ MNP 5

Function	Location	Description
SCTINT_1	0006H	Interrupt 0 Jump-In Point.
SCRINT_1	0016H	Interrupt 1 Jump-In Point.
SPINT_1	0026H	Serial Port Interrupt Jump-In Point.
MSG_CP	0030H	Exar Copyright Message.
P_ECRAM_1		0060H After Escape MNP Re-Entry Point.
MSG_CPY	0063H	Exar Copyright Calling Subroutine.
MNP_IN	0066H	MNP Program Immediate Re-Entry Point for modifying MNP Program.
SPD_INM	0069H	Speed Conversion Program Jump-In Point.
INI_SPDM	006CH	Speed Conversion Initialization Routine.
V21_IN_1	006FH	300 BPS Speed Conversion Timer Set-Up.
EC_MAIN	0080H	Calling Main MNP Program. This is the only location which will initiate the MNP program.

XR-2442 Re-Entry Points

Function	Location	Description
PWR_ONS	C000H	Power On
OUT_SCT	C003H	Interrupt 0
OUT_T0	C006H	Timer 0
OUT_SCR	C009H	Interrupt 1
OUT_T1	C00CH	Timer 1
OUT_SP	C00FH	Serial Port Interrupt
OUT_T2	C0012H	Timer 2
MNP_OUT	C0015H	MNP Program Intermediate Point
CHK070S	C01BH	MNP 'ESC' Jump Out Point
DISCONNECTS	C01EH	MNP Disconnect
ON_LOOPS	C021H	Auto-Reliable Fallback Point.
SPD-OUTS	C024H	Speed Conversion Jump Out Point.
V21_INS	C027H	Call Speed Conversion ASM for 300 BPS.
SPD_TXD	C02AH	Put TXDATA to Modem Chip.
SPD_RXD	C02DH	Get RXDATA From Modem Chip.

RAM Locations

The stack in the 'AT' program starts from 0C0H on page 1 and occupies 64 bytes of space. Internal RAM on page 0 has 23 bytes and page 1, 64 bytes of free indicator space.

The external RAM data memory is as follows:

1) Error Control	8000H-8FFFH
2) Data Compression Buffer	9000H-93FFH
3) FAX / Remote Buffer	9400H-95FFH
4) Available for use	9600H-97FFH
5) V.42	9800H-98FFH
6) Break Buffer	9A00H-9AFFH
7) DTE TX Buffer	9B00H-9BFFH
8) DTE RX Buffer	9C00H-9CFFH
9) Misc. Registers	9D00H-9DFFH
10) MNP RAM Backup Buffer	9E00H-9EFFH
11) 'AT' RAM Backup Buffer	9F00H-9FFFH

Note: For program control, the XR-2442 backs up the entire 256 bytes of internal RAM into external RAM before jumping into or out of the MNP program. The 'AT' program RAM is 9F00H and MNP program RAM is 9E00H-9EFFH.

Interrupt Vectors

The XR-2442 brings out all interrupt vectors to the external program. This allows easy customer modification of service routines to suit a particular application. The interrupt vectors of the XR-2442 are as follows:

```
            ORG   0
            LJMP  PWR_ONS; Jump to Power On
                           Set Up Routine
            ORG   3H
EXT_INTO:                  ;Interrupt 0 for SCT
            LJMP  OUT_SCT
SCTINT1:
            LJMP  SCTINT
            ORG   0BH
T_INTO:                    ;Timer 0 Interrupt
            LJMP  OUT_TO
            ORG   13H
EXT_INT1:                  ;Interrupt 1 forSCR
            LJMP  OUT_SCR
SCRINT_1:
            LJMP  SCRINT
            ORG   1BH
T_INT1:                    ;Timer 1 Interrupt
            LJMP   OUT_T1
            ORG    23H
INT_SER:                   ;Serial Port Interrupt
            LJMP   OUT_SP
SPINT_1:
            LJMP   SPINT
            ORG    2BH
T_INT2:                    ;Timer 2 Interrupt
            LJMP   OUT_T2
```

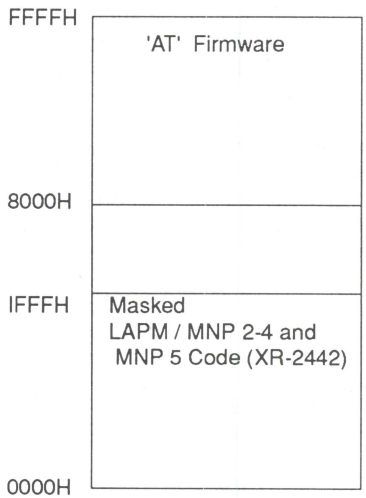
XR-2442 PROGRAM/DATA MEMORY MAPS

Tables 2, 3 and 4 show the ROM and RAM memory maps for XR-2442.

As it is indicated in Table 2, 32K bytes of EPROM is assigned to 'AT' command firmware. This section of the ROM is located between 8000H and FFFFH address locations of the memory space.

LAPM, MNP 2-4 and MNP5 code is masked in the microcontroller (XR-2442), and resides in the 8K bytes of memory, between address locations 0000H and 1FFFH.

Table 3 shows the RAM map, in which the space between 0000H and 002CH address locations is used for modem chip address. Table 4 shows the modem chip address assignment.



Note: 27C256 = 32K Byte EPROM

Table 2. XR-2442 ROM Map

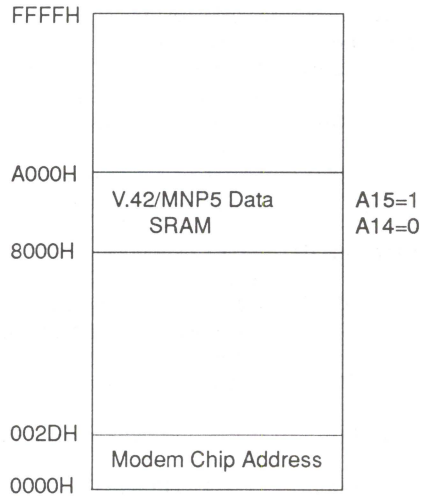


Table 3. XR-2442 RAM Map

MODEM CHIP	RAM ADDRESS	$\overline{CS}$
XR-2402A	0000H - 0003H	A15=0
XR-2321	0028H - 002CH	A5=1 and A15=0
XR-2100	0028H - 0029H	A5=1 and A15 =0

Table 4. Modem Chip Address

Also RAM space between 8000H and 9FFFH is assigned for V.42 and MNP 5 data. RAM locations between A000H and FFFFH, as well as RAM locations between 002DH and 7FFFH are available for I/O ports such as LED, EIA,etc.

V.42 / MNP OPERATION

The XR-2442 when coupled with the XR-2400 V.22bis modem chip set allows the implementation of an **error-free, increased throughput** 2400 BPS modem. To gain an understanding of V.42/MNP 5 modes of operation, the following basic information has been included. A basic understanding of error correction techniques, flow control, speed buffering, and data compression will allow the designer to better understand a V.42/MNP5 modems capabilities and how to best utilize them.

V.42 is a **CCITT** recommended error correction protocol which allows asynchronous DTE's (Data Terminal Equipment) to communicate error-free with other such equipped modems.

The actual error correction protocol used in V.42 is an **HDLC** (High-Level Data Link Control) based protocol called LAPM, for **Link Access Procedure for Modems.** For additional detailed information beyond the following basic description, refer to the CCITT Recommendations, Series V, 'Data Communication Over the Telephone Network'. The latest version is known as the **'Blue Book'** (Blue Covers) or Series, dated 1988 (Melbourne), a recent update from the **'Red Book'.**

V.42 Basic Operation/Features

- **HDLC**-based error correction protocol-LAPM
- Asynchronous (Async or 'start/stop') DTE Communication - error free
- Actual line transmission is synchronous (sync)- no start or stop bits (stripped from data), however initial handshake, subsequent to modem handshake is async
- Error Correction
  - Data sent in 'frames' or blocks with a nominal size (default) of 128 Octets (Octet - 8 bit) data frames
  - Start/Stop bit elimination from data creates an actual data throughput improvement, roughly 120% of nominal. 2400 BPS becomes about 2900 BPS
  - Encoded information added to data frame for receiver to 'decode' and determine if the block was error free. 16-bit cyclic redundancy (CRC) methods are used for data encoded information to (1) indicate correct data and (2) recog nize imperfect data frame
  - Retransmission (automatic) of determined imperfect frames to ensure perfect data is received

V.42 operation is found to be virtually identical (specifically to variable parameters) to that of MNP reliable or normal modes of operation. For this reason the MNP command set is also used for V.42 variables control.

MNP OPERATION

MNP, or Microcom Networking Protocol was developed by Microcom, Inc., a modem manufacturer. Since conception, it has been in a constant state of update/improvement. For this reason 'classes' of operation emerged to signify each major update or improvement.

Relative to V.22bis or 2400 BPS modems, up to class or level 5 has become the 'standard'.

MNP CLASSES

(Throughput data is based on **2400 BPS** line speed).

Class 1 A half duplex protocol and not included in many new designs. Throughput was about 70% or 1690 BPS. The XR-2442 does not support this class.

Class 2 Asynchronous operation with byte oriented data formatting. Throughput is roughly 84% of nominal or about 2000 BPS.

Class 3 Conversion to synchronous, bit oriented data handling is transmitted in blocks consist ing of 1 to 64 characters. Throughput is about 108% or 2600 BPS. Class 3 was the "industry standard" in 1987.

Class 4 Basic characters are the same as Class 3 but block size is dynamic, up to 256 Bytes, (flexible size is based on data transmission quality). Throughput is 120% or 2900 BPS.

Class 5 Includes Class 3 and 4 with data compression techniques added. The compression effectiveness is dependent on the type of data, but typical throughput enhancements are up to 200% or 4800 BPS.

ERROR CORRECTION

Modem users have come to expect sophisticated circuitry like adaptive equalization for varying phone characteristics and retrain modes for ensuring continued optimal performance. These techniques dramatically improve performance characteristics such as BER vs S/N, the probability of errors when the modem signal is in the presence of noise. But try as they may, BER values do not go to zero, especially as modem speeds increase.

The previously mentioned techniques are aimed at improving the modem data pump through analog (or digitally synthesized) circuitry. Techniques are becoming popular for not only improving, but virtually eliminating data errors through protocols implemented in the modems command microcontroller (µC). Prior to these 'hardware' based schemes, error correction provided in the applications software was available, such as XMODEM or Kermit for asynchronous file transfer. In mainframe environments, SDLC or HDLC schemes were used.

Software based error correction schemes do however have their disadvantages. One important one being reduced data throughput. The throughput performance varies, but all schemes reduce data transfer below its nominal rate. Typical values of 91% are common, equating to only about 2200 BPS for a 2400 BPS modem.

The hardware based error correction protocols supported by the XR-2442 are those as specified by the **CCITT, LAPM,** and **MNP.** These schemes convert asynchronous data to be transmitted to a synchronous format (start and stop bits are stripped) for a bit-oriented protocol. Throughput values again vary, however typical values of 108% for the lower MNP Class 3 and 120% for MNP Class 4 or LAPM. These equate to roughly 2600 - 2900 BPS for 2400 BPS modems.

Actual error correction is based on adding information to the block-oriented data, through a 16-bit CRC (Cyclic Redundancy Check) calculation. The receiving side calculates CRC values for each block and if found to be incorrect, a retransmission of that block will be requested.

Typical frame sizes for LAPM are 128 Octets (8-bit start/stop bit stripped characters).

DATA COMPRESSION

The CCITT recommendation for V.42 only specifies error correction modes, as provided by LAPM and MNP 2-4. Modem controller protocols have advanced to the point where in addition to providing error-free data transfer, they can also offer other significant enhancements. One very significant enhancement is the addition of data compression operation. Simply put, this technique dramatically enhances the actual data throughput of the modem.

This data compression scheme, MNP5, although not specifically part of the V.42 recommendation, has been included in the XR-2442 to serve only as a further enhancement to the XR-2442 based modems.

MNP Class 5 is the protocol for **data compression**. It is by far the most accepted protocol for this function. CCITT recommendations are adding a data compression mode to V.42, called **V.42bis**. The **XR-2443** supports the CCITT recommended **BTLZ** data compression.

MNP 5 data compression offers the XR-2400 V.22bis modem chip set roughly an 100% increase in throughput, or 200% of nominal. This translates to a maximum modem throughput of 2400 BPS x 2 = 4800 BPS.

MNP 5 techniques utilize a scheme which abbreviates redundant data characters for a much higher transmission efficiency or throughput increase. Because of its dependency on redundant characters the amount of improvement will vary. Typical improvement values are in the range of 75 to 125%, or 4200 to 5400 BPS for 2400 BPS modems.

FLOW CONTROL

As previously outlined, a method for regulating the flow of data to be transmitted is necessary when DTE data rates exceed line rates. Figure 2 illustrates a basic modem connection and helps illustrate where flow controls fit in.

Flow control can be under **hardware** or **software** control.

HARDWARE FLOW CONTROL

Hardware Flow Control allows the modem to lower or raise its CTS (Clear to Send) line to the DTE. This provides an ON/OFF control of data flow from DTE to modem. If the modem data buffer becomes full it lowers the CTS line to stop transmit data flow to allow the modem to "catch-up".

SOFTWARE FLOW CONTROL

An alternative to hardware flow control is control by software, known as **Xon/Xoff**. This is accomplished by special characters inserted into the data stream to start and stop data flow. **Control Q (^Q)** is used to start or restart data flow and **Control S (^S)** to stop data flow.

Three different variations of Xon/Xoff control modes are:

- Send Only
- Normal
- Passthrough

XR-2442 V.42/MNP5 FUNCTIONS AND COMMANDS

The XR-2442 with external EPROM provides control for the following major functions:

FUNCTION	DESCRIPTION
• 'AT' Command Control	Provides 'AT' Command Set Control
• MNP Level 2-4	Provides error correction for 100% perfect data transfer.
• MNP Level 5	Allows roughly a 100% increase (4800 BPS for V.22bis mode) in data throughput, though data compression techniques.
• V.42 (LAPM)	100% perfect data transfer
• Speed Conversion	Maintain up to 9600 BPS DTE terminal speed for 300 BPS to 2400 BPS line speeds, both for LAPM/MNP and non-error correcting connections.

PROTOCOL NEGOTIATION

The XR-2442 supports error correcting or reliable modes of operation for not only LAPM, but also MNP type protocols. Also, although data compression operation is not specified by CCITT V.42 specifications, it has been included through MNP 5 for increased compatibility. Because of these multiple protocols supported, the XR-2442 offers two temporary protocol negotiation modes:

1) **AT\M0** Default Mode. This command selects an automatic protocol negotiation mode. **First LAPM** negotiation will be attempted. If not posstible, MNP 2-4,5 operation will be negotiated. The highest possible class of MNP operation will be negotiated (Compression negotiation will be attempted depending upon the setting of the %C command). If the remote modem does not support error correction, normal 2400 BPS (or1200/300 BPS) operation will be supported.

2) **AT\M1** This command will **disable LAPM** operation. Here only MNP 2-5 and non-error correcting modes of operation will be supported.

The following is a command set summary for the XR-2442. Provided are:

1) Basic Connection/Dialing Commands
2) Dialing Modifiers
3) Standard Hayes 'AT' Command Set
4) 'S' Register Descriptions/Functions. These registers are used for controlling the value or function of various 'AT' commands.
5) MNP/LAPM Commands. The entire list represents the MNP command set. Most of the MNP commands also apply to LAPM, with the exceptions indicated.

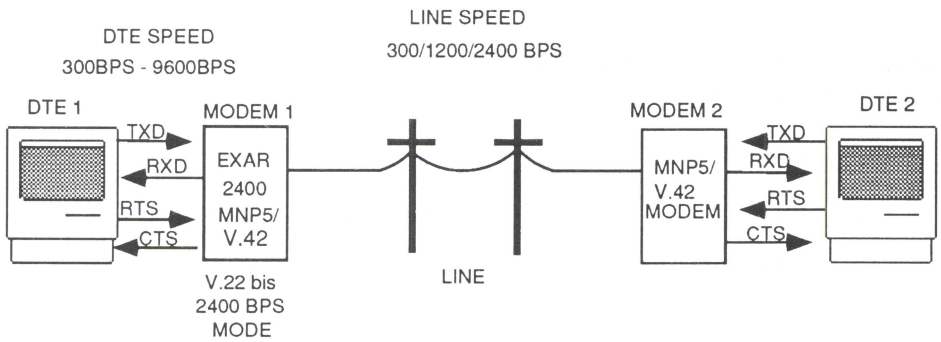


Figure 2. Basic Modem Test Configuration For Throughput

COMMAND	DESCRIPTION / RANGE - SIZE
A/	Execute previous command, without striking <CR> key
AT	Attention
ATA	Answer Immediate
ATB0	CCITT V.22 mode
ATB1	Bell 212A mode **DEFAULT**
ATB2	V.23 mode
ATD	Dial Command
ATDP	Dial Using pulse dial
ATDT	Dial Using DTMF tone dial **DEFAULT**
The following 8 modifiers will dial using the previously used technique (pulse or tone), or the T or P command can be added after the D (dial) command. 0-9 A B C D * #	
ATDW	Wait for Dial Tone for Period Set by S7 Register
ATD@	Quiet Answer: Wait for 5 Seconds of Silence Before Dialing
ATD!	Hookflash: Commonly Used PBX Systems
ATDR	Reverse Answer Mode
ATDS=n	Dial Stored Number when n= 0-3
ATD/	Wait 0.125 Seconds
ATD;	Return to Command Mode After Dialing
ATD,	Pause for Time Set by S8 Register
ATE0	Command Echo Disabled
ATE1	Command Mode Echo Enabled **DEFAULT**
ATH0	Go On Hook (Open Relay)
ATH1	Go Off Hook (Close Relay)
ATI0	Identification Code
ATI1	Identification Code
ATI2	"OK" Response if Checksum Verifies
ATI3	EXAR EPROM Revision Date
ATL0	Lowest Volume Setting
ATL1	Same as ATL0
ATL2	Medium Volume Setting **DEFAULT**
ATL3	Maximum Volume
ATM0	Speaker Always Off
ATM1	Speaker On Until Carrier Is Detected **DEFAULT**
ATM2	Speaker Always On
ATM3	DTMF Tones are not Heard, but Speaker is on Until Carrier Detected
ATO	Originate Immediate or Return to Data Mode
ATO1	Request a Retrain When in V.22bis Mode
ATQ0	Provide Result Codes **DEFAULT**
ATQ1	Disable Result Code
ATSn?	Provide S Register Value
ATSn=	Set S Register Value
ATV0	Terse (and Verbose) Responses, affected by \Vn

NUMERIC	DESCRIPTION / RANGE - SIZE	
		\V1
0	OK	Command Executed
1	CONNECT	Connection at 0 to 300 BPs
2	RING	Ring Signal Detected
3	NO CARRIER	Carrier Signal not Detected
4	ERROR	Error
5	CONNECT 1200	Connection at 1200 BPS
6	NO DIALTONE	No DialTone Detected
7	BUSY	Busy Signal Detected
8	NO ANSWER	No Silence Detected
10	CONNECT 2400	Connection at 2400 BPS
11	CONNECT 4800	Connection at 4800 BPS
12	CONNECT 9600	Connection at 9600 BPS
14	CONNECT 19200	Connection at 19200 BPS
		\V1
22	CONNECT 1200/REL 4	MNP Class 4 Link
22	CONNECT 1200/REL 5	MNP Class 5 Link
23	CONNECT 2400/REL 4	MNP Class 4 Link
23	CONNECT 2400/REL 5	MNP Class 5 Link
22	CONNECT 1200/V.42	V.42 Link
23	CONNECT 2400/V.42	V.42 Link

COMMAND	DESCRIPTION / RANGE - SIZE
ATV1	Verbose Response **DEFAULT**. See ATV0 for Responses
ATX0	Enable Result Codes 0-4
ATX1	Enable Result Codes 0-5, 10
ATX2	Enable Result Codes 0-6, 10
ATX3	Enables Result Codes 0-5 and 7 and 10
ATX4	Enables Result Codes 0-10 **DEFAULT**
ATY0	Disable Long Space Disconnect **DEFAULT**
ATY1	Enable Long Space Disconnect
ATZ0	Software Reset, Restore S Register from profile location 0 in NVRAM
ATZ1	Restore S Registers From Profile Location 1 in NVRAM
AT&C0	EIA Carrier Line Always Forced on **DEFAULT**
AT&C1	EIA Carrier Line Follows Data Carrier
AT&D0	DTR Always on **DEFAULT**
AT&D1	Modem Goes to Command Mode When DTR Goes Off
AT&D2	Modem Goes on HOOK and Returns to Command Mode When DTR Goes Off
AT&D3	Modem Initializes When DTR Goes Off
AT&F	Fetch S Registers From EPROM for Factory Default
AT&G0	No Guard Tone **DEFAULT**
AT&G1	550 Hz Guard Tone Enabled
AT&G2	1800 Hz Guard Tone Enabled
AT&J0	RJ-11 Select **DEFAULT**
AT&K0	Flow Control Disabled
AT&K1	No Function
AT&K2	No Function
AT&K3	RTS/CTS Flow Control **Default**
AT&K4	Xon/Xoff Flow Control
AT&K5	Xon/Xoff Pass Through
AT&L0	Switched Line Select **DEFAULT**
AT&L1	Leased Line Select
AT&M0	Asynchronous Mode **DEFAULT**
AT&M1	Synchronous Mode With Asynchronous Dial
AT&M2	Synchronous Mode and Dial the Stored Number Immediately
AT&M3	Synchronous Mode With DTR Controlling Data/Talk
AT&P0	US Make/Break Ratio For Pulse Dialing **DEFAULT**
AT&P1	UK Make/Break Ratio For Pulse Dialing
AT&Q0	Direct mode (same as Hayes)
AT&Q1	Same as &M1
AT&Q2	Same as &M2
AT&Q3	Same as &M3
AT&Q5	Error Control Mode
AT&Q6	Normal Mode
AT&R0	Clear To Send (CTS) Follows RTS **DEFAULT**
AT&R1	CTS Always On
AT&S0	Data Set Ready (DSR) Always on **DEFAULT**
AT&S1	DSR Normal
AT&T0	Terminate Test in Progress **DEFAULT**
AT&T1	Initiate Local Analog Loopback For Time Set by Register S18

COMMAND	DESCRIPTION / RANGE - SIZE
AT&T2	Not Defined
AT&T3	Initiate Digital Loopback for Time Set by Register
AT&T4	(Not Supported)
AT&T5	Disable Remote Digital Loopback (RDLB) Response
AT&T6	Initiate RDLB
AT&T7	Initiate RDLB with Self Test
AT&T8	Initiate ALB with Self Test (for Direct / Normal Mode only)
AT&W0	Write User Profile 0 into NVRAM
AT&W1	Write User Profile 1 into NVRAM
AT&X0	Modem Provides Transmit Clock
AT&X1	DTE Supplies Transmit Clock (Not Supported)
AT&X2	Slave Clock Mode (Not Supported)
AT&Y0	Power Up Recall User Profile 0
AT&Y1	Power Up Recall User Profile 1
AT&V	List Configuration both Active and Stored
AT&Z m=An	Store Telephone Number into NVRAM (XL93C46) where: *m* is the number location (0-3) *A* is *P* or *T* (Pulse or Tone) *n* is the telephone number

COMMAND	LAPM Yes/No	DESCRIPTION/RANGE - SIZE	FUNCTION
AT\M0*	Y	LAPM Enabled	Attempt LAPM Negotiation
AT\M1	N	LAPM Disabled	Do Not Attempt LAPM Negotiation
AT \ N0	Y	Normal	
AT \ N1	Y	Direct	
AT \ N2	Y	MNP 2-5/Reliable	
AT \ N3	N	MNP 2-5/Auto Reliable	
AT \ N4	Y	V.42 Mode	
AT \ N5	Y	V.42 Mode Auto Reliable	
AT \ N6	Y	V.42 / MNP 2-5 Reliable	
AT \ N7*	Y	V.42 / MNP 2-5 Auto Reliable	
AT \ A0	N	64 Characters	Transmit Block Size
AT \ A1	N	128 Characters	
AT \ A2	N	192 Characters	
AT \ A3*	N	256 Characters	
AT%An	Y	n = 0-127 ASCII	Auto-Reliable Fallback Character
AT \ L0*	N	Stream Link	Block MNP Link
AT \ L1	N	Block Link \L1 = \L0	(Stream Mode)
AT \ O	N	Initiate Reliable Link After Escape Command Independent of Modem Initial mode (ANS or ORG)	Originate Reliable Link
AT \ U	N	Accept Reliable Link after Escape Command request from Initiator of Link	Accept Reliable Link
AT \ Y	N	Establish Reliable Link after Connecting in Normal Mode	Switch to Reliable Mode
AT \ Z	N	Switch to Normal Mode After Establishing a Reliable Link	Switch to Normal Mode
AT % C0	Y	Compression Disabled	Compression On/Off Control
AT % C1*	Y	Compression Enabled	
AT \ V0	Y	Standard Non-MNP Result Codes	Result Code Form
AT \ V1*	Y	Modified MNP Result Codes (As Listed Below)	
AT \ Bn	Y	N = 0 - 9 (100ms Increments) Used in Normal Mode Default = 3, Error Control Mode Always 300ms	Transmit Break for Normal Data Mode
AT \ C0*	Y	Does not buffer Data Default	Set Auto-Reliable Buffer Break Control
AT \ C1	Y	Buffers All Data on Answering Modem until 200 Characters (Non-Sync) are Returned	
AT \ C2	Y	Does Not Buffer Data on Answering Modem, according to % An to fall back	
AT \ K1	Y	"Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed	Break Control for Reliable Data Mode

COMMAND	LAPM Yes/No	DESCRIPTION / RANGE - SIZE	FUNCTION
AT \ K3	Y	"Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained	
AT \ K5*	Y	"In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break	
AT \ K0,2,4	-	Not Supported (Will be equal to AT \ K5 if selected)	
AT \ Tn	Y	N = 0-90 min N* = 0 (disable)	Inactivity Timer
%D0*	Y	Hang up without clearing buffer	
%D1	Y	Clear the receive buffer before hang up	
AT \ I	-	Not Functional	Interface Protocol
AT \ J0*	Y	BPS Rate Adjust Disabled	Speed Conversion Control Disable
AT \ J1	Y	BPS Rate Adjust Enabled	Modem Port Rate Adjustment
AT \ S	Y	List Profiles	
AT \ G0*	Y	Disables Modem Port Flow Control	Set Modem Port
AT \ G1	Y	Sets Modem Port Flow Control to Xon / Xoff	Flow Control
AT \ X0*	Y	Does Not Pass Xon / Xoff to Remote Modem	Xon / Xoff Pass Through Control
AT \ X1	Y	Passes Xon / Xoff to Remote Modem	
AT \ Q0	Y	Disable Flow Control	Serial Port Flow Control
AT \ Q1	Y	Bidirectional Xon / Xoff Enabled	
AT \ Q2*	Y	Unidirectional Hardware Control by CTS	
AT \ Q3	Y	Bidirectional Hardware Control by RTS / CTS	
AT \ Q4	Y	Unidirectional Xon /Xoff Send Only	
AT \ Q5		Keep CTS off until connect unidirectional hardware flow control	
AT \ Q6		Keep CTS off until connect bidirectional hardware flow control	
AT % U	Y	Not Functional	Clear Serial Port Speed Serial Port
AT - P0*	Y	Ignores Parity for Special Characters	Check Parity
AT - P1	Y	Processes Special Characters Only if they have Correct Parity	

*Note: * Denotes Default Condition*

See Command AT \ V1 Above

STANDARD RESULT CODES\V0			MODIFIED RESULT CODES \V1	
Verbose	**Numeric**		**Verbose**	**Numeric**
CONNECT	1			
CONNECT 1200	5		CONNECT 1200 / REL 4 or 5	22
CONNECT 2400	10		CONNECT 2400 / REL 4 or 5	23
CONNECT 4800	11			
CONNECT 9600	12		CONNECT 1200/V.42	22
CONNECT 19200	14		CONNECT 2400/V.42	23

S	REGISTER FUNCTION
S0	Number of Rings to Answer: **Default** = 0 (no answer)(stored)
S1	Ring Count: Stores Number of Rings: Resets After Every Call
S2	Escape Code Character: **Default** = 043 (ASCII for "+")
S3	Carriage return Character: **Default** = 013
S4	Line Feed Character: **Default** = 010
S5	Back Space Character: **Default** = 008
S6	Wait for Dial Tone: **Default** = 002 (seconds) (minimum setting)
S7	Wait for Carrier After Dial: **Default** = 030 (seconds)
S8	Duration of Delay for Comma: **Default** = 002 (seconds)
S9	Carrier Detect Response Time: **Default** = 0.6 (seconds)
S10	Loss of Carrier Response Time **Default** = 1.4 (seconds)
S11	Touch Tone Duration: **Default** = 095 (milliseconds)
S12	Escape Code Guard Time: **Default** = 1 (second)
S13	Reserved
S14	Bit Mapped Register: Stored in NVRAM (XL93C46) Bit 0 Reserved Bit 1 Echo Bit 2 Result Codes Bit 3 Numeric Result Codes Bit 4 Always 0 Bit 5 Tone/Pulse Dialing Bit 6 Reserved Bit 7 Answer/Originate
S15	Reserved
S16	Test Register Bit 0 ALB Bit 1 Reserved Bit 2 Local Digital Loopback Bit 3 Remote Digital Loopback (Not Supported) Bit 4 Initiate Remote Test Bit 5 Initiate Remote Test With Self Test Bit 6 Analog Loopback With Self Test Bit 7 Reserved
S17	Reserved
S18	Test Time Stored in NVRAM (XL93C46) Default = 000 (seconds)
S19	Reserved
S20	Reserved
S21	Bit Mapped Register Stored in NVRAM (XL93C46) READ ONLY Bit 0 0 = RJ11 Jack Bit 1 Not Used Bit 2 CTS RTS Function Bit 3 DTR Function Bit 4 DTR Function Bit 4 / Bit 3 / Function 0 / 0 / DTR Always True Default 0 / 1 / DTR Off, Forces Command State 1 / 0 / DTR Off, Forces Modem Offline 1 / 1 / Modem Initializes With DTR OFF (ATZ)

REGISTER NUMBER	REGISTER FUNCTION
	Bit 5 EIA Carrier Status Bit 6 Bit 7 Guard Tone Select Bit 7 Bit 6 Function 0 0 No Guard Tone Default 0 1 550 Hz Guard Tone 1 0 1800 Hz Guard Tone 1 1 Reserved
S22	Option Bit - Mapped Register Bit 0 Determines Speaker Volume Bit 1 Bit 1 Bit 0 Speaker Volume 0 0 Low 0 1 Low 1 0 Medium Default 1 1 High Bit 2 Determines the Speaker Status Bit 3 Bit 3 Bit 2 Speaker Status 0 0 Always Off 0 1 On Until Carrier is Detected Default 1 0 Always On 1 1 As '01', Except Off for Dialing Bit 4, 5 and 6 Determine Response Messages Bit 6 Bit 5 Bit 4 Message 0 0 0 Basic Message Set 1 0 0 Extended with Connect 1200 and Connect 2400 1 0 1 Extended with 'No Dial Tone' 1 1 0 Extended with 'Busy' 1 1 1 Extended with All Messages Default Bit 7 Determines Off Hook/On Hook (Make/Break) Ratio for Pulse Dialing Bit 7 Ratio 0 39/61 (USA and Canada) Default 1 33/67 (UK and Hong Kong)
S23	Option Bit Mapped Register (LSB) Bit 0 Not Supported Bit 3 Bit 2 Bit 1 0 0 0 300 0 0 1 Not Used 0 1 0 1200 0 1 1 2400 1 0 0 4800 1 0 1 9600 1 1 0 19200 1 1 1 38400(reserved) Bit 4 Determines the Parity for Transmitting and Receiving Data

REGISTER NUMBER	REGISTER FUNCTION
	Bit 5 Bit 5 Bit4 Parity 0 0 Even Default 0 1 Space/None 1 0 Odd 1 1 Mark Bit 6 Determines Guard Tone Frequency Bit 7 (Used in European Applications) Bit 7 Bit 6 Guard Tone (Hz) 0 0 Disabled Default 0 1 550 1 0 1800 1 1 Reserved
S24	Not Used
S25	Delay to DTR (Stored in NVRAM) Default = 005 (seconds)
S26	RTS to CTS Delay (Synchronous Mode Only) Default = 1 (milliseconds)
S27	Bit Mapped Register STORED IN NVRAM Bit 0 Bit 1 Transmission Mode Bit 1 Bit 0 Function 0 0 Asynchronous Mode Default 0 1 Synchronous Mode 1 1 0 Synchronous Mode 2 1 1 Synchronous Mode 3 Bit 2 Reserved Bit 3 Reserved Bit 4 Bit 5 Transmission Mode Bit 5 Bit 4 Function 0 0 Internal Modem Clock Used Default 0 1 DTE Supplied Clock 1 0 Slave Clock Mode 1 1 Same as 00 Bit 6 CCITT or Bell Handshaking Standard 0 CCITT 1 Bell (including CCITT V.22bis) Default Bit 7 Reserved
S28-35	Reserved
S36	Negotiate Failure Fallback (Affected by %C and \N) Bits 0 Hang Up 1 Attempt a standard asynchronous connection (&Q0) 3 Attempt an asynchronous connection using automatic speed buffering (&Q6) 4 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails, attempt a standard asynchronous connection 5 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails attempt a standard asynchronous connection
S37	Not Supported

REGISTER NUMBER	REGISTER FUNCTION
S38	Not Supported
S39	Reserved
S40	Not Supported
S41	Not Supported
S43-45	Reserved
S46	Protocol Selection: Bits 136 LAPM only (V.42)
S47	Not Supported
S48	Feature Negotiation Action 0 Negotiation disabled; presume the remote modem is configured for and has the capabilities necessary for the connection selected with S46 3 Negotiation enabled, but originating modem remains silent during detection phase. For connections with MNP modems; defeats connection sequence with other V.42 modems 7 Negotiation enabled 128 Negotiation disabled; forces fallback options specified in S36 to be taken immediately
S82	Break Handling: Affected by \K commands 3 "Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained 7 "Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed 128 "In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break
S86	Not Supported

Special Notes regarding the use of S registers above S27 and AT/n Commands.

1. Changes of S register values above S27 will effect the profile display for AT/n Commands. AT/n Commands however, do not modify the setting of S registers.

2. It is intended that a user or application software package will use only one method (S register \ n Commands) to effect the error control functions. Use of a combination could result in unpredictable behavior.

APPLICATIONS INFORMATION

The XR-2442 is shown in the XR-2400 modem schematic. The XR-2442 provides the command controller function for the XR-2400 V.22bis modem chip set, providing a high quality 2400 BPS modem. The modem operates error-free through LAPM or MNP 2-4 modes and can offer increased throughput with MNP 5. The XR-2321 device included adds CCITT V.21 and V.23 FSK modes, optional and can be eliminated for designs not requiring these modes.

Detailed information for the XR-2400 is available in XR-2400 V.22bis modem chip set datasheet. **Note** that the Analog Front End (AFE) used in this design is the XR-2402A. This device is an improved, pin-to-pin replacement for the XR-2402, details available in its own datasheet.

Layout Hints

In order for the XR-2442 to provide optimal support for best performance of the modem, some design hints/rules should be followed.

- Locate the XR-2402A AFE near the DAA section
  - provide for a short transmit / receive carrier input path, away from Bus/Digital lines.
- Maintain separate analog and digital grounds/ power lines back to the power supply sources.
- Bypass (capacitor decouple) the XR-2401, XR-2402A, XR-2442 and op amp power supplies with both 0.01µF ceramic and 0.47µF tantalum capacitors near their actual pins. Ensure analog/digital supplies are bypassed to their respective ground.
- Crystal - parallel resonant type. Typical loading capacitors are 18pF.

SYSTEM PERFORMANCE

Performance for an error-correcting modem has two major areas.

1) DATA PUMP PERFORMANCE
With error-correction capabilities turned off, the integrity of the data pump to pass data in the presence of impairments. Most often the major specification measured here is the probability of data errors with the receive carrier impaired by noise, or BER (bit error rate) vs S/N (Signal-to-Noise ratio).

Figure 3 shows BER vs S/N for the circuit in the XR-2400 modem schematic, as measured with the test set-up in Figure 4.

2) ERROR CONTROLLER PERFORMANCE
The XR-2442, when in LAPM or MNP modes provides the control and correction required to yield perfect data transfer.

Beyond error correction, throughput, or data transfer rate, is another important parameter to the modems overall performance.

LAPM and MNP 2-4 Modes are not specifically provided for increased throughput. However an additional benefit of their error-correcting schemes is roughly a 20% increase in throughput. Using the 'Quick Brown Fox....' pattern, both LAPM and MNP 4 modes yielded better than a 20% throughput increase. V.22bis mode was used for this test, with an actual throughput of better than 2900 BPS measured.

MNP 5 Data Compression Included in the XR-2442 allows roughly a 100% throughput increase over the modems nominal data rate. As previously discussed, the throughput performance of MNP 5 varies with different types of data. (Figure 5 shows data for various data patterns). (Figure 6 illustrates the test set-up used for measuring the XR-2400 modem performance).

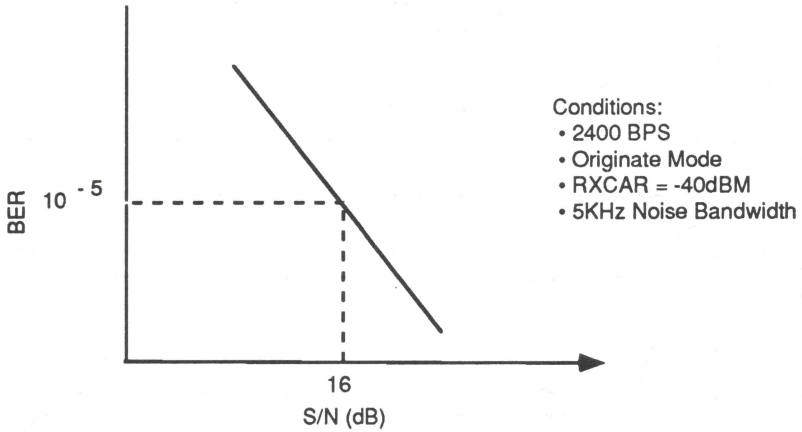


Figure 3. 2400 BPS Ber vs. S/N (Non-Error Correcting)

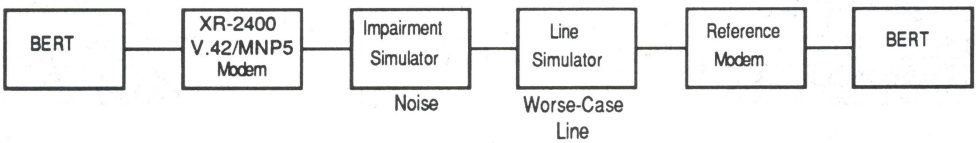


Figure 4. Data Quality Test Set-Up

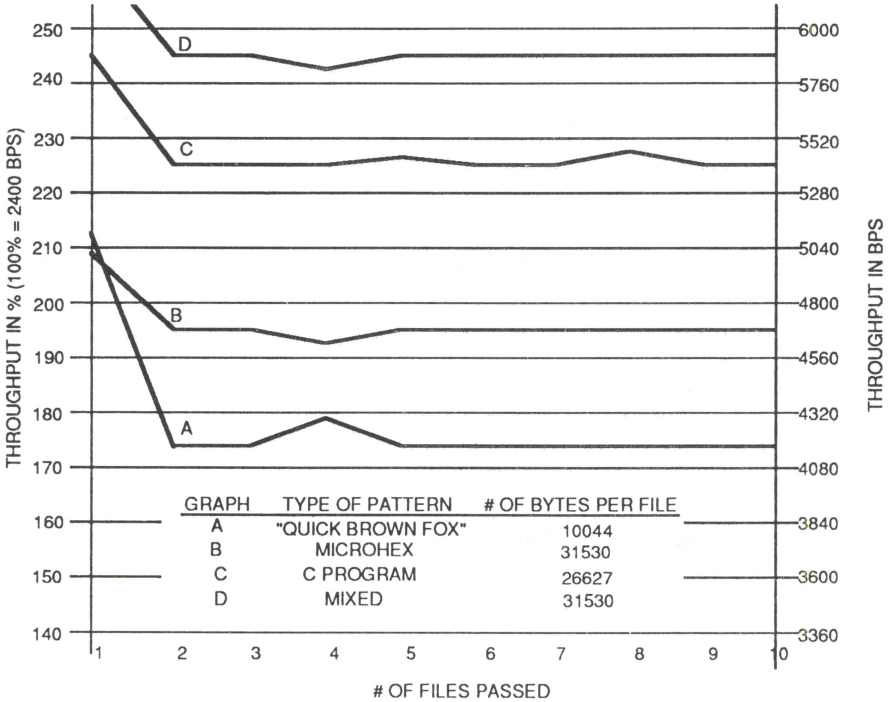
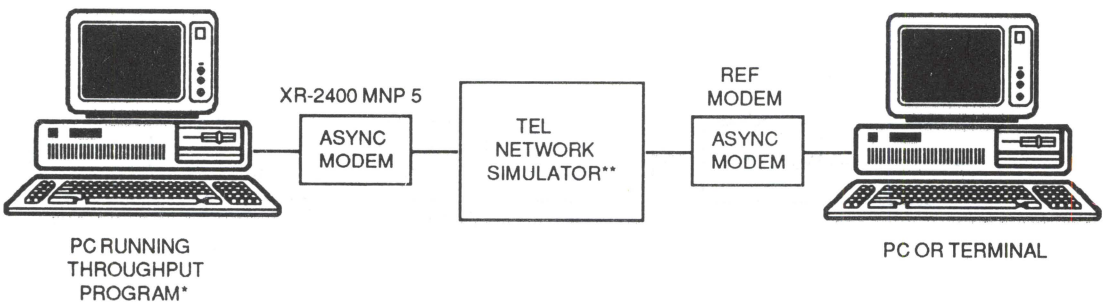
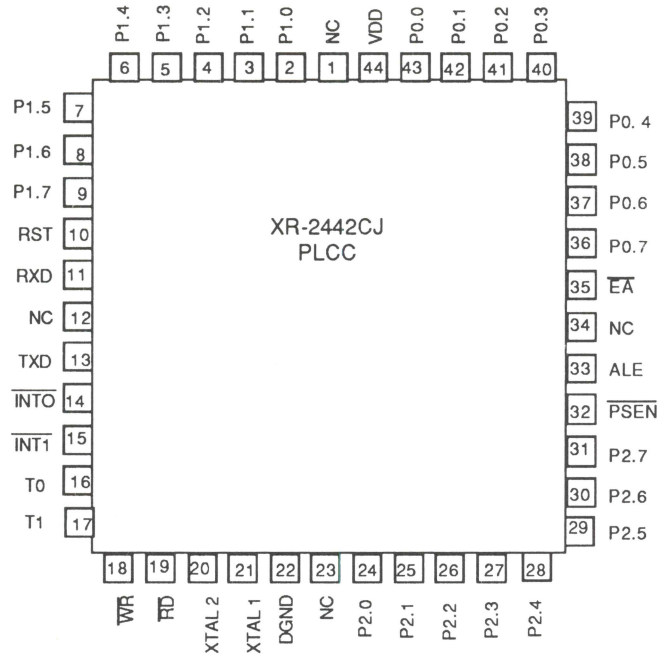


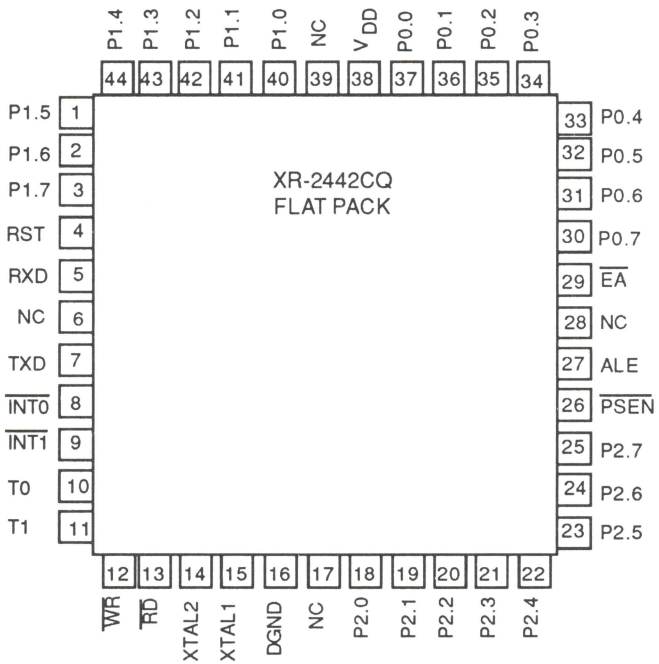
Figure 5. Effective Data Throughput



* APT (Asynchronous Performance Tester), also contains data or files to be used during measurement. Product of Concord Data Systems.
** Simulates line impairment and attenuation conditions.

Figure 6. MNP5 Throughput Measurement Test


XR-2442CJ
PLCC
P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0 43
P0.1 42
P0.2 41
P0.3 40
P1.5 7
P1.6 8
P1.7 9
RST 10
RXD 11
NC 12
TXD 13
INTO 14
INT1 15
T0 16
T1 17
39 P0. 4
38 P0.5
37 P0.6
36 P0.7
35 EA
34 NC
33 ALE
32 PSEN
31 P2.7
30 P2.6
29 P2.5
18 WR
19 RD
20 XTAL 2
21 XTAL 1
22 DGND
23 NC
24 P2.0
25 P2.1
26 P2.2
27 P2.3
28 P2.4


XR-2442CQ
FLAT PACK
P1.4 44
P1.3 43
P1.2 42
P1.1 41
P1.0 40
NC 39
VDD 38
P0.0 37
P0.1 36
P0.2 35
P0.3 34
P1.5 1
P1.6 2
P1.7 3
RST 4
RXD 5
NC 6
TXD 7
INT0 8
INT1 9
T0 10
T1 11
33 P0.4
32 P0.5
31 P0.6
30 P0.7
29 EA
28 NC
27 ALE
26 PSEN
25 P2.7
24 P2.6
23 P2.5
12 WR
13 RD
14 XTAL2
15 XTAL1
16 DGND
17 NC
18 P2.0
19 P2.1
20 P2.2
21 P2.3
22 P2.4



NOTES



XR-2443 Modem Microcontroller with V.42bis

GENERAL DESCRIPTION

The XR-2443 is a dedicated microcontroller that provides command control for the XR-2400 V.22bis modem chip set. The XR-2443 provides control for CCITT recommended V.42 error correction, including LAPM and MNP 2-4 protocols, with V.42bis BTLZ / MNP 5 data compression. Also supported is the complete AT command set and registers used to control these functions.

The system architecture of the XR-2443 allows the actual command sets for the 'AT', MNP, LAPM and V.42bis to reside external to the XR-2443, allowing ease of customization. Exar provides these command sets to use as is, or the customer can modify to the requirements of the design.

The XR-2443 operates from a single +5 volt power supply, offering low power consumption through CMOS technology.

FEATURES *

V.22bis/V.22/Bell 212A /Bell 103 Modem
Error Free Data Transfer: DATA Mode
- LAPM
- MNP 2-4

MNP Class 5 Data Compression
- 4800 BPS Throughput

Increased Data Throughput by V.42bis Data Compression
- 9600 BPS Throughput

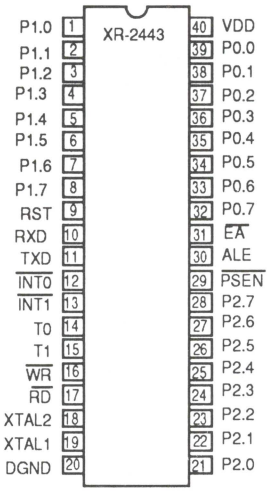
'AT' Command Control
- Easily Modified, Exar Supplied 'AT'/MNP/V.42/V.42bis

(Apply when used with XR-2400 V.22bis modem chip set)

APPLICATIONS

Error Free Data Modem Applications
Stand-Alone Data Modems
Smart Modems
Laptop Modems (Send and Receive error free Data)
Networked Modems

PIN ASSIGNMENT



(For other pin assignment diagrams, refer to the end of this datasheet)

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2443CP	40 Pin Plastic Dip	0°C to 70°C
XR-2443CJ	44 Pin PLCC	0°C to 70°C
XR-2443CQ	44 pin QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7V
Input Voltage	-0.7V to (VDD +0.3V)
DC Input Current (any input)	±10mA
Power Dissipation **(Package Limitation)**	1W
Derate above 25°C	11 mW/°C
Storage Temperature Range	-65°C to +150°C

SYSTEM DESCRIPTION

The XR-2443, when coupled to the XR-2400 V.22bis modem chip set, allows the implementation of a 2400 BPS V.22bis modem. With MNP/V.42/V.42bis operation included, compressed and error-free operation is provided.

The XR-2443 is just one in the family of controller options for the XR-2400 V.22 bis modem chip set, including:

FUNCTION	CONTROLLER
'AT'	8031
'AT'/MNP 2-5	XR-2403B
'AT/V.42/MNP 5	XR-2442
'AT'/V.42/V.42bis/MNP 5	XR-2443

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V ±10%, F_{CLK} = 11.0592MHz ±0.05%, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}	Power Supply Voltage	4.5	5	5.5	V	
I_{DD}	Power Supply Current		18	22	mA	
V_{IH}	Input High Voltage	1.8			V	Except XTAL1 and RST
V_{IH}	Input High Voltage	3.5			V	XTAL 1 and RST
V_{OH}	Output High Voltage	2.4			V	Ports 1,2,3 I_{OH} = -60µA
V_{OH}	Output High Voltage	2.4			V	Port 0 (External Bus Mode) ALE, $\overline{PSEN}$ I_{OH} = -800 µA
V_{OL}	Output Low Voltage			0.45	V	Ports 1,2,3 I_{OL} = 1.6 mA
V_{OL}	Output Low Voltage			0.45	V	Port 0, ALE, $\overline{PSEN}$ I_{OL} = 3.2 mA
I_{IH}	Input High Current (Leakage)			±10	µA	0.45V ≤VIN ≤V_{DD}
I_{IL}	Input Low Current			-50	µA	V_{IN} = 0.45V

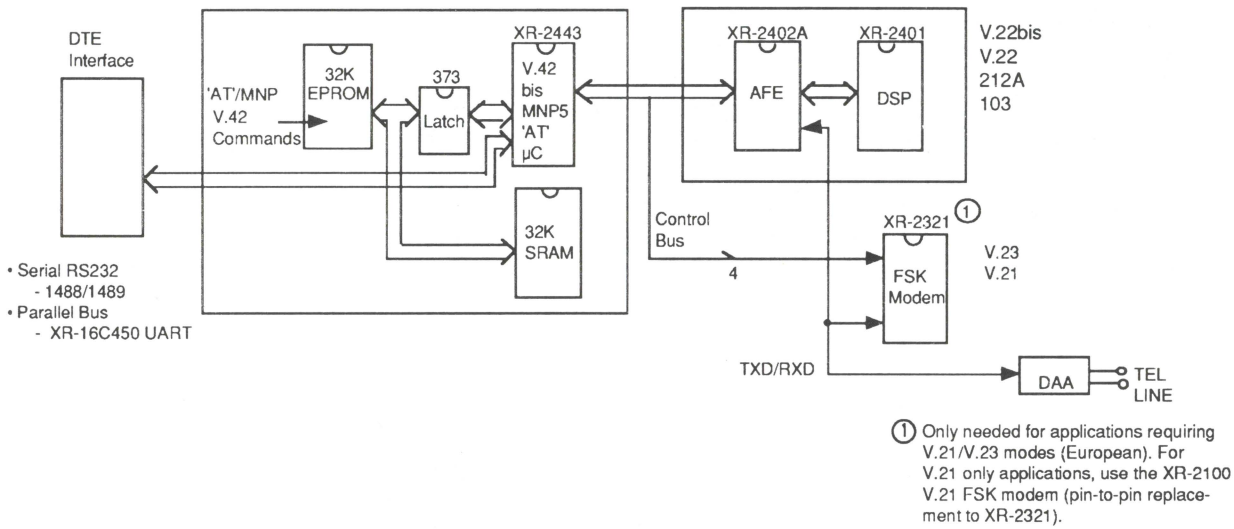


Figure 1. 2400 BPSP Modem with V.42 bis / MNP 5 Block Diagram

SYSTEM OPERATION

A typical application utilizing the XR-2443 to support the XR-2400 V.22bis modem chip set, is shown in Figure 1. The XR-2400 provides the complete modem data pump function for:

CCITT	V.22bis	2400 BPS
	V.22	1200 BPS
	*V.23	1200BPS / 75 BPS
	*V.21	300 BPS
Bell	212A	1200 BPS
	103	300 BPS

** Supported by the XR-2321*

Command control is supported by the XR-2443 for:

MNP 2-4	Microcom Error Correction
MNP 5	Microcom Data Compression
LAPM	CCITT Recommended V.42 Error Correction
BTLZ	British Telecom Lempel Ziv (V.42bis)
'AT'	Industry Standard 'AT'

Although the XR-2443 does provide complete command control, the actual commands for the various modes reside in an external EPROM - 27C256, 32k Byte. With this architecture and an EXAR supplied command set, maximum flexibility is offered. The command set can be used as is, or customer tailored to a particular design.

The unique architecture utilized by the XR-2400 and command controller allow the **same** hardware (Printed Circuit Board (PCB)) to support several different types of Data modems, including an upgrade to FAX/DATA. By changing available pin-to-pin microcontrollers, the Data modem types listed in Table 1 are all possible with the same printed circuit board. As mode types are changed by the µC, EPROM supported command sets and SRAM size change and/or elimination are also required. In each case EXAR provides complete production worthy, command sets which may be used as is, or easily modified to meet specific application requirements. To aid in software modifications, Tables 2, 3 and 4 list the XR-2443 memory mapping, indicating customer usable regions.

External memory modifications requiring µC (XR-2443) support will need entry/re-entry point information. This point is important as the XR-2443 contains program memory with EXAR proprietary V.42bis /V.42/MNP5 functions not accessible externally (fusible link protected) or available to EXAR customers.

2400 BPS Modem Type	Microcontroller Part Number	External Memory Requirements (Bytes)	
		EPROM	SRAM
'AT'	8031 (Generic ROMLESS µP)	16k	NONE
'AT / MNP 2-5	XR-2403B	16k/32k	8k
'AT' / MNP5/V.42	XR-2442	32k	8k / 32k
'AT'/MNP5/V.42/ V.42bis	XR-2443	32k	32k

ENTRY POINTS AND MEMORY MAPPING

Status / Mode Setting Memory Locations

Status	Location	Description
SPD_FLG	20 H.7	Speed Conversion Enable Flag.
BK_PRE	51 H	Break Prescaler Timer
BK_TMR	52 H	Break Timer (Only in Normal Mode)
MRCVP2	803BH	Disconnect to Check Auto-Reliable Fallback Mode.
PASS_ B	9D14H	Escape Code Checking Byte in Speed Conversion Mode.
SPEED	9D15H	Speed Indicator For All Modes. 0-19200 BPS (not used) 1 - 9600 BPS 2 - 4800 BPS 3- 2400 BPS 4 - 1200 BPS 5 - 300 BPS
Z_BUF	9D16H	Auto Reliable Fallback Character.
BACK_RAM	9D1AH	Starting Address for Command Buffer Back-up.
OPT_P	9D50H	Output Port Selection Option (F0FF H to 40 FFH).This Parameter is Initialized Immediately After Power On and constantly monitored by MNP Module.
MNP_S	9E22H	Reliable Link Indicator
RETRAN	24H.0	Retransmission Bit

Function Call Locations - V.42bis/V.42/ MNP 5

Function	Location	Description
SCTINT_1	0006H	Interrupt 0 Jump-In Point.
SCRINT_1	0016H	Interrupt 1 Jump-In Point.
SPINT_1	0026H	Serial Port Interrupt Jump-In Point.
MSG_CP	0030H	Exar Copyright Message.
P_ECRAM_1	0060H	After Escape MNP Re-Entry Point.
MSG_CPY	0063H	Exar Copyright Calling Subroutine.
MNP_IN	0066H	MNP Program Immediate Re-Entry Point for modifying MNP Program.
SPD_INM	0069H	Speed Conversion Program Jump-In Point.
INI_SPDM	006CH	Speed Conversion Initialization Routine.
V21_IN_1	006FH	300 BPS Speed Conversion Timer Set-Up.
EC_MAIN	0080H	Calling Main MNP Program. This is the only location which will initiate the MNP program.

XR-2443 Re-Entry Points

Function	Location	Description
PWR_ONS	C000H	Power On
OUT_SCT	C003H	Interrupt 0
OUT_T0	C006H	Timer 0
OUT_SCR	C009H	Interrupt 1
OUT_T1	C00CH	Timer 1
OUT_SP	C00FH	Serial Port Interrupt
OUT_T2	C0012H	Timer 2
MNP_OUT	C0015H	MNP Program Intermediate Point
CHK070S	C01BH	MNP 'ESC' Jump Out Point
DISCONNECT	C01EH	MNP Disconnect
ON_LOOPS	C021H	Auto-Reliable Fallback Point
SPD_OUTS	C024H	Speed Conversion Jump Out Point.
V21_INS	C027H	Call Speed Conversion ASM for 300 BPS.
SPD_TXD	C02AH	Put TXDATA to Modem Chip
SPD_RXD	C02DH	Get RXDATA From Modem Chip
I_TXSYNTTQ	C030H	GET TX CRC-CCITT CALCULATION ROUTINE
I_RXSYNTT	C033H	GET RX CRC-16 CALCULATION ROUTINE
I_TXASYN16	C036H	GET TX CRC-16 CALCULATION ROUTINE
I_RXASYN16	C039H	GET RX CRC-16 CALCULATION ROUTINE
I_SNDREL	C03CH	GET SENDING RESULT CODE SUBROUTINE
I_MNPINIT	C03FH	MNP PARAMETER INITIALIZATION ROUTINE
I_V42INIT	C042H	V42 PARAMETER INITIALIZATION ROUTINE
I_SETURMNP	C045H	UART SETTING ROUTINE
I_ENCODE	C048H	BTLZ ENCODING ROUTINE
I_DECODE	C04BH	BTLZ DECODING ROUTINE
I_BTFLUSH	C04EH	BTLZ DATA FLUSHING ROUTINE
I_BTINIT	C051H	BTLZ COMPRESSION INITIALIZATION

RAM Locations

The stack in the 'AT' program starts from 0C0H on page 1 and occupies 64 bytes of space. Internal RAM on page 0 has 23 bytes and page 1, 64 bytes of free space.

The external RAM data memory is as follows:

1)	Error Control	8000H-8FFFH
2)	Data Compression Buffer	9000H-93FFH
3)	FAX/Remote Access	9400H-99FFH
4)	Available for use	9600H-97FFH
5)	V.42 / V.42bis	9800H-99FFH
6)	Break Buffer	9A00H-9AFFH
7)	DTE TX Buffer	9B00H-9BFFH
8)	DTE RX Buffer	9C00H-9CFFH
9)	Misc. Registers	9D00H-9DFFH
10)	MNP Program RAM Backup Buffer	9E00H-9EFFH
11)	'AT' Program RAM Backup Buffer	9F00H-9FFFH
12)	BTLZ Compression Dictionary	C000H-FFFFH

Note: For program control, the XR-2443 backs up the entire 256 bytes of internal RAM into external RAM before jumping into or out of the MNP program. The 'AT' program RAM is from 9F00H to 9FFFH and MNP program RAM is 9E00H-9EFFH.

The miscellaneous register function list is provided below. The option code control allows the firmware engineer to change the factory defaults in source code and then reassemble.

Interrupt Vectors

The XR-2443 brings out all interrupt vectors to the external program. This allows easy customer modification of service routines to suit a particular application. The interrupt vectors of the XR-2443 are as follows:

```
        ORG   0
        LJMP  PWR_ONS;Jump to Power
                      On Set Up Routine
        ORG   3H
EXT_INTO:             ; Interrupt 0 for SCT
        LJMP  OUT_SCT
SCTINT1:
        LJMP  SCTINT
        ORG   0BH
T_INTO:               ;Timer 0 Interrupt
        LJMP  OUT_T0
        ORG   13H
EXT_INT1:             ;Interrupt 1 for SCR
        LJMP  OUT_SCR
SCRINT_1:
        LJMP  SCRINT
        ORG   1BH
T_INT1:               ;Timer 1 Interrupt
        LJMP  OUT_T1
        ORG   23H
INT_SER:              ;Serial Port Interrupt
        LJMP  OUT_SP
SPINT_1:
        LJMP  SPINT
        ORG   2BH
        T_INT2:       ;Timer 2 Interrupt
        LJMP  OUT_T2
```

XR-2443 PROGRAM/DATA MEMORY MAPS

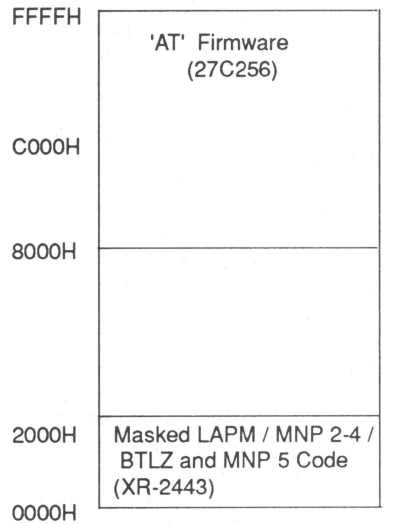
Tables 2, 3 and 4 show the ROM and RAM memory maps for XR-2443. It should be noted that without the use of separate CS (Chip Select) for the XR-2402A and the XR-2321, there would be an overlap of address locations.

As it is indicated in Table 2, 32K bytes of EPROM is assigned to 'AT' command firmware. This section of the ROM is located between 8000H and FFFFH, where chip select pin is connected to A15.

BTLZ, LAPM, MNP 2-4 and MNP 5 code is masked in the microcontroller (XR-2443), and resides in the 8K bytes of memory, between address locations 0000H and IFFFH.

Table 3 shows the RAM map, in which the space between 0000H and 002CH address locations is used for modem chip address. Table 4 shows the modem chip (XR-2402A) address assignment. Included is addressing for the XR-2321 and XR-2100. These chips are optional to the system design, but may be added where V.21 or V.23/V.21 standards are required. The XR-2321 provides both V.23 and V.21 FSK data standards, while the XR-2100 only V.21. See XR-2321 or XR-2100 datasheets for details.

Also RAM space between 8000H and FFFFH is assigned for the V.42bis dictionary and MNP 5 data. RAM locations between 002DH and 7FFFH are available for I/O ports such as LED, EIA, etc.



Note: 27256 = 32K Byte EPROM

Table 2. XR-2443 ROM Map

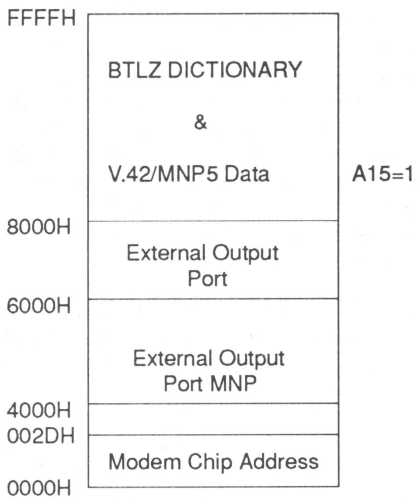


Table 3. XR-2443 RAM Map

MODEM CHIP	RAM ADDRESS	$\overline{CS}$
XR-2402A	0000H - 0003H	A15=0
XR-2321	0028H - 002CH	A5=1 and A15=0
XR-2100	0028H - 0029H	A5=1 and A15 =0

Table 4. Modem Chip Address

V.42 / MNP OPERATION

The XR-2443 when coupled with the XR-2400 V.22bis modem chip set allows the implementation of an **error-free, increased throughput** 2400 BPS data modem. To gain an understanding of V.42bis/V.42/MNP 5 modes for data operation, the following basic information has been included. A basic understanding of error correction techniques, flow control, speed buffering, and data compression will allow the designer to better understand a V.42bis/V.42/MNP5 modems capabilities and how to best utilize them. One excellent introductory book on the subject of data compression for both fax and data modes is DATA COMPRESSION by Gilbert Held. The publisher is WILEY.

V.42 is a **CCITT** recommended error correction protocol which allows asynchronous DTE's (Data Terminal Equipment) to communicate error-free with other such equipped modems.

The actual error detection protocol used in V.42 is an **HDLC** (High-level Data Link Control) based protocol called LAPM, for **Link Access Procedure for Modems.** For additional detailed information beyond the following basic description, refer to the CCITT Recommendations, Series V, 'Data Communication Over the Telephone Network'. The latest version is known as the **'Blue Book'** (Blue Covers) or Series, dated 1988 (Melbourne), a recent update from the **'Red Book'.**

V.42 Basic Operation/Features

- **HDLC**-based error correction protocol-LAPM
- Asynchronous (Async or 'start/stop') DTE Communication - error free
- Actual line transmission is synchronous (sync)- no start or stop bits (stripped from data), however initial handshake, subsequent to modem handshake is asynchronous
- Error Detection
  - Data sent in 'frames' or blocks with a nominal size (default) of 128 Octets (Octet - 8 bit) data frames.
  - Start/Stop bit elimination from data creates an actual data throughput improvement, roughly 120% of nominal. 2400 BPS becomes about 2900 BPS.
  - Encoded information added to data frame for receiver to 'decode' and determine if the block was error free. 16-bit cyclic redundancy check (CRC) methods are used for data encoded information to (1) indicate correct data and (2) recognize imperfect data frame.
  - Retransmission (automatic) of determined imperfect frames to ensure perfect data is received.

V.42 operation is found to be virtually identical (specifically to variable parameters) to that of MNP reliable or normal modes of operation. For this reason the MNP command set is also used for V.42 variables control.

DATA COMPRESSION

Two general families exist of data compression techniques. The first is logical compression, which is limited to a defined file type. It is called logical because fixed defined paths exist for the compression and decompression; e.g. year, month date, or the type of account: savings or checking. This technique would substitute a number 4 for April placing in 3 bits what would require 40 bits (7 bits and parity per character). To allow the inclusion of other months (above July, the seventh month) would require an additional bit, but the net number of bits being sent is reduced.

For compressing the type of account, a single bit would allow the encoding of either 'checking' or 'savings', rather than using the ASCII representation which would require up to 64 bits to transfer the two words. Both of these examples would require positioning limitations or the use of packets, where the location in the packet determines what logical decompression technique should be used to decode the information stored. This result is in an overhead of bits being needed to allow reliable decompression of the information.

The second technique is physical compression. This technique does not limit itself to certain types of information and files, but is more complicated to be implemented. Physical encoding compresses redundant characters substituting coded characters. As an extreme example, a page full of the letter 'a' could be sent as 'a5610', noting the fact that 5,610 'a's appear on the page. In this example the throughput would be 1122 times normal. Unfortunately, the situation to send such a large amount of compressed data does not occur too often. In addition to the encoded data, a start encoding symbol is needed to inform the decoder on the receiving side that the standard decoding technique should be used.

The two sub groups of physical compression is block encoding and stream encoding. Block encoding in general is a slower process, for it requires the entire file to be processed before sending. The use of stream encoding allows the mix of on-line information (entered by keyboard for example) and stored data. The default for the XR-2443 is stream mode. This is controlled by the \L command.

BTLZ® OPERATION

BTLZ is a patented technique to increase throughput to nearly 4 times an uncompressed file. To produce this greater performance BTLZ uses an adaptive dictionary that is partially reset from time to time to adapt to the possibly changing file. This 2-Dimensional dictionary allow for a greater compression ratio than the 1 Dimensional technique used by MNP® 5 which take ASCII codes and provide a shortened code.

The dictionary is created using data that is transmitted, therefore, no transmission time is needed to exchange dictionary data. The resetting , presetting or updating of the dictionary is under lock-step, where each deletion is predefined. Either a full reset to the first level occurs (most common letters and space character found in files), or removal of dead ends. This adaptive process provides two things. If not done, the dictionary would need to be infinite in size, for all possible data combinations (words) would have a path. In a repetitive data pattern situation this is ideal. For example, "THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG" repeated over an over would be learned by the XR-2443 using BTLZ and compression would reach the maximum set between the DTE and DCE (9.6 kBPS). However, in a real life situation such files have limited usefulness. With a typical text file, random for the short term the compression ratio is around 3.4:1.

It is this randomness that Mr. Jacob Ziv and Mr. Abraham Lempel based their compression theory upon. The idea that for short duration data transfer, a repetitive pattern can be seen, however for longer term data transfer, editing of the dictionary is needed. Their introductory paper: On the Complexity of Finite Sequences (IEEE Transactions on Information Theory, Volume IT-22 Number 1; January 1976; PP 75-81) goes into some detail as to how their compression technique was developed. This information is not needed to use the XR-2443.

British Telecom Lempel Ziv is a patented Data Compression technique used in the V.42bis standard.

MNP® OPERATION

MNP, or Microcom Networking Protocol was developed by Microcom, Inc., a modem manufacturer. Since conception, it has been in a constant state of update/improvement. For this reason 'classes' of operation emerged to signify each major update or improvement.

Relative to the V.22bis or 2400 BPS modems, up to class or level 5 has become the 'standard'. As mentioned before HDLC framing techniques are used.

MNP CLASSES

*(Throughput data is based on **2400 BPS** line speed).*

Class 1. A half duplex protocol and not included in many new designs. Throughput was about 70% or 1690BPS. The XR-2443 does not support this class.

Class 2. Asynchronous operation with byte oriented data formatting. Throughput is roughly 84% of nominal or about 2000 BPS.

Class 3. Conversion to synchronous, bit oriented data handling is transmitted in blocks consisting of 1 to 64 characters. Throughput is about 108% or 2600 BPS.

Class 4. Basic characters are the same as Class 3, but block size is dynamic, up to 256 Bytes, (flexible size is based on data transmission quality). Throughput is 120% or 2900 BPS.

Class 5. Includes Class 3 and 4 with data compression techniques added. The compression effectiveness is dependent on the type of data, but typical throughput enhancements of a text file are up to 200% or 4800 BPS.

ERROR CORRECTION

Modem users have come to expect sophisticated circuitry like adaptive equalization for varying phone characteristics and retrain modes for ensuring continued optimal performance. These techniques dramatically improve performance characteristics which is quantified by BER vs S/N measurements, the probability of errors when the modem signal is in the presence of noise.

The previously mentioned techniques are aimed at improving the modem data pump through analog (or digitally synthesized) circuitry. Techniques are becoming popular for not only improving, but virtually eliminating data errors through protocols implemented in the modems command microcontroller (µC). Prior to these 'hardware' based schemes, error correction provided in the applications software was available, such as X-MODEM or Kermit for asynchronous file transfer. In mainframe environments, SDLC or HDLC schemes were used.

Software based error correction schemes do however have their disadvantages. One important one being reduced data throughput. The throughput performance varies, but all schemes reduce data transfer below its nominal rate. Typical values of 30% are common, equating to only about 800 BPS for a 2400 BPS connection.

The hardware based error correction protocols supported by the XR-2443 for data mode are those as specified by the **CCITT LAPM,** and **MNP.** These schemes convert asynchronous data to be transmitted to a synchronous format (start and stop bits are stripped) for a packet-oriented protocol. Throughput values again vary, however typical values of 108% for the lower MNP Class 3 and 120% for MNP Class 4 or LAPM. These equate to roughly 2600 - 2900 BPS for 2400 BPS modems.

Actual error correction is based on adding information to the block-oriented data, through a 16-bit CRC (Cyclic Redundancy Check) calculation. The receiving side calculates CRC values for each block and if found to be incorrect, a retransmission of that block will be requested.

Typical frame sizes for LAPM are 128 Octets (8-bit start/stop bit stripped characters).

DETERMINATION OF BLOCK SIZE SETTING

The block size adjustment allows the user to compensate for situations where a high probability of errors exists. This condition occurs when the signal to noise ratio is extremely low. The XR-2400 provides performance curves for 2400 BPS(V.22bis) operation and single points BER data for 1200 and 300 BPS. As a rule of thumb, under typical dial-up telephone connections, the negotiate block size feature of MNP and V.42 provides satisfactory results (generally 256 characters/block). However, if the signal to noise ratio is much less than 15 dB S/N (at 2400 BPS) the probability of receiving data with an error is much greater, which would require retransmission of the entire block. By reducing the block size, the amount that is needed to be retransmitted is reduced, which increases the throughput. Under poor line conditions, the throughput would be reduced for a greater number of link acknowledgments would be needed.

For BTLZ 2 dimensional encoding, the maximum number of character setting (register S90) can help in obtaining a higher throughput earlier than if the straight learning mode of BTLZ is used. If it is known that a certain number of characters are repetitive, that setting will provide an increase in throughput. However, if the file contents change, become more random, a reduction in throughput will occur. The default setting of 32 characters is a compromise for a typical text file.

DATA COMPRESSION

The CCITT recommendation for V.42bis specifies data compression modes, as provided by British Telecom Lempel-Ziv (BTLZ). Modem controller protocols have advanced to the point where in addition to providing error-free data transfer with the use of LAPM or MNP 2-4, they can also offer data compression operation.

These data compression schemes are BTLZ and MNP 5. Although MNP 5 is not specifically part of the V.42bis recommendation, it has been included in the XR-2443 to serve only as a further enhancement to the XR-2400 based modems and ensure data compression compatibility with the established MNP 5 modems.

MNP Class 5 is the protocol for **data compression**. It is by far the most accepted protocol for this function. CCITT recommendations have updated the V.42 standard to include the BTLZ data compression technique. This new standard is **V.42bis**.

MNP 5 data compression offers the XR-2400 V.22bis modem chip set roughly an 100% increase in throughput (in data mode), or 200% of nominal. This translates to a maximum modem throughput of 2400 BPS x 2 = 4800 BPS for a text file.

XR-2443 V.42/MNP FUNCTIONS AND COMMANDS

The XR-2443 with external EPROM provides control for the following major functions:

FUNCTION	DESCRIPTION
• 'AT' Command Control	Provides 'AT' Command Set Control
• MNP Level 2-4	Provides error correction for 100% perfect data transfer.
• MNP Level 5	Allows roughly a 100% increase (4800 BPS for V.22bis mode) in data throughput, through data compression techniques.
• V.42bis (BTLZ®)	Using 2-dimensional adaptive coding a 400 % or more improvement in data throughput is possible.
• V.42 (LAPM)	100% perfect data transfer
• Speed Conversion	Maintain up to 9600 BPS DTE (terminal speed) for 300 BPS to 2400 BPS connect speeds, both for LAPM/MNP non-error correcting connections.

MNP 5 techniques utilize a scheme which abbreviates redundant data characters for a much higher transmission efficiency or throughput increase. Because of its dependency on redundant characters, the amount of improvement will vary. Typical improvement values are in the range of 75 to 125%, or 4200 to 5400 BPS for a 2400 BPS modem link.

FLOW CONTROL

A method for regulating the flow of data to be transmitted is necessary when DTE data rates exceed line rates. Figure 2 illustrates a basic modem connection and helps illustrate where flow controls fit in.

Flow control can be under **hardware** or **software control.**

HARDWARE FLOW CONTROL

Hardware Flow Control allows the modem to lower or raise its CTS (Clear to Send) line to the DTE. This provides an ON/OFF control of data flow from DTE to modem. If the modem data buffer becomes full it lowers the CTS line to stop transmit data flow to allow the modem to "catch-up".

SOFTWARE FLOW CONTROL

An alternative to hardware flow control is control by software, known as **Xon/Xoff.** This is accomplished by special characters inserted into the data stream to start and stop data flow. **Control Q (^Q)** is used to start or restart data flow and **Control S (^S)** to stop data flow.

Three different variations of Xon/Xoff control modes are:

- Send Only
- Normal
- Pass through

Application Software Interface

The firmware of the XR-2443 (combined masked and supporting code) will work with a variety of software programs on the market, as well as with dumb terminals. The largest factor that can affect throughput is the speed of the Data Terminal Equipment (DTE). It has been found that both hardware and software flow control cannot occur quickly enough on a 4.7 MHz PC to prevent corruption of data. For this reason, 9.5 MHz or faster XT and AT computers are recommended for best results and to compare the throughput values given in this data sheet.

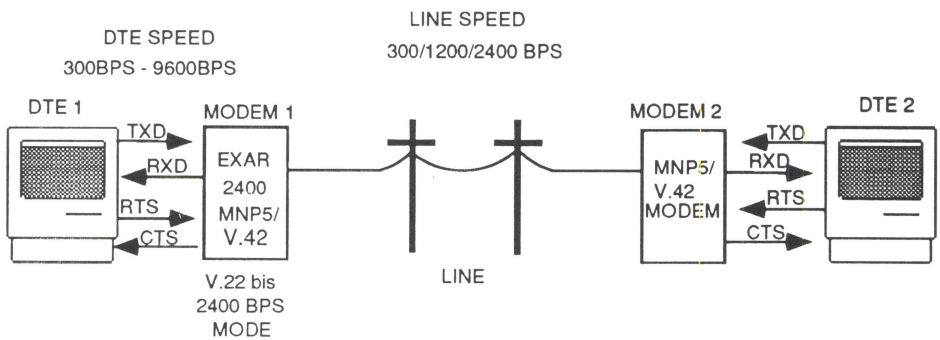


Figure 2. Basic Modem Test Configuration for Throughput

PROTOCOL NEGOTIATION

The XR-2443, for data mode, supports error correcting or reliable modes of operation for not only LAPM, but also MNP type protocols. Also, since data compression operation is specified by the CCITT V.42bis specifications, BTLZ has been included along with the industry standard MNP® 5 for increased compatibility. Because of these multiple protocols supported,and to simplify the command process the XR-2443 offers two temporary protocol negotiation commands:

1) **AT\M0 Default** Mode. This command selects an automatic protocol negotiation mode. **First LAPM** negotiation will be attemped. If not possible, MNP operation will be negotiated. The highest possible class of MNP operation will be negotiated (Compression negotiation will be attempted depending upon the setting of the %C command). If the remote modem does not support error correction, normal 2400 BPS (or1200/300 BPS) operation will be supported.

2) **AT\M1**. This command will **disable LAPM** operation. Here only MNP 2-5 and non-error correcting modes of operation will be supported.

It is recommended that the default conditions be used when first starting to use the sophisticated features of the XR-2443. The default conditions have been selected to provide effortless use of the XR-2443.

The following is a command set summary for the XR-2443. Provided are:

Data Mode

1) Basic Connection/Dialing Commands
2) Dialing Modifiers
3) Standard Hayes 'AT' Command Set
4) 'S' Register Descriptions/Functions. These registers are used for controlling the value or function of various 'AT' commands.
5) BTLZ/MNP/LAPM Commands. The entire list represents the MNP command set. Most of the MNP commands also apply to LAPM, with the exceptions indicated.

COMMAND	DESCRIPTION / RANGE - SIZE
A/	Execute previous command, without striking <CR> key
AT	Attention
ATA	Answer Immediate
ATB0	CCITT V.22 mode
ATB1	Bell 212A mode **DEFAULT**
ATB2	V.23 mode
ATD	Dial Command
ATDP	Dial Using pulse dial
ATDT	Dial Using DTMF tone dial **DEFAULT**
The following 8 modifiers will dial using the previously used technique (pulse or tone), or the T or P command can be added after the D (dial) command. 0-9 A B C D * #	
ATDW	Wait for Dial Tone for Period Set by S7 Register
ATD@	Quiet Answer: Wait for 5 Seconds of Silence Before Dialing
ATD!	Hookflash: Commonly Used PBX Systems
ATDR	Reverse Answer Mode
ATDS=n	Dial Stored Number when n= 0-3
ATD/	Wait 0.125 Seconds
ATD;	Return to Command Mode After Dialing
ATD,	Pause for Time Set by S8 Register
ATE0	Command Echo Disabled
ATE1	Command Mode Echo Enabled **DEFAULT**
ATH0	Go On Hook (Open Relay)
ATH1	Go Off Hook (Close Relay)
ATI0	Identification Code
ATI1	Identification Code
ATI2	"OK" Response if Checksum Verifies
ATI3	EXAR EPROM Revision Date
ATL0	Lowest Volume Setting
ATL1	Same as ATL0
ATL2	Medium Volume Setting **DEFAULT**
ATL3	Maximum Volume
ATM0	Speaker Always Off
ATM1	Speaker On Until Carrier Is Detected **DEFAULT**
ATM2	Speaker Always On
ATM3	DTMF Tones are not Heard, but Speaker is on Until Carrier Detected
ATO	Originate Immediate or Return to Data Mode
ATO1	Request a Retrain When in V.22bis Mode
ATQ0	Provide Result Codes **DEFAULT**
ATQ1	Disable Result Code
ATSn?	Provide S Register Value
ATSn=	Set S Register Value
ATV0	Terse (and Verbose) Responses, affected by \Vn

NUMERIC	DESCRIPTION / RANGE - SIZE	
		\V1
0	OK	Command Executed
1	CONNECT	Connection at 0 to 300 BPs
2	RING	Ring Signal Detected
3	NO CARRIER	Carrier Signal not Detected
4	ERROR	Error
5	CONNECT 1200	Connection at 1200 BPS
6	NO DIALTONE	No DialTone Detected
7	BUSY	Busy Signal Detected
8	NO ANSWER	No Silence Detected
10	CONNECT 2400	Connection at 2400 BPS
11	CONNECT 4800	Connection at 4800 BPS
12	CONNECT 9600	Connection at 9600 BPS
14	CONNECT 19200	Connection at 19200 BPS
		\V1
22	CONNECT 1200/REL 4	MNP Class 4 Link
22	CONNECT 1200/REL 5	MNP Class 5 Link
23	CONNECT 2400/REL 4	MNP Class 4 Link
23	CONNECT 2400/REL 5	MNP Class 5 Link
22	CONNECT 1200/V.42	V.42 Link
23	CONNECT 2400/V.42	V.42 Link
22	CONNECT 1200/V.42bis	V.42bis Link
23	CONNECT 2400/V.42bis	V.42bis Link

COMMAND	DESCRIPTION / RANGE - SIZE
ATV1	Verbose Response **DEFAULT**. See ATV0 for Responses
ATX0	Enable Result Codes 0-4
ATX1	Enable Result Codes 0-5, 10
ATX2	Enable Result Codes 0-6, 10
ATX3	Enables Result Codes 0-5 and 7 and 10
ATX4	Enables Result Codes 0-10 **DEFAULT**
ATY0	Disable Long Space Disconnect **DEFAULT**
ATY1	Enable Long Space Disconnect
ATZ0	Software Reset, Restore S Register from profile location 0 in NVRAM
ATZ1	Restore S Registers From Profile Location 1 in NVRAM
AT&C0	EIA Carrier Line Always Forced on **DEFAULT**
AT&C1	EIA Carrier Line Follows Data Carrier
AT&D0	DTR Always on **DEFAULT**
AT&D1	Modem Goes to Command Mode When DTR Goes Off
AT&D2	Modem Goes on HOOK and Returns to Command Mode When DTR Goes Off
AT&D3	Modem Initializes When DTR Goes Off
AT&F	Fetch S Registers From EPROM for Factory Default
AT&G0	No Guard Tone **DEFAULT**
AT&G1	550 Hz Guard Tone Enabled
AT&G2	1800 Hz Guard Tone Enabled
AT&J0	RJ-11 Select **DEFAULT**
AT&K0	Flow Control Disabled
AT&K1	No Function
AT&K2	No Function
AT&K3	RTS/CTS Flow Control **Default**
AT&K4	Xon/Xoff Flow Control
AT&K5	Xon/Xoff Pass Through
AT&L0	Switched Line Select **DEFAULT**
AT&L1	Leased Line Select
AT&M0	Asynchronous Mode **DEFAULT**
AT&M1	Synchronous Mode With Asynchronous Dial
AT&M2	Synchronous Mode and Dial the Stored Number Immediately
AT&M3	Synchronous Mode With DTR Controlling Data/Talk
AT&P0	US Make/Break Ratio For Pulse Dialing **DEFAULT**
AT&P1	UK Make/Break Ratio For Pulse Dialing
AT&Q0	Direct mode (same as Hayes)
AT&Q1	Same as &M1
AT&Q2	Same as &M2
AT&Q3	Same as &M3
AT&Q5	Error Control Mode
AT&Q6	Normal Mode
AT&R0	Clear To Send (CTS) Follows RTS **DEFAULT**
AT&R1	CTS Always On
AT&S0	Data Set Ready (DSR) Always on **DEFAULT**
AT&S1	DSR Normal
AT&T0	Terminate Test in Progress **DEFAULT**
AT&T1	Initiate Local Analog Loopback For Time Set by Register S18
AT&T2	Not Defined
AT&T3	Initiate Digital Loopback for Time Set by Register

COMMAND	DESCRIPTION / RANGE - SIZE
AT&T4	(Not Supported)
AT&T5	Disable Remote Digital Loopback (RDLB) Response
AT&T6	Initiate RDLB
AT&T7	Initiate RDLB with Self Test
AT&T8	Initiate ALB with Self Test (for Direct / Normal Mode only)
AT&W0	Write User Profile 0 into NVRAM
AT&W1	Write User Profile 1 into NVRAM
AT&X0	Modem Provides Transmit Clock
AT&X1	DTE Supplies Transmit Clock (Not Supported)
AT&X2	Slave Clock Mode (Not Supported)
AT&Y0	Power Up Recall User Profile 0
AT&Y1	Power Up Recall User Profile 1
AT&V	List Configuration both Active and Stored
AT&Z m=An	Store Telephone Number into NVRAM (XL93C46) where: *m* is the number location (0-3) *A* is *P* or *T* (pulse or Tone) *n* is the telephone number

COMMAND	LAPM Yes/No	DESCRIPTION/RANGE - SIZE	FUNCTION
AT \ M0	Y	LAPM Enabled	Attempt LAPM Negotiation
AT \ M1	N	LAPM Disabled	Do Not Attempt LAPM Negotiation
AT \ N0	Y	Normal	
AT \ N1	Y	Direct	
AT \ N2	Y	MNP 2-5/Reliable	
AT \ N3	N	MNP 2-5/Auto Reliable	
AT \ N4	Y	V.42 Mode	
AT \ N5	Y	V.42 Mode Auto Reliable	
AT \ N6	Y	V.42 / MNP 2-5 Reliable	
AT \ N7*	Y	V.42 / MNP 2-5 Auto Reliable	
AT \ A0	N	64 Characters	Transmit Block Size
AT \ A1	N	128 Characters	
AT \ A2	N	192 Characters	
AT \ A3*	N	256 Characters	
AT%An	Y	n = 0-127 ASCII	Auto-Reliable Fallback Character
AT \ L0*	N	Stream Link	Block MNP Link
AT \ L1	N	Block Link \L1 = \L0	(Stream Mode)
AT \ O	N	Initiate Reliable Link After Escape Command Independent of Modem Initial mode (ANS or ORG)	Originate Reliable Link
AT \ U	N	Accept Reliable Link after Escape Command request from Initiator of Link	Accept Reliable Link
AT \ Y	N	Establish Reliable Link after Connecting in Normal Mode	Switch to Reliable Mode
AT \ Z	N	Switch to Normal Mode After Establishing a Reliable Link	Switch to Normal Mode
AT % C0	Y	Compression Disabled	Compression On/Off Control
AT % C1*	Y	Compression Enabled	
AT \ V0	Y	Standard Non-MNP Result Codes	Result Code Form
AT \ V1*	Y	Modified MNP Result Codes (As Listed Below)	
AT \ Bn	Y	N = 0 - 9 (100ms Increments) Used in Normal Mode Default = 3, Error Control Mode Always 300ms	Transmit Break for Normal Data Mode
AT \ C0*	Y	Does not buffer Data Default	Set Auto-Reliable Buffer Break Control
AT \ C1	Y	Buffers All Data on Answering Modem until 200 Characters (Non-Sync) are Returned	
AT \ C2	Y	Does Not Buffer Data on Answering Modem, according to % An to fall back	
AT \ K1	Y	"Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed	Break Control for Reliable Data Mode

COMMAND	LAPM Yes/No	DESCRIPTION / RANGE - SIZE	FUNCTION
AT \ K3	Y	"Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained	
AT \ K5*	Y	"In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break	
AT \ K0,2,4	-	Not Supported (Will be equal to AT \ K5 if selected)	
AT \ Tn	Y	N = 0-90 min N* = 0 (disable)	Inactivity Timer
%D0*	Y	Hang up without clearing buffer	
%D1	Y	Clear the receive buffer before hang up	
- Cn	Y	Maximum String Length (BTLZ) Range: 6-250 Characters Default: 32 Characters	
- Dn	Y	Dictionary Size and One / Two-way Mode(BTLZ), - Dictionary size options 0-512 entries, 1-1024(1K) entries, *2-2048(2K) entries, 3-4069(4K) entries	
AT \ I	-	Not Functional	Interface Protocol
AT \ J0*	Y	BPS Rate Adjust Disabled	Speed Conversion Control Disable
AT \ J1	Y	BPS Rate Adjust Enabled	Modem Port Rate Adjustment
AT \ S	Y	List Profiles	
AT \ G0*	Y	Disables Modem Port Flow Control	Set Modem Port
AT \ G1	Y	Sets Modem Port Flow Control to Xon / Xoff	Flow Control
AT \ X0*	Y	Does Not Pass Xon / Xoff to Remote Modem	Xon / Xoff Pass Through Control
AT \ X1	Y	Passes Xon / Xoff to Remote Modem	
AT \ Q0	Y	Disable Flow Control	Serial Port Flow Control
AT \ Q1	Y	Bidirectional Xon / Xoff Enabled	
AT \ Q2*	Y	Unidirectional Hardware Control by CTS	
AT \ Q3	Y	Bidirectional Hardware Control by RTS / CTS	
AT \ Q4	Y	Unidirectional Xon /Xoff Send Only	
AT \ Q5		Keep CTS off until connect unidirectional hardware flow control	
AT \ Q6		Keep CTS off until connect for bidirectional hardware flow control	
AT % U	Y	Not Functional	Clear Serial Port Speed Serial Port
AT - P0*	Y	Ignores Parity for Special Characters	Check Parity
AT - P1	Y	Processes Special Characters Only if they have Correct Parity	

*Note: * Denotes Default Condition*

See Command AT \ V1 Above

STANDARD RESULT CODES\V0			MODIFIED RESULT CODES \V1	
Verbose	**Numeric**		**Verbose**	**Numeric**
CONNECT	1			
CONNECT 1200	5		CONNECT 1200 / REL 4 or 5	22
CONNECT 2400	10		CONNECT 2400 / REL 4 or 5	23
CONNECT 4800	11			
CONNECT 9600	12		CONNECT 1200/V.42	22
CONNECT 19200	14		CONNECT 2400/V.42	23
			CONNECT 1200/V.42bis	22
			CONNECT 2400/V.42bis	23

S	REGISTER FUNCTION
S0	Number of Rings to Answer: **Default** = 0 (no answer)(stored)
S1	Ring Count: Stores Number of Rings: Resets After Every Call
S2	Escape Code Character: **Default** = 043 (ASCII for "+")
S3	Carriage return Character: **Default** = 013
S4	Line Feed Character: **Default** = 010
S5	Back Space Character: **Default** = 008
S6	Wait for Dial Tone: **Default** = 002 (seconds) (minimum setting)
S7	Wait for Carrier After Dial: **Default** = 030 (seconds)
S8	Duration of Delay for Comma: **Default** = 002 (seconds)
S9	Carrier Detect Response Time: **Default** = 0.6 (seconds)
S10	Loss of Carrier Response Time **Default** = 1.4 (seconds)
S11	Touch Tone Duration: **Default** = 095 (milliseconds)
S12	Escape Code Guard Time: **Default** = 1 (second)
S13	Reserved
S14	Bit Mapped Register: Stored in NVRAM (XL93C46) Bit 0 Reserved Bit 1 Echo Bit 2 Result Codes Bit 3 Numeric Result Codes Bit 4 Always 0 Bit 5 Tone/Pulse Dialing Bit 6 Reserved Bit 7 Answer/Originate
S15	Reserved
S16	Test Register Bit 0 ALB Bit 1 Reserved Bit 2 Local Digital Loopback Bit 3 Remote Digital Loopback (Not Supported) Bit 4 Initiate Remote Test Bit 5 Initiate Remote Test With Self Test Bit 6 Analog Loopback With Self Test Bit 7 Reserved
S17	Reserved
S18	Test Time Stored in NVRAM (XL93C46) Default = 000 (seconds)
S19	Reserved
S20	Reserved
S21	Bit Mapped Register Stored in NVRAM (XL93C46) READ ONLY Bit 0 0 = RJ11 Jack Bit 1 Not Used Bit 2 CTS RTS Function Bit 3 DTR Function Bit 4 DTR Function Bit 4 / Bit 3 / Function 0 / 0 / DTR Always True Default 0 / 1 / DTR Off, Forces Command State 1 / 0 / DTR Off, Forces Modem Offline 1 / 1 / Modem Initializes With DTR OFF (ATZ)

<table>
<tr><th>REGISTER NUMBER</th><th>REGISTER FUNCTION</th></tr>
<tr><td>S22</td><td>
Bit 5 EIA Carrier Status
Bit 6
Bit 7 Guard Tone Select
<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>No Guard Tone Default</td></tr>
<tr><td>0</td><td>1</td><td>550 Hz Guard Tone</td></tr>
<tr><td>1</td><td>0</td><td>1800 Hz Guard Tone</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
Option Bit - Mapped Register
Bit 0 Determines Speaker Volume
Bit 1
<table>
<tr><th>Bit 1</th><th>Bit 0</th><th>Speaker Volume</th></tr>
<tr><td>0</td><td>0</td><td>Low</td></tr>
<tr><td>0</td><td>1</td><td>Low</td></tr>
<tr><td>1</td><td>0</td><td>Medium Default</td></tr>
<tr><td>1</td><td>1</td><td>High</td></tr>
</table>
Bit 2 Determines the Speaker Status
Bit 3
<table>
<tr><th>Bit 3</th><th>Bit 2</th><th>Speaker Status</th></tr>
<tr><td>0</td><td>0</td><td>Always Off</td></tr>
<tr><td>0</td><td>1</td><td>On Until Carrier is Detected Default</td></tr>
<tr><td>1</td><td>0</td><td>Always On</td></tr>
<tr><td>1</td><td>1</td><td>As '01', Except Off for Dialing</td></tr>
</table>
Bit 4, 5 and 6 Determine Response Messages
<table>
<tr><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Message</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Basic Message Set</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Extended with Connect 1200 and Connect 2400</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Extended with 'No Dial Tone'</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Extended with 'Busy'</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Extended with All Messages Default</td></tr>
</table>
Bit 7 Determines Off Hook/On Hook (Make/Break) Ratio for Pulse Dialing
<table>
<tr><th>Bit 7</th><th>Ratio</th></tr>
<tr><td>0</td><td>39/61 (USA and Canada) Default</td></tr>
<tr><td>1</td><td>33/67 (Uk and Hong Kong)</td></tr>
</table>
</td></tr>
<tr><td>S23</td><td>
Option Bit Mapped Register
(LSB) Bit 0 Not Supported
<table>
<tr><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>300</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Not Used</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1200</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2400</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4800</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>9600</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19200</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>38400(reserved)</td></tr>
</table>
Bit 4 Determines the Parity for Transmitting and Receiving Data
</td></tr>
</table>

REGISTER NUMBER	REGISTER FUNCTION
	Bit 5 Bit 5 Bit4 Parity 0 0 Even Default 0 1 Space/None 1 0 Odd 1 1 Mark Bit 6 Determines Guard Tone Frequency Bit 7 (Used in European Applications) Bit 7 Bit 6 Guard Tone (Hz) 0 0 Disabled Default 0 1 550 1 0 1800 1 1 Reserved
S24	Not Used
S25	Delay to DTR (Stored in NVRAM) Default = 005 (seconds)
S26	RTS to CTS Delay (Synchronous Mode Only) Default = 1 (milliseconds)
S27	Bit Mapped Register STORED IN NVRAM Bit 0 Bit 1 Transmission Mode Bit 1 Bit 0 Function 0 0 Asynchronous Mode Default 0 1 Synchronous Mode 1 1 0 Synchronous Mode 2 1 1 Synchronous Mode 3 Bit 2 Reserved Bit 3 Reserved Bit 4 Bit 5 Transmission Mode Bit 5 Bit 4 Function 0 0 Internal Modem Clock Used Default 0 1 DTE Supplied Clock 1 0 Slave Clock Mode 1 1 Same as 00 Bit 6 CCITT or Bell Handshaking Standard 0 CCITT 1 Bell (including CCITT V.22bis) Default Bit 7 Reserved
S28-35	Reserved
S36	Negotiate Failure Fallback (Affected by %C and \N) Bits 0 Hang Up 1 Attempt a standard asynchronous connection (&Q0) 3 Attempt an asynchronous connection using automatic speed buffering (&Q6) 4 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails, attempt a standard asynchronous connection 5 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails attempt a standard asynchronous connection
S37	Not Supported

REGISTER NUMBER	REGISTER FUNCTION
S38	Not Supported
S39	Reserved
S40	Not Supported
S41	Not Supported
S43-45	Reserved
S46	Protocol Selection: Bits 136 LAPM only (V.42)
S47	Not Supported
S48	Feature Negotiation Action 0 Negotiation disabled; presume the remote modem is configured for and has the capabilities necessary for the connection selected with S46 3 Negotiation enabled, but originating modem remains silent during detection phase. For connections with MNP modems; defeats connection sequence with other V.42 modems 7 Negotiation enabled 128 Negotiation disabled; forces fallback options specified in S36 to be taken immediately
S82	Break Handling: Affected by \K commands 3 "Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained 7 "Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed 128 "In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break
S86	Not Supported

Special Notes regarding the use of S registers above S27 and AT/n Commands.

1. Changes of S register values above S27 will effect the profile display for AT/n Commands. AT/n Commands however, do not modify the setting of S registers.

2. It is intended that a user or application software package will use only one method (S register \ n Commands) to effect the error control functions. Use of a combination could result in unpredictable behavior.

APPLICATIONS INFORMATION

The XR-2443 is shown in the XR-2400 modem schematic. The XR-2443 provides the command controller function for the XR-2400 V.22bis modem chip set. For data operation the modem operates error-free through LAPM or MNP 2-4 modes and can offer increased throughput with V.42bis or MNP 5. The XR-2321 device included adds CCITT V.21 and V.23 FSK modes, it is optional and can be eliminated for designs not requiring these modes.

Detailed information for the XR-2400 is available in XR-2400 V.22bis modem chip set datasheet.

Layout Hints

In order for the XR-2443 to provide optimal support for best performance of the modem, some design hints/rules should be followed.

- Locate the XR-2402A AFE near the DAA section - provide for a short transmit / receive carrier input path, away from any digital control lines.

- Maintain separate analog and digital ground / power lines back to the power supply.

- Bypass (capacitor decouple) the XR-2401, XR-2402A, XR-2443 and op amp power supplies with both 0.01μF ceramic and 0.47μF tantalum capacitors near their actual pins. Ensure analog/digital supplies are by-passed to their respective ground.

- Crystal - parallel resonant type. Typical loading capacitors are 18pF.

SYSTEM PERFORMANCE

Performance for an error-correcting modem has two major areas.

1) DATA PUMP PERFORMANCE
With error-detection capabilities turned off, the integrity of the data pump to pass data in the presence of impairments. Most often the major specification measured here is the probability of data errors with the receive carrier impaired by noise, or BER (bit error rate) vs S/N (Signal-to-Noise ratio).

Figure 3 shows BER vs S/N for the XR-2400 modem, as measured with the test set-up in Figure 4.

2) ERROR CONTROLLER PERFORMANCE
The XR-2443, when in LAPM or MNP modes provides the control and detection required to yield perfect data transfer (Data Modem mode).

Beyond error correction, throughput, or data transfer rate, is another important parameter to the modems overall performance.

LAPM and MNP 2-4 Modes are not specifically provided for increased throughput. However an additional benefit of their error-detecting schemes is roughly a 20% increase in throughput. Using the 'Quick Brown Fox....' pattern, both LAPM and MNP 4 modes yielded better than a 20% throughput increase. V.22bis mode was used for this test, with an actual throughput of better than 2900 BPS measured.

MNP 5 Data Compression Included in the XR-2443 allows roughly a 100% throughput increase over the modems nominal data rate. As previously discussed, the throughput performance of MNP 5 varies with different types of data. (Figure 5 shows data for various data patterns). (Figure 6 illustrates the test set-up used for the measurement).

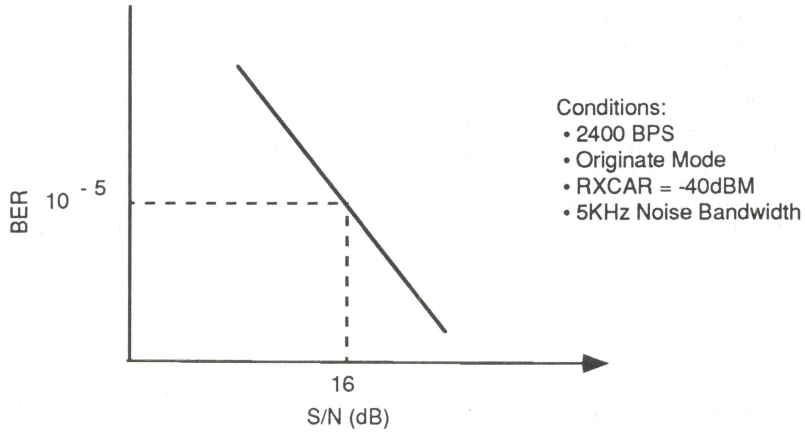


Figure 3. 2400 BPS Ber vs. S/N (Non-Error Correcting)

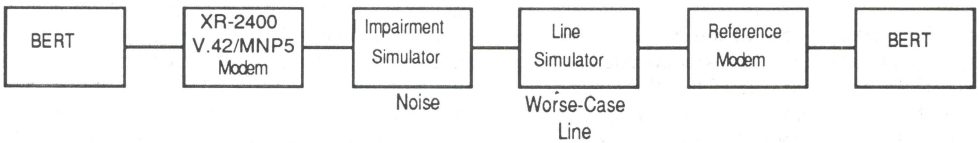


Figure 4. Data Quality Test Set-Up

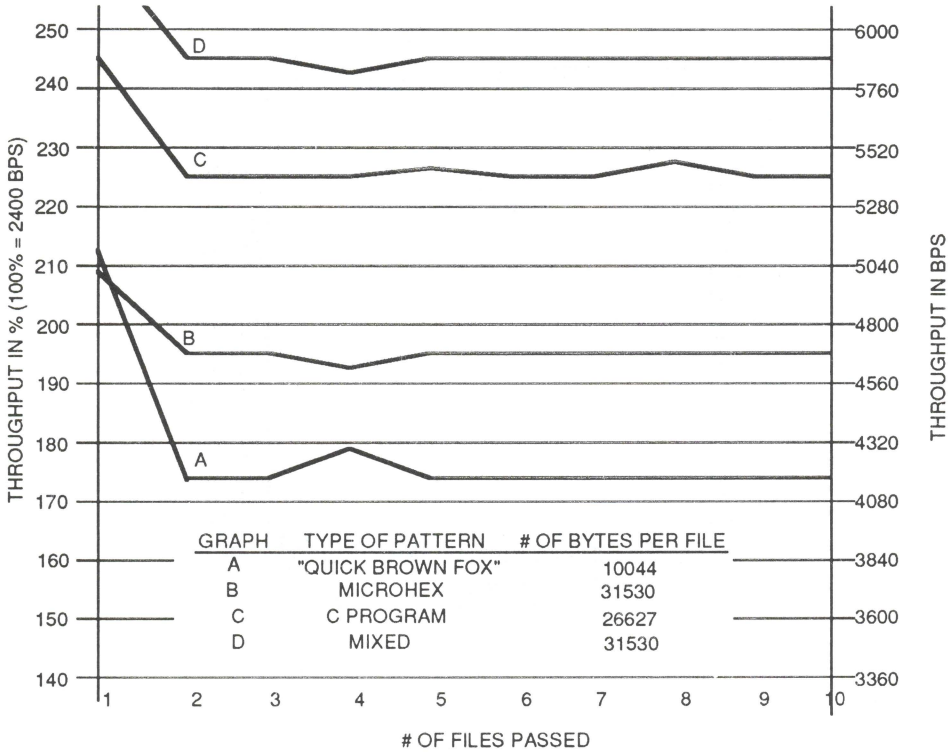
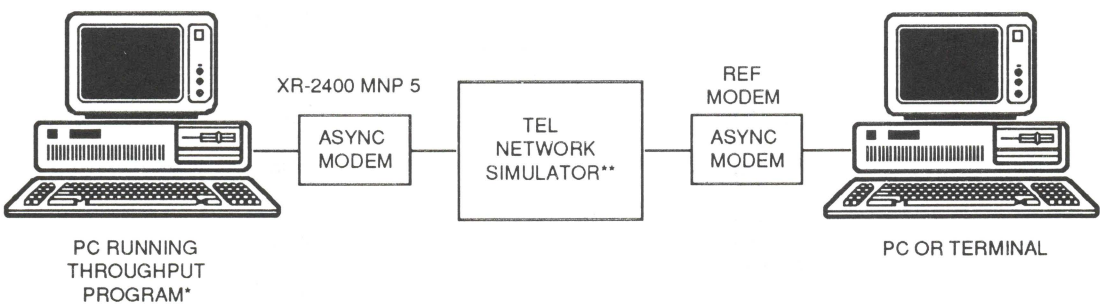


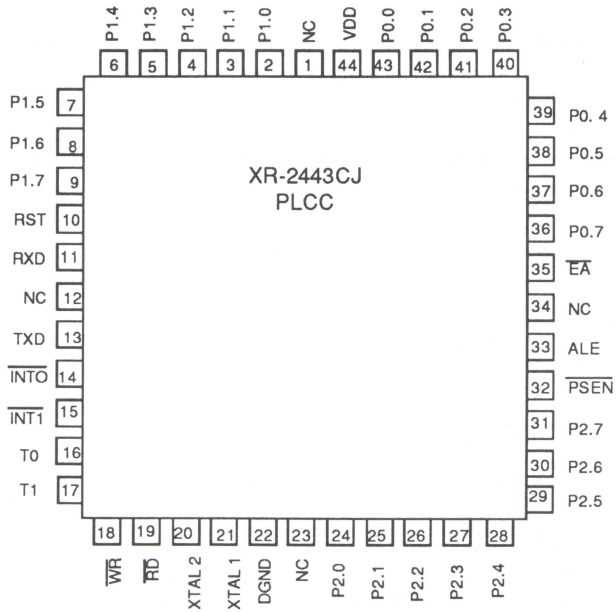
Figure 5. Effective Data Throughput

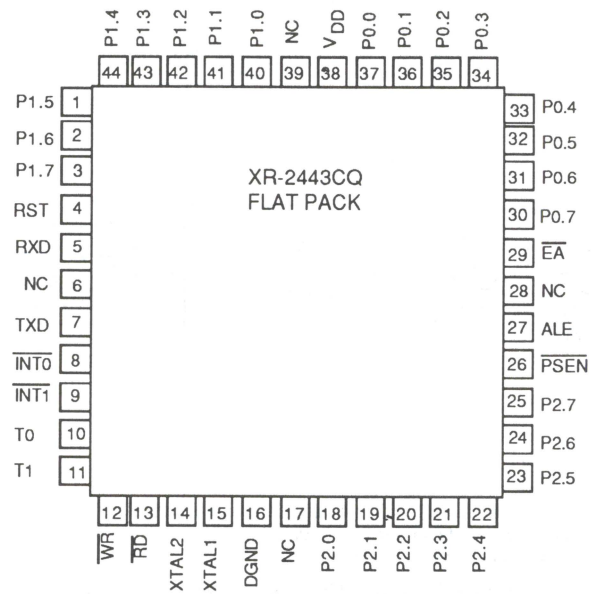


* APT (Asynchronous Performance Tester), also contains data or files to be used during measurement. Product of Concord Data Systems.

** Simulates line impairment and attenuation conditions.

Figure 6. MNP5 Throughput Measurement Test


XR-2443CJ
PLCC
P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0 43
P0.1 42
P0.2 41
P0.3 40
P1.5 7
P1.6 8
P1.7 9
RST 10
RXD 11
NC 12
TXD 13
INTO 14
INT1 15
T0 16
T1 17
39 P0. 4
38 P0.5
37 P0.6
36 P0.7
35 EA
34 NC
33 ALE
32 PSEN
31 P2.7
30 P2.6
29 P2.5
18 WR
19 RD
20 XTAL 2
21 XTAL 1
22 DGND
23 NC
24 P2.0
25 P2.1
26 P2.2
27 P2.3
28 P2.4


XR-2443CQ
FLAT PACK
P1.4 44
P1.3 43
P1.2 42
P1.1 41
P1.0 40
NC 39
VDD 38
P0.0 37
P0.1 36
P0.2 35
P0.3 34
P1.5 1
P1.6 2
P1.7 3
RST 4
RXD 5
NC 6
TXD 7
INT0 8
INT1 9
T0 10
T1 11
33 P0.4
32 P0.5
31 P0.6
30 P0.7
29 EA
28 NC
27 ALE
26 PSEN
25 P2.7
24 P2.6
23 P2.5
12 WR
13 RD
14 XTAL2
15 XTAL1
16 DGND
17 NC
18 P2.0
19 P2.1
20 P2.2
21 P2.3
22 P2.4

XR-29V00 Fax/Data/Voice Modem Data Pump with Caller ID

GENERAL DESCRIPTION

The XR-29V00 is a two chip set that provides the complete data pump function for Group III 9600 bit per second (bps) fax, V.22bis data, Voice and Caller ID operation.

The XR-29V00 consists of the XR-29V01 and the XR-29P02. The XR-29V01 is a digital signal processor-based chip supporting:

- Modulation/demodulation
- ADPCM
- DTMF generation and detection functions.

The XR-29P02 is a combination analog and digital chip. Its analog portions support:

- Transmit and receive filters
- A/D and D/A functions
- Transmit level attenuator
- Programmable gain amplifier.

The digital portion of the XR-29P02 supports:

- Transmit clock
- Async/sync converter
- Interface circuit between XR-29V01 and microcontroller
- Receive digital phase locked loop.

When the XR-29V00 is combined with an XR-2942, XR-2943 or an 80C31µc(with EXAR firmware), the standard features are:

Extended AT commands, Class 2 Fax interface, all the functions for Group III 9600 bps fax, V.22bis data, Voice with 4:1 compression and Caller ID operation.

The XR-2942 and XR-2943 are enhanced microcontrollers and offer additional features:

XR-2942: V.42 error control, MNP 2-5 error control / data (2:1) compression

XR-2943: V.42 error control,V.42 bis data (4:1) compression, MNP 2-5 error control / data (2:1) compression

The XR-29V01 and XR-29P02 are available in 52 pin PLCC, 52 pin QFP and 64 pin SQFP packages respectively. Power required is a single +5 volt for the XR-29V01 and ±5 volts for the XR-29P02. Both chips utilize CMOS technology for low power operation.

3

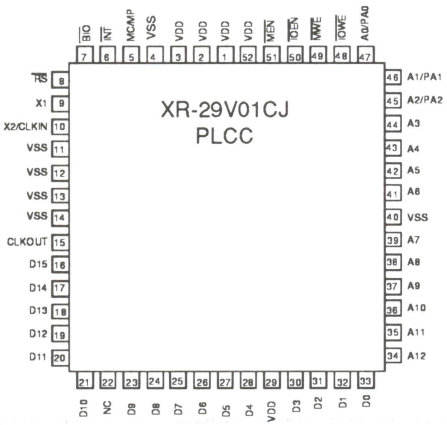
FEATURES

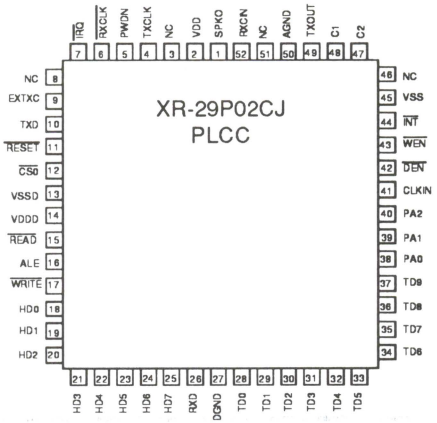
V.29 / V.27ter / V.21 Ch. 2 Fax Modes
V.22bis / V.22 / 212A / 103 Data Modes
Standard Microcontroller Interface
Analog, Remote and Local Digital Test Facilities
DTMF Generator and DTMF Decoder
2400 / 1200 / 300 BPS Full Duplex DATA Mode
CMOS Technology
Automatic Adaptive Equalization
Guard Tone Generators
Call Progress Monitor Mode
ADPCM Voice Compression
Caller Identification

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-29V01CJ	PLCC	0°C to 70°C
XR-29V01CQ	QFP	0°C to 70°C
XR-29V01CSQ	SQFP	0°C to 70°C
XR-29P02CJ	PLCC	0°C to 70°C
XR-29P02CQ	QFP	0°C to 70°C
XR-29P02CSQ	SQFP	0°C to 70°C

PIN ASSIGNMENT *(For other pin assignment diagrams refer to the end of this datasheet)*







NOTES



XR-2900 Fax/Data Modem Chip Set

GENERAL DESCRIPTION

The XR-2900 is a two chip set that provides the modem data pump function for 9600 BPS half duplex / 2400 BPS full duplex applications. The XR-2900 supplies all the functions for implementing a modem for facsimile or V.29 applications. Also included is a complete V.22 bis data modem.

The XR-2901 is a digital signal processor-based chip supporting primarily the modulation/demodulation function. The XR-2902 is a combination analog and digital chip. Its analog portions support the transmit and receive filters, A/D and D/A functions, transmit level attenuator, and programmable gain amplifier.

The digital portion of the XR-2902 supports the transmit clock, and async/sync converter, interface circuit between XR-2901 and host controller, and a receive clock digital phase locked loop.

Both chips utilize CMOS technology for low power operation. The XR-2901 and XR-2902 are available in 40 and 48 pin dip, 44 and 52 pin PLCC and 44 and 52 pin QFP packages respectively. Power required is a single +5 volt for the XR-2901 and ±5 volts for the XR-2902.

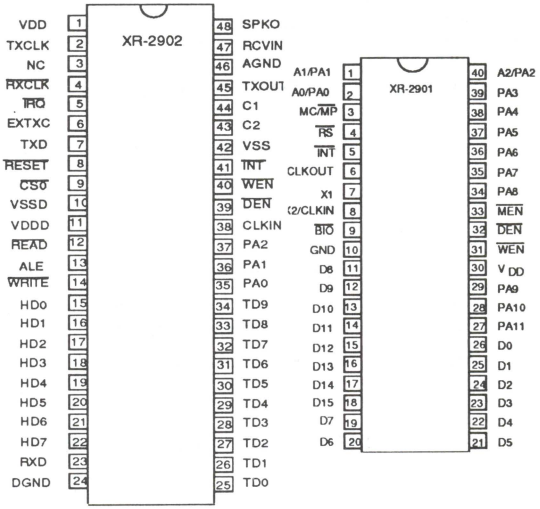
FEATURES

V.29 / V.27ter / V.21 Ch. 2 Fax Modes
V.22bis / V.22 / 212A / 103 Data Modes
Standard Microcontroller Interface
Analog, Remote and Local Digital Test Facilities
DTMF Generator
9600 / 7200 / 4800 / 2400 / 300 BPS Half Duplex Operation
2400 / 1200 / 300 BPS Full Duplex DATA Mode
CMOS Technology
Automatic Adaptive Equalization
Guard Tone Generators
Call Progress Monitor Mode

APPLICATIONS

V.29 Modems
Fax Machine Modem
PC Fax/Data Modem
Hayes Compatible Modems

PIN ASSIGNMENT



(For other pin assignments refer to the end of this datasheet)

ORDERING INFORMATION

Part Number.	Package	Operating Temperature
XR-2901CP	Plastic DIP	0°C to 70°C
XR-2901CJ	PLCC	0°C to 70°C
XR-2901CQ	QFP	0°C to 70°C
XR-2902CP	Plastic DIP	0°C to 70°C
XR-2902CJ	PLCC	0°C to 70°C
XR-2902CQ	QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3 to 7V
V_{SS}	0.3 to -7V
Input Voltage	V_{SS} -0.7V to V_{DD} +0.3V
Power Dissipation *(package limitation)*	
Plastic	1 watt
Derate above +25°C	5 mw/°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS: XR-2901 Test Conditions: T_A = 25°C, V_{DD} = 5V ± 5%, GND =0VDC, CLKIN = 20.2752MHz ±0.01%, unless otherwise specified

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{DD}	Positive Supply Current		45	70	mA	
V_{IL}	Low Level Input Voltage			0.8	V	All inputs except MC/$\overline{MP}$
				0.6	V	MC/$\overline{MP}$ input
V_{IH}	High Level Input Voltage	2.0			V	All inputs except X2/CLKIN
		3.0			V	X2/CLKIN
I_I	Input Current			±20	µA	All inputs except X2/CLKIN
				±50	µA	X2/CLKIN
V_{OH}	High Level Output Voltage	2.4	3.0		V	I_{OH} = 300µA
V_{OL}	Output Logic Low voltage		0.3	0.5	V	I_{OL} = 2mA
I_{OH}	High Level Output Current			-300	µA	
I_{OL}	Low Level Output Current			2	mA	

ELECTRICAL CHARACTERISTICS : XR-2902 Test Conditions: V_{DD} = 5 VDC ± 5%. V_{SS} =-5 VDC ± 5%, T_A = 25°C, CLKIN = 5.0688MHz ±0.01% unless otherwise specified.

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{DD}	Positive Supply Current		15	25	mA	
	PWRD Mode			5	mA	
I_{SS}	Negative Supply Ciurrent		-15	25	V	
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2.0			V	
I_I	Input Current			10	µA	
V_{OH}	Output Logic High Voltage	3.0			V	I_{OH} = 300µA
V_{OL}	Output Logic Low Voltage			0.4	mA	I_{OH} = 2mA
I_{OH}	Logic High Output Current		-300		µA	
I_{OL}	Logic Low Output Current		1.6		mA	

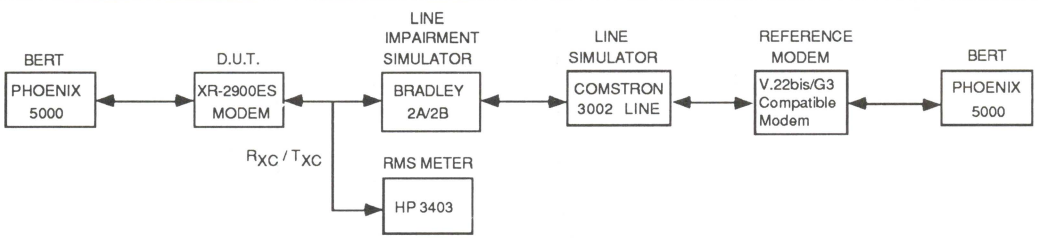
SYSTEM DESCRIPTION

The XR-2901/2902 chip set provides the complete data pump function for both G3 9600 BPS fax, as well as V.22bis data modes of operation. A complete microcontroller interface for popular devices such as 8031 types, is also included.

For fax modes of operation, fallback from 9600 BPS to 7200 BPS, 4800 BPS, or 2400 BPS is provided for poor line quality conditions. Data mode operation provides high compatibility with 2400 BPS, as well as 1200 BPS and 300 BPS modems.

AC CHARACTERISTICS *Refer to Figure 1, (ADD = Address)*

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
T_{ALE}	Address Latch Enable Pulse Width	100			ns	
T_{LCM}	Minimum Latch to $\overline{READ}/\overline{WRITE}$ Control	60			ns	
T_{READ}	$\overline{READ}$ Pulse	0		160	ns	
T_{RWL}	$\overline{READ}/\overline{WRITE}$ Control to Latch	20			ns	
T_{WRITE}	$\overline{WRITE}$ Pulse Width	.140		25	µs	
T_{AL}	ADD/$\overline{CS}$ Set-up Before ALE	40			ns	
T_{LAH}	ADD/$\overline{CS}$ Hold After Latch	40			ns	
T_{DRD}	Valid Data From $\overline{READ}$	0		140	ns	
T_{DAR}	Data Held After $\overline{READ}$	0		200	ns	
T_{WS}	Write Data Set-up After $\overline{WRITE}$	150			ns	
T_{DHAW}	Data Hold After $\overline{WRITE}$	40			ns	
TRANSMITTER POWER LEVELS						
TX_{CAR}	Transmit Carrier Power	-.6			dBm	QAM, DPSK, FSK Modulation
$TX_{CAR\ 550}$	550 Hz Guard Tone Power	-1.7		-.4	dBm	GTE=1, GTS=0
$TX_{CAR1800}$	1800Hz Guard Tone Power	-5.2		-3.4	dBm	GTE=1, GTS=1
SYSTEMS SPECIFICATIONS *See Performance Test Set-Up*						
DYNMC	Dynamic Range Min Limits	-43			dBm	
S/N V.22bis	Signal-to-Noise Ratio for V.22bis		17		dB	2400BPS operation BER ≤ $1/10^{-5}$
S/N V.29	Signal-to-Noise Ratio for V.29 (9600BPS)		23		dB	9600BPS operation BER ≤ $1/10^{-5}$
PCD	Carrier Detect Level		-43		dBm	
CDHYT	Carrier Detect Hysteresis		3		dB	



Performance Test Set-Up

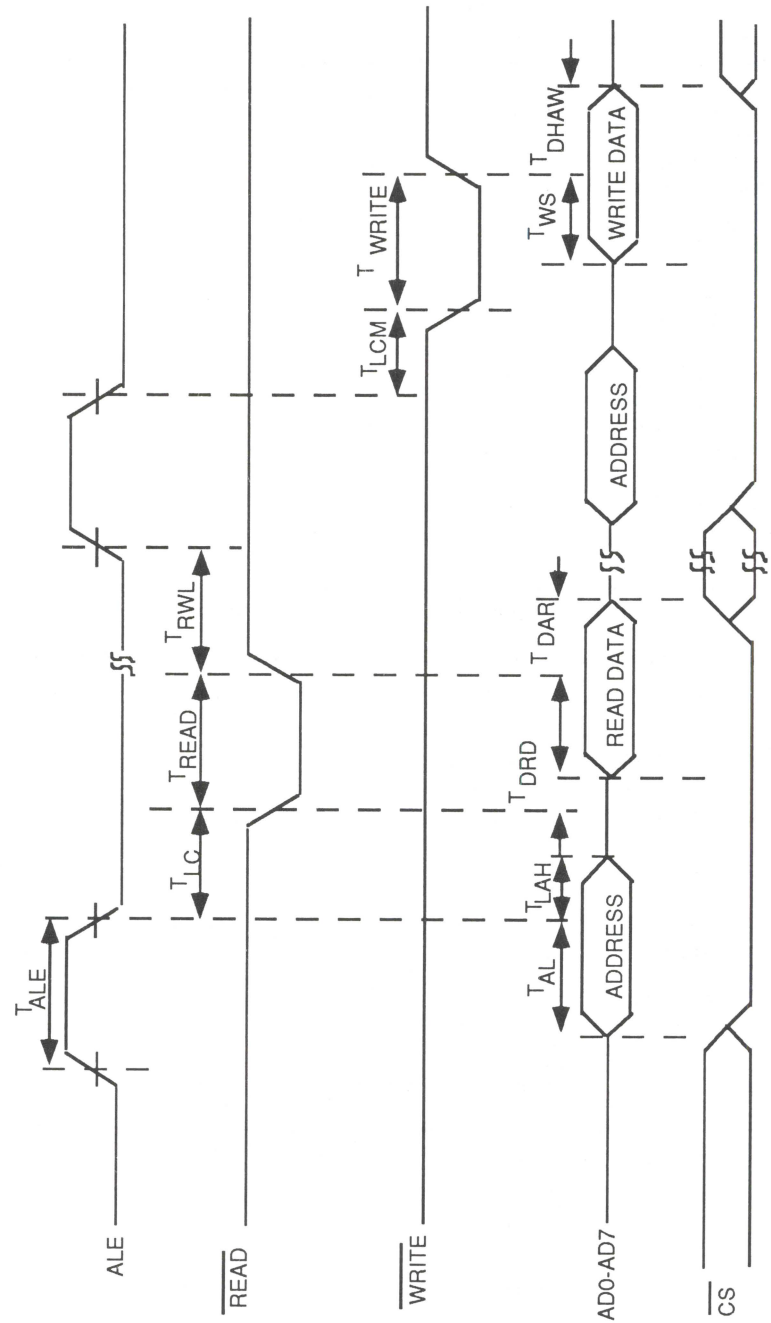
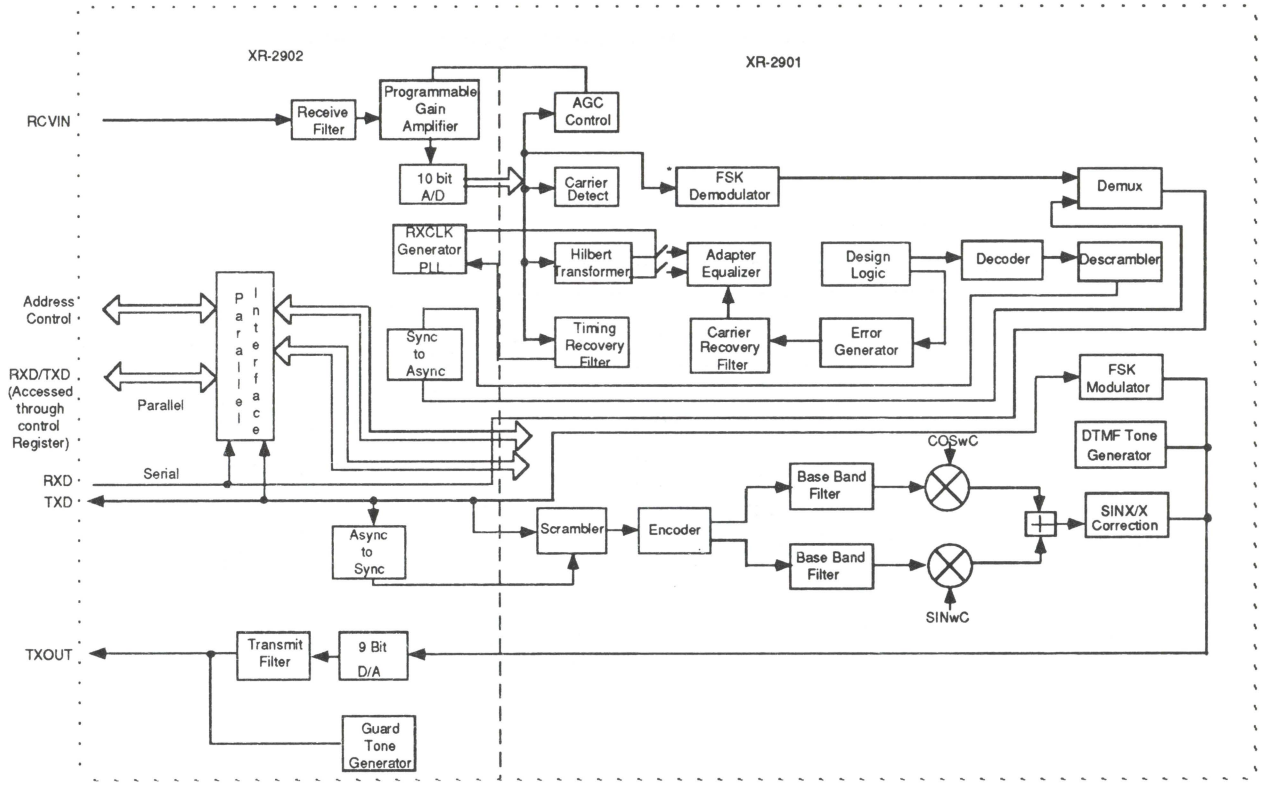


Figure 1. A.C. Timing Diagram



*Actually in XR-2902, shown in XR-2901 for Simplicity

Figure 2. Equivalent Block Diagram

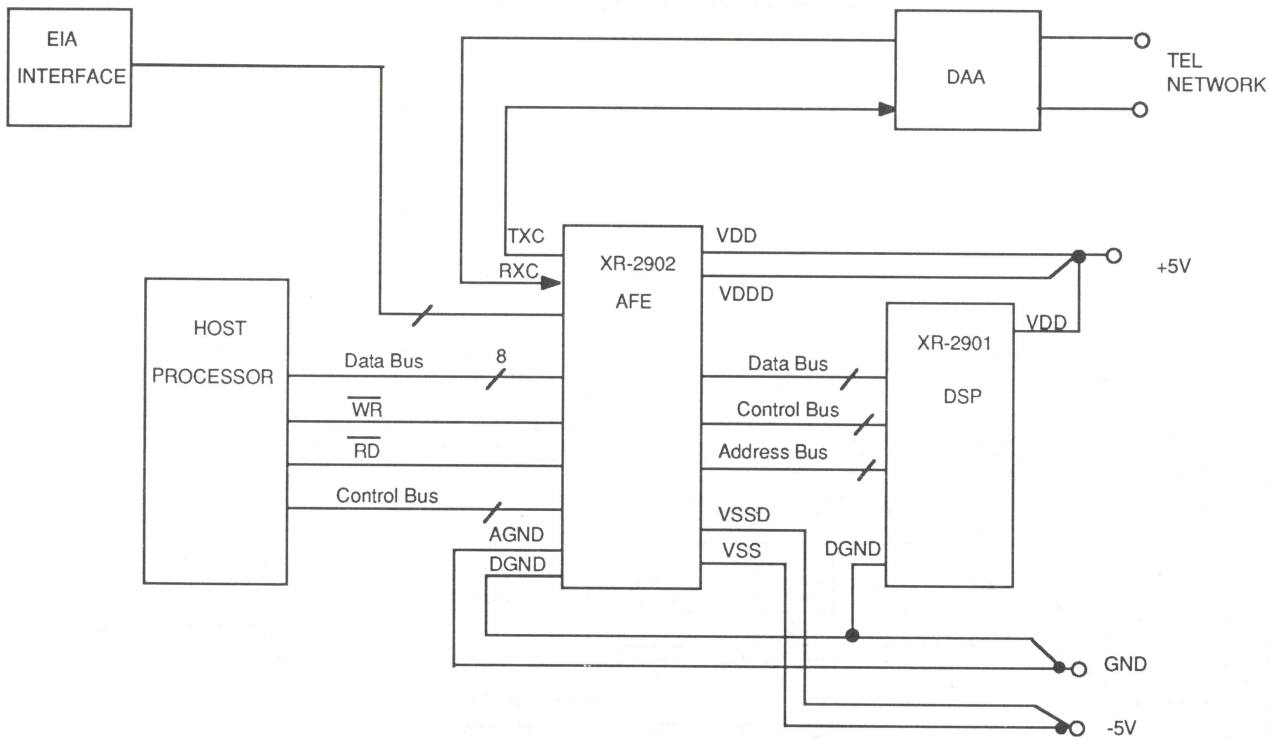


Figure 3. XR-2900 Generalized system Connection

PIN DESCRIPTIONS: XR-2901 *(DIP Package Pin Numbers)*

Pin #	Symbol	I/O	Description
1,2,40	A0/PA0-A2/PA2	I/O	Input/Output Port Address
3	MC/$\overline{MP}$	I	Micro-controller/Micro-processor control input
4	$\overline{RS}$	I	$\overline{RESET}$, used to initialize the device.
5	$\overline{INT}$	I	External Interrupt Input
6	CLKOUT	O	Clock Output equal to 1/4 of master 20.2752MHz clock (5.0688MHz)
7	X1	O	Crystal Oscillator Output
8	X2/CLKIN	I	Crystal Oscillator Input / External Clock Input
9	$\overline{BIO}$	I	Polling Input
10	GND	I	Ground
11-18	D8-D15	I/O	Data Lines 8-15
19-26	D7-D0	I/O	Data Lines 7-0
27-29	A11-A9	O	Address Lines 11-9
30	VDD	I	Positive Power Supply Input (+5 Volt)
31	$\overline{WEN}$	O	$\overline{Write\ Enable}$ Output
32	$\overline{DEN}$	O	$\overline{Data\ Enable}$ Output
33	$\overline{MEN}$	O	$\overline{Memory\ Enable}$ Output
34-39	A8-A3	O	Address Lines 8-3

PIN DESCRIPTIONS: XR-2902 *(DIP Package Pin Numbers)*

Pin #	Symbol	I/O	Description
1	VDD	I	Positive Analog Power Supply Input (+5 V)
2	TXCLK	O	Transmit Clock Output
3	NC		
4	$\overline{RXCLK}$	O	Receive Clock Output
5	$\overline{IRQ}$	O	Interrupt Request. Open collector type output
6	EXTXC	I	External Transmit Clock Input
7	$\overline{TXD}$	I	$\overline{Serial\ Transmit\ Data}$ Input
8	$\overline{RESET}$	I	$\overline{Reset}$ Input
9	$\overline{CS0}$	I	$\overline{Chip\ Select}$ Input
10	VSSD	I	Negative Digital Power Supply Input (-5Volt)
11	VDDD	I	Positive Digital Power $\overline{Supply\ Input}$ (+5 Volt)
12	$\overline{READ}$	I	$\overline{Read\ Enable}$ Input
13	ALE	I	Address Latch Enable Input
14	$\overline{WRITE}$	I	$\overline{Write\ Enable}$ Input
15-22	HD0-HD7	I/O	Address/Data Bus Input / Output
23	RXD	O	Serial Receive Data Output, Open Collector
24	DGND	I	Digital Ground
25-34	TD0-TD9	I/O	DSP Data Bus
35-37	PA0-PA2	I/O	Port Address Input / Output
38	CLKIN	I	Master Clock Input. 5.0688MHz
39	$\overline{DEN}$	I	$\overline{Data\ Enable}$ Input
40	$\overline{WEN}$	I	$\overline{Write\ Enable}$ Input
41	$\overline{INT}$	O	Interrupt Output
42	VSS	I	Negative Analog Power Supply Input (-5 Volt)
43	C2	I	AGC Input
44	C1	O	AGC Output
45	TXOUT	O	Transmit Carrier Output
46	AGND	I	Analog (Signal) Ground
47	RCVIN	I	Receive Carrier Input
48	SPKO	O	Speaker Output

MODES OF OPERATION

The XR-2900 supports various modes of operation for both fax and data standards, as shown in figure 4.

FAX (Half Duplex)		DATA (Full Duplex)	
Standard	Data Rate (BPS)	Standard	Data Rate (BPS)
V.29	9600	V.22bis	2400
	7200	V.22	1200
		*212A	1200
V.27ter	4800	*103	300
	2400		
**V.21 Ch.2	300		

**Bell Standard, all others are CCITT.*
***Used only for signalling, not a data mode.*

Figure 4. XR-2900 Fax/Data Modes

To support the various standards and speeds, as shown in Figure 5, three different modulation schemes are utilized:

- FSK Frequency Shift Keying
  -Two discrete frequencies are used to represent binary data.
- PSK Phase Shift Keying
  -Phase changes in a constant fre quency carrier represent data to be transmitted.
- QAM Quadrature Amplitude Modulation
  -Both phase and amplitude modula tion of a constant frequency carrier are used to represent data to be transmitted.

These different modulation schemes are necessary due to phone line bandwidth limitations. As data rates increase, each discrete change (frequency/phase/amplitude) is used to represent groups of data. The changes are known as baud, the rate of change being the modems baud rate. Figure 5 shows the relationship between the actual data transfer rate in bits per second (BPS) and baud rate. The data encoding indicates how many bits of data are represented by each baud change.

Mode	Data Rate (BPS)	Baud Rate	Data Encoding	Modulation Scheme	Carrier Frequency (Hz)	*Transmit CarrierShaping
V.29	9600	2400	Quadbit	QAM	1700	20%
V.29	7200	2400	Tribit	QAM	1700	20%
V.29	4800	2400	Dibit	QAM	1700	20%
V.27ter	4800	1600	Tribit	PSK	1800	50%
V.27ter	2400	1200	Dibit	PSK	1800	90%
V.22bis	2400	600	Quadbit	QAM	1200/2400	75%
V.22	1200	600	Dibit	PSK	1200/2400	75%
212A	1200	600	Dibit	PSK	1200/2400	75%
103	300	300	-	FSK	1070/1270 2025/2225	-
V.21	300	300	-	FSK	980/1180 1650/1850	-

**Square root raised cosine shaping*

Figure 5. Data/Baud Rate Relationships

Modem baud changes may be shown as a signal constellation, illustrating possible combinations. Figure 6 illustrates the constellations for various modes of operation (not to scale).

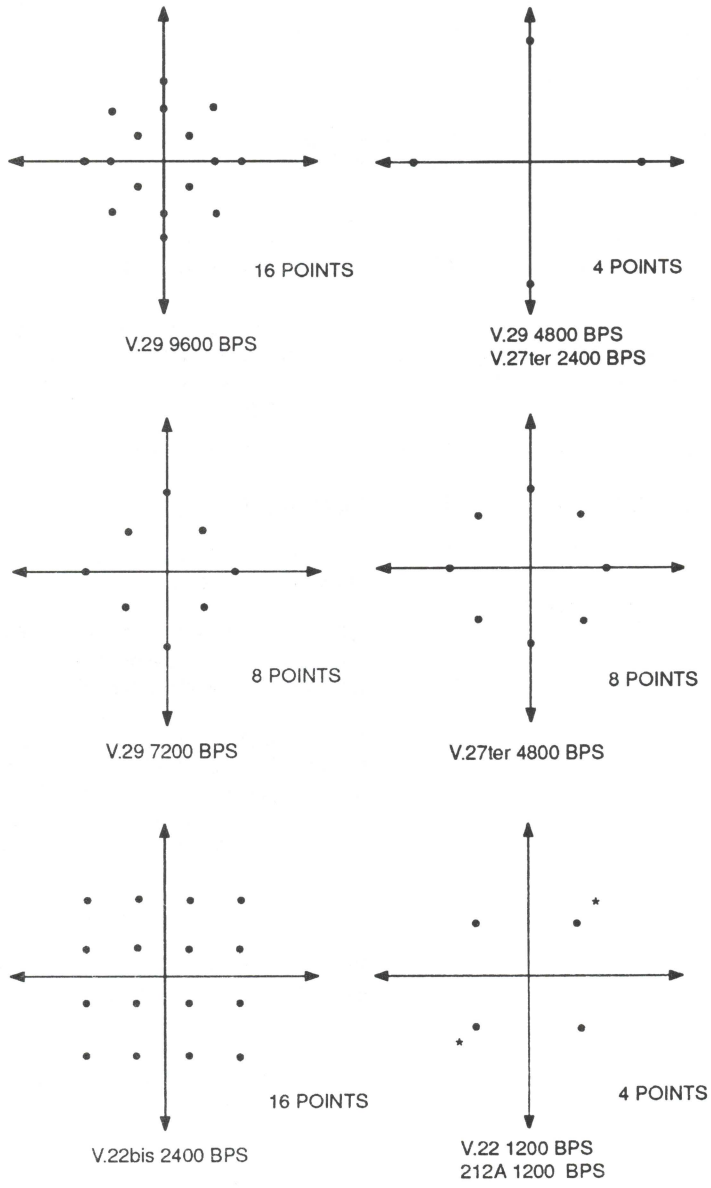


Figure 6. Signal Constellations

(FSK constellation will be two point, not to scale)*

The XR-2900 must generate several different tones to provide the necessary handshaking, guard tones, and other functions. Figure 7 lists these tones and related accuracy.

TONE (Hz)	FUNCTION	ACCURACY (%)
462	Procedure Interrupt	0.01
550/1800	Guard Tones	0.1
1100	Line Conditioning Signal/Calling Tone	0.01
2100	Answer Tone	0.1

Figure 7. Tone Generator Frequencies/Accuracy

REGISTER DESCRIPTION

The XR-2900 utilizes a set of 32, 8 bit, registers for controlling fax or data functions. A register plane is selected and then various modes/functions within that plane are programmed for fax or data operation. The MCFN bit is used for programming fax or data mode. A reset input will automatically default to the data plane.

REGISTERS FOR FAX OPERATION - INTERFACE MEMORY *(Refer to Figure 9)*

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
0:0	0-7	TXRXD	R/W	**TRANSCEIVER DATA:** Provides input for transmit data or output for receive data.
0:1	0-7	RESERVED		
0:2	0-7	FREQL	R/W	**RAM DATA/FREQUENCY SELECT LOW ORDER BYTE:** Low order byte of tone generator select.
0:3	0-7	FREQM	R/W	**RAM DATA/FREQUENCY SELECT HIGH ORDER BYTE:** High order byte of tone generator select. To enable the tone transmit mode, register 4, modem configuration must be set to Hex 80. The tone generator is controlled by a 16 bit, two byte, word written to the FREQL and FREQM reg isters from the host processor. The control word, N, repre sents the desired frequency by the relationship:

$$N = \frac{\text{Frequency}}{0.14648}$$

Below commonly used tones and the Hexadecimal num bers which are written to the FREQL/FREQM registers are listed.

Frequency (Hz)	FREQM	FREQL
462	0C	52
1100	1D	55
1650	2C	00
1850	31	55
2100	38	00

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION

DTMF tone generation mode is selected by setting the modem configuration register to Hex 81. Tone pairs are then controlled by bits 0-3 of register 2, as shown below:

Dial Digit	Register Value D3	D2	D1	D0	Tone Pairs fLow(Hz)	fHigh(Hz)
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	852	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477
A	1	1	0	0	697	1633
B	1	1	0	1	770	1633
C	1	1	1	0	852	1633
D	1	1	1	1	941	1633

0:4 0-7 MCFN R/W **MODEM CONFIGURATION:** This register provides mode control. This value, when the set up bit is set, controls the XR-2900 mode of operation. Figure 8 shows the mode/ register value relationship.

MCFN, Register 4, Bits 7	6	5	4	3	2	1	0	Hex	Mode
0	0	0	1	0	1	0	0	14	V.29 9600 BPS
0	0	0	1	0	0	1	0	12	V.29 7200 BPS
0	0	0	1	0	0	0	0	11	V.29 4800 BPS
0	0	0	0	1	0	1	1	0A	V.27ter 4800 BPS
0	0	0	0	1	0	0	1	09	V.27ter 2400 BPS
0	0	1	0	0	0	0	0	20	V.21 300 BPS
1	0	0	0	0	0	0	0	80	Tone Transmit
1	0	0	0	0	0	0	1	81	DTMF Tones Transmit
0	1	1	0	0	0	0	1	61	Bell 103 300 BPS
0	1	1	0	0	0	1	0	62	V.22bis/Bell 212A

Figure 8. Mode Programming

0:5 0-1 RESERVED

2 SQEXT R/W **SQUELCH EXTEND:** When set, receive carriers are gated out for 130mS after the transmitter is turned off.

3 EPT R/W **ECHO PROTECTION TONE:** When set, an unmodulated carrier (frequency determined by modem configuration register) is transmitted for 185mS, followed by 20mS of quiet, and then the normal training sequence.

4 RESERVED

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	5	RAMW	R/W	**RAM WRITE:** This bit is set when a write routine to the diagnostic RAM is needed. This bit will be reset when a diagnostic read routine is executed.
	6	TDIS	R/W	**TRAINING DISABLED:** When set, the modem goes directly to receive mode, bypassing the training sequence. If the modem is transmitting the training sequence will not occur at the start of transmission.
	7	RTS	R/W	**REQUEST TO SEND:** When set, the transmit sequence is initiated.
0:6	0-7	RESERVED		
0:7	0-3	RESERVED		
	4	RCVG	R/W	**RECEIVE FILTER GAIN CONTROL:** An additional 10dB of receive path gain (13dB for fax) can be selected by reset ting this bit. When set, fax 3dB of gain is selected for high receive level applications, such as leased line.
	5-7	RESERVED		
0:8	0-5	RESERVED		
	6	$\overline{CTS}$	R	**CLEAR TO SEND:** When low, indicates the XR-2900 is ready to send (transmit) data.
	7	RESERVED		
0:9	0-7	RESERVED		
0:A	0-3	RESERVED		
	4	SPC	R/W	**SPEAKER CONTROL:** When set, the speaker output is enabled.
	5	VOL 1	R/W	**VOLUME CONTROL 1:** See Volume Control 2 for description.
	6	VOL 2	R/W	**VOLUME CONTROL 2:** These two bits, Vol 1/Vol 2, control the signal amplitude at the speaker output, as shown below:

Vol 1	Vol 2	Relative Level
0	0	Low
0	1	Low
1	0	Medium
1	1	Maximum

	7	RESERVED		
0:B	0-7	RESERVED		
0:C	0-7	RESERVED		
0:D	0-3	TXL 1-4	R/W	**TRANSMIT LEVEL CONTROL:** These four bits control the transmit carrier level, as shown below. The values listed are attenuations from nominal transmitter output.

TXL4	TXL3	TXL2	TXL1	TXOUT Attenuation(dB)
0	0	0	0	-15
0	0	0	1	-14
0	0	1	0	-13
0	0	1	1	-12
0	1	0	0	-11
0	1	0	1	-10
0	1	1	0	-9

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
				0 1 1 1 -8 1 0 0 0 -7 1 0 0 1 -6 1 0 1 0 -5 1 0 1 1 -4 1 1 0 0 -3 1 1 0 1 -2 1 1 1 0 -1 1 1 1 1 -0
	4	RDEQ	R/W	**DELAY EQUALIZER ENABLE:** When set, a delay equalizer is enabled for compensating the telephone line characteristics.
	5	CAB 1	R/W	**CABLE EQUALIZER CONTROL 1:** See CAB 2.
	6	CAB 2	R/W	**CABLE EQUALIZER CONTROL 2:** CAB 1/CAB 2 control the cable equalizer amplitude compensation, as shown below:

CAB 1	CAB2	Length
0	0	0.0 Meters
0	1	1.8 Km
1	0	3.6 Km
1	1	7.2 Km

	7	RESERVED		
0:E	0	MDAO	R	**MODEM DATA AVAILABLE:** When high, data is ready for host processor to read or write data to register 0, during parallel data mode.
	1	RESERVED		
	2	IEO	R/W	**INTERRUPT ENABLE:** When set, the IRQ output will be set low, assuming MDA0 bit is set to a high.
	3	SETUP	R/W	**SETUP:** This bit must be set whenever a change is made to register 4. After configuration change is complete, this bit will be reset automatically.
	4-6	RESERVED		
	7	IAO	R	**INTERRUPT ACTIVE:** This bit will be set when IRQ is active
0:F	0-6	RMAA	W	**RAM ACCESS ARRANGEMENT:** This register is used to read various diagnostic functions from the XR-2901. The process of reading the functions is described in data plane, register 0:F (Bits 0-6).
	7	PDM	R/W	**PARALLEL DATA MODE:** When set, the modem is put in parallel data mode and the diagnostic RAM cannot be read.
1:0	0-7	RESERVED		
1:1	0-7	RESERVED		
1:2	0-7	RESERVED		
1:3	0-7	RESERVED		
1:4	0-1	RESERVED		
	2	$\overline{\text{P2DET}}$	R	**P2 DETECTION:** This bit, when low, indicates that the P2 pattern has been received.
	3-7	RESERVED		
1:5	0-5	RESERVED		
	6	$\overline{\text{FED}}$		True Energy Detect
	7	RESERVED		

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
1:6	0-7	RESERVED		
1:7	0	$\overline{\text{CDET}}$	R	**CARRIER DETECT:** When low, indicates the presence of a received signal within the passband of the received filters. $\overline{\text{CDET}}$ will remain high during a training sequence. CDET will go low at the start of data state and return to a one at the end of the receive signal.
	1-5	RESERVED		
	6	$\overline{\text{PNDET}}$	R	**PN DETECT:** When low, the PN sequence has been detected during the training sequence.
	7	RESERVED		
1:8	0-7	RESERVED		
1:9	0-7	RESERVED		
1:A	0-7	RESERVED		
1:B	0-4	RESERVED		
	5	FR1	R	**FREQUENCY 1 DETECT:** When high, a 2100 Hz tone has been detected. This register is only active if V.21 mode has been set.
	6	FR2	R	**FREQUENCY 2 DETECT:** When high, a 1100 Hz tone has been detected.
	7	FR3	R	**FREQUENCY 3 DETECT:** When high, a 462 Hz tone has been detected.
1:C	0-7	RESERVED		
1:D	1	$\overline{\text{FRT}}$	R/W	**FREEZE TAPWEIGHTS:** This bit, when reset, freezes the last positions of the tapweights of the adaptive equalizer. This bit can be used to compensate for a momentary loss of receive carrier in fax reception.
	0,2-7	RESERVED		
1:E	0-7	RESERVED		
1:F	0-7	RESERVED		

REGISTERS FOR DATA MODE OPERATION - Modem Register Plane.
Refer to Figure 10. NOTE 1: See fax register for description.

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
0:0	0-7	PRXD	R	**PARALLEL RECEIVER DATA:** In parallel mode, the received data is read from this register, when PDM bit (register 0F, Bit 7) is set.
0:1	0-7	PTXD	W	**PARALLEL TRANSMIT DATA:** Data to be transmitted, in parallel mode is written to this register, when PDM bit (register0 F, Bit 7) is set.
0:1	0	STXD	W	**SERIAL TRANSMIT DATA:** When the PDM bit is set and the SPDM bit is set, this bit can be used to send data in serial/parallel mode. This serial/parallel mode is data input into a parallel register, but bit by bit (one bit at a time).
0:2	0-7	FREQL	R/W	NOTE 1
0:3	0-7	FREQM	R/W	NOTE 1
0:4	0-7	MCFN	R/W	NOTE 1
0:5	0	REQ	R/W	**RESET EQUALIZER:** The setting of this bit sets the adaptive equalizer of the XR-2901.
	1	UNDEFINED		

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	2	SCR	R/W	**SCRAMBLER ENABLE:** When this bit is set, the scrambler for the transmitter and descrambler for the receiver are enabled.
	3	RXSP	R/W	**RECEIVER SPEED SELECT:** This bit, when set, selects 2400 BPS and when low, 1200 BPS modes of operation.
	4	TXSP	R/W	**TRANSMITTER SPEED SELECT:** This bit, when set selects 2400 BPS and when low, 1200 BPS modes of operation.
	5	UNDEFINED		
	6	UNDEFINED		
	7	RTS	R/W	**REQUEST TO SEND:** This bit controls the XR-2900 transmitter. When set, the transmitter is on. A low level stops the transmitter carrier.
0:6	0-7	UNDEFINED		
0:7	0	UNDEFINED		
	1	MOD	W	**MODE SELECT:** When set, answer mode and when reset, originate modes of operation are selected.
	2	GTE	R/W	**GUARD TONE ENABLE:** This bit, when set, enables either a 550 Hz or 1800 Hz tone to be transmitted.
	3	GTS	R/W	**GUARD TONE SELECT:** This bit, when set, selects an 1800 Hz tone, and when reset, a 550 Hz tone.
	4	RCVG	R/W	**RECEIVE FILTER GAIN CONTROL:** When set, 16dB of receive gain is selected. Resetting this bit lowers the gain to 6dB.
	5	PWRD	R/W	**POWER DOWN:** Setting this bit puts the XR-2902 into a low power mode. (See Electrical Characteristics for supply current values.)
	6	CPM	R/W	**CALL PROGRESS MONITORING:** When set, call progress mode of operation will be selected.
	7	ALB	R/W	**ANALOG LOOP BACK:** This bit, when set, enables the analog loop back mode of the XR-2900. The transmitted signal bypasses the receive filter and is applied to the demodulator input. Originate/Answer modes are selected by the Mode bit.
0:8	0	RXD	R	**RECEIVE DATA OUTPUT:** This bit represents the receive data in a serial format. The data at this point has not yet passed through the data buffer (sync-to-async converter.)
	1	URXD	R	**UNSCRAMBLED RECEIVE DATA OUTPUT:** The data available at this location is directly from the demodulator output, prior to the demodulator. This signal is used during handshaking and DLB initiation.
	2	CD	R	**CARRIER DETECT:** this bit is the output of the energy detect circuit, and is the logical inversion of FED.
	3	SGQ	R	**SIGNAL QUALITY:** When high, this bit indicates a degradation of signal quality and increased chance for errors. Less severe signal degradations will cause this output to 'chatter', and an averaging may be necessary.
	4	S1D	R	**S1 SIGNAL DETECT:** This bit, when high, indicates the detection of an S1 pattern.
	5	DOT	R	**DOTTING PATTERN DETECTORS:** A high at this bit indicates the reception of a dotting pattern, as used in a request for remote digital loopback.

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	6	UNDEFINED		
	7	UNDEFINED		
0:9	0	CRXD	R/W	**CLAMP RECEIVE DATA:** When set, the receive data output will be clamped to a high level.
	1	SPDM	R/W	**SERIAL DATA MODE SELECT:** When set, the serial/parallel data mode is selected. See STXD (Register 1, Bit 0) for mode description.
	2	SLAVE	R/W	**SLAVE MODE:** When this bit is set, the transmit clock is internally connected to the receive clock.
	3	ETE	R/W	**EXTERNAL TRANSMIT CLOCK ENABLE:** This bit, when set, allows an external transmit clock to be applied to pin 6 of the XR-2902.
	4	DLB	R/W	**DIGITAL LOOP BACK:** When enabled, set to a high, the transmit clock will track the receive clock, and transmit data will be tied to the receive data. This bit is used to enable remote digital loopback after a receive signal dotting pattern is detected.
	5	NTD	R/W	**NORMAL TRANSMIT DATA:** When this bit is set, the transmit path is from the STXD, transmit byte register, or TXD pin. When reset, the special transmit pattern bits control the data to be transmitted.
	6	STC1	R/W	**SPECIAL TRANSMIT PATTERN CONTROL 1:** See STC2
	7	STC2	R/W	**SPECIAL TRANSMIT PATTERN CONTROL 2:** STC1/STC2 control the generation of special transmit patterns, as described below:

STC2	STC1	PATTERN
0	0	Space
1	0	Mark
1	1	Dotting
1	0	300Hz for S1 Pattern

0:A	0	DBEN	R/W	**DATA BUFFER ENABLE:** This bit, when set, enables the async-to-sync and sync-to-async converters.
	1	DSPD	R/W	**DATA BUFFER OVERSPEED SELECT:** This bit, when set, extends the allowable asynchronous data rate from its normal +1% / -2.5% to +2.3% / -2.5%.
	2-3	BC1/BC2	R/W	**BIT PER CHARACTER SELECTION:** The asynchronous character lengths are controlled according to the following table:

BC2	BC1	Character Length (1 start+data+1 stop)
0	0	8 Bits
0	1	9 Bits
1	0	10 Bits
1	1	11 Bits

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	4	SPC	R/W	**SPEAKER CONTROL:** This bit, when set, enables the speaker output.
	5,6	VOL1, VOL2	R/W	**VOLUME CONTROL 1/2:** NOTE 1
	7	RESERVED	R/W	**SPECIAL EXAR TEST BIT.** This bit must be set to low for normal operation.
0:B	0-7	RESERVED		
0:C	0-7	RESERVED		
0:D	0-3	TXL1-4	R/W	**TRANSMIT LEVEL CONTROLS:** NOTE 1
	4-7	RESERVED		
0:E	0	MDA0	R	**MODEM DATA AVAILABLE:** NOTE 1
	1	MDAT	R	**TRANSMIT MODEM DATA AVAILABLE:** This bit, when set indicates transmit data can be applied to the transmit register.
	2	IEO	R/W	**RECEIVE INTERRUPT ENABLE:** This bit will go low when the receive data buffer is full.
	3	SETUP	R/W	**SETUP:** This bit must be set whenever a change is made to register 4. When the change is complete, the bit will be reset.
	4	IET	R/W	**INTERRUPT ENABLE:** This bit will be high when the transmit buffer is empty.
	5-6	RESERVED	R/W	
	7	IAO	R	**INTERRUPT ACTIVE:** This output indicates when the XR-2902 has requested an interrupt.
0:F	0-6	RMAA	R/W	**RAM ACCESS ADDRESS:** These bits select the RAM address for the XR-2901 for diagnostic purposes. Figure 10 contains the function information. The process of reading these locations is as follows: •Load desired RAM location into location 0F, Bits 0-6. •Read Register 0; this resets register 0E, Bit 0. •When Register 0E, Bit 0, returns to a Logic 1, data is present at Register 0:3 as described in Figure 10.
	7	PDM	R/W	**PARALLEL MODE:** This bit, when set, allows TXD/RXD to go through parallel bus.
1:0-1:4	0-7	RESERVED		
1:5	0-5	RESERVED		
	6	FED	R	**FAST ENERGY DETECT:** NOTE 1
	7	RESERVED		
1:6-1:A	0-7	RESERVED		
1:B	0-4	RESERVED		
	5, 6, 7	FR1, FR2, FR3	R	**FREQUENCY 1, 2, 3 DETECT:** NOTE 1
1:C	0-7	RESERVED		
1:D	0	RESERVED		
	1	FRT	R/W	**FREEZE EQUALIZER TAPS:** When set, the equalizer taps are fixed at their last value. This is used to compensate for a momentary loss of receive carrier.
	2-7	RESERVED		
1:E-1:F	0-7	RESERVED		

Location BIT	7	6	5	4	3	2	1	0
1 F								
1 E								
1 D							$\overline{\text{FRT}}$	
1 C								
1 B	FR3	FR2	FR1					
1 A								
1 9								
1 8								
1 7		$\overline{\text{PNDET}}$						$\overline{\text{CDET}}$
1 6								
1 5		$\overline{\text{FED}}$						
1 4						P2DET		
1 3								
1 2								
1 1								
1 0								
0 F	PDM	RAM Access Address						
0 E	IA0				SETUP	IE0		MDA0
0 D		CAB2	CAB1	RDEQ	TXL4	TXL3	TXL2	TXL1
0 C								
0 B								
0 A	TEST	VOL2	VOL1	SPC				
0 9								
0 8		$\overline{\text{CTS}}$						
0 7				RCVG				
0 6								
0 5	RTS	TDIS	RAMW		EPT	SQEXT		
0 4	Modem Configuration							
0 3	RAM Data XSM; FREQM							
0 2	RAM Data XSL; FREQL							
0 1								
0 0	Transceiver PTXRXD							

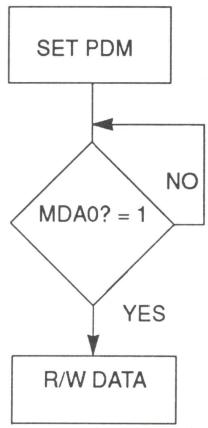
Figure 9. XR-2900 Control Register Plane for Fax Operation

Location	7	6	5	4	3	2	1	0
1 F								
1 E								
1 D							FRT	
1 C								
1 B	FR3	FR2	FR1					
1 A								
1 9								
1 8								
1 7								
1 6								
1 5		FED						
1 4								
1 3								
1 2								
1 1								
1 0								
0 F	PDM	RAM Access Address						
0 E	IA0			IET	SETUP	IE0	MDAT	MDA0
0 D	GTE				TXL4	TXL3	TXL2	TXL1
0 C								
0 B								
0 A	TEST	VOL2	VOL1	SPC	BC2	BC1	DSPD	DBEN
0 9	STC2	STC1	NTD	DLB	ETE	SLAVE	SPDM	CRXD
0 8			DOT	S1D	SGQ	CD	URXD	RXD
0 7	ALB	CPM	PWRD	RCVG	GTS	GTE	MOD	- -
0 6								
0 5	RTS			TXSP	RXSP	SCR		REQ
0 4	Modem Configuration							
0 3	RAM Data XSM; FREQM							
0 2	RAM Data XSL; FREQL							
0 1	Parallel Transmit Data PTXD							STXD
0 0	Parallel Receiving Data PRXD							

Figure 10. XR-2900 Control Register Plane for Data Mode

Read / Write Parallel Data Transfer to the XR-2900 -Transferring data to and from the XR-2900 is done differently, depending whether polling or interrupt driven.

POLLING



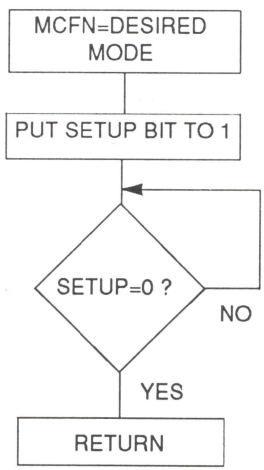
REG O: F (HEX15) BIT 7

INTERRUPT

FULL DUPLEX
1. Set PDM
2. Set IE0 IET to Enable Interrupt
3. Depending on Transmit or Receive Data
   MDA0 - For RXD
   MDAT - For TXD
   Reset INT to low
4. When Data is ready the interrupt will go low

HALF DUPLEX
1. Set PDM Mode
2. Set IEQ to Enable Interrupt
3. When Data is ready, the interrupt will go low

XR-2900 Mode Setting - The following flow diagram describes the XR-2900 mode setting procedure.



REG 0:E (HEX 14) BIT 3

POWER ON RESET

The XR-2900 contains an automatic internal hardware power-on reset/initialization routine. On power up the chip set is configured for V.29/9600 BPS fax operation. The following lists the functions within the fax mode set by the reset routine, with respective registers/values.

Mode/Function	(FAX Plane) Control Register	Register Value(HEX)
•V.29 / 9600 BPS	04	14
•Serial Data Transfer		
•Training Enabled		
•Echo Protector Tone Enabled	05	08
•No Extended Squelch		
•High Receive Gain Selected (16 dB)	07	00
•Unused Register	09	00
•Speaker Output is Disabled	0A	00
•Set Transmit Carrier Amplitude and Disable Receiver Cable Equalizer	0D	00

Call Progress Mode Operation

Call Progress Mode (CPM) is a mode of operation (during Data Mode) which allows the modem to detect various telephone signals. These signals are:

- Busy Tone
- Dial Tone
- Ring Back
- Answer Tone (Modem)

As the telephone signals fall in a different frequency band than the modem carriers, filtering requirements must change. To achieve this, the receive filter is changed for moniroting the various tones, as shown in table 1. In each case the carrier detect (CD) bit, bit2/Register 0:8 in data plane, is monitored. Sensing not only high or low, but also the duration and repetition rate of the CD active state is required.

CPM	MOD	CD
1	0	Receive High Band Monitor Answer Tone
1	1	Receive Low Band: Monitor Dial Tone, BusyTone and Ring Back Signal.
0	0	Normal High Band Energy Detect
0	1	Normal Low Band Energy Detect

CPM: REG 0:7, Bit 6
MOD: REG 0:7, Bit 1
CD: REG 0:8, Bit 2

Table 1. CD Frequency Band Assignments

APPLICATIONS INFORMATION

The XR-2900 Fax/Data chip set provides the complete data pump function for implementing a modem supporting 9600 BPS G3 facsimile operation, as well as full duplex data capability at 2400 BPS, 1200 BPS, and 300 BPS. The generalized system connection, figure 3, illustrates the remaining functions supporting the XR-2900 to complete the modem, also described here:

•Data Pump - XR-2900/XR-2901 chip set
- Modulation/demodulation for Fax/ Data Modes
- Signals for Handshaking/Establishing Connections/Telephone Signals (call progress, dialing)
- Test Modes
- Interface for Host Controller

•Telephone Line Interface (DAA)
- Line Interface Functions Required by FCC
- DC Isolation
- High Voltage Protectio
- Out of Band Frequency Suppression
- Hybrid Function for Separating Transmit and Receive Signals

•DTE (Data Terminal Equipment) Interface
- Serial (Stand-alone type modem)
- EIA Level Translation (RS-232C)
- Parallel (Internal Type Modem)

UART- (Serial to Parallel Conversion)

•Host Controller
- Timing/Control for Handshaking
- Command (Hayes®, MNP®, Fax Control) Interpretation
- ROM (EPROM) for Commands
- RAM (MNP, Data Mode)

EXAR's modem schematic illustrates a practical example of a stand-alone Fax/Data modem where a 8031 type microprocessor provides the system control for the XR-2901/XR-2902 chip set. An external EPROM contains the control commands, such as Hayes commands for data mode. EXAR will also offer a masked ROM controller, supporting MNP 5 V.42 and V.42bis operation during data mode (pin-to-pin replacement for generic 8031 controller).

LAYOUT CONSIDERATIONS

The XR-2900 provides the heart of the modem system, which processes signals from very low level analog to logic level digital. This mix of sensitive analog with noise causing digital signals calls for some special care in system layout.

Referring to figure 3, the generalized connection, the most critical signals path is that of the transmit (TXOUT) and receive (RCVIN) signals. They are passed from the telephone network through the line interface circuit (DAA) and on to the XR-2902 AFE. This path should be kept as short as possible and away from the digital circuitry, microcontroller and its memory components, and XR-2901 DSP. Figure 11 illustrates this concept.

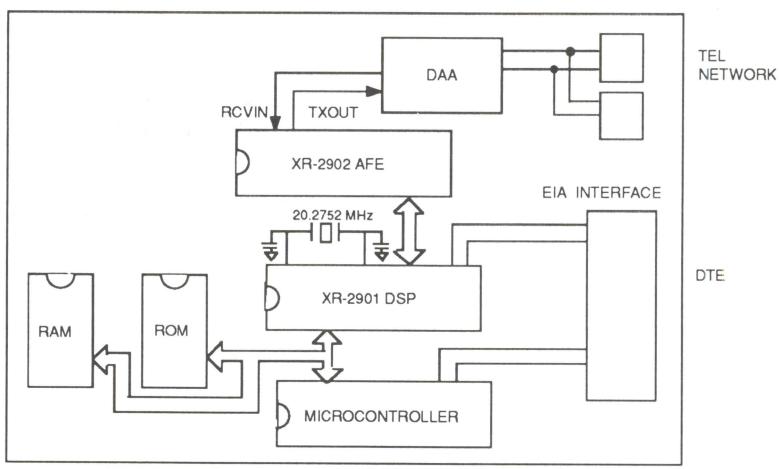


Figure 11. XR-2900 System Layout

CRYSTAL OSCILLATOR

The XR-2900 master clock, typically generated from a 20.2752 MHz crystal is another area requiring special attention. As with the analog and digital signal considerations, the crystal should be kept away from the TXC/RXC signal paths.

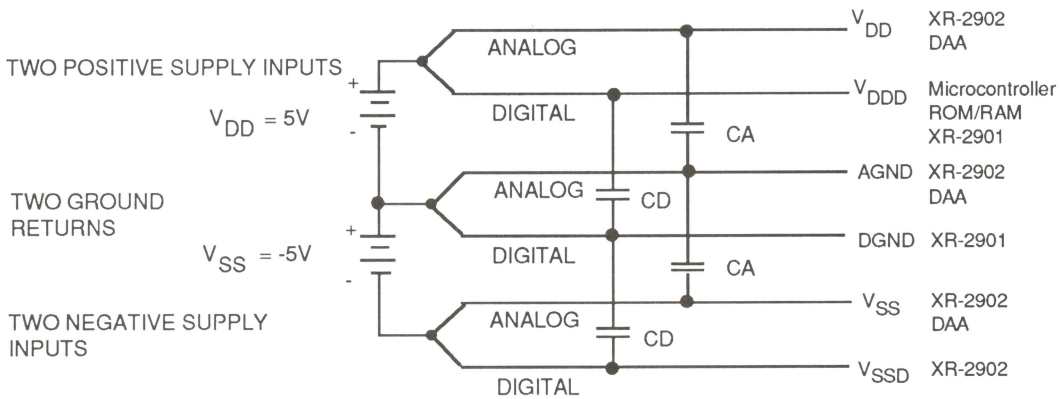
The accuracy and stability of the clock circuit are also extremely important. Per system specifications, it must have an accuracy of less than ±0.01 percent from nominal. The type of oscillator circuitry within the XR-2901 requires a parallel resonant type crystal. Typical external load capacitance (which can vary for different crystals) is 17pF. The capacitors should be returned to digital ground. The lines from the crystal to the XR-2901 should be kept short to minimize stray capacitance.

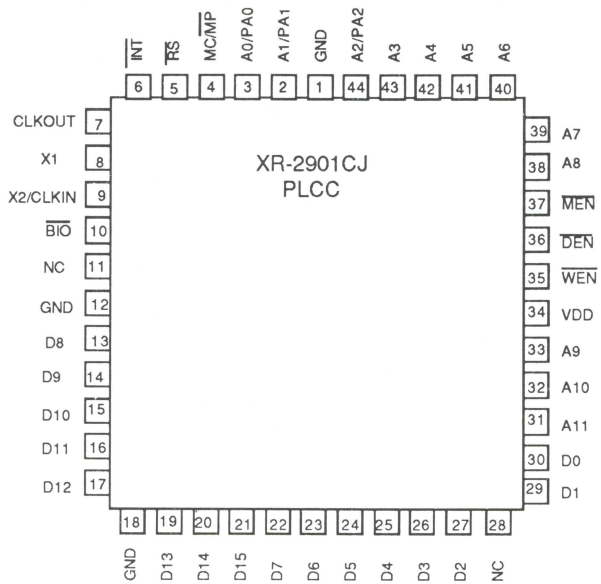
POWER / GROUND PRECAUTIONS

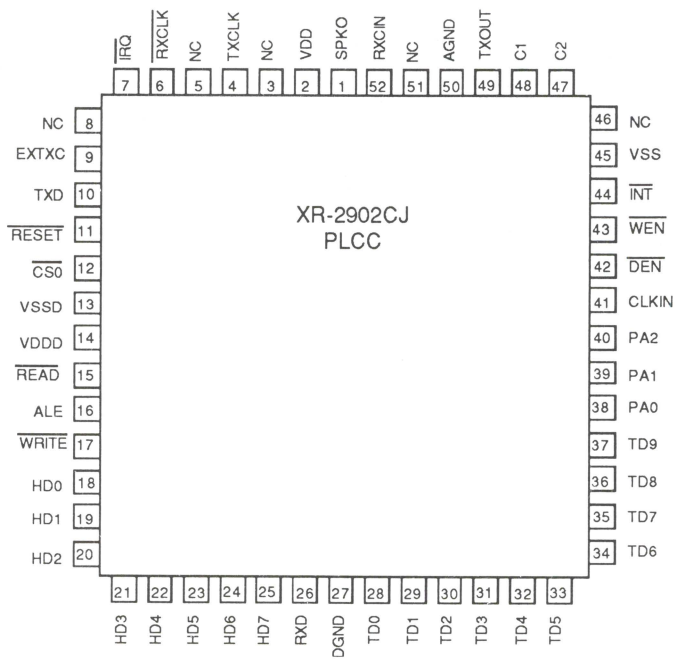
To help keep analog and digital circuitry separated, the system should incorporate independent paths for the power and signal supplies and gounds. As illustrated below, the digital and analog lines should be kept separated up to the power supply where they are single point connected.

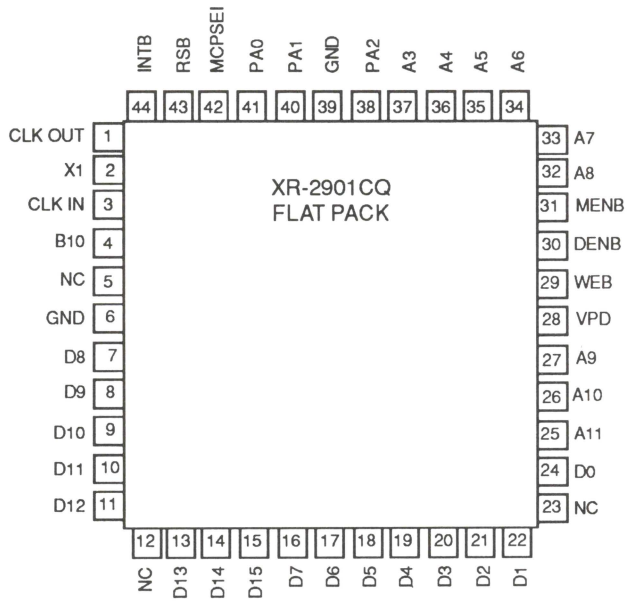
Supply bypassing is important with both VDD (VDDD) and VSS (VSSD), each having several bypassing capacitors distributed around the board. The VSS line near the XR-2902 is particularly critical and should have bypassing near it. Capacitors on analog supplies are returned to analog ground, and likewise digital to digital.

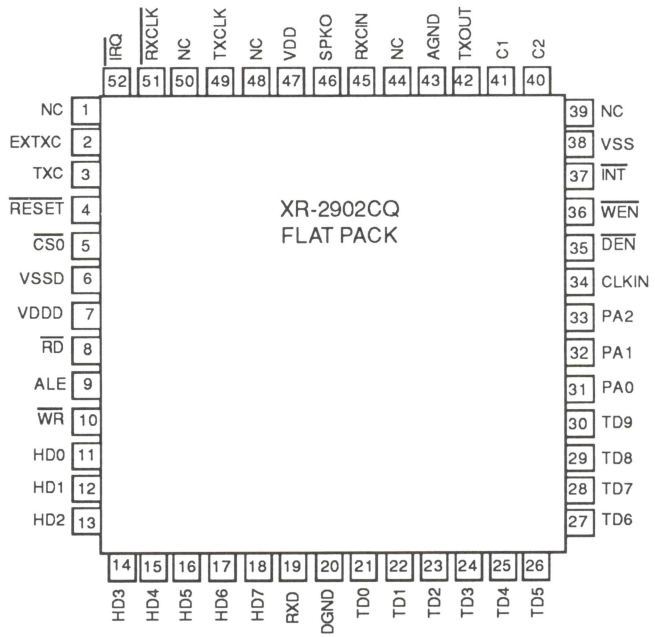
Capacitor valves around the board of 0.01µF are usually adequate, with a larger value, 4.7µF, at the power supply.




XR-2901CJ
PLCC
INT 6
RS 5
MC/MP 4
A0/PA0 3
A1/PA1 2
GND 1
A2/PA2 44
A3 43
A4 42
A5 41
A6 40
CLKOUT 7
X1 8
X2/CLKIN 9
BIO 10
NC 11
GND 12
D8 13
D9 14
D10 15
D11 16
D12 17
39 A7
38 A8
37 MEN
36 DEN
35 WEN
34 VDD
33 A9
32 A10
31 A11
30 D0
29 D1
18 GND
19 D13
20 D14
21 D15
22 D7
23 D6
24 D5
25 D4
26 D3
27 D2
28 NC


XR-2902CJ
PLCC
IRQ 7
RXCLK 6
NC 5
TXCLK 4
NC 3
VDD 2
SPKO 1
RXCIN 52
NC 51
AGND 50
TXOUT 49
C1 48
C2 47
NC 8
EXTXC 9
TXD 10
RESET 11
CS0 12
VSSD 13
VDDD 14
READ 15
ALE 16
WRITE 17
HD0 18
HD1 19
HD2 20
46 NC
45 VSS
44 INT
43 WEN
42 DEN
41 CLKIN
40 PA2
39 PA1
38 PA0
37 TD9
36 TD8
35 TD7
34 TD6
21 HD3
22 HD4
23 HD5
24 HD6
25 HD7
26 RXD
27 DGND
28 TD0
29 TD1
30 TD2
31 TD3
32 TD4
33 TD5


XR-2901CQ
FLAT PACK
1 CLK OUT
2 X1
3 CLK IN
4 B10
5 NC
6 GND
7 D8
8 D9
9 D10
10 D11
11 D12
12 NC
13 D13
14 D14
15 D15
16 D7
17 D6
18 D5
19 D4
20 D3
21 D2
22 D1
23 NC
24 D0
25 A11
26 A10
27 A9
28 VPD
29 WEB
30 DENB
31 MENB
32 A8
33 A7
34 A6
35 A5
36 A4
37 A3
38 PA2
39 GND
40 PA1
41 PA0
42 MCPSEI
43 RSB
44 INTB


XR-2902CQ
FLAT PACK
1 NC
2 EXTXC
3 TXC
4 RESET
5 CS0
6 VSSD
7 VDDD
8 RD
9 ALE
10 WR
11 HD0
12 HD1
13 HD2
14 HD3
15 HD4
16 HD5
17 HD6
18 HD7
19 RXD
20 DGND
21 TD0
22 TD1
23 TD2
24 TD3
25 TD4
26 TD5
27 TD6
28 TD7
29 TD8
30 TD9
31 PA0
32 PA1
33 PA2
34 CLKIN
35 DEN
36 WEN
37 INT
38 VSS
39 NC
40 C2
41 C1
42 TXOUT
43 AGND
44 NC
45 RXCIN
46 SPKO
47 VDD
48 NC
49 TXCLK
50 NC
51 RXCLK
52 IRQ



NOTES



XR-2942 Fax/Data Microcontroller

GENERAL DESCRIPTION

The XR-2942 is a dedicated microcontroller that provides command control for the XR-2900 Fax/Data modem chip set. The XR-2942 provides control for CCITT recommended V.42 error detection, including LAPM and MNP 2-4 protocols, with MNP class 5 data compression included for greater compatibility. Also supported is the CLASS 2 (EIA PN2388) standard 'AT+F' extended command set.

The system architecture of the XR-2942 allows the actual command sets for the 'AT', 'AT+F', MNP, and LAPM to reside external to the XR-2942, allowing ease of customization. Exar provides these command sets to use as is, or the designer can modify to the requirements of the design.

The XR-2942 operates from a single +5 volt power supply, offering low power consumption through CMOS technology.

FEATURES*

Group 3 Send/Receive Fax
Compatibility with Available Applications Software
Error Free Data Transfer:
DATA Mode
- LAPM
- MNP 2-4

Increased Data Throughput by MNP 5 Data Compression
- 4800 BPS Throughput

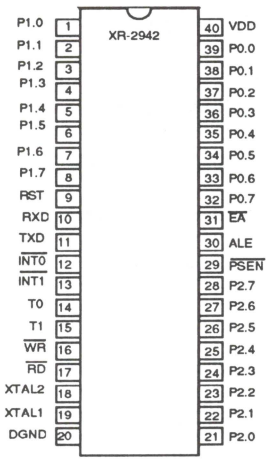
'AT' Command Control
EIA 2388 (CL2) Standard Commands ('AT + F')
- Easily Modified, Exar Supplied Commands
- 'AT'/'AT+F'/MNP/V.42

Possible Chip Upgrade to V.42bis (XR-2943)
*(Apply when used with XR-2900 Fax/Data modem chip set)

APPLICATIONS

Error Free Fax/Data Modem Applications
Stand-Alone Fax/Data Modems
Smart Modems
Laptop Modems (Send and Receive Fax or Data)
Networked Fax Machines

PIN ASSIGNMENT



(For other pin assignments, refer to the end of this datasheet)

3

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2942CP	40 Pin Plastic Dip	0°C to 70°C
XR-2942CJ	44 Pin PLCC	0°C to 70°C
XR-2942CQ	44 Pin QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7V
Input Voltage	-0.7V to (VDD +0.3V)
DC Input Current (any input)	±10mA
Power Dissipation **(Package Limitation)**	1W
Derate above 25°C	11 mW/°C
Storage Temperature Range	-65°C to +150°C

SYSTEM DESCRIPTION

The XR-2942, when coupled to the XR-2900 Fax/Data modem chip set, allows the implementation of a Group 3 fax/2400 BPS V.22bis modem. With MNP/V.42 operation included for data mode, error-free operation is provided.

The XR-2942 is just one in the family of controller options for the XR-2900 Fax/Data modem chip set, including:

FUNCTION	CONTROLLER
'AT' and 'AT+F'	8031
'AT'/'AT+F'/V.42/MNP 5	XR-2942
'AT'/'AT+F'/V.42/V.42bis/MNP 5	XR-2943

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $F_{CLK} = 11.0592MHz \pm 0.05\%$, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}	Power Supply Voltage	4.5	5	5.5	V	
I_{DD}	Power Supply Current		18	22	mA	
V_{IH}	Input High Voltage	1.8			V	(Except XTAL1 and RST)
V_{IH}	Input High Voltage	3.5			V	XTAL 1 and RST
V_{OH}	Output High Voltage	2.4			V	Ports 1,2,3 $I_{OH} = -60\mu A$
V_{OH}	Output High Voltage	2.4			V	Port 0 (External Bus Mode) ALE, PSEN $I_{OH} = -400\ \mu A$
V_{OL}	Output Low Voltage			0.45	V	Ports 1,2,3, $I_{OL} = 1.6$ mA
V_{OL}	Output Low Voltage			0.45	V	Port 0, ALE, PSEN $I_{OL} = 3.2$ mA
I_{IH}	Input High Current (Leakage)			±10	µA	$0.45V \leq V_I \leq V_{DD}$
I_{IL}	Input Low Current			-50	µA	$V_I = 0.45V$

SYSTEM OPERATION

A typical application utilizing the XR-2942 to support the XR-2900 Fax/Data chip set, is shown in Figure 1. The XR-2900 provides the complete modem data pump function for:

CCITT	V.29	9600, 7200 BPS and 4800BPS
	V.27ter	4800 and 2400 BPS
	V.22bis	2400 BPS
	V.22	1200 BPS
	*V.23(mode 2)	1200/75 BPS
	V.21(Ch 2)	300 BPS
Bell	212A	1200 BPS
	103	300 BPS

* Supported by the XR-2321

Command control is supported by the XR-2942 for:

MNP 2-4	Microcom Error Correction
MNP 5	Microcom Data Compression
LAPM	CCITT Recommended V.42 Error Correction
'AT'	Industry Standard 'AT'
'AT+F'	EIA2388 (CL2) Fax Commands

Although the XR-2942 does provide complete command control, the actual commands for the various modes reside in an external EPROM - 27256, 32k Byte. With this architecture and an Exar supplied command set, maximum flexibility is offered. The command set can be used as is, or customer tailored to a particular design.

The unique architecture utilized by the XR-2900 and command controller allow the **same** hardware (Printed Circuit Board (PCB)) to support several different types of Fax/Data modems. By changing available pin-to-pin compatible microcontrollers, the Fax/Data modem types listed in Table 1 are all possible with the same printed circuit board. As mode types are changed by the µC, EPROM supported command sets and SRAM size change and/or elimination are also required. In each case Exar provides complete production worthy command sets which may be used as is, or easily modified to meet specific application requirements. To aid in software modifications, Tables 2, 3 and 4 list the XR-2942 memory mapping, indicating customer usable regions.

External memory modifications requiring µC (XR-2942) support will need entry/re-entry point information. This point is important as the XR-2942 contains program memory with Exar proprietary V.42/MNP5 / Auto Fax / Data Select functions not accessible externally (fusible link protected) or available to Exar customers. The Auto Fax/Data select is in external EPROM, however source code is not provided for this routine.

2400 BPS Data Mode	Microcontroller Part Number	External Memory Requirements (Bytes)	
		EPROM	SRAM
'AT'	8031 (Generic ROMLESS µP)	32K	8k / 32k
'AT' / MNP5/V.42	XR-2942	32K	8K / 32K
'AT'/MNP5/V.42/ V.42bis	XR-2943	32K	32K

Table 1. 2900 BPS Modem Options / µC, EPROM, RAM Requirements

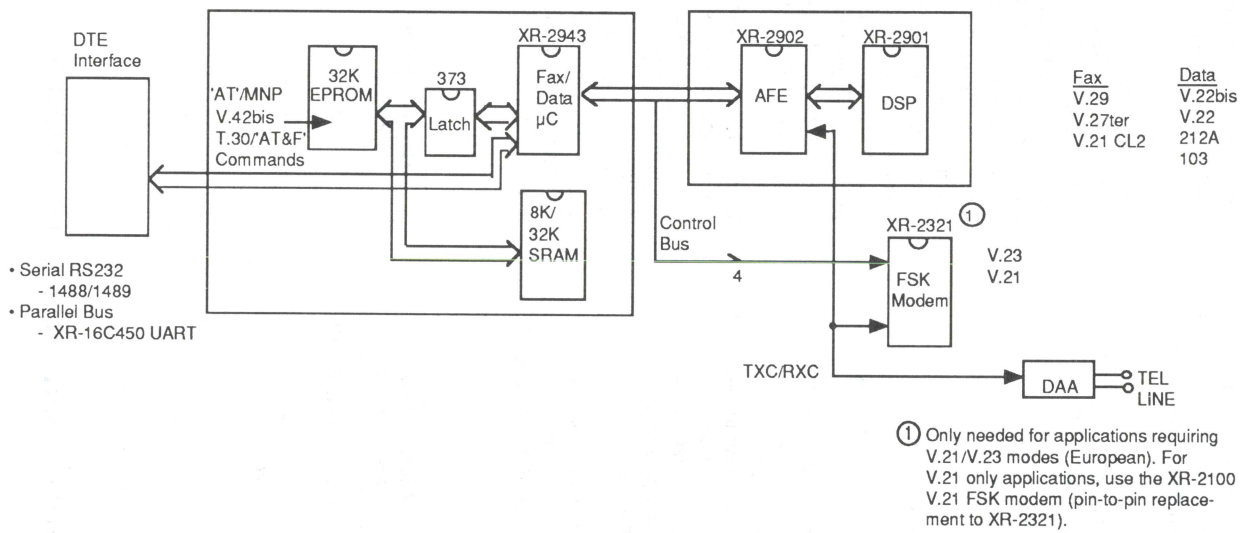


Figure 1. Fax/Data Modem with V.42bis/MNP5 (Data Mode) Block Diagram

ENTRY POINTS AND MEMORY MAPPING

Status / Mode Setting Memory Locations

Status	Location	Description
SPD_FLG	20 H.7	Speed Conversion Enable Flag.
BK_PRE	51 H	Break Prescaler Timer
BK_TMR	52 H	Break Timer (Only in Normal Mode)
MRCVP2	803BH	Disconnect to Check Auto-Reliable Fallback Mode.
PASS_ B	9D14H	Escape Code Checking Byte in Speed Conversion Mode.
SPEED	9D15H	Speed Indicator For All Modes. 0-19200 BPS 1 - 9600 BPS 2 - 4800 BPS 3- 2400 BPS 4 - 1200 BPS 5 - 300 BPS
Z_BUF	9D16H	Auto Reliable Fallback Character.
BACK_RAM	9D1AH	Starting Address for Command Buffer Back-up.
OPT_P	9D50H	Output Port Selection Option (F0FF H to 40FFH). This Parameter is Initialized Immediately After Power On and constantly monitored by MNP Module.
MNP_S	9E22H	Reliable Link Indicator
RETRAN	24H.0	RETRANSMISSION

Function Call Locations - V.42bis/V.42/ MNP 5 Program Entry Points

Function	Location	Description
SCTINT_1	0006H	Interrupt 0 Jump-In Point.
SCRINT_1	0016H	Interrupt 1 Jump-In Point.
SPINT_1	0026H	Serial Port Interrupt Jump-In Point.
MSG_CP	0030H	Exar Copyright Message.
P_ECRAM_1		0060H After Escape MNP Re-Entry Point.
MSG_CPY	0063H	Exar Copyright Calling Subroutine.
MNP_IN	0066H	MNP Program Immediate Re-Entry Point for modifying MNP Program.
SPD_INM	0069H	Speed Conversion Program Jump-In Point.
INI_SPDM	006CH	Speed Conversion Initialization Routine.
V21_IN_1	006FH	300 BPS Speed Conversion Timer Set-Up.
EC_MAIN	0080H	Calling Main MNP Program. This is the only location which will initiate the MNP program.

XR-2942Re-Entry Points

Function	Location	Description
PWR_ONS	C000H	Power On
OUT_SCT	C003H	Interrupt 0
OUT_T0	C006H	Timer 0
OUT_SCR	C009H	Interrupt 1
OUT_T1	C00CH	Timer 1
OUT_SP	C00FH	Serial Port Interrupt
OUT_T2	C012H	Timer 2
MNP_OUT	C015H	MNP Program Intermediate Point
CHK070S	C01BH	MNP 'ESC' Jump Out Point
DISCONNECT S		C01EH MNP Disconnect
ON_LOOPS	C021H	Auto-Reliable Fallback Point.
SPD_OUTS	C024H	Speed Conversion Jump Out Point.
V21_INS	C027H	Call Speed Conversion ASM for 300 BPS.
SPD_TXD	C02AH	Put TXDATA to Modem Chip.
SPD_RXD	C02DH	Get RXDATA From Modem Chip.
I_TXSYNTT	C030H	GET TX CRC-CCITT CALCULATION ROUTINE
I_RXSYNTT	C033H	GET RX CRC-16 CALCULATION ROUTINE
I_TXASYN16		C036H GET TX CRC-16 CALCULATION ROUTINE
I_RXASYN16		C039H GET RX CRC-16 CALCULATION ROUTINE
I_SNDREL	C03CH	GET SENDING RESULT CODE SUBROUTINE
I_MNPINIT	C03FH	MNP PARAMETER INITIALIZATION ROUTINE
I_V42INIT	C042H	V42 PARAMETER INITIALIZATION ROUTINE
I_SETURMNP		C045H UART SETTING ROUTINE

RAM Locations

The stack in the 'AT' program starts from 0C0H on page 1 and occupies 64 bytes of space. Internal RAM on page 0 has 23 bytes and page 1, 64 bytes of free indicator space.

The external RAM data memory is as follows:

1) Error Control	8000H-8FFFH
2) Data Compression Buffer	9000H-93FFH
3) FAX/Remote Access	9400H-95FFH
4) Available for use	9600H-97FFH
5) V.42	9800H-98FFH
6) Break Buffer	9A00H-9AFFH
7) DTE TX Buffer	9B00H-9BFFH
8) DTE RX Buffer	9C00H-9CFFH
9) Misc. Registers	9D00H-9DFFH
10) MNP RAM Backup Buffer	9E00H-9EFFH
11) 'AT' RAM Backup Buffer	9F00H-9FFFH
12) BTLZ Compression Dictionary	C000H-FFFFH

Note: Before jumping into the MNP program the control code will backup the entire 256 bytes of AT RAM into external RAM. In addition, before jumping out of the MNP program it will backup the entire 256 bytes of MNP RAM into external RAM.

The Miscellaneous register function list is provided below. The option code control allows the firmware engineer to change the factory defaults in source code, then reassemble.

OPTION	LOCATION	PARAMETER	COMMAND	DESCRIPTION
Opt_0	9D09H	0	\NO	Non-MNP
		1	\N2	Reliable Mode
		2*	\N3	Auto _reliable Mode
Opt_1	9D0AH	0	\Q1	Normal XON/XOFF
		1		Not Used
		5*	\Q2	Unidirectional RTS/CTS
		3	\X1	Xon/Xoff Pass Through
		4	\Q4	Xon/Xoff Send Only
		2	\Q3	Bidirectional RTS/CTS
		6	\Q0	Disable Flow Control
Opt_2	9D0BH (BIT0)	0		Disable Speed Conversion
		1		Enable Speed Conversion
Opt_2	9D0BH (BIT1)	0	\J0	Disable Serial port rate adjust
		1*	\J1	Enable Serial port rate adjust
Opt_2	9D0BH (BIT2)	0*	\G0	Disable modem port flow control
		1	\G1	Enable modem port flow control to XON/XOFF (for normal mode only)
Opt_2	9D0BH (BIT3)	0*	-P0	Parity bit for checking XON/XOFF
		1	-P1	Ignore parity bit checking for XON/XOFF
Opt_2	9D0BH (BIT4)	0*		Not Used
		1		
Opt_2	9D0BH (BIT5)	0*		Not Used
		1		
Opt_2	9D0BH (BIT6)	0*	\M0	V.42 Mode
		1	\M1	MNP Mode
Opt_2	9D0BH (BIT7)	0	%C0	Disable Data Compression
		1*	%C1	Enable Data Compression

OPTION	LOCATION	PARAMETER	COMMAND	DESCRIPTION
Opt_3	9D0CH	0	\A0	Block size to transmit, 64bytes
		1	\A1	128 bytes
		2	\A2	192 bytes
		3*	\A3	256 bytes
Opt_4	9D0DH	0-9	\Bn	Xmit break during normal mode
		3*		at data mode, n=100ms
Opt_5	9D0EH	1	\K1	Expedited, Destructive
		2	\K3	Expedited, Non-destructive
		3*	\K5	Non-expedited, Non-destructive
Opt_6	9D12	(81H)	\0	Originate Reliable Link
Opt_6	9D12H	(82H)	\U	Accept Reliable
Opt_6	9D12H	(80H)	\Y	Switch to Reliable Link
Cpt_7	9D13	1		For 300 BPS connect indicator
	(BIT0)	0		For other speed
Opt_8	9D0FH	0	\V0	Standard Result code form
	(BIT1,0)	1*	\V1	Result code for MNP
		2	\V2	
		3	\V3	
Opt_8	9D0FH	0*	\C0	No set for Auto-reliable buffer
	(BIT3,2)	1	\C1	Set Auto-reliable buffer
		2	\C2	Set fall back character
Opt_8	9D0FH	0	\L0	MNP Stream mode
	(BIT4)	1*	\L1	MNP Block mode
Opt_8	9D0FH	0	\Q0-\Q4	
	(BIT5)	1*	\Q5,\Q6	For \Q5, \Q6 turnoff CTS
Opt_8	9D0FH	0*		
	(BIT6)	1		V.42 only negotiation
Opt_8	9D0FH	0*		
	(BIT7)	1		Eliminate ODP for V.42
Opt_9	9D10H	0*	%An	Auto-reliable fallback
		N		character
Opt_A	9D11H	0*	\Tn	Inactivity Timer
		N		
Opt_B	9D51H	0*	%Dn	**Default**
	(BIT4)	1		Clear RX Buffer after disconnect

Interrupt Vectors

The XR-2942 brings out all interrupt vectors to the external program. This allows easy customer modification of service routines to suit a particular application. The interrupt vectors of the XR-2942 are as follows:

```
        ORG     0
        LJMP    PWR_ONS; Jump to Power On
                         Set Up Routine
        ORG     3H
EXT_INTO:               ; Interrupt 0 for SCT
        LJMP    OUT_SCT
SCTINT1:
        LJMP    SCTINT
        ORG     0BH
T_INTO:                 ;Timer 0 Interrupt
        LJMP    OUT_T0
        ORG     13H
EXT_INT1:               ;Interrupt 1 for SCR
        LJMP    OUT_SCR
SCRINT_1:
        LJMP    SCRINT
        ORG     1BH
T_INT1:                 ;Timer 1 Interrupt
        LJMP    OUT_T1
        ORG     23H
INT_SER:                ;Serial Port Interrupt
        LJMP    OUT_SP
SPINT_1:
        LJMP    SPINT
        ORG     2BH
T_INT2:                 ;Timer 2 Interrupt
        LJMP    OUT_T2
```

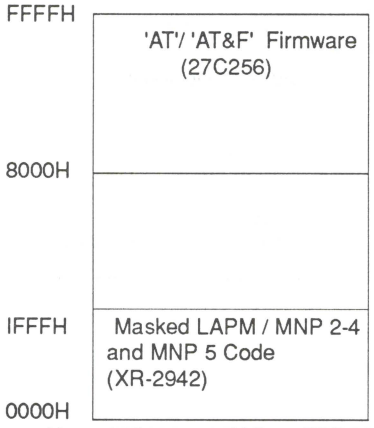
XR-2942 PROGRAM/DATA MEMORY MAPS

Tables 2, 3 and 4 show the ROM and RAM memory maps for XR-2942. It should be noted that without the use of separate CS(chip select) of the XR-2902 and the XR-2321, there would be an overlap of address locations.

As it is indicated in Table 2, 32K bytes of EPROM is assigned to 'AT' command firmware. This section of the ROM is located between 8000H and FFFFH.

LAPM, MNP2-4 and MNP5 code is masked in the microcontroller (XR-2942), and resides in the 8K bytes of memory, between address locations 0000H and 1FFFH.

Table 3 shows the RAM map, in which the space between 0000H and 002CH address locations is used for modem chip address. Table 4 shows the modem chip (XR-2902) address assignment. Included is addressing for the XR-2321 and XR-2100. These chips are optional to the system design, but may be added where V.21 or V.23/V.21 standards are required. The XR-2321 provides both V.23 and V.21 FSK data standards, while the XR-2100 provides only V.21. See XR-2321 or XR-2100 datasheets for details.



Note: 27C256 = 32K Byte EPROM

Table 2. XR-2942 ROM Map

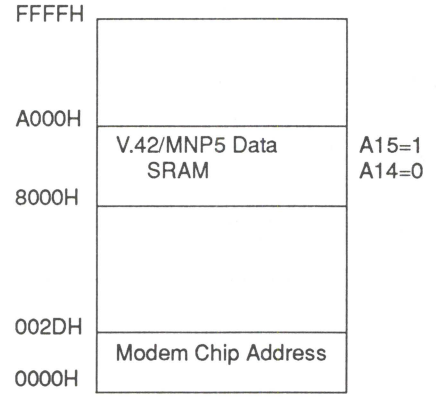


Table 3. XR-2942 RAM Map

MODEM CHIP	RAM ADDRESS	$\overline{CS}$
XR-2902	0000H - 001FH	A15=0 and A5=0
XR-2321	0028H - 002CH	A5=1 and A15=0
XR-2100	0028H - 0029H	A5=1 and A15 =0

Table 4. Modem Chip Address

Also RAM space between 8000H and 9FFFH is assigned for V.42 and MNP5 data or fax data. RAM locations between A000H and FFFFH, as well as RAM locations between 002FH and 7FFFH are available for I/O ports such as LED, EIA, etc.

V.42 / MNP OPERATION

The XR-2942 when coupled with the XR-2900 Fax/Data modem chip set allows the implementation of a group 3 fax and an **error-free, increased throughput** 2400 BPS data modem. To gain an understanding of V.42/MNP 5 modes for data operation, the following basic information has been included. A basic understanding of error correction techniques, flow control, speed buffering, and data compression will allow the designer to better understand a V.42/MNP5 modems capabilities and how to best utilize them. One excellent reference is "Data Compression", by Gilbert Held. The publisher is Wiley.

V.42 is a **CCITT** recommended error correction protocol which allows asynchronous DTE's (Data Terminal Equipment) to communicate error-free with other such equipped modems.

The actual error detection protocol used in V.42 is an **HDLC** (High-level Data Link Control) based protocol called LAPM, for **Link Access Procedure for Modems.** For additional detailed information beyond the following basic description, refer to the CCITT Recommendations, Series V, 'Data Communication Over the Telephone Network'. The latest version is known as the **'Blue Book'** (Blue Covers) or Series, dated 1988 (Melbourne), a recent update from the **'Red Book'.**

V.42 Basic Operation/Features

- **HDLC**-based error correction protocol-LAPM
- Asynchronous (Async or 'start/stop') DTE Communication - error free
- Actual line transmission is synchronous (sync)- no start or stop bits (stripped from data), however initial handshake, subsequent to modem handshake is asynchronous
- Error Detection
  - Data sent in 'frames' or blocks with a nominal size (default) of 128 Octets (Octet - 8 bit) data frames
  - Start/Stop bit elimination from data creates an actual data throughput improvement, roughly 120% of nominal. 2400 BPS becomes about 2900 BPS
  - Encoded information added to data frame for receiver to 'decode' and determine if the block was error free. 16-bit cyclic redundancy (CRC) methods are used for data encoded information to (1) indicate correct data and (2) recognize imperfect data frame
  - Retransmission (automatic) of determined imperfect frames to ensure perfect data is received

V.42 operation is found to be virtually identical (specifically to variable parameters) to that of MNP reliable or normal modes of operation. For this reason the MNP command set is also used for V.42 variables control.

MNP® OPERATION

MNP, or Microcom Networking Protocol was developed by Microcom, Inc., a modem manufacturer. Since conception, it has been in a constant state of update/improvement. For this reason 'classes' of operation emerged to signify each major update or improvement.

Relative to the V.22bis or 2400 BPS modems, up to class or level 5 has become the 'standard'. MNP is not used with the FAX modes of operation, as mentioned before HDLC framing techniques are used.

MNP CLASSES

(Throughput data is based on **2400 BPS** line speed).

Class 1 A half duplex protocol and not included in many new designs. Throughput was about 70% or 1690 BPS. The XR-2942 does not support this class.

Class 2 Asynchronous operation with byte orient ed data formatting. Throughput is rough ly 84% of nominal or about 2000 BPS.

Class 3 Conversion to synchronous, bit oriented data handling is transmitted in blocks consisting of 1 to 64 characters. Throughput is about 108% or 2600 BPS.

Class 4 Basic characters are the same as Class 3, but block size is dynamic, up to 256 Bytes, (flexible size is based on data transmission quality). Throughput is 120% or 2900 BPS.

Class 5 Includes Class 3 and 4 with data com pression techniques added. The com pression effectiveness is dependent on the type of data, but typical throughput enhancements of up to 200% or 4800BPS.

ERROR CORRECTION

Modem users have come to expect sophisticated circuitry like automatic adaptive equalization for varying phone characteristics and retrain modes for ensuring continued optimal performance. These techniques dramatically improve performance characteristics which is quantified by BER vs S/N measurements, the probability of errors when the modem signal is in the presence of noise.

The previously mentioned techniques are aimed at improving the modem data pump through analog (or digitally synthesized) circuitry. Techniques are becoming popular for not only improving, but virtually eliminating data errors through protocols implemented in the modems command microcontroller (μC). Prior to these 'hardware' based schemes, error correction provided in the applications software was available, such as X-MODEM or Kermit for asynchronous file transfer. In mainframe environments, SDLC or HDLC schemes were used.

Software based error correction schemes do however have their disadvantages. One important one being reduced data throughput. The throughput performance varies, but all schemes reduce data transfer below its nominal rate. Typical values of 31% are common, equating to only about 600 BPS for a 2400 BPS connection.

The hardware based error correction protocols supported by the XR-2942 for data mode are those as specified by the **CCITT LAPM,** and **MNP.** These schemes convert asynchronous data to be transmitted to a synchronous format (start and stop bits are stripped) for a packet-oriented protocol. Throughput values again vary, however typical values of 108% for the lower MNP Class 3 and 120% for MNP Class 4 or LAPM. These equate to roughly 2600 - 2900 BPS for 2400 BPS modems.

Actual error correction is based on adding information to the block-oriented data, through a 16-bit CRC (Cyclic Redundancy Check) calculation. The receiving side calculates CRC values for each block and if found to be incorrect, a retransmission of that block will be requested.

Typical frame sizes for LAPM are 128 Octets (8-bit start/stop bit stripped characters).

DATA COMPRESSION

The CCITT recommendation for V.42 only specifies error correction modes, as provided by LAPM and MNP 2-4. Modem controller protocols have advanced to the point where in addition to providing error-free data transfer, they can also offer other significant enhancements. One very significant enhancement is the addition of data compression operation. Simply put, this technique substantially enhances the data throughput of the modem.

This data compression scheme, MNP 5, although not specifically part of the V.42 recommendation, has been included in the XR-2942 to serve only as a further enhancement to the XR-2942 based modems.

MNP Class 5 is the protocol for **data compression.** It is by far the most accepted protocol for this function. CCITT recommendations are adding a data compression mode to V.42, called **V.42bis.** The upcoming **XR-2943** will support the future CCITT recommended **BTLZ** data compression.

MNP 5 data compression offers the XR-2900 Fax/Data modem chip set roughly 100% increase in throughput (in data mode), or 200% of nominal. This translates to a maximum modem throughput of 2400 BPS x 2 = 4800 BPS for a text file.

MNP 5 techniques utilize a scheme which abbreviates redundant data characters for a much higher transmission efficiency or throughput increase. Because of its dependency on redundant characters, the amount of improvement will vary. Typical improvement values are in the range of 75 to 125%, or 4200 to 5400 BPS for a 2400 BPS modem link.

FLOW CONTROL

As previously outlined, a method for regulating the flow of data to be transmitted is necessary when DTE data rates exceed line rates. Figure 2 illustrates a basic modem connection and helps illustrate where flow controls fit in.
Flow control can be under **hardware** or **software** control.

HARDWARE FLOW CONTROL

Hardware Flow Control allows the modem to lower or raise its CTS (Clear to Send) line to the DTE. This provides an ON/OFF control of data flow from DTE to modem. If the modem data buffer becomes full it lowers the CTS line to stop transmit data flow to allow the modem to "catch-up".

SOFTWARE FLOW CONTROL

An alternative to hardware flow control is control by software, known as **Xon/Xoff**. This is accomplished by special characters inserted into the data stream to start and stop data flow. **Control Q (^Q)** is used to start or restart data flow and **Control S (^S)** to stop data flow.

Three different variations of Xon/Xoff control modes are:

- Send Only
- Normal
- Passthrough

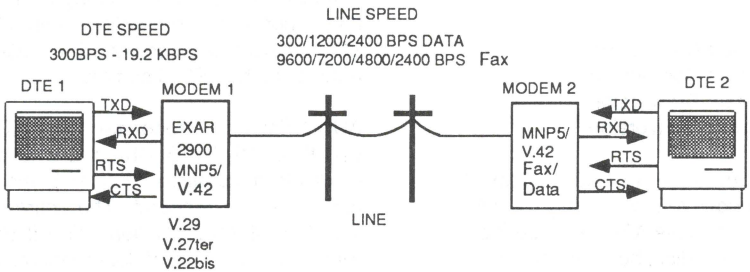


Figure 2. Basic Modem Connection

XR-2942 V.42/MNP FUNCTIONS AND COMMANDS

The XR-2942 with external EPROM provides control for the following major functions:

FUNCTION	DESCRIPTION
• 'AT' Command Control	Provides 'AT' Command Set Control
• 'AT+F' Commands	Provides control of the FAX functions
• MNP Level 2-4	Provides error correction for 100% perfect data transfer.
• MNP Level 5	Allows roughly a 100% increase (4800 BPS for V.22bis mode) in data throughput, through data compression techniques.
• V.42 (LAPM)	100% perfect data transfer
• Speed Conversion	Maintain up to 19,200 BPS DTE (terminal) speed for 300 BPS to 9600 BPS line speeds, both for LAPM/MNP and non-error correcting connections.

Application Software Interface

The firmware of the XR-2942 (combined masked and supporting code) supports the working document of the Telecommunication Industry Association for Fax/Data modems, assigned the EIA part number 2388. The level of support is service Class 2, which places most of the CCITT T.30 command functions in the modem (XR-2901, XR-2902 and XR-2942). Figure 3 indicates the approximate division between modem (DCE) and PC (DTE).

The command section of the XR-2942 data sheet defines the commands, responses and functions of the firmware supplied with the XR-2942. It is possible to send those commands to the XR-2900 system by hand, visually monitor the responses and send or receive data of the proper format. However, to use the XR-2900 modem system effectively, it is best to use an application software package that automatically monitors the response strings and acts accordingly.

In general the application software would be required to perform:

- ASCII to Bitmap Conversion
- PCX to Bitmap Conversion
- TIFF to Bitmap Conversion
- PICT to Bitmap Conversion

In an imbedded system, such as a text editor, the above list could be reduced to include only the ASCII to Bitmap conversion. Because ASCII is encoded, information as to the font, italics, bold, underline, and other word processor options is lost. It is expected that either the communication packages will start recognizing some Word processor options, or an integration of word processors and communication software such as seen today. The second step is to perform:

- BITMAP to 1 Dimensional Coding or
- BITMAP to 2 Dimensional Coding

as per the CCITT T.4 specification.

Figure 4 shows the process of taking text and encoding it 1 dimensionally using the CCITT T.4 Huffman codes. The entire line must total 1728 picture elements or pels. The application software will need to convert from files set up for 640 pels per line to one containing 1728 or more.

In the Vertical dimension, either 98 dpi (dots per inch) or 1968 dpi would be selected. This would determine the number of scan lines needed per page as well as determine the quality of the reproduced image. Two dimensional Huffman encoding is supported. Both of these modes would need to be enabled by using the VR (vertical resolution) and DF (data format) subparameter of the +FDIS command.

AUTO Fax/Data Negotiate: The XR-2942 supports the EIA PN 2388 Class 2 standard and auto Fax/Data negotiation. Figure 5 shows the flow for this process to proceed. The entire process requires less than 4 seconds permitting it to be compatible with fax machines and data modems available today.

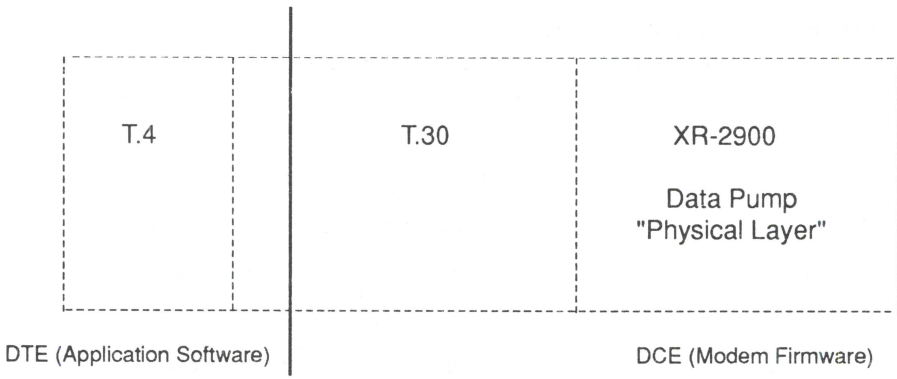


Figure 3. T.4/T.30 Partitioning for DCE/DTE

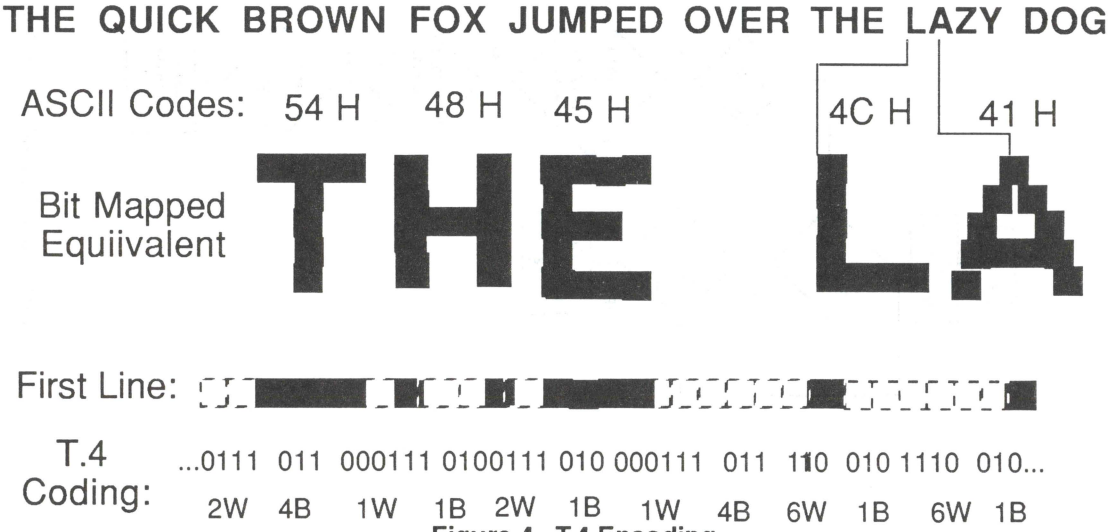


Figure 4. T.4 Encoding

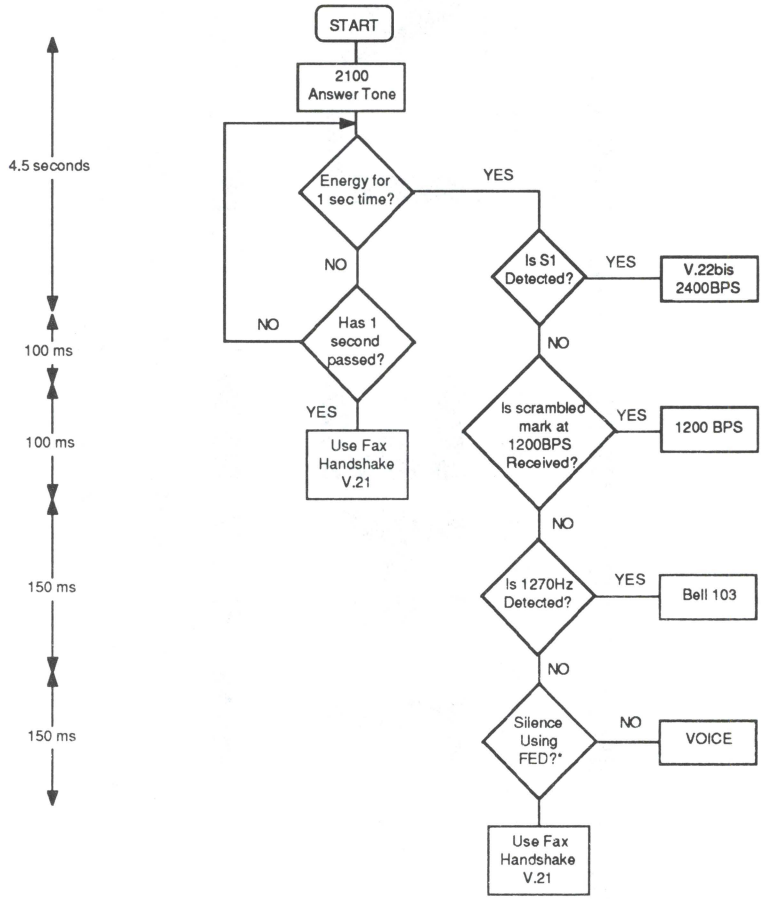


Figure 5. Auto Fax/Data Negotiation For Answer Mode

T.30 Description

The CCITT T.30 specification was intended to standardize the signaling between two fax machines. This permits any group 3 fax card or machine to communicate with another also meeting the standard.

The T.30 specification defines the fax transmission and reception process into five steps or phases:

Phase A: Call Establishment
Phase B: Negotiation of data rate, and capabilities of both machines
Phase C: Message (Page) Transmission
Phase D: Post Message (Page) Transmission; confirm send; possibly more pages
Phase E: Call Release (Hang up)

Figure 6 provides a general flow chart of the process.

Phase A of the CCITT T.30 specification establishes that a fax modem is answering the line and not a data modem. The uniqueness of this handshake allows the ability to add the feature of switching between fax and data modes with the XR-2900 Fax/Data modem chip set. In addition, the optional identification of the called and calling unit takes place using CCITT V.21 modulation and demodulation. The data is framed (synchronous) to ensure reliable communication at this point, even on an extremely poor phone line. By taking this extra step the CCITT has provided a means to negotiate (during Phase B) the data rate to a lower rate, as required. This can be utilized by the application software developer to add a security mode: if the correct response is not provided, the session can be ended at this point.

Phase B is the exchange of information as to capabilities of the two fax modems, again using V.21 channel 2 synchronous transmission and reception. Information such as scanning speed, number of dimensions of Huffman encoding, and grey scale encoding is sent at this time.

Phase B also includes the phasing and training process for the fax modem data pump. The calling (originating) modem transmits a bi-phase signal at the proper baud rate for the transmission (2400 symbols/second for 9600 BPS) to allow the called (answering) modem to adjust for group delay distortion as well as gain loss of the line. If not successful, a failure to train (FTT) is sent from the called modem to the calling modem at 300 BPS using the framing described above. The calling modem tries at the next lower speed. Once this process is successful, the called modem confirms that it is programmed to receive.

The sending of the page or information occurs during **Phase C** at the maximum negotiated data rate (9600 BPS for the XR-2900).

Phase D is the confirmation of the end of message and of receiving the page. This usually indicates that the page has been received properly. At this time the optional multiple pages signal can be sent. If another page is to be sent or received, phase C is repeated.

Phase E disconnects the phone line (on hook).

The XR-2942 supports automatic call establishment, for it is felt that the manual process is not practical in a Fax/Data product where interaction between the host computer (to perform the file conversion and T.4 encoding) and the modem is needed. However this does not preclude a manual to automatic process, using an external dialer and starting the application program to send the fax (off hook immediate and wait for **Phase A** to begin).

The process is similar when receiving a call. However, with the Exar proprietary Fax/Data auto select, the modem will determine during phase A whether a fax machine/card or data modem is calling. Details for this is provided in this datasheet.

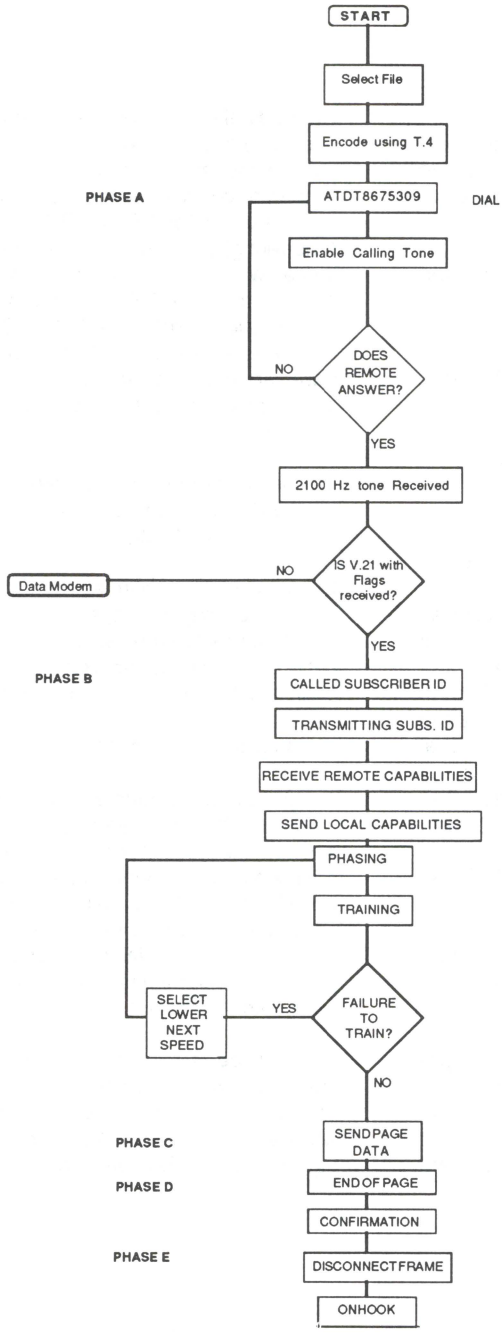


Figure 6. CCITT T.30 Process Sequence (Transmit a Single Page)

PROTOCOL NEGOTIATION

The XR-2942, for data mode, supports error correcting or reliable modes of operation for not only LAPM, but also MNP2-4 type protocols. Also, although data compression operation is not specified by CCITT V.42 specifications, it has been included through MNP 5 for increased compatibility. Because of these multiple protocols supported, the XR-2942 offers two protocol negotiation modes:

1) AT\M0 Default Mode
   This command selects an automatic protocol negotiation mode. **First LAPM** negotiation will be attempted. If not possible, MNP2-4,5 operation will be negotiated. The highest possible class of MNP operation will be negotiated (depending upon setting on %C command). If the remote modem does not support error correction, normal 2400 BPS (or1200/300 BPS) operation will be supported.

2) AT\M1
   This command will **disable LAPM** operation. Here only MNP 2-5 and non-error correcting modes of operation will be supported.

The following is a command set summary for the XR-2942. Provided are:

Data Mode

1) Basic Connection/Dialing Commands
2) Dialing Modifiers
3) Standard Hayes 'AT' Command Set
4) 'S' Register Descriptions/Functions. These registers are used for controlling the value or function of various 'AT' commands.
5) MNP/LAPM Commands. The entire list represents the MNP command set. Most of the MNP commands also apply to LAPM, with the exceptions indicated.

Fax Mode

6) Extended 'AT + F' Commands per EIA PN 2388 (Class 2) operation
7) Fax responses

COMMAND	DESCRIPTION / RANGE - SIZE
A/	Execute previous command, without striking <CR> key
AT	Attention
ATA	Answer Immediate
ATB0	CCITT V.22 mode
ATB1	Bell 212A mode **DEFAULT**
ATB2	V.23 mode
ATD	Dial Command
ATDP	Dial Using pulse dial
ATDT	Dial Using DTMF tone dial **DEFAULT**
The following 8 modifiers will dial using the previously used technique (pulse or tone), or the T or P command can be added after the D (dial) command. 0-9 A B C D * #	
ATDW	Wait for Dial Tone for Period Set by S7 Register
ATD@	Quiet Answer: Wait for 5 Seconds of Silence Before Dialing
ATD!	Hookflash: Commonly Used PBX Systems
ATDR	Reverse Answer Mode
ATDS=n	Dial Stored Number when n= 0-3
ATD/	Wait 0.125 Seconds
ATD;	Return to Command Mode After Dialing
ATD,	Pause for Time Set by S8 Register
ATE0	Command Echo Disabled
ATE1	Command Mode Echo Enabled **DEFAULT**
ATH0	Go On Hook (Open Relay)
ATH1	Go Off Hook (Close Relay)
ATI0	Identification Code
ATI1	Identification Code
ATI2	"OK" Response if Checksum Verifies
ATI3	EXAR EPROM Revision Date
ATL0	Lowest Volume Setting
ATL1	Same as ATL0
ATL2	Medium Volume Setting **DEFAULT**
ATL3	Maximum Volume
ATM0	Speaker Always Off
ATM1	Speaker On Until Carrier Is Detected **DEFAULT**
ATM2	Speaker Always On
ATM3	DTMF Tones are not Heard, but Speaker is on Until Carrier Detected
ATO	Originate Immediate or Return to Data Mode
ATO1	Request a Retrain When in V.22bis Mode
ATQ0	Provide Result Codes **DEFAULT**
ATQ1	Disable Result Code
ATSn?	Provide S Register Value
ATSn=	Set S Register Value
ATV0	Terse (and Verbose) Responses, affected by \Vn

NUMERIC	DESCRIPTION / RANGE - SIZE	
		\V1
0	OK	Command Executed
1	CONNECT	Connection at 0 to 300 BPs
2	RING	Ring Signal Detected
3	NO CARRIER	Carrier Signal not Detected
4	ERROR	Error
5	CONNECT 1200	Connection at 1200 BPS
6	NO DIALTONE	No DialTone Detected
7	BUSY	Busy Signal Detected
8	NO ANSWER	No Silence Detected
10	CONNECT 2400	Connection at 2400 BPS
11	CONNECT 4800	Connection at 4800 BPS
12	CONNECT 9600	Connection at 9600 BPS
14	CONNECT 19200	Connection at 19200 BPS
		\V1
22	CONNECT 1200/REL 4	MNP Class 4 Link
22	CONNECT 1200/REL 5	MNP Class 5 Link
23	CONNECT 2400/REL 4	MNP Class 4 Link
23	CONNECT 2400/REL 5	MNP Class 5 Link
22	CONNECT 1200/V.42	V.42 Link
23	CONNECT 2400/V.42	V.42 Link

COMMAND	DESCRIPTION / RANGE - SIZE
ATV1	Verbose Response **DEFAULT**. See ATV0 for Responses
ATX0	Enable Result Codes 0-4
ATX1	Enable Result Codes 0-5, 10
ATX2	Enable Result Codes 0-6, 10
ATX3	Enables Result Codes 0-5 and 7 and 10
ATX4	Enables Result Codes 0-10 **DEFAULT**
ATY0	Disable Long Space Disconnect **DEFAULT**
ATY1	Enable Long Space Disconnect
ATZ0	Software Reset, Restore S Register from profile location 0 in NVRAM
ATZ1	Restore S Registers From Profile Location 1 in NVRAM
AT&C0	EIA Carrier Line Always Forced on **DEFAULT**
AT&C1	EIA Carrier Line Follows Data Carrier
AT&D0	DTR Always on **DEFAULT**
AT&D1	Modem Goes to Command Mode When DTR Goes Off
AT&D2	Modem Goes on HOOK and Returns to Command Mode When DTR Goes Off
AT&D3	Modem Initializes When DTR Goes Off
AT&F	Fetch S Registers From EPROM for Factory Default
AT&G0	No Guard Tone **DEFAULT**
AT&G1	550 Hz Guard Tone Enabled
AT&G2	1800 Hz Guard Tone Enabled
AT&J0	RJ-11 Select **DEFAULT**
AT&K0	Flow Control Disabled
AT&K1	No Function
AT&K2	No Function
AT&K3	RTS/CTS Flow Control **Default**
AT&K4	Xon/Xoff Flow Control
AT&K5	Xon/Xoff Pass Through
AT&L0	Switched Line Select **DEFAULT**
AT&L1	Leased Line Select
AT&M0	Asynchronous Mode **DEFAULT**
AT&M1	Synchronous Mode With Asynchronous Dial
AT&M2	Synchronous Mode and Dial the Stored Number Immediately
AT&M3	Synchronous Mode With DTR Controlling Data/Talk
AT&P0	US Make/Break Ratio For Pulse Dialing **DEFAULT**
AT&P1	UK Make/Break Ratio For Pulse Dialing
AT&Q0	Direct mode (same as Hayes)
AT&Q1	Same as &M1
AT&Q2	Same as &M2
AT&Q3	Same as &M3
AT&Q5	Error Control Mode
AT&Q6	Normal Mode
AT&R0	Clear To Send (CTS) Follows RTS **DEFAULT**
AT&R1	CTS Always On
AT&S0	Data Set Ready (DSR) Always on **DEFAULT**
AT&S1	DSR Normal
AT&T0	Terminate Test in Progress **DEFAULT**
AT&T1	Initiate Local Analog Loopback For Time Set by Register S18
AT&T2	Not Defined
AT&T3	Initiate Digital Loopback for Time Set by Register

COMMAND	DESCRIPTION / RANGE - SIZE
AT&T4	(Not Supported)
AT&T5	Disable Remote Digital Loopback (RDLB) Response
AT&T6	Initiate RDLB
AT&T7	Initiate RDLB with Self Test
AT&T8	Initiate ALB with Self Test (for Direct / Normal Mode only)
AT&W0	Write User Profile 0 into NVRAM
AT&W1	Write User Profile 1 into NVRAM
AT&X0	Modem Provides Transmit Clock
AT&X1	DTE Supplies Transmit Clock (Not Supported)
AT&X2	Slave Clock Mode (Not Supported)
AT&Y0	Power Up Recall User Profile 0
AT&Y1	Power Up Recall User Profile 1
AT&V	List Configuration both Active and Stored
AT&Z m=An	Store Telephone Number into NVRAM (XL93C46) where: *m* is the number location (0-3) *A* is *P* or *T* (pulse or Tone) *n* is the telephone number

COMMAND	LAPM Yes/No	DESCRIPTION/RANGE - SIZE	FUNCTION
AT \ N0	Y	Normal	
AT \ N1	Y	Direct	
AT \ N2	Y	MNP 2-5/Reliable	
AT \ N3	N	MNP 2-5/Auto Reliable	
AT \ N4	Y	V.42 Mode	
AT \ N5	Y	V.42 Mode Auto Reliable	
AT \ N6	Y	V.42 / MNP 2-5 Reliable	
AT \ N7*	Y	V.42 / MNP 2-5 Auto Reliable	
AT \ A0	N	64 Characters	Transmit Block Size
AT \ A1	N	128 Characters	
AT \ A2	N	192 Characters	
AT \ A3*	N	256 Characters	
AT%An	Y	n = 0-127 ASCII	Auto-Reliable Fallback Character
AT \ L0*	N	Stream Link	Block MNP Link
AT \ L1	N	Block Link \L1 = \L0	(Stream Mode)
AT \ O	N	Initiate Reliable Link After Escape Command Independent of Modem Initial mode (ANS or ORG)	Originate Reliable Link
AT \ U	N	Accept Reliable Link after Escape Command request from Initiator of Link	Accept Reliable Link
AT \ Y	N	Establish Reliable Link after Connecting in Normal Mode	Switch to Reliable Mode
AT \ Z	N	Switch to Normal Mode After Establishing a Reliable Link	Switch to Normal Mode
AT % C0	Y	Compression Disabled	Compression On/Off Control
AT % C1*	Y	Compression Enabled	
AT \ V0	Y	Standard Non-MNP Result Codes	Result Code Form
AT \ V1*	Y	Modified MNP Result Codes (As Listed Below)	
AT \ Bn	Y	N = 0 - 9 (100ms Increments) Used in Normal Mode Default = 3, Error Control Mode Always 300ms	Transmit Break for Normal Data Mode
AT \ C0*	Y	Does not buffer Data Default	Set Auto-Reliable Buffer Break Control
AT \ C1	Y	Buffers All Data on Answering Modem until 200 Characters (Non-Sync) are Returned	
AT \ C2	Y	Does Not Buffer Data on Answering Modem, according to % An to fall back	
AT \ K1	Y	"Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed	Break Control for Reliable Data Mode
AT \ K3	Y	"Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained	

COMMAND	LAPM Yes/No	DESCRIPTION / RANGE - SIZE	FUNCTION
AT \ K5*	Y	"In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break	
AT \ K0,2,4	-	Not Supported (Will be equal to AT \ K5 if selected)	
AT \ Tn	Y	N = 0-90 min N* = 0 (disable)	Inactivity Timer
%D0*	Y	Hang up without clearing buffer	
%D1	Y	Clear the receive buffer before hang up	
AT \ I	-	Not Functional	Interface Protocol
AT \ J0*	Y	BPS Rate Adjust Disabled	Speed Conversion Control Disable
AT \ J1	Y	BPS Rate Adjust Enabled Adjustment	Modem Port Rate
AT \ S	Y	List Profiles	
AT \ G0*	Y	Disables Modem Port Flow Control	Set Modem Port
AT \ G1	Y	Sets Modem Port Flow Control to Xon / Xoff	Flow Control
AT \ X0*	Y	Does Not Pass Xon / Xoff to Remote Modem	Xon / Xoff Pass Through Control
AT \ X1	Y	Passes Xon / Xoff to Remote Modem	
AT \ Q0	Y	Disable Flow Control	Serial Port Flow Control
AT \ Q1	Y	Bidirectional Xon / Xoff Enabled	
AT \ Q2*	Y	Unidirectional Hardware Control by CTS	
AT \ Q3	Y	Bidirectional Hardware Control by RTS / CTS	
AT \ Q4	Y	Unidirectional Xon /Xoff Send Only	
AT \ Q5		Keep CTS off until connect unidirectional hardware flow control	
AT \ Q6		Keep CTS off until connect for bidirectional hardware flow control	
AT % U	Y	Not Functional	Clear Serial Port Speed Serial Port
AT - P0*	Y	Ignores Parity for Special Characters	Check Parity
AT - P1	Y	Processes Special Characters Only if they have Correct Parity	

Note: ** Denotes Default Condition*

See Command AT \ V1 Above

STANDARD RESULT CODES\V0			MODIFIED RESULT CODES \V1	
Verbose	**Numeric**		**Verbose**	**Numeric**
CONNECT	1			
CONNECT 1200	5		CONNECt 1200 / REL 4 or 5	22
CONNECT 2400	10		CONNECT 2400 / REL 4 or 5	23
CONNECT 4800	11			
CONNECT 9600	12		CONNECT 1200/V.42	22
CONNECT 19200	14		CONNECT 2400/V.42	23

S	REGISTER FUNCTION
S0	Number of Rings to Answer: **Default** = 0 (no answer)(stored)
S1	Ring Count: Stores Number of Rings: Resets After Every Call
S2	Escape Code Character: **Default** = 043 (ASCII for "+")
S3	Carriage return Character: **Default** = 013
S4	Line Feed Character: **Default** = 010
S5	Back Space Character: **Default** = 008
S6	Wait for Dial Tone: **Default** = 002 (seconds) (minimum setting)
S7	Wait for Carrier After Dial: **Default** = 030 (seconds)
S8	Duration of Delay for Comma: **Default** = 002 (seconds)
S9	Carrier Detect Response Time: **Default** = 0.6 (seconds)
S10	Loss of Carrier Response Time **Default** = 1.4 (seconds)
S11	Touch Tone Duration: **Default** = 095 (milliseconds)
S12	Escape Code Guard Time: **Default** = 1 (second)
S13	Reserved
S14	Bit Mapped Register: Stored in NVRAM (XL93C46) Bit 0 Reserved Bit 1 Echo Bit 2 Result Codes Bit 3 Numeric Result Codes Bit 4 Always 0 Bit 5 Tone/Pulse Dialing Bit 6 Reserved Bit 7 Answer/Originate
S15	Reserved
S16	Test Register Bit 0 ALB Bit 1 Reserved Bit 2 Local Digital Loopback Bit 3 Remote Digital Loopback (Not Supported) Bit 4 Initiate Remote Test Bit 5 Initiate Remote Test With Self Test Bit 6 Analog Loopback With Self Test Bit 7 Reserved
S17	Reserved
S18	Test Time Stored in NVRAM (XL93C46) Default = 000 (seconds)
S19	Reserved
S20	Reserved
S21	Bit Mapped Register Stored in NVRAM (XL93C46) READ ONLY Bit 0 0 = RJ11 Jack Bit 1 Not Used Bit 2 CTS RTS Function Bit 3 DTR Function Bit 4 DTR Function Bit 4 / Bit 3 / Function 0 / 0 / DTR Always True Default 0 / 1 / DTR Off, Forces Command State 1 / 0 / DTR Off, Forces Modem Offline 1 / 1 / Modem Initializes With DTR OFF (ATZ)

REGISTER NUMBER	REGISTER FUNCTION
	Bit 5 EIA Carrier Status Bit 6 Bit 7 Guard Tone Select Bit 7 / Bit 6 / Function 0 / 0 / No Guard Tone Default 0 / 1 / 550 Hz Guard Tone 1 / 0 / 1800 Hz Guard Tone 1 / 1 / Reserved
S22	Option Bit - Mapped Register Bit 0 Determines Speaker Volume Bit 1 Bit 1 / Bit 0 / Speaker Volume 0 / 0 / Low 0 / 1 / Low 1 / 0 / Medium Default 1 / 1 / High Bit 2 Determines the Speaker Status Bit 3 Bit 3 / Bit 2 / Speaker Status 0 / 0 / Always Off 0 / 1 / On Until Carrier is Detected Default 1 / 0 / Always On 1 / 1 / As '01', Except Off for Dialing Bit 4, 5 and 6 Determine Response Messages Bit 6 / Bit 5 / Bit 4 / Message 0 / 0 / 0 / Basic Message Set 1 / 0 / 0 / Extended with Connect 1200 and Connect 2400 1 / 0 / 1 / Extended with 'No Dial Tone' 1 / 1 / 0 / Extended with 'Busy' 1 / 1 / 1 / Extended with All Messages Default Bit 7 Determines Off Hook/On Hook (Make/Break) Ratio for Pulse Dialing Bit 7 / Ratio 0 / 39/61 (USA and Canada) Default 1 / 33/67 (Uk and Hong Kong)
S23	Option Bit Mapped Register (LSB) Bit 0 Not Supported Bit 3 / Bit 2 / Bit 1 0 / 0 / 0 / 300 0 / 0 / 1 / Not Used 0 / 1 / 0 / 1200 0 / 1 / 1 / 2400 1 / 0 / 0 / 4800 1 / 0 / 1 / 9600 1 / 1 / 0 / 19200 1 / 1 / 1 / 38400(reserved) Bit 4 Determines the Parity for Transmitting and Receiving Data

REGISTER NUMBER	REGISTER FUNCTION
	Bit 5 Bit 5 Bit4 Parity 0 0 Even Default 0 1 Space/None 1 0 Odd 1 1 Mark Bit 6 Determines Guard Tone Frequency Bit 7 (Used in European Applications) Bit 7 Bit 6 Guard Tone (Hz) 0 0 Disabled Default 0 1 550 1 0 1800 1 1 Reserved
S24	Not Used
S25	Delay to DTR (Stored in NVRAM) Default = 005 (seconds)
S26	RTS to CTS Delay (Synchronous Mode Only) Default = 1 (milliseconds)
S27	Bit Mapped Register STORED IN NVRAM Bit 0 Bit 1 Transmission Mode Bit 1 Bit 0 Function 0 0 Asynchronous Mode Default 0 1 Synchronous Mode 1 1 0 Synchronous Mode 2 1 1 Synchronous Mode 3 Bit 2 Reserved Bit 3 Reserved Bit 4 Bit 5 Transmission Mode Bit 5 Bit 4 Function 0 0 Internal Modem Clock Used Default 0 1 DTE Supplied Clock 1 0 Slave Clock Mode 1 1 Same as 00 Bit 6 CCITT or Bell Handshaking Standard 0 CCITT 1 Bell (including CCITT V.22bis) Default Bit 7 Reserved
S28-35	Reserved
S36	Negotiate Failure Fallback (Affected by %C and \N) Bits 0 Hang Up 1 Attempt a standard asynchronous connection (&Q0) 3 Attempt an asynchronous connection using automatic speed buffering (&Q6) 4 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails, attempt a standard asynchronous connection 5 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails attempt a standard asynchronous connection
S37	Not Supported

REGISTER NUMBER	REGISTER FUNCTION
S38	Not Supported
S39	Reserved
S40	Not Supported
S41	Not Supported
S43-45	Reserved
S46	Protocol Selection: Bits 136 LAPM only (V.42)
S47	Not Supported
S48	Feature Negotiation Action 0 Negotiation disabled; presume the remote modem is configured for and has the capabilities necessary for the connection selected with S46 3 Negotiation enabled, but originating modem remains silent during detection phase. For connections with MNP modems; defeats connection sequence with other V.42 modems 7 Negotiation enabled 128 Negotiation disabled; forces fallback options specified in S36 to be taken immediately
S82	Break Handling: Affected by \K commands 3 "Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained 7 "Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed 128 "In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break
S86	Not Supported

Special Notes regarding the use of S registers above S27 and AT/n Commands.

1. Changes of S register values above S27 will effect the profile display for AT/n Commands. AT/n Commands however, do not modify the setting of S registers.

2. It is intended that a user or application software package will use only one method (S register \ n Commands) to effect the error control functions. Use of a combination could result in unpredictable behavior.

"AT + F" COMMANDS

The following are the list of commands supported by the XR-2900. They follow the Aug. 20, 1990 EIA standard PN-2388 (class 2).

All of the commands listed can be used in a string length of up to 40 characters, always preceeded by "AT". For example, "AT&D2E1V0+FCLASS=2<CR>" is a valid command sequence. A semicolon(;) must be used to separate =F commands.

COMMAND	DESCRIPTION	RESPONSE	COMMENTS
+FCLASS =*n*	Establish Class	OK	*n* integer values are 0 or 2 0 for Data mode 2 for FAX mode
+FCLASS=?		0,2	Provides service Class list
+FCLASS?	Service Class Setting	0 or 2	Indicates latest setting
	Default Fax Parameters	OK	Each number's location in the
+FDCC=VR, BR, WD, LN, DF, ER, FT, ST	DCE Capability		string represents the function listed below:
+FDCS=VR, BR, WD, LN, DF, ER, FT, ST	Current Session Parameters	OK	
+FDIS=VR, BR, WD, LN, DF, ER, FT, ST	Parameters for Session	OK	VR Vertical Resolution *0 for 98 dpi (dots/inch) 1 for 196 dpi BR DCE Bit Rate (modulation) 0 = 2400 BPS V.27ter 1 = 4800 BPS V.27 ter 2 = 7200 BPS V.29 *3 = 9600 BPS V.29 WD Page Width *0 = 1728 PIXELS IN 215 mm 1 = 2048 pixels in 255 mm 2 = 2432 pixels in 303 mm 3 = 1216 pixels in 151 mm 4 = 864 pixels in 107 mm LN Page Length *0 = A4, 297 mm 1 = B4, 364 mm 2 = unlimited DF Data Format *0 = 1. D Modified Huffman 1 = Not Supported 2 = Not Supported ER ErrorFree Mode *0 = Disable 1 = Not Supported

COMMAND	DESCRIPTION	RESPONSE	COMMENTS
			FT Binary File Transfer *0 = Disable 1 = Not Supported ST Scan Time 5 = 20 ms
+FLID = "Local ID"	Local FAX ID String	OK	20 character alpha numeric string for identification 0-9 space, +, ASCI 32-127
+FCR = 0	Capability to Receive	OK	DCE will not receive, but will answer and handshake
+FCR = 1		OK	
+FCQ = 0,1	Copy Quality	OK	n = 2 , Not Supported
+FBUG = 0, 1	Debug Mode: HDLC Frame	OK	
FMINSP = 0, 1, 2, 3	Minimum Transmit Speed	OK	0: 2400, 1: 4800, 2: 7200, 3: 9600
+FBOR = 0	Bit Order (DCE to DTE)	OK	MSB First
+FBOR = 1		OK	LSB First
+FDR	Begin Phase C Reception	CONNECT	Beginning of file is noted by DC2(12H) character
+FAA = 0	Auto Answer Mode	OK	FAX only communication
+FAA = 1		OK	Auto Fax/Data determination
+FDT =	Begin Sending Page	CONNECT	Marks beginning of Phase C data
+FHPS=0, 1	Handshake Protocol	OK	0: OK 1: Error
+FET=0,2	End of page	OK	1: Not Supported Indicates additional pages if any 0 for another page no parameter changes

RESPONSES from XR-2900 FIRMWARE:

The following lists valid responses to be expected from the XR-2942 firmware. The standardization of these responses allows the Application software to verify that a particular mode has been entered and monitoring of the fax transmission or reception process is easier.

RESPONSE	DESCRIPTION	COMMENTS
+FCON	FAX connection	Occurs after V.21 flags received
+FCSI:	Called Station ID	Report ID being Received (originate)
+FTSI:	Transmit Station ID	
+FDIS:	Session Negotiation Parameters	Uses format shown in Commands Section
+FDCS:	Report of DCS Frame Information	The Format is the same as +FDIS command
+FET:0, 2	Post Page Message Response	0: Another Page coming same document 1: Not Supported 2: No more pages or documents
+FPTS: 1, 2		1: Message Confirmation 2: Bad quality
+FHNG: 0	Call terminated status	Normal and proper connections

APPLICATIONS INFORMATION

The XR-2942 is shown in a typical "stand-alone" application in the modem schematic. The XR-2942 provides the command controller function for the XR-2900 Fax/Data modem chip set. For data operation the modem operates error-free through LAPM or MNP 2-4 modes and can offer increased throughput with MNP 5. The XR-2321 device included adds CCITT V.21 and V.23 FSK modes, it is optional and can be eliminated for designs not requiring these modes.

Detailed information for the XR-2900 is available in XR-2900 Fax/Data modem chip set datasheet.

Layout Hints

In order for the XR-2942 to provide optimal support for best performance of the modem, some design hints/rules should be followed.

- Locate the XR-2902 AFE near the DAA section
  - provide for a short transmit / receive carrier input path, away from any digital control lines.
- Maintain separate analog and digital grounds/ power lines back to the power supply.
- Bypass (capacitor decouple) the XR-2901, XR-2902, XR-2942 and op amp power supplies with both 0.01μF ceramic and 0.47μF tantalum capacitors near their actual pins. Ensure analog/digital supplies are bypassed to their respective ground.
- Crystal - parallel resonant type. Typical loading capacitors are 18pF.

SYSTEM PERFORMANCE

Performance for an error-correcting modem (data mode) has two major areas.

1) DATA PUMP PERFORMANCE
With error-detection capabilities turned off, the integrity of the data pump to pass data in the presence of impairments. Most often the major specification measured here is the probability of data errors with the receive carrier impaired by noise, or BER (bit error rate) vs S/N (Signal-to-Noise ratio).

Figure 8 shows BER vs S/N for the circuit in Figure 12, as measured with the test set-up in Figure 9.

2) ERROR CONTROLLER PERFORMANCE
The XR-2942, when in LAPM or MNP modes provides the control and detection required to yield perfect data transfer (Data Modem mode).

Beyond error correction, throughput, or data transfer rate, is another important parameter to the modems overall performance.

LAPM and MNP 2-4 Modes are not specifically provided for increased throughput. However an additional benefit of their error-detecting schemes is roughly a 20% increase in throughput. Using the 'Quick Brown Fox....' pattern, both LAPM and MNP 4 modes yielded better than a 20% throughput increase. V.22bis mode was used for this test, with an actual throughput of better than 2900 BPS measured.

MNP 5 Data Compression Included in the XR-2942 allows roughly a 100% throughput increase over the modems nominal data rate. As previously discussed, the throughput performance of MNP 5 varies with different types of data. Figure 10 shows data for various data patterns. Figure 11 illustrates the test set-up used for measuring the circuit of Figure 12.

Fax S/N performance is shown in the XR-2900 performance/ compatibility summary bulletin.

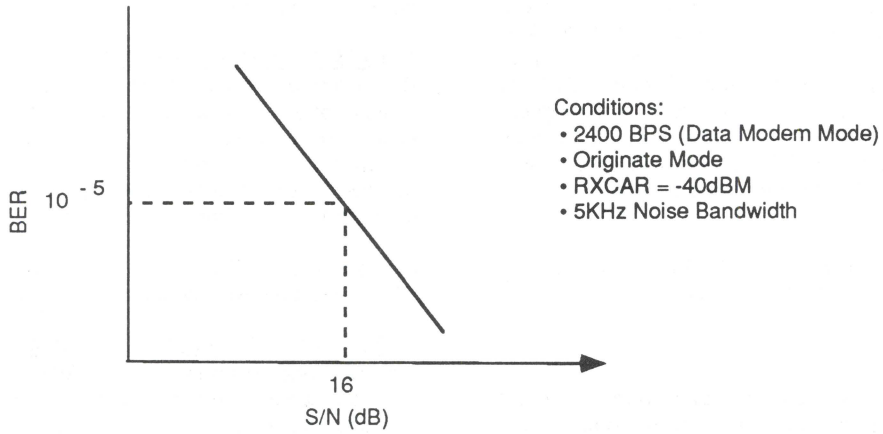


Figure 8. 2400 BPS Data Mode BER vs S/N (Non-Error Correcting)

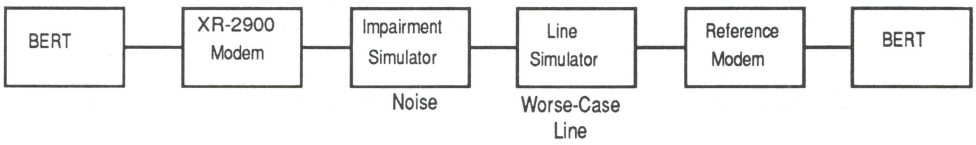


Figure 9. Data Quality Test Set-up

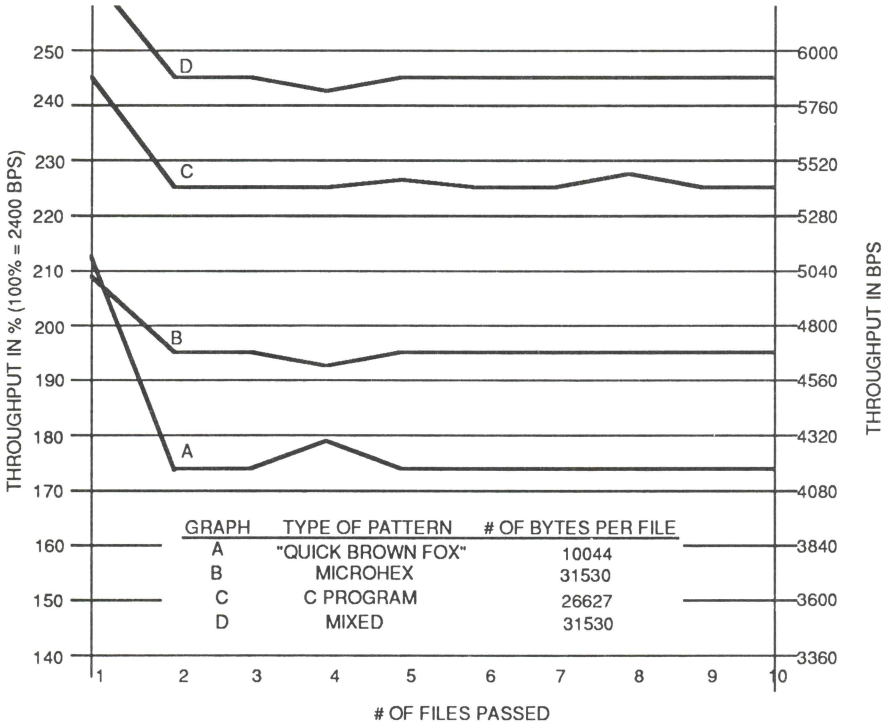
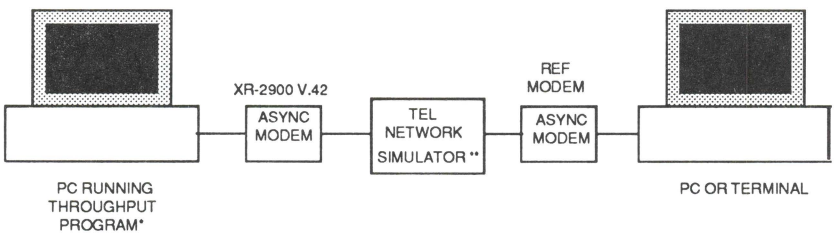
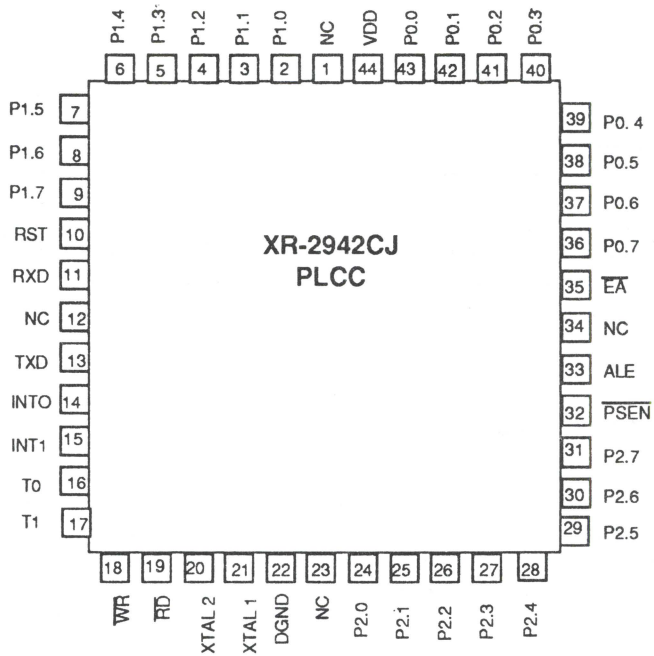


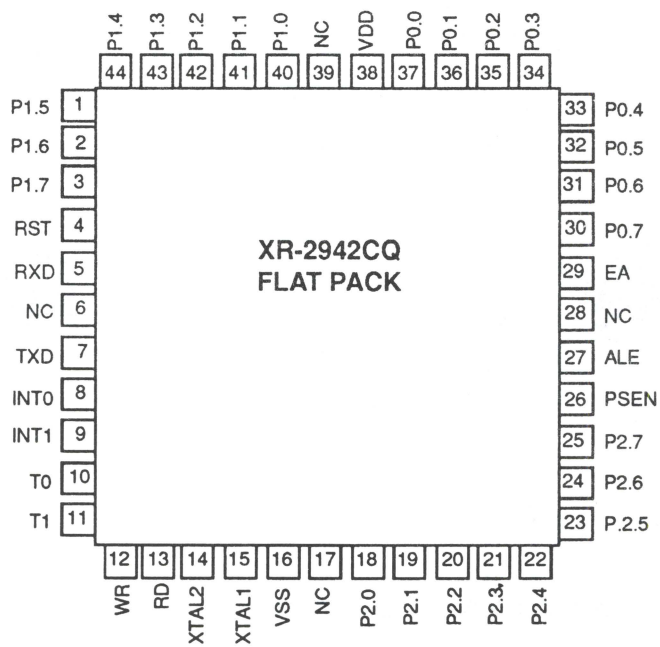
Figure 10. Effective Data Throughput



* APT (asynchronous Performance Tester), also contains data or files to be used during measurement. Productof Concord Data Systems.
** Simulates line impairment and attenuation condi tions.

Figure 11. MNP5 Throughput Measurement Test (Data Mode)


XR-2942CJ
PLCC
P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0 43
P0.1 42
P0.2 41
P0.3 40
P1.5 7
P1.6 8
P1.7 9
RST 10
RXD 11
NC 12
TXD 13
INTO 14
INT1 15
To 16
T1 17
39 P0. 4
38 P0.5
37 P0.6
36 P0.7
35 EA
34 NC
33 ALE
32 PSEN
31 P2.7
30 P2.6
29 P2.5
18 WR
19 RD
20 XTAL 2
21 XTAL 1
22 DGND
23 NC
24 P2.0
25 P2.1
26 P2.2
27 P2.3
28 P2.4


XR-2942CQ
FLAT PACK
P1.4 44
P1.3 43
P1.2 42
P1.1 41
P1.0 40
NC 39
VDD 38
P0.0 37
P0.1 36
P0.2 35
P0.3 34
P1.5 1
P1.6 2
P1.7 3
RST 4
RXD 5
NC 6
TXD 7
INT0 8
INT1 9
T0 10
T1 11
33 P0.4
32 P0.5
31 P0.6
30 P0.7
29 EA
28 NC
27 ALE
26 PSEN
25 P2.7
24 P2.6
23 P.2.5
12 WR
13 RD
14 XTAL2
15 XTAL1
16 VSS
17 NC
18 P2.0
19 P2.1
20 P2.2
21 P2.3
22 P2.4

Fax/Data Microcontroller with V.42bis

GENERAL DESCRIPTION

The XR-2943 is a dedicated microcontroller that provides command control for the XR-2900 Fax/Data modem chip set. The XR-2943 provides control for CCITT recommended V.42 error detection, including LAPM and MNP 2-4 protocols, with V.42bis BTLZ / MNP 5 data compression. Also supported is the Class 2 (EIA PN 2388) standard 'AT+F' extended command set.

The system architecture of the XR-2943 allows the actual command sets for the 'AT', 'AT+F', MNP, and LAPM and V.42 bis to reside external to the XR-2943, allowing ease of customization. Exar provides these command sets to use as is, or the designer can modify to the requirements of the design.

The XR-2943 operates from a single +5 volt power supply, offering low power consumption through CMOS technology.

FEATURES *

Group 3 Send/Receive Fax
Compatibility with Available Applications Software
Error Free Data Transfer:
DATA Mode
- LAPM
- MNP 2-4

MNP Class 5 Data Compression
- 4800 BPS Throughput

Increased Data Throughput by V.42bis Data Compression
- 9600 BPS Throughput

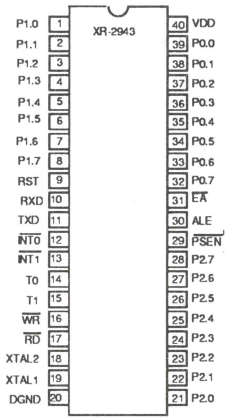
'AT' Command Control
EIA PN 2388 (CL2) Standard Commands ('AT+F')
- Easily Modified, Exar Supplied 'AT'/'AT+F'/MNP/V.42/V.42bis

*(Apply when used with XR-2900 Fax/Data modem chip set)

APPLICATIONS

Error Free Fax/Data Modem Applications
Stand-Alone Fax/Data Modems
Smart Modems
Laptop Modems (Send and Receive Fax or Data)
Networked Fax Machines

PIN ASSIGNMENT



(See back pages for PLCC and QFP packages)

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-2943CP	40 Pin Plastic Dip	0°C to 70°C
XR-2943CJ	44 Pin PLCC	0°C to 70°C
XR-2943CQ	44 Pin QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3V to + 7V
Input Voltage	-0.7V to (VDD +0.3V)
DC Input Current (any input)	±10mA
Power Dissipation **(Package Limitation)**	1W
Derate above 25°C	11 mW/°C
Storage Temperature Range	-65°C to +125°C

SYSTEM DESCRIPTION

The XR-2943, when coupled to the XR-2900 Fax/Data modem chip set, allows the implementation of a Group 3 fax/2400 BPS V.22bis modem. With MNP/ V.42/V.42bis operation included for data mode, compressed and error-free operation is provided.

The XR-2943 is just one in the family of controller options for the XR-2900 Fax/Data modem chip set, including:

FUNCTION	CONTROLLER
'AT' and 'AT+F'	8031
'AT'/'AT+F'/V.42/MNP 5	XR-2942
'AT'/'AT+F'/V.42/V.42bis/MNP 5	XR-2943

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5V ±10%, F_{CLK} = 11.0592MHz ±0.05%, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}	Power Supply Voltage	4.5	5	5.5	V	
I_{DD}	Power Supply Current		18	22	mA	
V_{IH}	Input High Voltage	1.8			V	Except XTAL1 and RST
V_{IH}	Input High Voltage	3.5			V	XTAL 1 and RST
V_{OH}	Output High Voltage	2.4			V	Ports 1,2,3 I_{OH} = -60µA
V_{OH}	Output High Voltage	2.4			V	Port 0 (External Bus Mode) ALE, PSEN I_{OH} = -400 µA
V_{OL}	Output Low Voltage			0.45	V	Ports 1,2,3, I_{OL} = 1.6 mA
V_{OL}	Output Low Voltage			0.45	V	Port 0, ALE, $\overline{PSEN}$ I_{OL} = 3.2 mA
I_{IH}	Input High Current (Leakage)			±10	µA	0.45 ≤VI ≤V_{DD}
I_{IL}	Input Low Current			-50	µA	V_{IN} = 0.45V

SYSTEM OPERATION

A typical application utilizing the XR-2943 to support the XR-2900 Fax/Data chip set, is shown in Figure 1. The XR-2900 provides the complete modem data pump function for:

CCITT	V.29	9600, 7200 BPS and 4800BPS
	V.27ter	4800 and 2400 BPS
	V.22bis	2400 BPS
	V.22	1200 BPS
	V.23(mode 2)	1200 / 75 BPS
	V.21(Ch 2)	300 BPS
Bell	212A	1200 BPS
	103	300 BPS

Command control is supported by the XR-2943 for:

MNP 2-4	Microcom Error Correction
MNP 5	Microcom Data Compression
LAPM	CCITT Recommended V.42 Error Correction
BTLZ	British Telecom Lempel Ziv (V.42bis)
'AT'	Industry Standard 'AT'
'AT+F'	EIA2388(CL2) Fax Commands

Although the XR-2943 does provide complete command control, the actual commands for the various modes reside in an external 32k Bytes EPROM. With this architecture and an Exar supplied command set, maximum flexibility is offered. The command set can be used as is, or customer tailored to a particular design.

The unique architecture utilized by the XR-2900 and command controller allow the **same** hardware (Printed Circuit Board (PCB)) to support several different types of Fax/Data modems. By changing available pin-to-pin compatible microcontrollers, the Fax/Data modem types listed in Table 1 are all possible with the same printed circuit board. As mode types are changed by the µC, EPROM supported command sets and SRAM size change and/or elimination are also required. In each case Exar provides complete production worthy command sets which may be used as is, or easily modified to meet specific application requirements. To aid in software modifications, Tables 2, 3 and 4 list the XR-2943 memory mapping, indicating customer usable regions.

External memory modifications requiring µC (XR-2943) support will need entry/re-entry point information. This point is important as the XR-2943 contains program memory with Exar proprietary V.42/MNP5/Auto Fax/Data Select functions not accessible externally (fusible link protected) or available to Exar customers. The V.42bis algorithm is located in external EPROM, however, source code is not provided for this routine.

2400 BPS Data Mode	Microcontroller Part Number	External Memory Requirements (Bytes)	
		EPROM	SRAM
'AT'	8031 (Generic ROMLESS µP)	32k	8k/32k
'AT' / MNP5/V.42	XR-2942	32K	8K/32K
'AT'/MNP5/V.42/ V.42bis	XR-2943	32K	32K

Table 1. 2900 BPS Modem Options / µC, EPROM, RAM Requirements

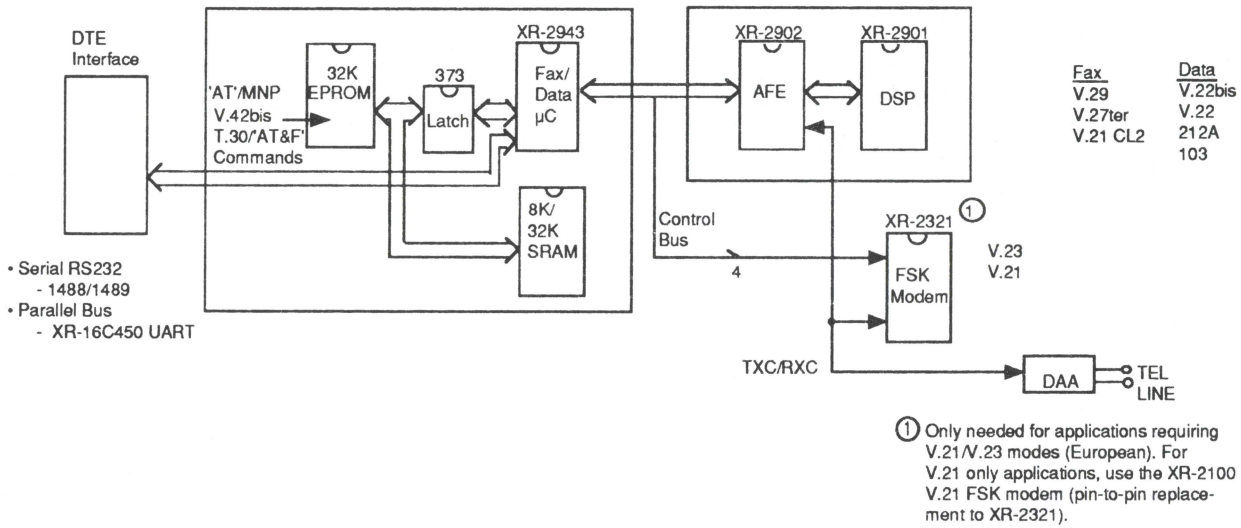


Figure 1. Fax/Data Modem with V.42bis/MNP5 (Data Mode) Block Diagram

ENTRY POINTS AND MEMORY MAPPING

Status / Mode Setting Memory Locations

Status	Location	Description
SPD_FLG	20 H.7	Speed Conversion Enable Flag.
BK_PRE	51 H	Break Prescaler Timer
BK_TMR	52 H	Break Timer (Only in Normal Mode)
MRCVP2	803BH	Disconnect to Check Auto-Reliable Fallback Mode.
PASS_ B	9D14H	Escape Code Checking Byte in Speed Conversion Mode.
SPEED	9D15H	Speed Indicator For All Modes. 0-19200 BPS 1 - 9600 BPS 2 - 4800 BPS 3- 2400 BPS 4 - 1200 BPS 5 - 300 BPS
Z_BUF	9D16H	Auto Reliable Fallback Character.
BACK_RAM	9D1AH	Starting Address for Command Buffer Backup.
OPT_P	9D50H	Output Port Selection Option (F0FF H to 40 FFH). This Parameter is Initialized Immediately After Power On and constantly monitored by MNP Module.
MNP_S	9E22H	Reliable Link Indicator
RETRAN	24H.0	RETRANSMISSION

Function Call Locations - V.42bis/V.42/ MNP 5 Program Entry Points

Function	Location	Description
SCTINT_1	0006H	Interrupt 0 Jump-In Point.
SCRINT_1	0016H	Interrupt 1 Jump-In Point.
SPINT_1	0026H	Serial Port Interrupt Jump-In Point.
MSG_CP	0030H	Exar Copyright Message.
P_ECRAM_1	0060H	After Escape MNP Re-Entry Point.
MSG_CPY	0063H	Exar Copyright Calling Subroutine.
MNP_IN	0066H	MNP Program Immediate Re-Entry Point for modifying MNP Program.
SPD_INM	0069H	Speed Conversion Program Jump-In Point.
INI_SPDM	006CH	Speed Conversion Initialization Routine.
V21_IN_1	006FH	300 BPS Speed Conversion Timer SetUp.
EC_MAIN	0080H	Calling Main MNP Program. This is the only location which will initiate the MNP program.

XR-2943 Re-Entry Points

Function	Location	Description
PWR_ONS	C000H	Power On
OUT_SCT	C003H	Interrupt 0
OUT_T0	C006H	Timer 0
OUT_SCR	C009H	Interrupt 1
OUT_T1	C00CH	Timer 1
OUT_SP	C00FH	Serial Port Interrupt
OUT_T2	C012H	Timer 2
MNP_OUT	C015H	MNP Program Intermediate Point
CHK070S	C01BH	MNP 'ESC' Jump Out Point
DISCONNECT	C01EH	MNP Disconnect
ON_LOOPS	C021H	Auto-Reliable Fallback Point.
SPD_OUTS	C024H	Speed Conversion Jump Out Point.
V21_INS	C027H	Call Speed Conversion ASM for 300 BPS.
SPD_TXD	C02AH	Put TXDATA to Modem Chip.
SPD_RXD	C02DH	Get RXDATA From Modem Chip.
I_TXSYNTTQ	C030H	GET TX CRC-CCITT CALCULATION ROUTINE
I_RXSYNTT	C033H	GET RX CRC-16 CALCULATION ROUTINE
I_TXASYN16	C036H	GET TX CRC-16 CALCULATION ROUTINE
I_RXASYN16	C039H	GET RX CRC-16 CALCULATION ROUTINE
I_SNDREL	C03CH	GET SENDING RESULT CODE SUBROUTINE
I_MNPINIT	C03FH	MNP PARAMETER INITIALIZATION ROU TINE
I_V42INIT	C042H	V42 PARAMETER INITIALIZATION ROUTINE
I_SETURMNP	C045H	UART SETTING ROUTINE
I_ENCODE	C048H	BTLZ ENCODING ROTINE
I_DECODE	C04BH	BTLZ DECODING ROTINE
I_BTFLUSH	C04EH	BTLZ DATA FLUSHING ROUTINE
I_BTINIT	C051H	BTLZ COMPRESSION INITIALIZATION

RAM Locations

The stack in the 'AT' program starts from 0C0H on page 1 and occupies 64 bytes of space. Internal RAM on page 0 has 23 bytes and page 1, 64 bytes of free indicator space.

The external RAM data memory is as follows:

1) Error Control	8000H-8FFFH
2) Data Compression Buffer	9000H-93FFH
3) FAX/Remote Access	9400H-95FFH
4) Available for use	9600H-97FFH
5) V.42/V.42 bis	9800H-99FFH
6) Break Buffer	9A00H-9AFFH
7) DTE TX Buffer	9B00H-9BFFH
8) DTE RX Buffer	9C00H-9CFFH
9) Misc. Registers	9D00H-9DFFH
10) MNP RAM Backup Buffer	9E00H-9EFFH
11) 'AT' RAM Backup Buffer	9F00H-9FFFH
12) BTLZ Compression Dictionary	C000H-FFFFH

Note: Before jumping into the MNP program the control code will backup the entire 256 bytes of AT RAM into external RAM. In addition, before jumping out of the MNP program it will backup the entire 256 bytes of MNP RAM into external RAM.

The Miscellaneous register function list is provided below. The option code control allows the firmware engineer to change the factory defaults in source code , then reassemble.

OPTION	LOCATION	PARAMETER	COMMAND	DESCRIPTION
Opt_0	9D09H	0	\N0	Non-MNP
		1	\N2	Reliable Mode
		2*	\N3	Auto_Reliable Mode
Opt_1	9F0AH	0	\Q1	Normal XON/XOFF
		1		Not used
		5*	\Q2	Unidirectional RTS/CTS
		3	\X1	XON/XOFF Pass Through
		4	\Q4	XON/XOFF Send Only
		2	\Q3	Bidirectional RTS/CTS
		6	\Q0	Disable Flow Control
Opt_2	9D0BH (BIT0)	0		Disable Speed Conversion
		1		Enable Speed Conversion
Opt_2	9D0BH (BIT1)	0	\J0	Disable Serial port rate adjust
		1*	\J1	Enable Serial port rate adjust
Opt_2	9D0BH (BIT2)	0*	\G0	Disable modem port flow control
		1	\G1	Enable modem port flow control to XON/XOFF (for Normal mode only)
Opt_2	9D0BH (BIT3)	0*	-P0	Parity bit for checking XON/XOFF
		1	-P1	Ignore parity bit checking for XON/XOFF
Opt_2	9D0BH (BIT4)	0*		Not used
		1		
Opt_2	9D0BH (BIT5)	0*		Not used
		1		

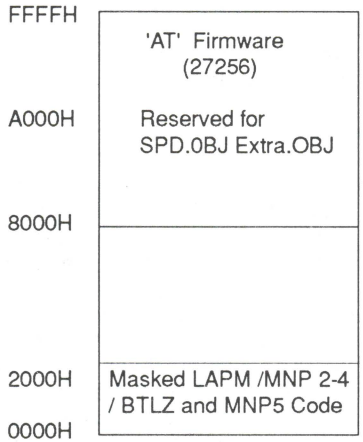
OPTION	LOCATION	PARAMETER	COMMAND	DESCRIPTION
Opt_2	9D0BH (BIT6)	0* 1	\M0 \M1	V.42 Mode MNP Mode
Opt_2	9D0BH (BIT7)	0 1*	%C0 %C1	Disable Data Compression Enable Data Compression
Opt_3	9D0CH	0 1 2 3*	\A0 \A1 \A2 \A3	Block size to transmit, 64bytes 128 bytes 192 bytes 256 bytes
Opt_4	9D0DH	0-9 3*	\Bn	Xmit break during normal mode at data mode, n=100ms
Opt_5	9D0EH	1 2 3*	\K1 \K3 \K5	Expedited, Destructive Expedited, Non-destructive Non-expedited, Non-destructive
Opt_6	9D12	(81H)	\0	Originate Reliable Link
Opt_6	9D12H	(82H)	\U	Accept Reliable
Opt_6	9D12H	(80H)	\Y	Switch to Reliable Link
Opt_7	9D13 (BIT0)	1 0		For 300 BPS connect indicator For other speed
Opt_8	9D0FH (BIT1,0)	0 1* 2 3	\V0 \V1 \V2 \V3	Standard Result code form Result code for MNP
Opt_8	9D0FH (BIT3,2)	0* 1 2	\C0 \C1 \C2	No set for Auto-reliable buffer Set Auto-reliable buffer Set fall back character
Opt_8	9D0FH (BIT4)	0 1*	\L0 \L1	MNP Stream mode MNP Block mode
Opt_8	9D0FH (BIT5)	0 1*	\Q0-\Q4 \Q5,\Q6	For \Q5, \Q6 turnoff CTS
Opt_8	9D0FH (BIT6)	0* 1		V.42 only negotiation
Opt_8	9D0FH (BIT7)	0* 1		Eliminate ODP for V.42
Opt_9	9D10H	0* N	%An	Auto-reliable fallback character

OPTION	LOCATION	PARAMETER	COMMAND	DESCRIPTION
Opt_A	9D11H	0* N	\Tn	Inactivity Timer
Opt-B	9D51H (BIT4)	0* 1	%Dn	**Default** Clear RX Buffer after disconnect
Opt_C	9D52H	6-250 32*	S90	Maximum String Length (BTLZ) character
Opt_D	9D53H (BOIT1,0)	0 1 2 3*		Disable BTLZ Compression Enable BTLZ one-way encode only Enable BTLZ one-way decode only Enable BTLZ two-way compression
Opt_D	9D53H (BIT1,0)	0 1 2* 3		Dictionary size option-512 entry 1024 (1K) entries 2048 (2K) entries 4048 (1K) entries
Opt_E	9D56H			

Interrupt Vectors

The XR-2943 brings out all interrupt vectors to the external program. This allows easy customer modification of service routines to suit a particular application. The interrupt vectors of the XR-2943 are as follows:

```
            ORG     0
            LJMP    PWR_ONS; Jump to Power
                            OnSet Up
                            Routine
            ORG     3H
EXT_INTO:                   ; Interrupt 0 for
                            SCT
            LJMP    OUT_SCT
SCTINT1:
            LJMP    SCTINT
            ORG     0BH
T_INTO:                     ;Timer 0 Interrupt
            LJMP    OUT_T0
            ORG     13H
EXT_INT1:                   ;Interrupt 1 for
                            SCR
            LJMP    OUT_SCR
SCRINT_1:
            LJMP    SCRINT
            ORG     1BH
T_INT1:                     ;Timer 1
                            Interrupt
            LJMP    OUT_T1
            ORG     23H
INT_SER:                    ;Serial Port Interrupt
            LJMP    OUT_SP
```



Note: 27256 = 32K Byte EPROM

Table 2. XR-2943 ROM Map

```
SPINT_1:
            LJMP    SPINT
            ORG     2BH
T_INT2:                     ;Timer 2 Interrupt
            LJMP    OUT_T2
```

XR-2943 PROGRAM/DATA MEMORY MAPS

Tables 2, 3 and 4 show the ROM and RAM memory maps for XR-2943. It should be noted that without the use of separate CS (Chip Select) for the XR-2902 and the XR-2321, there would be an overlap of address locations.

As it is indicated in Table 2, 32K bytes of EPROM is assigned to 'AT' command firmware. This section of the ROM is located between 8000H and FFFFH.

BTLZ, LAPM, MNP 2-4 and MNP 5 code is masked in the microcontroller (XR-2943), and resides in the 8K bytes of memory, between address locations 0000H and IFFFH.

Table 3 shows the RAM map, in which the space between 0000H and 002CH address locations is used for modem chip address. Table 4 shows the modem chip (XR-2902) address assignment. Included is addressing for the XR-2321 and XR-2100. These chips are optional to the system design, but may be added where V.21 or V.23/V.21 standards are required. The XR-2321 provides both V.23 and V.21 FSK data standards, while the XR-2100 provides only V.21. See XR-2321 or XR-2100 datasheets for details.

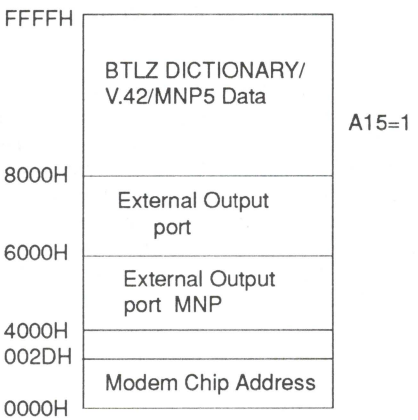


Table 3. XR-2943 RAM Map

MODEM CHIP	RAM ADDRESS	$\overline{CS}$
XR-2902	0000H - 001FH	A15=0 and A5 = 0
XR-2321	0028H - 002CH	A5=1 and A15=0
XR-2100	0028H - 0029H	A5=1 and A15 =0

Table 4. Modem Chip Address

Also RAM space between 8000H and FFFFH is assigned for the V.42bis dictionary, and MNP5 data and fax data. RAM locations between 4000H and 7FFFH are available for I/O ports such as LED, EIA, etc.

V.42 / MNP OPERATION

The XR-2943 when coupled with the XR-2900 Fax/Data modem chip set allows the implementation of a group 3 fax and an **error-free, increased throughput** 2400 BPS data modem. To gain an understanding of V.42bis/V.42/MNP 5 modes for data operation, the following basic information has been included. A basic understanding of error correction techniques, flow control, speed buffering, and data compression will allow the designer to better understand a V.42/MNP5/V.42bis modems capabilities and how to best utilize them. One excellent introductory book on the subject of data compression for both fax and data modes is DATA COMPRESSION by Gilbert Held. The publisher is WILEY.

V.42 is a **CCITT** recommended error correction protocol which allows asynchronous DTE's (Data Terminal Equipment) to communicate error-free with other such equipped modems.

The actual error detection protocol used in V.42 is an **HDLC** (High-level Data Link Control) based protocol called LAPM, for **Link Access Procedure for Modems.** For additional detailed information beyond the following basic description, refer to the CCITT Recommendations, Series V, 'Data Communication Over the Telephone Network'. The latest version is known as the **'Blue Book'** (Blue Covers) or Series, dated 1988 (Melbourne), a recent update from the **'Red Book'.**

V.42 Basic Operation/Features

- **HDLC**-based error correction protocol-LAPM
- Asynchronous (Async or 'start/stop') DTE Communication - error free
- Actual line transmission is synchronous (sync)- no start or stop bits (stripped from data), however initial handshake, subsequent to modem handshake is asynchronous
- Error Detection
  - Data sent in 'frames' or blocks with a nominal size (default) of 128 Octets (Octet - 8 bit) data frames.
  - Start/Stop bit elimination from data creates an actual data throughput improvement, roughly 120% of nominal. 2400 BPS becomes about 2900 BPS.
  - Encoded information added to data frame for receiver to 'decode' and determine if the block was error free. 16-bit cyclic redundancy check (CRC) methods are used for data encoded information to: (1) indicate correct data and (2) recognize imperfect data frame.
  - Retransmission (automatic) of determined imperfect frames to ensure perfect data is received.

V.42/ V.42bis operation is found to be virtually identical (specifically to variable parameters) to that of MNP reliable / normal modes of operation. For this reason the MNP command set is also used for V.42/V.42bis variables control.

DATA COMPRESSION

Two general families exist of data compression techniques. The first is logical compression, which is limited to a defined file type. It is called logical because fixed defined paths exist for the compression and decompression; e.g. year, month, date, or the type of account: savings or checking. This technique would substitute a number 4 for April placing in 3 bits what would require 40 bits (7 bits and parity per character). To allow the inclusion of other months (above July, the seventh month) would require an additional bit, but the net number of bits being sent is reduced.

For compressing the type of account, a single bit would allow the encoding of either 'checking' or 'savings', rather than using the ASCII representation which would require up to 64 bits to transfer the two words. Both of these examples would require positioning limitations or the use of packets, where the location in the packet determines what logical decompression technique should be used to decode the information stored. This result is in an overhead of bits being needed to allow reliable decompression of the information.

The second technique is physical compression. This technique does not limit itself to certain types of information and files, but is more complicated to be implemented. Physical encoding compresses redundant characters substituting coded characters. As an extreme example, a page full of the letter 'a' could be sent as 'a5610', noting the fact that 5,610 'a's appear on the page. In this example the throughput would be 1122 times normal. Unfortunately, the situation to send such a large amount of compressed data does not occur too often. In addition to the encoded data, a start encoding symbol is needed to inform the decoder on the receiving side that the standard decoding technique should be used.

The two sub groups of physical compression is block encoding and stream encoding. Block encoding in general is a slower process, for it requires the entire file to be processed before sending. The use of stream encoding allows the mix of on-line information (entered by keyboard for example) and stored data. The default for the XR-2943 is stream mode. This is controlled by the \L command.

BTLZ® OPERATION

BTLZ is a patented technique to increase throughput to nearly 4 times an uncompressed file. To produce this greater performance BTLZ uses an adaptive dictionary that is partially reset from time to time to adapt to the possibly changing file. This 2-Dimensional dictionary allow for a greater compression ratio than the 1 Dimensional technique used by MNP® 5 which take ASCII codes and provide a shortened code.

The dictionary is created using data that is transmitted, therefore, no transmission time is needed to exchange dictionary data. The resetting , presetting or updating of the dictionary is under lock-step, where each deletion is predefined. Either a full reset to the first level occurs (most common letters and space character found in files), or removal of dead ends. This adaptive process provides two things. If not done, the dictionary would need to be infinite in size, for all possible data combinations (words) would have a path. In a repetitive data pattern situation this is ideal. For example, "THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG" repeated over an over would be learned by the XR-2943 using BTLZ and compression would reach the maximum set between the DTE and DCE (19.2 kBPS). However, in a real life situation such files have limited usefulness. With a typical text file, random for the short term, the compression ratio is around 3.4:1.

It is this randomness that Mr. Jacob Ziv and Mr. Abraham Lempel based their compression theory upon. The idea that for short duration data transfer, a repetitive pattern can be seen, however for longer term data transfer, editing of the dictionary is needed. Their introductory paper: On the Complexity of Finite Sequences (IEEE Transactions on Information Theory, Volume IT-22 Number 1; January 1976; PP 75-81) goes into some detail as to how their compression technique was developed. This information is not needed to use the XR-2943.

British Telecom Lempel Ziv is a patented Data Compression technique used in the V.42bis standard.

MNP® OPERATION

MNP, or Microcom Networking Protocol was developed by Microcom, Inc., a modem manufacturer. Since conception, it has been in a constant state of update/improvement. For this reason 'classes' of operation emerged to signify each major update or improvement.

Relative to the V.22bis or 2400 BPS modems, up to class or level 5 has become the 'standard'. MNP is not used with the FAX modes of operation. As mentioned before HDLC framing techniques are used.

MNP CLASSES

(Throughput data is based on **2400 BPS** line speed).

Class 1 A half duplex protocol and no included in many new designs. Throughput was about 70% or1690 BPS. The XR-2943 does not support this class.

Class 2 Asynchronous operation with byte oriented data formatting. Throughput is roughly 84% of nominal or about 2000 BPS.

Class 3 Conversion to synchronous, bit oriented data handling is transmitted in blocks consisting of 1 to 64 characters. Throughput is about 108% or 2600 BPS.

Class 4 Basic characters are the same as Class 3, but block size is dynamic, up to 256 Bytes, (flexible size is based on data transmission quality). Throughput is 120% or 2900 BPS.

Class 5 Includes Class 3 and 4 with data compression techniques added. The compression effectiveness is dependent on the type of data, but typical throughput enhancements are up to 200% or 4800 BPS.

ERROR CORRECTION

Modem users have come to expect sophisticated circuitry like automatic adaptive equalization for varying phone characteristics and retrain modes for ensuring continued optimal performance. These techniques dramatically improve performance characteristics which is quantified by BER vs S/N measurements, the probability of errors when the modem signal is in the presence of noise.

The previously mentioned techniques are aimed at improving the modem data pump through analog (or digitally synthesized) circuitry. Techniques are becoming popular for not only improving, but virtually eliminating data errors through protocols implemented in the modem's command microcontroller (μC). Prior to these 'hardware' based schemes, error correction provided in the applications software was available , such as X-MODEM or Kermit for asynchronous file transfer. In mainframe environments, SDLC or HDLC schemes were used.

Software based error correction schemes do however have their disadvantages. One important one being reduced data throughput. The throughput performance varies, but all schemes reduce data transfer below its nominal rate. Values of 30% are common, equating to only about 800 BPS for a 2400 BPS connection.

The hardware based error correction protocols supported by the XR-2943 for data mode are those as specified by the **CCITT LAPM,** and **MNP.** These schemes convert asynchronous data to be transmitted to a synchronous format (start and stop bits are stripped) for a packet-oriented protocol. Throughput values again vary, however typical values of 108% for the lower MNP Class 3 and 120% for MNP Class 4 or LAPM. These equate to roughly 2600 - 2900 BPS for 2400 BPS modems.

Actual error correction is based on adding information to the block-oriented data, through a 16-bit CRC (Cyclic Redundancy Check) calculation. The receiving side calculates CRC values for each block and if found to be incorrect, a retransmission of that block will be requested.

Typical frame sizes for LAPM are 128 Octets (8-bit start/stop bit stripped characters).

DETERMINATION OF BLOCK SIZE SETTING

The block size adjustment allows the user to compensate for situations where a high probability of errors exist. This condition occurs when the signal to noise ratio is extremely low. The XR-2900 provides performance curves for 2400 BPS(V.22bis) operation and single points BERT data for 1200 and 300 BPS. As a rule of thumb, under typical dial-up telephone connections, the negotiate block size feature of MNP and V.42 provides satisfactory results (generally 256 characters/block). However, if the signal to noise ratio is much less than 16dB S/N (at 2400 BPS) the probability of receiving data with an error is much greater, which would require retransmission of the entire block. By reducing the block size, the amount that is needed to be retransmitted is reduced, which increases the throughput. Under poor line conditions, the throughput would be reduced for a greater number of link acknowledgments would be needed.

For BTLZ 2 dimensional encoding, the maximum number of character setting (register S90) can help in obtaining a higher throughput earlier than if the straight learning mode of BTLZ is used. If it is known that a certain number of characters are repetitive, that setting will provide an increase in throughput. However, if the file contents change, become more random, a reduction in throughput will occur. The default setting of 32 characters is a compromise for a typical text file.

DATA COMPRESSION

The CCITT recommendation for V.42bis specifies a data compression mode, as provided by British Telecom Lempel-Ziv (BTLZ). Modem controller protocols have advanced to the point where in addition to providing error-free data transfer with the use of LAPM or MNP 2-4, they can also offer data compression operation.

These data compression schemes are BTLZ and MNP 5. Although MNP 5 is not specifically part of the V.42bis recommendation, it has been included in the XR-2943 to serve only as a further enhancement to the XR-2943 based modems and ensure data compression compatibility with the established MNP 5 modems.

MNP Class 5 is the protocol for **data compression**. It is by far the most accepted protocol for this function. CCITT recommendations have updated the V.42 standard to include the BTLZ data compression technique. This new standard is **V.42bis**, which provides better throughput characteristics than MNP 5.

MNP 5 data compression offers the XR-2900 Fax/Data modem chip set roughly 100% increase in throughput (in data mode), or 200% of nominal. This translates to a maximum modem throughput of 2400 BPS x 2 = 4800 BPS for a text file.

MNP 5 techniques utilize a scheme which abbreviates redundant data characters for a much higher transmission efficiency or throughput increase. Because of its dependency on redundant characters, the amount of improvement will vary. Typical improvement values are in the range of 75 to 125%, or 4200 to 5400 BPS for a 2400 BPS modem link.

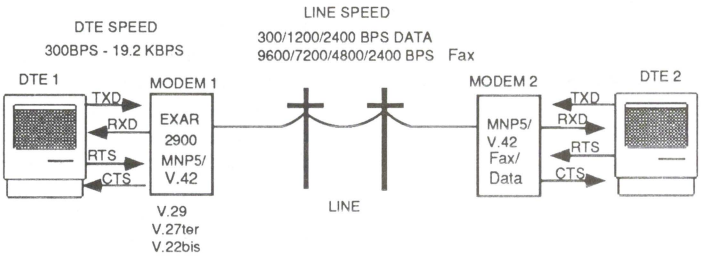


Figure 2. Basic Modem Connection

XR-2943 V.42/MNP FUNCTIONS AND COMMANDS

The XR-2943 with external EPROM provides control for the following major functions:

FUNCTION	DESCRIPTION
• 'AT' Command Control	Provides 'AT' Command Set Control
• 'AT+F' Commands	Provides control of the FAX functions EIA 2388 (CL2)
• MNP Level 2-4	Provides error correction for 100% perfect data transfer.
• MNP Level 5	Allows roughly a 100% increase (4800 BPS for V.22bis mode) in data throughput, through data compression techniques.
• V.42bis (BTLZ®)	Using 2-dimensional adaptive coding, 400 % of nominal data throughput is possible.
• V.42 (LAPM)	100% perfect data transfer
• Speed Conversion	Maintain up to 19,200 BPS DTE (terminal speed) for 300 BPS to 9600 BPS line speeds, both for LAPM/MNP and non-error correcting connections.

FLOW CONTROL

As previously outlined, a method for regulating the flow of data to be transmitted is necessary when DTE data rates exceed line rates. Figure 2 illustrates a basic modem connection and helps illustrate where flow controls fit in.
Flow control can be under **hardware** or **software control.**

HARDWARE FLOW CONTROL

Hardware Flow Control allows the modem to lower or raise its CTS (Clear to Send) line to the DTE. This provides an ON/OFF control of data flow from DTE to modem. If the modem data buffer becomes full it lowers the CTS line to stop transmit data flow to allow the modem to "catch-up".

SOFTWARE FLOW CONTROL

An alternative to hardware flow control is control by software, known as **Xon/Xoff**. This is accomplished by special characters inserted into the data stream to start and stop data flow. **Control Q (^Q)** is used to start or restart data flow and **Control S (^S)** to stop data flow.

Three different variations of Xon/Xoff control modes are:

- Send Only
- Normal
- Passthrough

Application Software Interface

The firmware of the XR-2943 (combined masked and supporting code) supports the working document of the Telecommunication Industry Association , for fax 'AT&F' commands , temporarily assigned the EIA part number 2388. The level of support is service class 2, which places most of the CCITT T.30 (fax handshaking) command functions in the modem (XR-2901, XR-2902 and XR-2943). Figure 3 indicates the approximate division between modem (DCE) and PC (DTE) for T.30 and T.4 (fax bit mapping).

The command section of the XR-2943 data sheet defines the commands, responses and functions of the firmware supplied with the XR-2943. It is possible to send those commands to the XR-2900 system by keyboard entry, visually monitor the responses and send or receive data of the proper format. However, to use the XR-2900 modem system effectively, it is best to use an application software package that automatically monitors the response strings and acts accordingly.

In general the application software would be required to perform:

- ASCII to Bitmap Conversion
- PCX to Bitmap Conversion
- TIFF to Bitmap Conversion
- PICT to Bitmap Conversion

In an imbedded system, such as a text editor, the above list could be reduced to include only the ASCII to Bitmap Conversion. Because ASCII is encoded, information as to the font, italics, bold, underline, and other word processor options are lost. It is expected that either the communication packages will start recognizing some Word processor options, or an integration of word processors and communication software such as seen today. The second step is to perform:

- BITMAP to 1 Dimensional Coding or
- BITMAP to 2 Dimensional Coding

as per the CCITT T.4 specification.

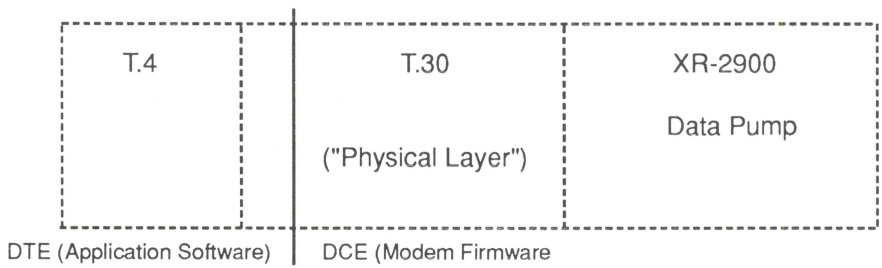


Figure 3. T.4/T.30 Partitioning For DCE/DTE

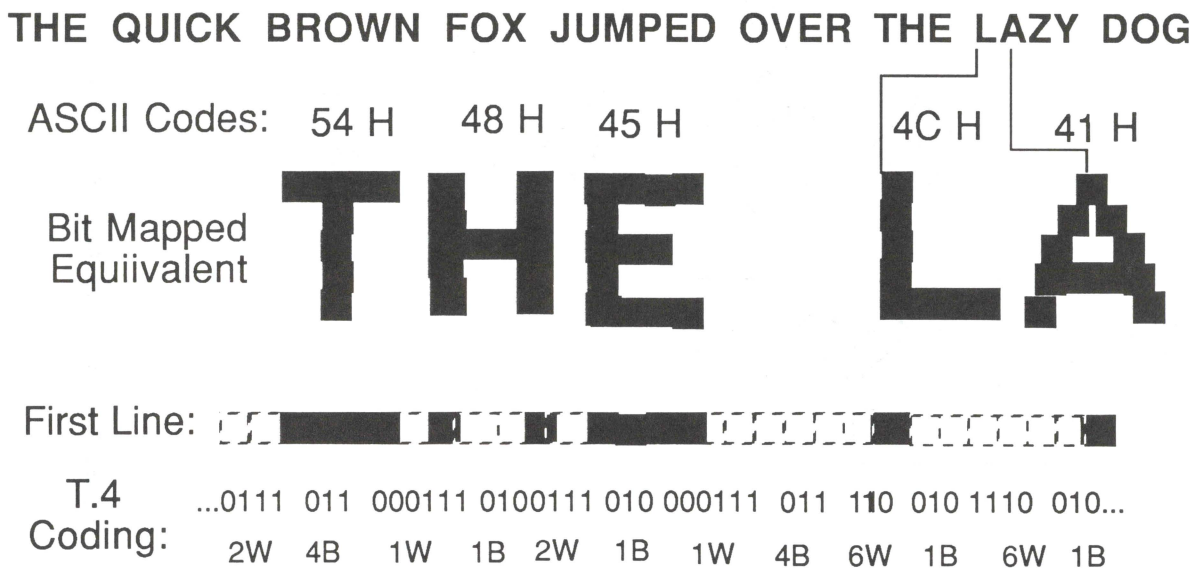


Figure 4. T.4 Encoding

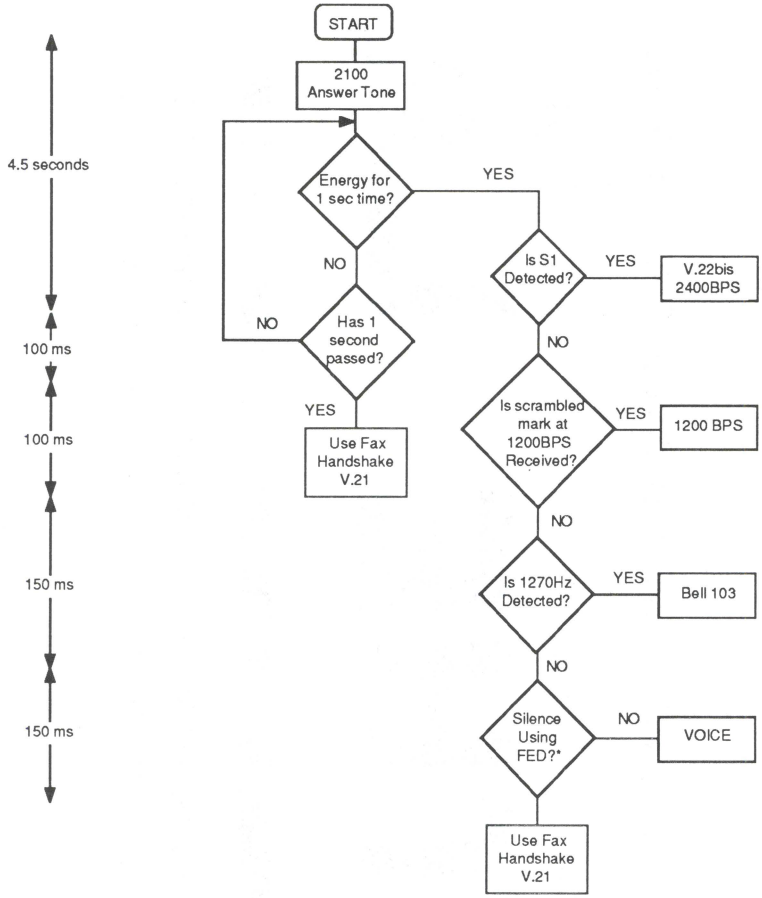


Figure 5. Auto Fax/Data Negotiation For Answer Mode

Figure 4 shows the process of taking text and encoding it 1 dimensionally using the CCITT T.4 Huffman codes. The entire line must total 1728 picture elements or pels. The application software will need to convert from files set up for 640 pels per line to one containing 1728 or more.

Modified Huffman encoding is a technique of data compression where unexpected lengths of either black or white are given long codes and the more common run lengths are given much smaller codes. In the example of figure 4, the lengths of white and black are much shorter than found in the typical file and the compres-- sion ratio is actually worse than if it was possible to send uncompressed.

In the Vertical dimension, either 98 dpi (dots per inch) or 198 dpi would be selected. This would determine the number of scan lines needed per page as well as determine the quality of the reproduced image. Two dimensional Huffman encoding is not supported. Both of these modes would need to be enabled by using the VR (vertical resolution) and DF (data format) subparameter of the +FDIS command.

AUTO Fax/Data Negotiate: The XR-2943 supports the EIA PN 2388 standard on auto Fax/Data negotiation. Figure 5 shows the flow for this process to proceed. The entire process requires less than 4 seconds permitting it to be compatible with fax machines and data modems available today.

T.30 Description

The CCITT T.30 specification was intended to standardize the signaling between two fax machines. This permits any group III fax card or machine to communicate with another also meeting the standard.

The T.30 specification defines the fax transmission and reception process into five steps or phases:

Phase A: Call Establishment
Phase B: Negotiation of data rate, and capabilities of both machines
Phase C: Message (Page) Transmission
Phase D: Post Message (Page) Transmission; confirm send; possibly more pages
Phase E: Call Release (Hang up)
Figure 6 provides a general flow chart of the process.

Phase A of the CCITT T.30 specification establishes that a fax modem is answering the line and not a data modem. The uniqueness of this handshake allows the ability to add the feature of switching between fax and data modes with the XR-2900 Fax/Data modem chip set. In addition, the optional identification of the called and calling unit takes place using CCITT V.21 modulation and demodulation. The data is framed (synchronous) to ensure reliable communication at this point, even on an extremely poor phone line. By taking this extra step the CCITT has provided a means to negotiate (during Phase B) the data rate to a lower rate, as required. This can be utilized by the application software developer to add a security mode: if the correct response is not provided, the session can be ended at this point.

Phase B is the exchange of information as to capabilities of the two fax modems, again using V.21 channel 2 synchronous transmission and reception. Information such as scanning speed, number of dimensions of Huffman encoding, and grey scale encoding is sent at this time.

Phase B also includes the phasing and training process for the fax modem data pump. The *calling* (originating) modem transmits a bi-phase signal at the proper baud rate for the transmission (2400 symbols/second for 9600 BPS) to allow the called (answering) modem to adjust for group delay distortion as well as gain loss of the line. If not successful, a failure to train (FTT) is sent from the *called* modem to the calling modem at 300 BPS using the framing described above. The *calling* modem tries at the next lower speed. Once this process is successful, the *called* modem confirms that it is programmed to receive.

The sending of the page or information occurs during **Phase C** at the maximum negotiated data rate (9600 BPS for the XR-2900).

Phase D is the confirmation of the end of message and of receiving the page. This usually indicates that the page has been received properly. At this time the optional multiple pages signal can be sent. If another page is to be sent or received, phase C is repeated.

Phase E disconnects the phone line (on hook).

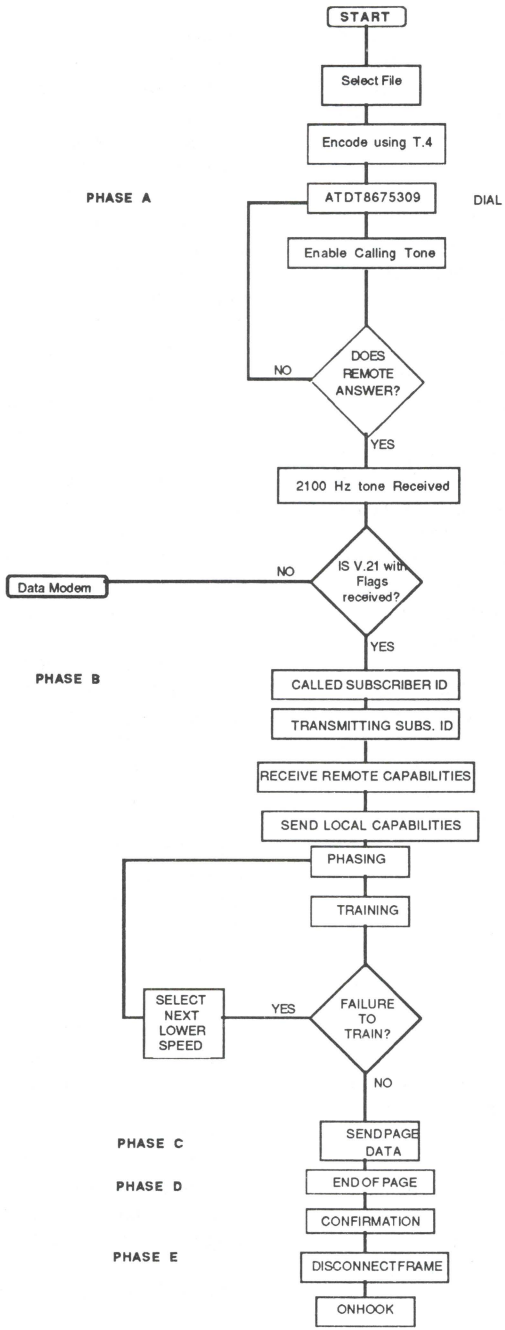


Figure 6. CCITT T.30 Process Sequence (Transmit a Single Page)

The XR-2943 supports automatic call establishment. However this does not preclude a manual to automatic process, using an external dialer and starting the application program to send the fax (off hook immediate and wait for phase A to begin).

The process is similar when receiving a call. However, with the Exar proprietary Fax/Data auto select, the modem will determine during phase A whether a fax machine/card or data modem is calling. Details for this are provided in this datasheet.

PROTOCOL NEGOTIATION

During data mode, the XR-2943 supports error correcting or reliable modes of operation for not only LAPM, but also MNP type protocols. Also, since data compression operation is specified by the CCITT V.42bis specifications, BTLZ has been included along with the industry standard MNP®5 for increased compatibility. Because of these multiple protocols supported, and to simplify the command process the XR-2943 offers two powerful protocol negotiation commands:

1) AT\M0 **Default** Mode
   This command selects an automatic protocol negotiation mode.
   First BTLZ (V.42bis) with LAPM negotiation will be attempted. If not possible, MNP operation will be negotiated. The highest possible class of MNP operation will be negotiated (depending upon setting of the %C command). If the remote modem does not support error correction, normal 2400 BPS (or1200/300 BPS) operation will be supported.

2) AT\M1
   This command will **disable LAPM and BTLZ** operation. Here only MNP 2-5 and non-error correcting modes of operation will be supported.

It is strongly recommended that the default conditions be used when first starting to use the sophisticated features of the XR-2943. The default conditions have been selected to provide effortless use of the XR-2943.

The following is a command set summary for the XR-2943. Provided are:

Data Mode
1) Basic Connection/Dialing Commands
2) Dialing Modifiers
3) Standard Hayes 'AT' Command Set
4) 'S' Register Descriptions/Functions. These registers are used for controlling the value or function of various 'AT' commands.
5) BTLZ/MNP/LAPM Commands. The entire list represents the MNP command set. Most of the MNP commands also apply to LAPM, with the exceptions indicated.

Fax Mode
6) Extended 'AT + F' Commands for class 2 (support of EIA PN 2388)
7) Fax responses

COMMAND	DESCRIPTION / RANGE - SIZE
A/	Execute previous command, without striking <CR> key
AT	Attention
ATA	Answer Immediate
ATB0	CCITT V.22 mode
ATB1	Bell 212A mode **DEFAULT**
ATB2	V.23 mode
ATD	Dial Command
ATDP	Dial Using pulse dial
ATDT	Dial Using DTMF tone dial **DEFAULT**
The following 8 modifiers will dial using the previously used technique (pulse or tone), or the T or P command can be added after the D (dial) command. 0-9 A B C D * #	
ATDW	Wait for Dial Tone for Period Set by S7 Register
ATD@	Quiet Answer: Wait for 5 Seconds of Silence Before Dialing
ATD!	Hookflash: Commonly Used PBX Systems
ATDR	Reverse Answer Mode
ATDS=n	Dial Stored Number when n= 0-3
ATD/	Wait 0.125 Seconds
ATD;	Return to Command Mode After Dialing
ATD,	Pause for Time Set by S8 Register
ATE0	Command Echo Disabled
ATE1	Command Mode Echo Enabled **DEFAULT**
ATH0	Go On Hook (Open Relay)
ATH1	Go Off Hook (Close Relay)
ATI0	Identification Code
ATI1	Identification Code
ATI2	"OK" Response if Checksum Verifies
ATI3	EXAR EPROM Revision Date
ATL0	Lowest Volume Setting
ATL1	Same as ATL0
ATL2	Medium Volume Setting **DEFAULT**
ATL3	Maximum Volume
ATM0	Speaker Always Off
ATM1	Speaker On Until Carrier Is Detected **DEFAULT**
ATM2	Speaker Always On
ATM3	DTMF Tones are not Heard, but Speaker is on Until Carrier Detected
ATO	Originate Immediate or Return to Data Mode
ATO1	Request a Retrain When in V.22bis Mode
ATQ0	Provide Result Codes **DEFAULT**
ATQ1	Disable Result Code
ATSn?	Provide S Register Value
ATSn=	Set S Register Value
ATV0	Terse (and Verbose) Responses, affected by \Vn

NUMERIC	DESCRIPTION / RANGE - SIZE	
		\V0
0	OK	Command Executed
1	CONNECT	Connection at 0 to 300 BPs
2	RING	Ring Signal Detected
3	NO CARRIER	Carrier Signal not Detected
4	ERROR	Error
5	CONNECT 1200	Connection at 1200 BPS
6	NO DIALTONE	No DialTone Detected
7	BUSY	Busy Signal Detected
8	NO ANSWER	No Silence Detected
10	CONNECT 2400	Connection at 2400 BPS
11	CONNECT 4800	Connection at 4800 BPS
12	CONNECT 9600	Connection at 9600 BPS
14	CONNECT 19200	Connection at 19200 BPS
		\V1
22	CONNECT 1200/REL 4	MNP Class 4 Link
22	CONNECT 1200/REL 5	MNP Class 5 Link
23	CONNECT 2400/REL 4	MNP Class 4 Link
23	CONNECT 2400/REL 5	MNP Class 5 Link
22	CONNECT 1200/V.42	V.42 Link
23	CONNECT 2400/V.42	V.42 Link
22	CONNECT 1200/V.42bis	V.42bis Link
23	CONNECT 2400/V.42bis	V.42 bisLink

COMMAND	DESCRIPTION / RANGE - SIZE
ATV1	Verbose Response **DEFAULT**. See ATV0 for Responses
ATX0	Enable Result Codes 0-4
ATX1	Enable Result Codes 0-5, 10
ATX2	Enable Result Codes 0-6, 10
ATX3	Enables Result Codes 0-5 and 7 and 10
ATX4	Enables Result Codes 0-10 **DEFAULT**
ATY0	Disable Long Space Disconnect **DEFAULT**
ATY1	Enable Long Space Disconnect
ATZ0	Software Reset, Restore S Register from profile location 0 in NVRAM
ATZ1	Restore S Registers From Profile Location 1 in NVRAM
AT&C0	EIA Carrier Line Always Forced on **DEFAULT**
AT&C1	EIA Carrier Line Follows Data Carrier
AT&D0	DTR Always on **DEFAULT**
AT&D1	Modem Goes to Command Mode When DTR Goes Off
AT&D2	Modem Goes on HOOK and Returns to Command Mode When DTR Goes Off
AT&D3	Modem Initializes When DTR Goes Off
AT&F	Fetch S Registers From EPROM for Factory Default
AT&G0	No Guard Tone **DEFAULT**
AT&G1	550 Hz Guard Tone Enabled
AT&G2	1800 Hz Guard Tone Enabled
AT&J0	RJ-11 Select **DEFAULT**
AT&K0	Flow Control Disabled
AT&K1	No Function
AT&K2	No Function
AT&K3	RTS/CTS Flow Control **Default**
AT&K4	Xon/Xoff Flow Control
AT&K5	Xon/Xoff Pass Through
AT&L0	Switched Line Select **DEFAULT**
AT&L1	Leased Line Select
AT&M0	Asynchronous Mode **DEFAULT**
AT&M1	Synchronous Mode With Asynchronous Dial
AT&M2	Synchronous Mode and Dial the Stored Number Immediately
AT&M3	Synchronous Mode With DTR Controlling Data/Talk
AT&P0	US Make/Break Ratio For Pulse Dialing **DEFAULT**
AT&P1	UK Make/Break Ratio For Pulse Dialing
AT&Q0	Direct mode (same as Hayes)
AT&Q1	Same as &M1
AT&Q2	Same as &M2
AT&Q3	Same as &M3
AT&Q5	Error Control Mode
AT&Q6	Normal Mode
AT&R0	Clear To Send (CTS) Follows RTS **DEFAULT**
AT&R1	CTS Always On
AT&S0	Data Set Ready (DSR) Always on **DEFAULT**

COMMAND	DESCRIPTION / RANGE - SIZE
AT&S1	DSR Normal
AT&T0	Terminate Test in Progress **DEFAULT**
AT&T1	Initiate Local Analog Loopback For Time Set by Register S18
AT&T2	Not Defined
AT&T3	Initiate Digital Loopback for Time Set by Register
AT&T4	(Not Supported)
AT&T5	Disable Remote Digital Loopback (RDLB) Response
AT&T6	Initiate RDLB
AT&T7	Initiate RDLB with Self Test
AT&T8	Initiate ALB with Self Test (for Direct / Normal Mode only)
AT&W0	Write User Profile 0 into NVRAM
AT&W1	Write User Profile 1 into NVRAM
AT&X0	Modem Provides Transmit Clock
AT&X1	DTE Supplies Transmit Clock (Not Supported)
AT&X2	Slave Clock Mode (Not Supported)
AT&Y0	Power Up Recall User Profile 0
AT&Y1	Power Up Recall User Profile 1
AT&V	List Configuration both Active and Stored
AT&Z m=An	Store Telephone Number into NVRAM (XL93C46) where: *m* is the number location (0-3) *A* is *P* or *T* (pulse or Tone) *n* is the telephone number

COMMAND	LAPM Yes/No	DESCRIPTION/RANGE - SIZE	FUNCTION
AT \ N0	Y	Normal	
AT \ N1	Y	Direct	
AT \ N2	Y	MNP 2-5/Reliable	
AT \ N3	N	MNP 2-5/Auto Reliable	
AT \ N4	Y	V.42 Mode	
AT \ N5	Y	V.42 Mode Auto Reliable	
AT \ N6	Y	V.42 / MNP 2-5 Reliable	
AT \ N7*	Y	V.42 / MNP 2-5 Auto Reliable	
AT \ A0	N	64 Characters	Transmit Block Size
AT \ A1	N	128 Characters	
AT \ A2	N	192 Characters	
AT \ A3*	N	256 Characters	
AT%An	Y	n = 0-127 ASCII	Auto-Reliable Fallback Character
AT \ L0*	N	Stream Link	Block MNP Link
AT \ L1	N	Block Link \L1 = \L0	(Stream Mode)
AT \ O	N	Initiate Reliable Link After Escape Command Independent of Modem Initial mode (ANS or ORG)	Originate Reliable Link
AT \ U	N	Accept Reliable Link after Escape Command request from Initiator of Link	Accept Reliable Link
AT \ Y	N	Establish Reliable Link after Connecting in Normal Mode	Switch to Reliable Mode
AT \ Z	N	Switch to Normal Mode After Establishing a Reliable Link	Switch to Normal Mode
AT % C0	Y	Compression Disabled	Compression On/Off Control
AT % C1*	Y	Compression Enabled	
AT \ V0	Y	Standard Non-MNP Result Codes	Result Code Form
AT \ V1*	Y	Modified MNP Result Codes (As Listed Below)	
AT \ Bn	Y	N = 0 - 9 (100ms Increments) Used in Normal Mode Default = 3, Error Control Mode Always 300ms	Transmit Break for Normal Data Mode
AT \ C0*	Y	Does not buffer Data Default	Set Auto-Reliable Buffer Break Control
AT \ C1	Y	Buffers All Data on Answering Modem until 200 Characters (Non-Sync) are Returned	
AT \ C2	Y	Does Not Buffer Data on Answering Modem, according to % An to fall back	
AT \ K1	Y	"Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed	Break Control for Reliable Data Mode
AT \ K3	Y	"Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained	

COMMAND	LAPM Yes/No	DESCRIPTION / RANGE - SIZE	FUNCTION
AT \ K5*	Y	"In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break	
AT \ K0,2,4	-	Not Supported (Will be equal to AT \ K5 if selected)	
AT \ Tn	Y	N = 0-90 min N* = 0 (disable)	Inactivity Timer
%D0*	Y	Hang up without clearing buffer	
%D1	Y	Clear the receive buffer before hang up	
- Cn	Y	Maximum String Length(BLTZ) Range: 6-250 Characters Default: 32 Characters	
- Dn	Y	Dictionary Size and One / Two-way Mode(BLTZ), - Dictionary size options 0 - 512 entries, 1 - 1024(1K) entries, *2 - 2048(2K) entries, 3 - 4069(4K) entries	
AT \ I	-	Not Functional	Interface Protocol
AT \ J0*	Y	BPS Rate Adjust Disabled	Speed Conversion Control Disable
AT \ J1	Y	BPS Rate Adjust Enabled	Modem Port Rate Adjustment
AT \ S	Y	List Profiles	
AT \ G0*	Y	Disables Modem Port Flow Control	Set Modem Port
AT \ G1	Y	Sets Modem Port Flow Control to Xon / Xoff	Flow Control
AT \ X0*	Y	Does Not Pass Xon / Xoff to Remote Modem	Xon / Xoff Pass Through Control
AT \ X1	Y	Passes Xon / Xoff to Remote Modem	
AT \ Q0	Y	Disable Flow Control	Serial Port Flow Control
AT \ Q1	Y	Bidirectional Xon / Xoff Enabled	
AT \ Q2*	Y	Unidirectional Hardware Control by CTS	
AT \ Q3	Y	Bidirectional Hardware Control by RTS / CTS	
AT \ Q4	Y	Unidirectional Xon /Xoff Send Only	
AT \ Q5		Keep CTS off until connect unidirectional hardware flow control	
AT \ Q6		Keep CTS off until connect for bidirectional hardware flow control	
AT % U	Y	Not Functional	Clear Serial Port Speed Serial Port
AT - P0*	Y	Ignores Parity for Special Characters	Check Parity
AT - P1	Y	Processes Special Characters Only if they have Correct Parity	

Note: * Denotes Default Condition

See Command AT \ V1 Above

STANDARD RESULT CODES\V0			MODIFIED RESULT CODES \V1	
Verbose	**Numeric**		**Verbose**	**Numeric**
CONNECT	1			
CONNECT 1200	5		CONNECt 1200 / REL 4 or 5	22
CONNECT 2400	10		CONNECT 2400 / REL 4 or 5	23
CONNECT 4800	11			
CONNECT 9600	12		CONNECT 1200/V.42 or V.42bis	22
CONNECT 19200	14		CONNECT 2400/V.42 or V.42bis	23

S	REGISTER FUNCTION
S0	Number of Rings to Answer: **Default** = 0 (no answer)(stored)
S1	Ring Count: Stores Number of Rings: Resets After Every Call
S2	Escape Code Character: **Default** = 043 (ASCII for "+")
S3	Carriage return Character: **Default** = 013
S4	Line Feed Character: **Default** = 010
S5	Back Space Character: **Default** = 008
S6	Wait for Dial Tone: **Default** = 002 (seconds) (minimum setting)
S7	Wait for Carrier After Dial: **Default** = 030 (seconds)
S8	Duration of Delay for Comma: **Default** = 002 (seconds)
S9	Carrier Detect Response Time: **Default** = 0.6 (seconds)
S10	Loss of Carrier Response Time **Default** = 1.4 (seconds)
S11	Touch Tone Duration: **Default** = 095 (milliseconds)
S12	Escape Code Guard Time: **Default** = 1 (second)
S13	Reserved
S14	Bit Mapped Register: Stored in NVRAM (XL93C46) Bit 0 Reserved Bit 1 Echo Bit 2 Result Codes Bit 3 Numeric Result Codes Bit 4 Always 0 Bit 5 Tone/Pulse Dialing Bit 6 Reserved Bit 7 Answer/Originate
S15	Reserved
S16	Test Register Bit 0 ALB Bit 1 Reserved Bit 2 Local Digital Loopback Bit 3 Remote Digital Loopback (Not Supported) Bit 4 Initiate Remote Test Bit 5 Initiate Remote Test With Self Test Bit 6 Analog Loopback With Self Test Bit 7 Reserved
S17	Reserved
S18	Test Time Stored in NVRAM (XL93C46) Default = 000 (seconds)
S19	Reserved
S20	Reserved
S21	Bit Mapped Register Stored in NVRAM (XL93C46) READ ONLY Bit 0 0 = RJ11 Jack Bit 1 Not Used Bit 2 CTS RTS Function Bit 3 DTR Function Bit 4 DTR Function Bit 4 / Bit 3 / Function 0 / 0 / DTR Always True Default 0 / 1 / DTR Off, Forces Command State 1 / 0 / DTR Off, Forces Modem Offline 1 / 1 / Modem Initializes With DTR OFF (ATZ)

REGISTER NUMBER	REGISTER FUNCTION
S22	Bit 5 EIA Carrier Status Bit 6 Bit 7 Guard Tone Select Bit 7 / Bit 6 / Function 0 / 0 / No Guard Tone Default 0 / 1 / 550 Hz Guard Tone 1 / 0 / 1800 Hz Guard Tone 1 / 1 / Reserved Option Bit - Mapped Register Bit 0 Determines Speaker Volume Bit 1 Bit 1 / Bit 0 / Speaker Volume 0 / 0 / Low 0 / 1 / Low 1 / 0 / Medium Default 1 / 1 / High Bit 2 Determines the Speaker Status Bit 3 Bit 3 / Bit 2 / Speaker Status 0 / 0 / Always Off 0 / 1 / On Until Carrier is Detected Default 1 / 0 / Always On 1 / 1 / As '01', Except Off for Dialing Bit 4, 5 and 6 Determine Response Messages Bit 6 / Bit 5 / Bit 4 / Message 0 / 0 / 0 / Basic Message Set 1 / 0 / 0 / Extended with Connect 1200 and Connect 2400 1 / 0 / 1 / Extended with 'No Dial Tone' 1 / 1 / 0 / Extended with 'Busy' 1 / 1 / 1 / Extended with All Messages Default Bit 7 Determines Off Hook/On Hook (Make/Break) Ratio for Pulse Dialing Bit 7 / Ratio 0 / 39/61 (USA and Canada) Default 1 / 33/67 (Uk and Hong Kong)
S23	Option Bit Mapped Register (LSB) Bit 0 Not Supported Bit 3 / Bit 2 / Bit 1 0 / 0 / 0 / 300 0 / 0 / 1 / Not Used 0 / 1 / 0 / 1200 0 / 1 / 1 / 2400 1 / 0 / 0 / 4800 1 / 0 / 1 / 9600 1 / 1 / 0 / 19200 1 / 1 / 1 / 38400(reserved) Bit 4 Determines the Parity for Transmitting and Receiving Data

REGISTER NUMBER	REGISTER FUNCTION
	Bit 5 Bit 5 Bit4 Parity 0 0 Even Default 0 1 Space/None 1 0 Odd 1 1 Mark Bit 6 Determines Guard Tone Frequency Bit 7 (Used in European Applications) Bit 7 Bit 6 Guard Tone (Hz) 0 0 Disabled Default 0 1 550 1 0 1800 1 1 Reserved
S24	Not Used
S25	Delay to DTR (Stored in NVRAM) Default = 005 (seconds)
S26	RTS to CTS Delay (Synchronous Mode Only) Default = 1 (milliseconds)
S27	Bit Mapped Register STORED IN NVRAM Bit 0 Bit 1 Transmission Mode Bit 1 Bit 0 Function 0 0 Asynchronous Mode Default 0 1 Synchronous Mode 1 1 0 Synchronous Mode 2 1 1 Synchronous Mode 3 Bit 2 Reserved Bit 3 Reserved Bit 4 Bit 5 Transmission Mode Bit 5 Bit 4 Function 0 0 Internal Modem Clock Used Default 0 1 DTE Supplied Clock 1 0 Slave Clock Mode 1 1 Same as 00 Bit 6 CCITT or Bell Handshaking Standard 0 CCITT 1 Bell (including CCITT V.22bis) Default Bit 7 Reserved
S28-35	Reserved
S36	Negotiate Failure Fallback (Affected by %C and \N) Bits 0 Hang Up 1 Attempt a standard asynchronous connection (&Q0) 3 Attempt an asynchronous connection using automatic speed buffering (&Q6) 4 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails, attempt a standard asynchronous connection 5 Attempt a V.42 Alternative Protocol connection (MNP compatible); if negotiation fails attempt a standard asynchronous connection

REGISTER NUMBER	REGISTER FUNCTION
S37	Not Supported
S38	Not Supported
S39	Reserved
S40	Not Supported
S41	Not Supported
S43-45	Reserved
S46	Protocol Selection: Bits 136 LAPM only (V.42) 138 V.42bis enable
S47	Not Supported
S48	Feature Negotiation Action 0 Negotiation disabled; presume the remote modem is configured for and has the capabilities necessary for the connection selected with S46 3 Negotiation enabled, but originating modem remains silent during detection phase. For connections with MNP modems; defeats connection sequence with other V.42 modems 7 Negotiation enabled 128 Negotiation disabled; forces fallback options specified in S36 to be taken immediately
S82	Break Handling: Affected by \K commands 3 "Expedited" signaling regardless of its sequence in data sent and received; data integrity maintained 7 "Destructive" signaling regardless of its sequence in data sent and received; data in process at time is destroyed 128 "In sequence" signaling as data is sent and received; data integrity maintained ahead of and after break
S86	Not Supported

Special Notes regarding the use of S registers above S27 and AT/n Commands.

1. Changes of S register values above S27 will effect the profile display for AT/n Commands. AT/n Commands however, do not modify the setting of S registers.

2. It is intended that a user or application software package will use only one method (S register \ n Commands) to effect the error control functions. Use of a combination could result in unpredictable behavior.

"AT + F" COMMANDS

The following are the list of commands supported by the XR-2900. They follow the Aug. 20, 1990 EIA standard PN-2388 (class 2).

All of the commands listed can be used in a string length of up to 40 characters, always preceeded by "AT". For example, "AT&D2E1V0+FCLASS=2<CR>" is a valid command sequence. A semicolon(;) must be used to separate =F commands.

COMMAND	DESCRIPTION	RESPONSE	COMMENTS
+FCLASS =*n*	Establish Class	OK	*n* integer values are 0 or 2 0 for Data mode 2 for FAX mode
+FCLASS=?		0,2	Provides service Class list
+FCLASS?	Service Class Setting	0 or 2	Indicates latest setting
	Default Fax Parameters	OK	Each number's location in the
+FDCC=VR, BR, WD, LN, DF, ER, FT, ST	DCE Capability		string represents the function listed below:
+FDCS=VR, BR, WD, LN, DF, ER, FT, ST	Current Session Parameters	OK	
+FDIS=VR, BR, WD, LN, DF, ER, FT, ST	Parameters for Session	OK	VR Vertical Resolution *0 for 98 dpi (dots/inch) 1 for 196 dpi BR DCE Bit Rate (modulation) 0 = 2400 BPS V.27ter 1 = 4800 BPS V.27 ter 2 = 7200 BPS V.29 *3 = 9600 BPS V.29 WD Page Width *0 = 1728 PIXELS IN 215 mm 1 = 2048 pixels in 255 mm 2 = 2432 pixels in 303 mm 3 = 1216 pixels in 151 mm 4 = 864 pixels in 107 mm LN Page Length *0 = A4, 297 mm 1 = B4, 364 mm 2 = unlimited DF Data Format *0 = 1. D Modified Huffman 1 = Not Supported 2 = Not Supported ER ErrorFree Mode *0 = Disable 1 = Not Supported

COMMAND	DESCRIPTION	RESPONSE	COMMENTS
			FT Binary File Transfer *0 = Disable 1 = Not Supported ST Scan Time 5 = 20 ms
+FLID = "Local ID"	Local FAX ID String	OK	20 character alpha numeric string for identification 0-9 space, +, ASCI 32-127
+FCR = 0	Capability to Receive	OK	DCE will not receive, but will
+FCR = 1		OK	answer and handshake
+FCQ = 0,1	Copy Quality	OK	n = 2 , Not Supported
+FBUG = 0, 1	Debug Mode: HDLC Frame	OK	
FMINSP = 0, 1, 2, 3	Minimum Transmit Speed	OK	0: 2400, 1: 4800, 2: 7200, 3: 9600
+FBOR = 0	Bit Order (DCE to DTE)	OK	MSB First
+FBOR = 1		OK	LSB First
+FDR	Begin Phase C Reception	CONNECT	Beginning of file is noted by DC2(12H) character
+FAA = 0	Auto Answer Mode	OK	FAX only communication
+FAA = 1		OK	Auto Fax/Data determination
+FDT =	Begin Sending Page	CONNECT	Marks beginning of Phase C data
+FHPS=0, 1	Handshake Protocol	OK	0: OK 1: Error
+FET=0,2	End of page	OK	1: Not Supported Indicates additional pages if any 0 for another page no parameter changes

RESPONSES from XR-2900 FIRMWARE:

The following lists valid responses to be expected from the XR-2942 firmware. The standardization of these responses allows the Application software to verify that a particular mode has been entered and monitoring of the fax transmission or reception process is easier.

RESPONSE	DESCRIPTION	COMMENTS
+FCON	FAX connection	Occurs after V.21 flags received
+FCSI:	Called Station ID	Report ID being Received (originate)
+FTSI:	Transmit Station ID	
+FDIS:	Session Negotiation Parameters	Uses format shown in Commands Section
+FDCS:	Report of DCS Frame Information	The Format is the same as +FDIS command
+FET:0, 2	Post Page Message Response	0: Another Page coming same document 1: Not Supported 2: No more pages or documents
+FPTS: 1, 2		1: Message Confirmation 2: Bad quality
+FHNG: 0	Call terminated status	Normal and proper connections

APPLICATIONS INFORMATION

The XR-2943 is shown in a typical 'stand-alone' application in the modem schematic. The XR-2943 provides the command controller function for the XR-2900 Fax/Data modem chip set yielding a high quality modem. For data operation the modem operates error-free through LAPM or MNP 2-4 modes and can offer increased throughput with V.42bis or MNP 5. The XR-2321 adds CCITT V.21 and V.23 FSK modes, it is optional and can be eliminated for designs not requiring these modes.

Detailed information for the XR-2900 is available in XR-2900 Fax/Data modem chip set datasheet.

Layout Hints

In order for the XR-2943 to provide optimal support for best performance of the modem, some design hints/rules should be followed.

- Locate the XR-2902 AFE near the DAA section
  - provide for a short transmit / receive carrier input path, away from any digital control lines.
- Maintain separate analog and digital grounds/power lines back to the power supply source.
- Bypass (capacitor decouple) the XR-2901, XR-2902, XR-2943 and op amp power supplies with both 0.01µF ceramic and 0.47µF tantalum capacitors near their actual pins. Ensure analog/digital supplies are bypassed to their respective ground.
- Crystal - parallel resonant type. Typical loading capacitors are 18pF.

SYSTEM PERFORMANCE

Performance for an error-correcting modem has two major areas.

1) DATA PUMP PERFORMANCE
With error-detection capabilities turned off, the integrity of the data pump to pass data in the presence of impairments. Most often the major specification measured here is the probability of data errors with the receive carrier impaired by noise, or BER (bit error rate) vs S/N (Signal-to-Noise ratio).

Figure 8 shows BER vs S/N for the circuit in Figure 12, as measured with the test set-up in Figure 9.

2) ERROR CONTROLLER PERFORMANCE
The XR-2943, when in LAPM or MNP modes provides the control and detection required to yield perfect data transfer (Data Modem mode).

Beyond error correction, throughput, or data transfer rate, is another important parameter to the modems overall performance.

LAPM and MNP 2-4 Modes are not specifically provided for increased throughput. However an additional benefit of their error-detecting schemes is roughly a 20% increase in throughput. Using the 'Quick Brown Fox....' pattern, both LAPM and MNP 4 modes yielded better than a 20% throughput increase. V.22bis mode was used for this test, with an actual throughput of better than 2900 BPS measured.

MNP 5 Data Compression Included in the XR-2943 allows roughly a 100% throughput increase over the modems nominal data rate. As previously discussed, the throughput performance of MNP 5 varies with different types of data. (Figure 10 shows data for various data patterns). (Figure 11 illustrates the test set-up used for measuring the circuit of Figure 12).

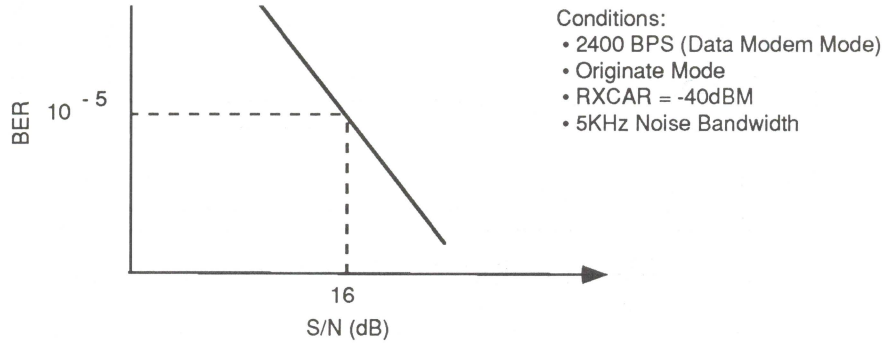


Figure 8. 2400 BPS Data Mode BER vs S/N (Non-Error Correcting)

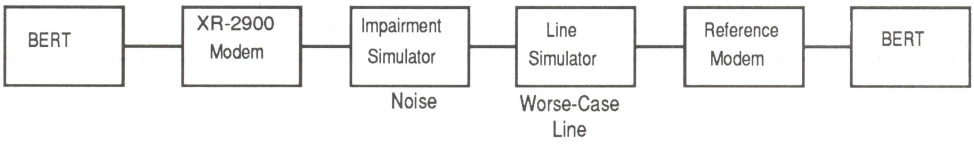


Figure 9. Data Quality Test Set-up

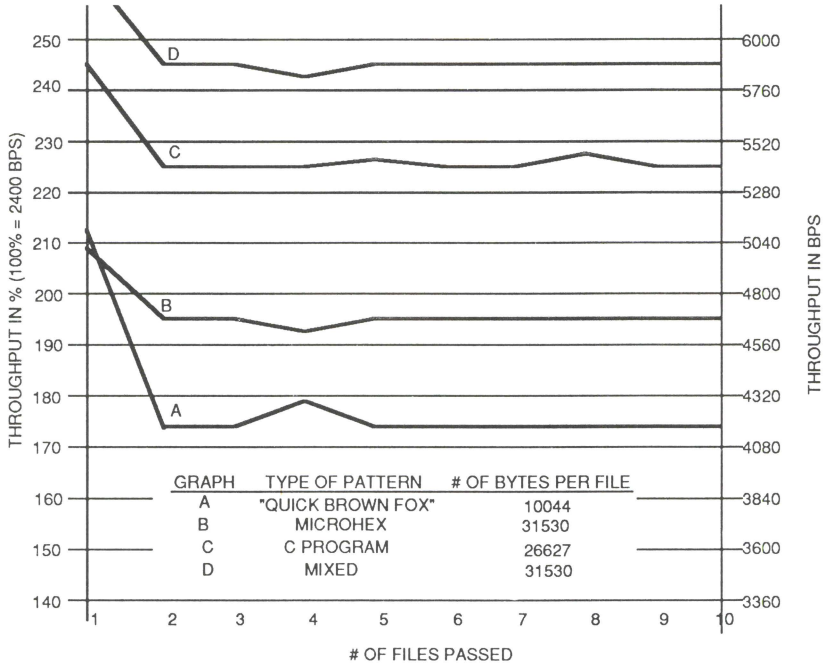
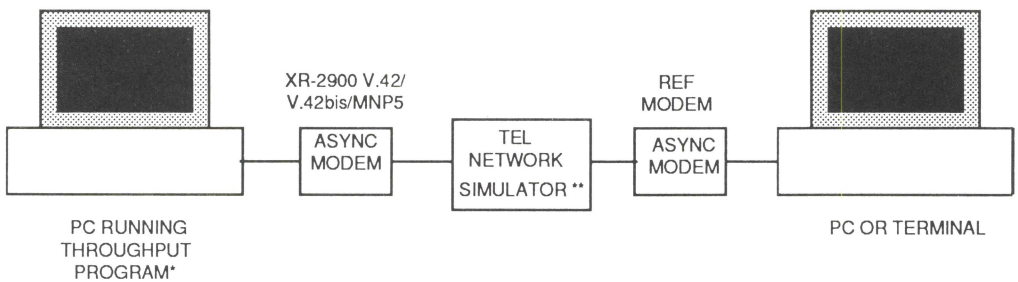


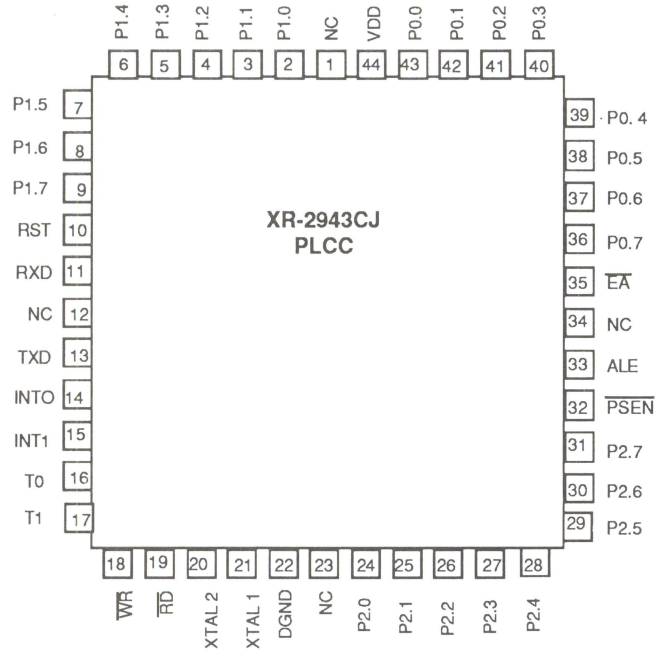
Figure 10. Effective Data Throughput For MNP5

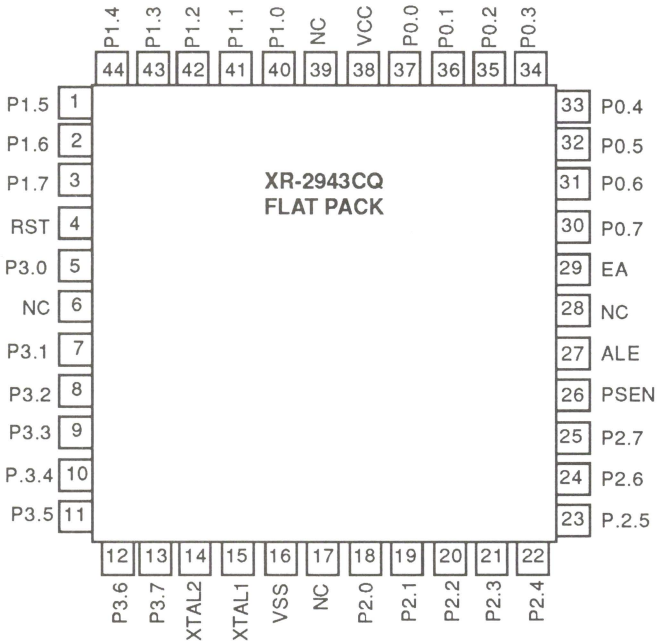


* APT (asynchronous Performance Tester), also contains data or files to be used during measurement. Productof Concord Data Systems.

** Simulates line impairment and attenuation condi tions.

Figure 11. MNP5 Throughput Measurement Test (Data Mode)


XR-2943CJ
PLCC
P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0 43
P0.1 42
P0.2 41
P0.3 40
P1.5 7
P1.6 8
P1.7 9
RST 10
RXD 11
NC 12
TXD 13
INTO 14
INT1 15
T0 16
T1 17
39 P0. 4
38 P0.5
37 P0.6
36 P0.7
35 EA
34 NC
33 ALE
32 PSEN
31 P2.7
30 P2.6
29 P2.5
18 WR
19 RD
20 XTAL 2
21 XTAL 1
22 DGND
23 NC
24 P2.0
25 P2.1
26 P2.2
27 P2.3
28 P2.4


XR-2943CQ
FLAT PACK
P1.4 44
P1.3 43
P1.2 42
P1.1 41
P1.0 40
NC 39
VCC 38
P0.0 37
P0.1 36
P0.2 35
P0.3 34
P1.5 1
P1.6 2
P1.7 3
RST 4
P3.0 5
NC 6
P3.1 7
P3.2 8
P3.3 9
P.3.4 10
P3.5 11
33 P0.4
32 P0.5
31 P0.6
30 P0.7
29 EA
28 NC
27 ALE
26 PSEN
25 P2.7
24 P2.6
23 P.2.5
12 P3.6
13 P3.7
14 XTAL2
15 XTAL1
16 VSS
17 NC
18 P2.0
19 P2.1
20 P2.2
21 P2.3
22 P2.4



NOTES



Asynchronous Receiver and Transmitter (UART)

GENERAL DESCRIPTION

The XR-16C450 is an universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56KHz, The XR-16C450 is fabricated in an advanced 2μ CMOS process to achieve low power, and high speed requirements.

FEATURES

Pin to pin and functionally compatible to INS8250, NS16C450
Modem control signals (CTS~,RTS~, DSR~, DTR~, R1~, DCD~)
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs, outputs

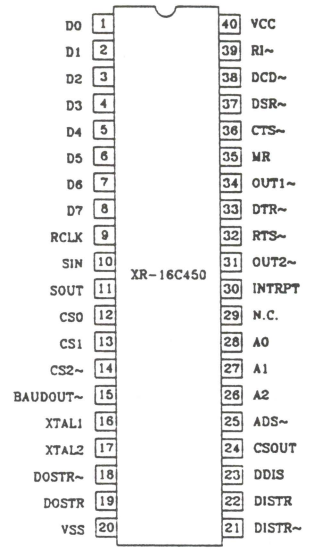
APPLICATIONS

RS232 receiver or transmitter
Serial to parallel / parallel to serial converter
Modem hand-shaking

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	7V
Voltage at any Pin	V_{SS} -0.3V to V_{CC} +0.3V
Storage Temperature	-55°C to +150°C
Power Dissipation	80 mW

PIN ASSIGNMENT



For other pin assignments, refer to the end of this datasheet

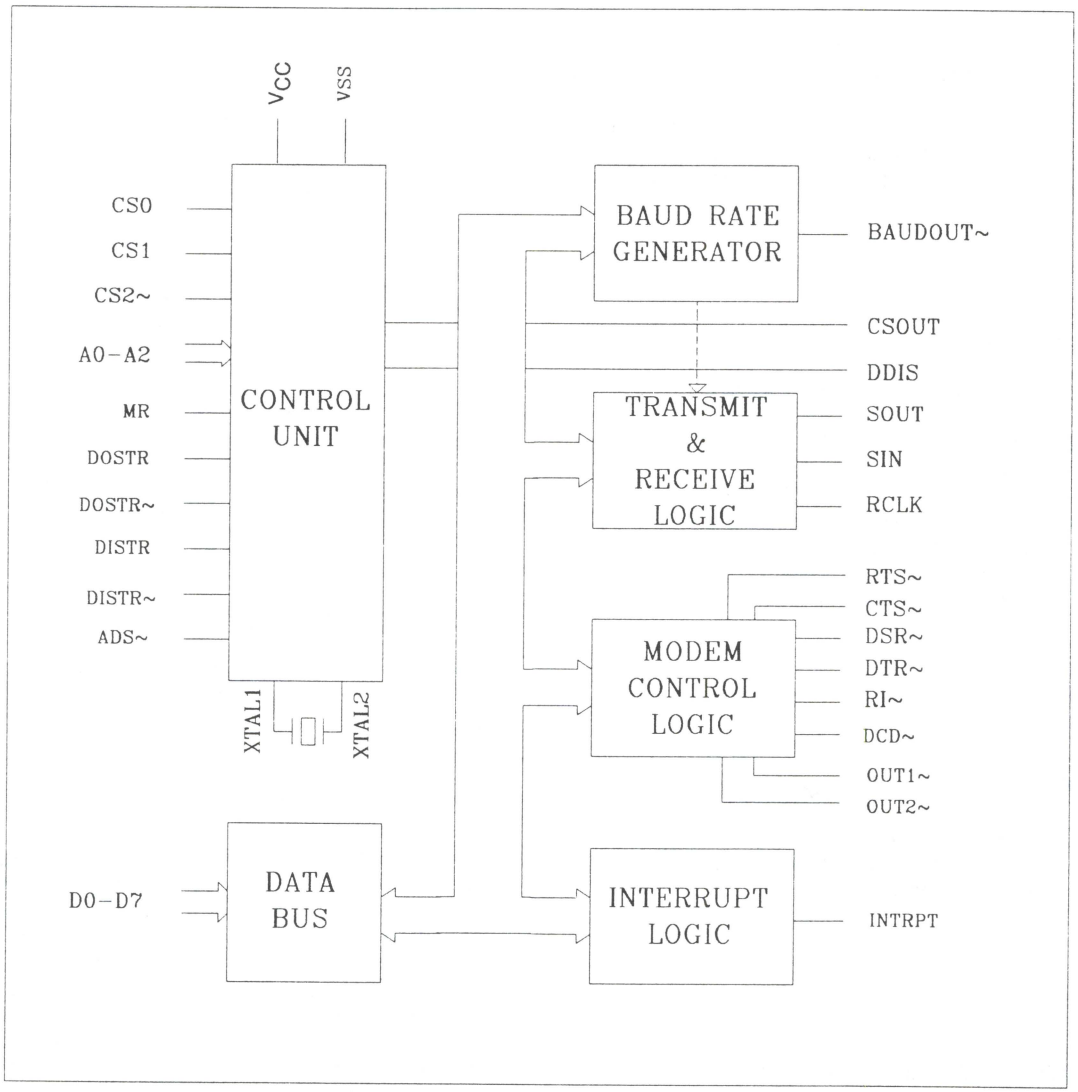
ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-16C450CP	Plastic DIP	0°C to +70°C
XR-16C450CJ	PLCC	0°C to +70°C

SYSTEM DESCRIPTION

The XR-16C450 is an improved version of the INS8250/ NS16C450 UART with higher speed operating access time. The XR-16C450 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on-board status registers will provide the error conditions, as well as type and status of the transfer operations being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the users requirements to minimize the computing required to handle the communications link. The XR- 16C450 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
D0-D7	1-8	I/O	**Bidirectional data I/0.** Eight bit, three-state data bus to transfer information to or from the CPU. D0 Is the least significant bit (LSB) of the data bus and is the first serial data bit to be received or transmitted.
RCLK	9	I	**Receive clock Input.**The external clock input to the XR-16C450 receive section, as well as baud rate divisor input.
SIN	10	I	**Serial data input.** The serial Information (data) received from MODEM or RS232 to XR-16C450 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SIN input is disabled from external connection and connected to the SOUT output internally.
SOUT	11	O	**Serial data output.** The serial data is transmitted via this pin with additional start, stop and parity bits. The SOUT will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	**Chip select 1 (active high).** A high at this pin (while CS1 = 1 and CS2 ~ = 0) will enable the UART / CPU data transfer operation.
CS1	13	I	**Chip select 2 (active high).** A high at this pin (while CSO = 1 and CS2 ~ = 0) will enable the UART / CPU data transfer operation.
CS2~	14	I	**Chip select 3 (active low).** A low at this pin (while CSO = 1 and CS1 = 1) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	I	**Baud rate generator clock output.** This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	**Crystal input 1 or external clock input.** A crystal (parallel resonant) can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock the internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	**Crystal input** 2. See XTAL1.
DOSTR~	18	I	**I/O write strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the UART.
DOSTR	19	I	**I/O write strobe.** (active high) Same as DOSTR~, but uses active high input. Note that only an active DOSTR ~ or DOSTR input is required to transfer data from CPU to XR-16C450 during write operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or VSS(DOSTR ~ =VCC or DOSTR =VSS).
VSS	20	O	**Signal and power ground.**
DISTR~	21	I	**I/O read strobe (active low).** A low level on this pin (while CS0 = 1, CS1 = 1 and CS2 ~ = 0) will transfer the contents of the XR-16C450 data bus to the CPU.

PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
DISTR	22	I	**I/O read strobe (active high).** Same as DISTR~, but uses active high input. Note that only an active DISTR~ or DISTR input is required to transfer data from XR-16C450 to CPU during read operation (while CSO = 1, CS1 = 1 and CS2 ~ = 0). The unused pin should be tied to V_{CC} or V_{SS} (DISTR ~ = V_{CC} or DISTR = V_{SS}).
DDIS~	23	O	**Drive disable (active low).** This pin goes low when CPU is reading data from XR-16C450 to disable the external transceiver or logic.
CSOUT	24	O	**Chip select out.** A high on this pin indicates that the chip has been selected by the chip select input pins.
ADS~	25	I	**Address strobe (active low).** A low on this pin will latch the state of the chip selects and addressed register. A rising edge is required if register and chip select pins are not stable during read and write operation.
A2	26	I	**Address line 2.** To select internal registers.
A1	27	I	**Address line 1.** To select internal registers.
A0	28	I	**Address line 0**. To select Internal registers.
INTRPT	30	O	**Interrupt output (active high).** This pin goes high (when enabled by the Interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
OUT2~	31	O	**General purpose output (active low).** User defined output. See bit-3 of the modem control register (BIT-3 = 1 makes OUT2 ~ = 0).
RTS~	32	O	**Request to send (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset, this pin will be set to high.
DTR~	33	O	**Data terminal ready (active low).** To indicate that XR-16C450 is ready to receive data. This pin can be controlled via the modem control regis ter (MCR bit-0). Writing a "1" to the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
OUT1~	34	O	**General purpose output (active low).** User defined output. See bit-2 of modem control register (BIT-2 = 1 makes OUT1 ~ = 0).
MR	35	I	**Master reset (active high).** A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
CTS~	36	I	**Clear to send (active low).** The CTS~ is a modem control input. It's startup can be tested by reading the MSR Bit-4. CTS~has no effect on the transmitter output.
DSR~	37	1	**Data set ready(active low).** A low on this pin indicates that MODEM is ready to exchange data with UART.
DCD~	38	1	**Carrier detect (active low).** A low on this pin indicates that carrier has been detected by the modem.
Ri~	39	1	**Ring detect indicator (active low).** A low on this pin indicates that the modem has received a ringing signal from the telephone line.
V_{CC}	40	1	**Positive power supply input.**

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
X	0	1	0	Interrupt Status Register	
X	0	1	1		Line Control Register
X	1	0	0		Modem Control Register
X	1	0	1	Line Status Register	
X	1	1	0	Modem Status Register	
X	1	1	1	Scratch-pad Register	Scratch-pad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}= 5.0V 110%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
T_1	Address strobe width	30			ns	
T_2	Address setup time	30			ns	
T_3	Address hold time	5			ns	
T_4	Chip select setup time	25			ns	
T_5	Chip select hold time	0			ns	
T_6	DISTR/DISTR ~ strobe width	75			ns	
T_7	Read cycle delay	50			ns	
T_8	Read cycle = $T_{20} + T_6 + T_7$	135			ns	
T_9	DISTR/DISTR ~ to drive to disable delay			35	ns	100 pF load
T_{10}	Delay from DISTR/DISTR ~ to data			75	ns	100 pF load
T_{11}	DISTR/DISTR ~ to floating data delay	0		50	ns	100 pF load
T_{12}	DOSTR/DOSTR ~ strobe width	50			ns	
T_{13}	Write cycle delay	55			ns	
T_{14}	Write cycle = $T_1 + T_{12} + T_{13}$	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{17}	Chip select output delay from select			50	ns	100 pF load
T_{18}	Address hold time from DISTR/DISTR ~	0			ns	Note: 1
T_{19}	Chip select hold time from DISTR/DISTR ~	0			ns	Note: 1
T_{20}	DISTR/DISTR ~ delay from address	10			ns	Note: 1
T_{21}	DISTR/DISTR ~ delay from chip select	10			ns	Note: 1
T_{22}	Address hold time from DOSTR/DOSTR ~	5			ns	Note: 1
T_{23}	Chip select hold time from DOSTR/DOSTR ~	5			ns	Note: 1
T_{24}	DOSTR/DOSTR ~ delay from address	25			ns	Note: 1
T_{25}	DOSTR/DOSTR ~ delay from select	10			ns	Note: 1
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock
TRANSMITTER						
T_{29}	Delay from rising edge of DOSTR/DOSTR ~ to reset interrupt			75	ns	100 pF load

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
T_{30}	Delay from initial INT reset to transmit start	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{32}	Delay from stop to next start			100	ns	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from DISTR/DISTR ~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{35}	Delay from DOSTR/ DOSTR ~ to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from DISTR/DISTR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		$2^{16}-1$		
T_{38}	Baud out negative edge delay			100	ns	100 pF load
T_{39}	Baud out positive edge delay			100	ns	100 pF load
T_{40}	Baud out down time	425			ns	100 pF load, Note: 2
T_{41}	Baud out up time	250			ns	100 pF load, Note: 2
RECEIVER						
T_{42}	Delay from RCLK to sample time			500	ns	
T_{43}	Delay from stop to set interrupt			1Rclk	ns	100 pF load
T_{44}	Delay from DISTR/DISTR ~ to reset interrupt			200	ns	100 pF load

Note 1: Applicable only when ADS ~ is tied low
Note 2: Fx = 3.1 MHz clock
* Baudout ~ cycle

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}= 5.0V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH} = -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER (THR & RHR)

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register. Writing to this register will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit,the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

XR-16C450 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	OP2~	OPI~	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

INTERRUPT ENABLE REGISTER (IER)
The Interrupt enable register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero

INTERRUPT STATUS REGISTER (ISR)

The XR-16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle, the XR-16C450 provides the highest interrupt level to be serviced by CPU, no other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR (Receiver Line Status Register)
2	RXRDY (Received Data Ready)
3	TXRDY (Transmitter holding register empty)
4	MSR (Modem Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:

These bits are not used and are set to zero.

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length and number of the stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:

The number of stop bits can be specified by this bit.
0=1 stop bit, when word length=5, 6, 7, 8 bits
1=1 and 1 /2 stop bit, when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:

Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data, receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the stick parity format.
0=parity bit is forced to "1" in the transmitted and received data.
1=parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit.
1=forces the transmitter output (SOUT) to go low to alert the communication terminal.
0=normal operating condition.

LCR BIT-7:

The internal baud rate counter latch enable(DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR ~ output to high.
1=force DTR ~ output to low.

MCR BIT-1:

0=force RTS ~ output to high.
1=force RTS ~ output to low.

MCR BIT-2:

0=set OUT1 output to high.
1=set OUT1 output to low.

MCR BIT -3:
0=set OUT2~ output to high.
1=set OUT2~ output to low.

MCR BIT -4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (SOUT) is set high (mark condition), the Receiver input (SIN), CTS~, DSR~, DCD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OUT1~ and OUT2~ are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupt are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to the CPU.

LSR BIT-0:
0=no data in receive holding register.
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received data did not have a valid stop bit.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (SIN was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. XR-16C450 will not accept any data for transmission.
1 =transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the DCD~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS~ in the MCR during loop mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR~ the MCR during loop mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OUT1~ in the MCR during loop mode. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OUT2~ in the MCR during loop mode. It is the compliment to the DCD~ input.

SCRATCH-PAD REGISTER (SR)
XR-16C450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

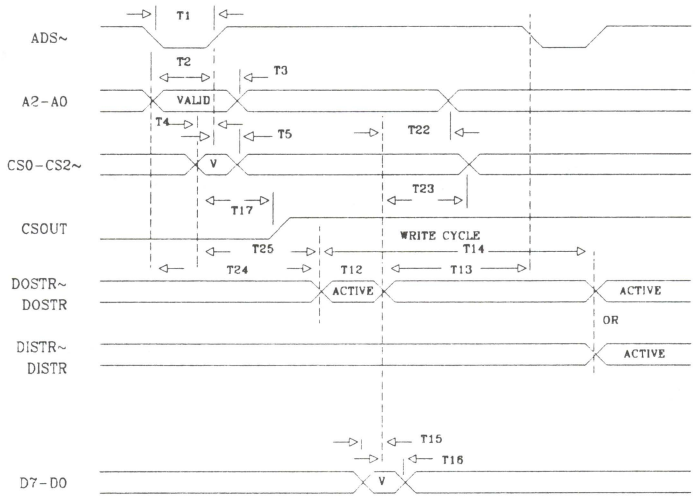
XR-16C450 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1, LSR BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
SOUT	High
OUT1~	High
OUT2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

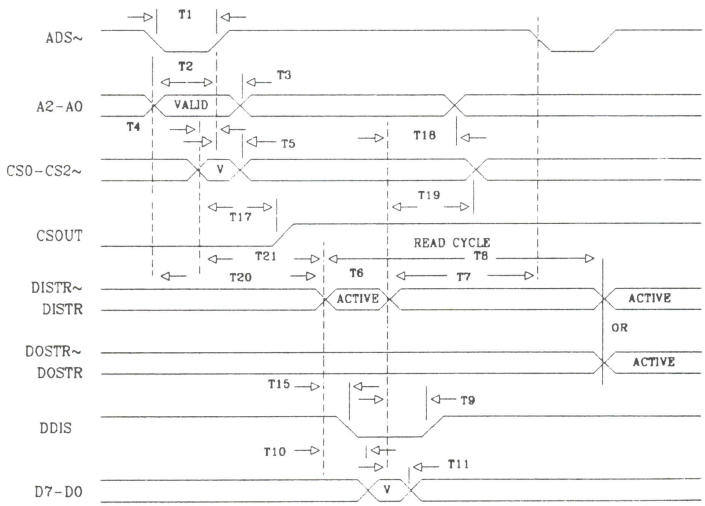
TIMING DIAGRAM

WRITE CYCLE TIMING



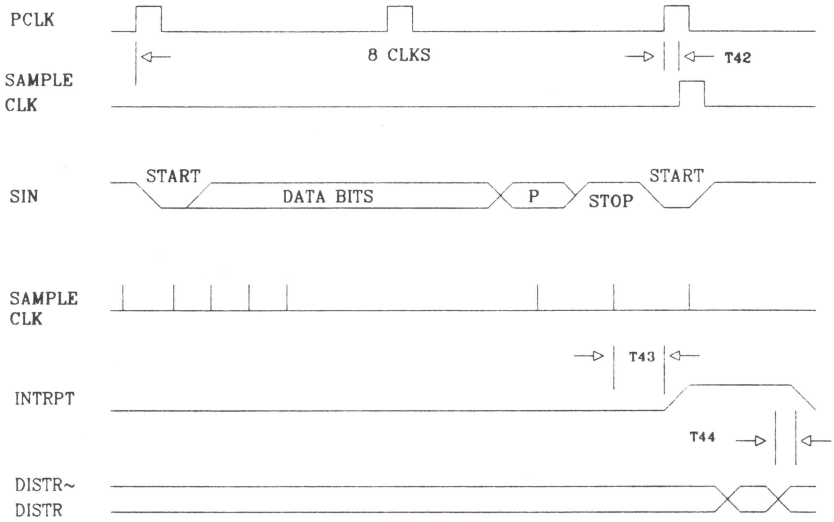
V = VALID
A = ACTIVE
P = PARITY

READ CYCLE TIMING

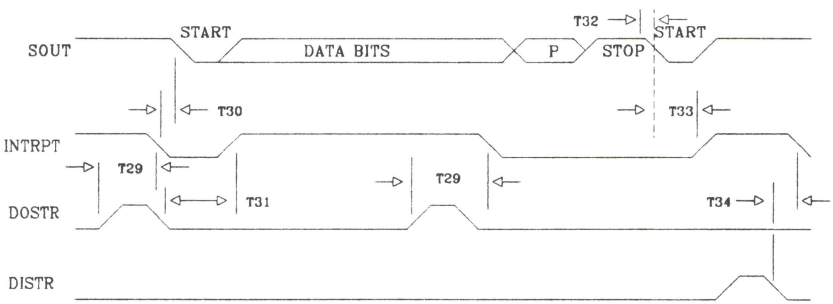


TIMING DIAGRAM

RECEIVER TIMING

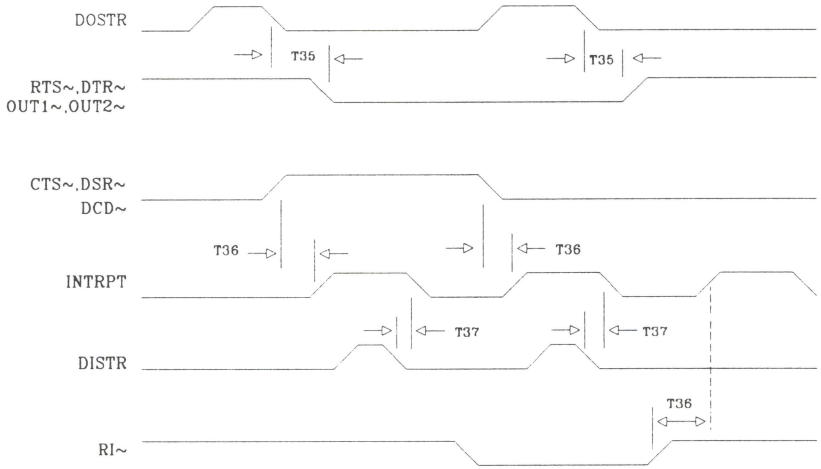


TRANSMITTER TIMING

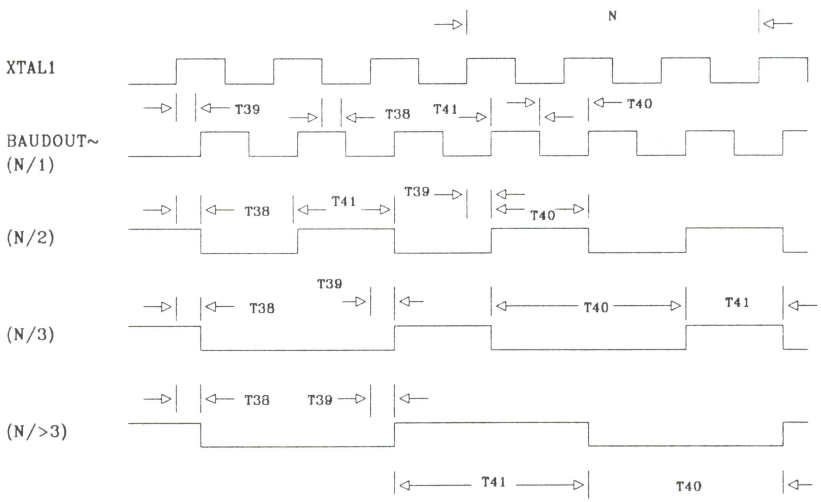


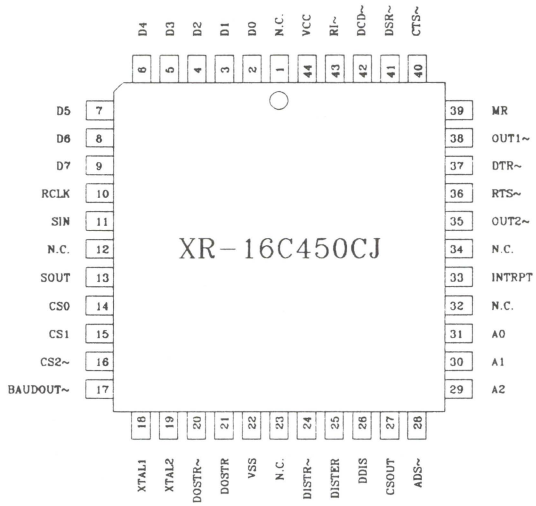
TIMING DIAGRAM

MODEM TIMING



BAUDOUT~ TIMING




D4 6
D3 5
D2 4
D1 3
D0 2
N.C. 1
VCC 44
RI~ 43
DCD~ 42
DSR~ 41
CTS~ 40
D5 7
D6 8
D7 9
RCLK 10
SIN 11
N.C. 12
SOUT 13
CS0 14
CS1 15
CS2~ 16
BAUDOUT~ 17
XR-16C450CJ
39 MR
38 OUT1~
37 DTR~
36 RTS~
35 OUT2~
34 N.C.
33 INTRPT
32 N.C.
31 A0
30 A1
29 A2
18 XTAL1
19 XTAL2
20 DOSTR~
21 DOSTR
22 VSS
23 N.C.
24 DISTR~
25 DISTER
26 DDIS
27 CSOUT
28 ADS~

Dual Universal Asynchronous Receiver and Transmitter with Parallel Printer Port

GENERAL DESCRIPTION

The XR-16C452 is a dual universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The XR-16C452 is fabricated on an advanced 1.2µm CMOS process to achieve low power consumption and high speed operation.

FEATURES

Pin-to-pin and functionally compatible to VL16C452
Fully compatible with all new bidirectional PS/2 printer port registers
Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs, outputs
Direct replacement of logic for PC/XT/AT
High data transfer rate 448 kHz transmit/receive operation with 7.372MHz external clock source
Bidirectional CENTRONICS printer port
Enhanced current drive capability on all I/O ports

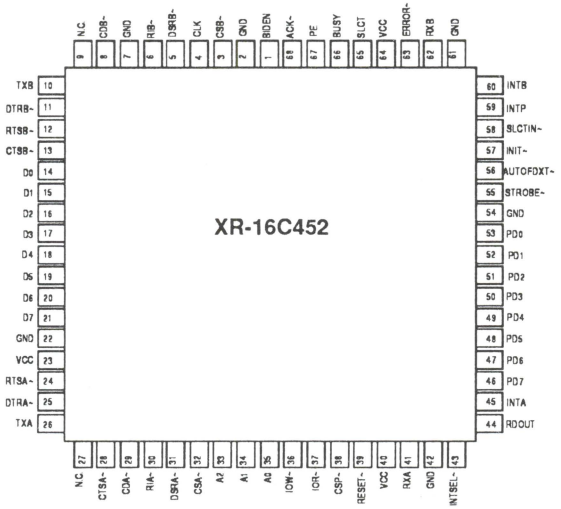
APPLICATIONS

Dual RS232 receiver and/or transmitter
Serial to parallel / parallel to serial converter Modem handshaking
CENTRONICS printer port
IBM PS/2 bidirectional printer port
External bidirectional I/O
IBM PC/XT/AT upgrade printer port

ABSOLUTE MAXIMUM RATINGS

Operating Supply Range	5 Volts ± 5%
Voltage at any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	0° C to +70° C
Storage Temperature	-40° C to +150° C
Package Dissipation	500 mW

PIN ASSIGNMENT



ORDERING INFORMATION

Part number	Package	Operating Temperature
XR-16C452CJ	PLCC	0° C to +70° C

SYSTEM DESCRIPTION

The XR-16C452 is an improved version of the VL16C452 with higher operating speed and lower access time. The XR-16C452 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The XR-16C452 also provides the user with a bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on chip status registers will provide the error conditions, as well as the type and status of the transfer operations being performed. The XR-16C452 also has a complete MODEM control capability, and a processor interrupt system. The latter may be software tailored to the user's requirements there-by allowing the user to minimize the computing time required to service the communications link. The XR-16C452 can interface easily to most popular microprocessors and communications link faults can be detected with an internal loop-back capability.

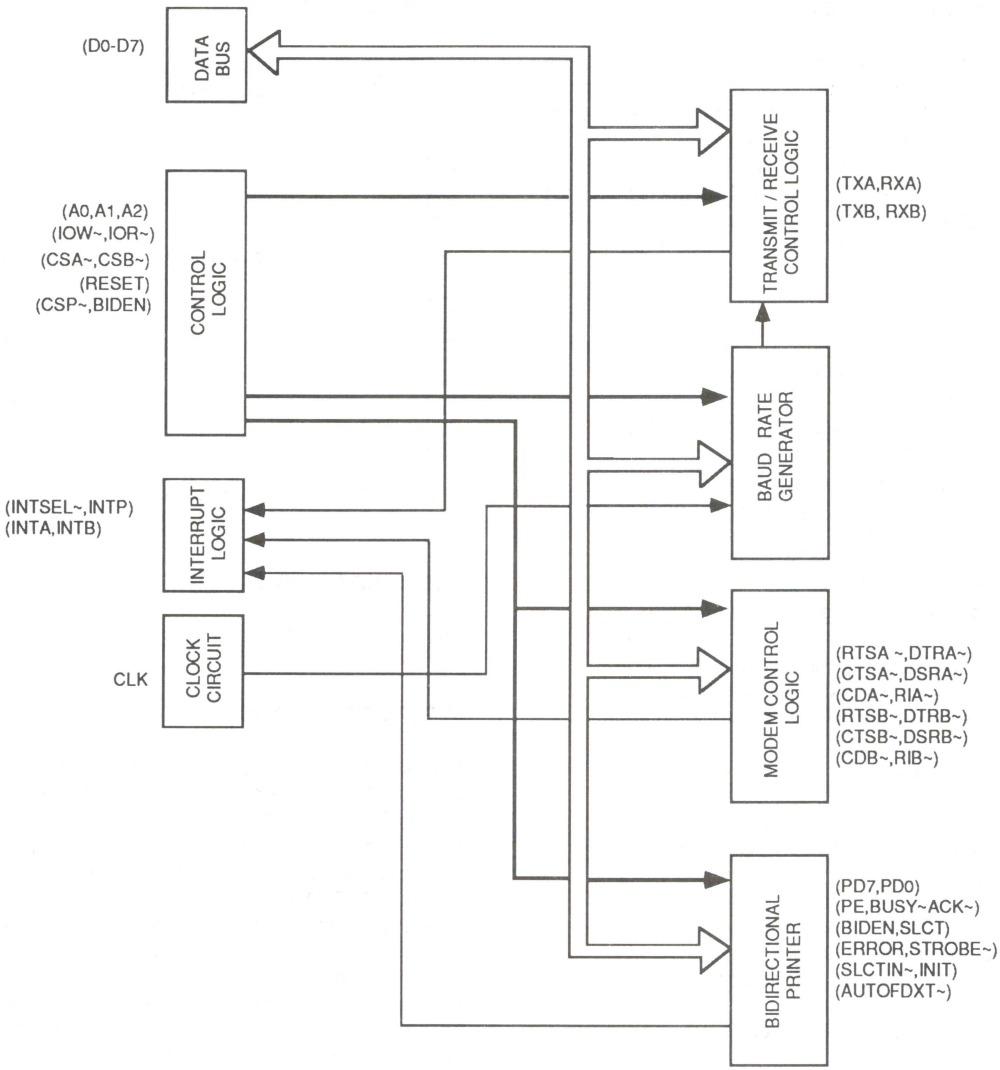


Figure 1. Block Diagram

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25° C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
VILCK	Clock input low level	-0.5		0.6	V	
VIHCK	Clock input high level	3.0		VCC	V	
VIL	Input low level	-0.5		0.8	V	
VIH	Input high level	2.2		VCC	V	
VOL	Output low level			0.4	V	IOL= 6.0 mA D7-D0 IOL= 20.0 mA PD7-PD0 IOL= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ IOL= 6.0 mA on all other outputs
VOH	Output high level	2.4			V	IOH= -6.0 mA D7-D0 IOH= -12.0 mA PD7-PD0 IOH= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ IOH= -6.0 mA on all other outputs
ICC	Avg power supply current			12	mA	
IIL	Input leakage			±10	µA	
ICL	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T1	Clock high pulse duration	55			ns	
T2	Clock low pulse duration	55			ns	External clock
T3	Clock rise/fall time					
T12	Address hold time from IOW~	20			ns	
T13	IOW~ delay from address	25			ns	
T14	IOW~ delay from chip select	10			ns	
T15	IOW~ strobe width	50			ns	
T16	Chip select hold time from IOW~	5			ns	
T17	Write cycle delay	55			ns	
TW	Write cycle=T15+T17	135			ns	
T18	Data setup time	20			ns	
T19	Data hold time	25			ns	
T20	Address hold time from IOR~	0			ns	
T21	IOR~ delay from address	10			ns	
T22	IOR~ delay from chip select	10			ns	
T23	IOR~ strobe width	75			ns	
T24	Chip select hold time from IOR~	0			ns	
T25	Read cycle delay	50			ns	
TR	Read cycle=T23+T25	135			ns	
T26	Delay from IOR~ to data			75	ns	100 pF load
T27	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ±5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
MODEM CONTROL						
T28	Delay from IOW~ to output			50	ns	100 pF load
T29	Delay to set interrupt from MODEM input			70	ns	100 pF load
T30	Delay to reset interrupt from IOR			70	ns	100 pF load
RECEIVER						
T31	Delay from stop to set interrupt			1 Rclk	ns	100 pF load
T32	Delay from IOR~ to reset interrupt			200	ns	100 pF load
TRANSMITTER						
T33	Delay from initial INT reset to transmit start	8		24		
T34	Delay from stop to interrupt			100	ns	
T35	Delay from IOW~ to reset interrupt			125	ns	
T36	Delay from initial Write to interrupt	16		24		
T37	Delay from IOR~ to reset interrupt			75	ns	100 pF load
PRINTER PORT						
T38	Delay from rising IOW~ to output data.	5			ns	
T39	ACK~ pulse width	75			ns	
T40	PD7 - PD0 setup time	10			ns	
T41	PD7 - PD0 hold time	25			ns	
T42	Delay from ACK~ low to interrupt high.	5			ns	
T43	Delay from IOR~ to reset interrupt	5			ns	

PIN DESCRIPTION

Pin#	Symbol	Type	Description
1	BIDEN	I	**Printer Direction Select.** A high puts the parallel port in the software controlled mode (input / output). A low puts the parallel port in the out mode.
3	CSB~	I	**Chip Select B (active low).** A low at this pin (while CSA~ and CSP~ =1) will enable the UARTB / CPU data transfer operation.
4	CLK	I	**External Clock Input.** An external clock can be used to clock the internal circuit and the baud rate generator for custom and standard transmission rates.
5	DSRB~	I	**Data Set Ready B (active low).** A low on this pin indicates that MODEM B is ready to exchange data with UARTB.
6	RIB~	I	**Ring Detect B Indicator (active low).** A low on this pin indicates that MODEM B has received a ringing signal from the telephone line.
8	CDB~	I	**Carrier Detect B (active low).** A low on this pin indicates that carrier has been detected by the MODEM B.
10	TXB	O	**Serial Data Output B.** The serial data is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loop-back mode or when the transmitter is disabled.
11	DTRB~	O	**Data Terminal Ready B (active low).** To indicate that XR-16C452 is ready to receive data. This pin can be controlled via the modem control register (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
12	RTSB~	O	**Request to Send B (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
13	CTSB~	I	**Clear to Send B (active low).** The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
14-21	D0-D7	I/O	**Bidirectional Data Bus.** Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
24	RTSA~	O	**Request to Send A (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

Pin#	Symbol	Type	Description
25	DTRA~	O	**Data Terminal Ready A (active low).** To indicate that XR-16C452 is ready to receive data. This pin can be controlled via the modem control register (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
26	TXA	O	**Serial Data Output A.** The serial data is transmitted via this pin with additional start, stop and parity bits. The TXA will be held in mark (high) state during reset, local loop-back mode or when the transmitter is disabled.
28	CTSA~	I	**Clear to Send A (active low).** The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
29	CDA~	I	**Carrier Detect A (active low).** A low on this pin indicates that carrier has been detected by the MODEM A.
30	RIA~	I	**Ring Detect A indicator (active low).** A low on this pin indicates that MODEM A has received a ringing signal from the telephone line.
31	DSRA~	I	**Data Set Ready A (active low).** A low on this pin indicates that MODEM A ready to exchange data with UART A.
32	CSA~	I	**Chip Select A (active low).** A low at this pin (while CSB~ and CSP~ =1) will enable the UARTA / CPU data transfer operation.
33	A2	I	**Address Line 2.** To select internal registers.
34	A1	I	**Address Line 1.** To select internal registers.
35	A0	I	**Address Line 0.** To select internal registers.
36	IOW~	I	**Write Strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the addressed register.
37	IOR~	I	**Read Strobe (active low).** A low level on this pin will transfer the contents of the XR-16C452 data bus to the CPU.
38	CSP~	I	**Chip Select P (active low).** To enable the XR-16C452 printer operation, this pin has to go low while CSA~ and CSB~ are high.
39	RESET~	I	**Master Reset (active low).** A low on this pin will reset all the outputs and internal registers. The parallel port of the XR-16C452 will be set to mode, the transmitter output and the output receiver input will be disabled during reset time.

Pin#	Symbol	Type	Description
41	RXA	I	**Serial Data Input A.** The serial information (data) received from MODEM or RS232 to XR-16C452 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode RXA input is disabled from external connection and connected to the TXA output internally.
43	INTSEL~	I	**Interrupt Select (active low).** The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to VCC, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
44	RDOUT	O	**Read Select Out.** A high on this pin indicates that the chip is being read by the CPU.
45	INTA	O	**UART A Interrupt Output (three state).** This pin goes high (when enabled by MCRA BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
46-53	PD7-PD0	I/O	**Bidirectional Parallel Ports (three state).** To transfer data in or out of the XR-16C452 parallel port. PD7-PD0 are latched during output mode.
55	STROBE~	I/O	**General Purpose I/O or Strobe Output (open drain, active low).** To transfer latched data to the external peripheral or printer.
56	AUTOFDXT~	I/O	**General Purpose I/O or Line Printer Autofeed (open drain, active low).** To signal the printer for continuous form feed.
57	INIT~	I/O	**General Purpose I/O or Line Printer Initialize (open drain, active low).** To signal the line printer to enter internal initialization routine.
58	SLCTIN~	I/O	**General Purpose I/O or Line Printer Select (open drain, active low).** To select the line printer.
59	INTP	O	**Printer Interrupt Output (active high).** To signal the state of the printer port.
60	INTB	O	**UART B Interrupt Output (three state).** This pin goes high (when enabled by MCRB BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
62	RXB	I	**Serial Data Input B.** The serial information (data) received from MODEM or RS232 to XR-16C452 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXB input is disabled from external connection and connected to the TXB output internally.
63	ERROR~	I	**General Purpose Input or Line Printer Error (active low).** This is an output from the printer to indicate an error by holding it low during error condition.

Pin#	Symbol	Type	Description
65	SLCT	I	**General Purpose Input or Line Printer Selected (active high).** This is an output from the printer to indicate that the line printer has been selected.
66	BUSY	I	**General Purpose Input or Line Printer Busy (active high).** An output from the printer to indicate printer is not ready to accept data.
67	PE	I	**General Purpose Input or Line Printer Paper Empty (active high).** An output from the printer to indicate out of paper.
68	ACK~	I	**General Purpose Input or Line Printer Acknowledge (active low).** An output from the printer to indicate that data has been accepted successfully.
2,7,22 42,54,61	GND	O	**Signal and Power Ground.** All pins must be tied to ground.
23,40, 64	VCC	I	**Power Supply Input.** All pins must be tied to supply voltage.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

Transmit and Receive Holding Register

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input. Receiver status codes will be posted in the Line Status Register A/B.

INTERRUPT ENABLE REGISTER

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0=disable receiver ready interrupt
1=enable receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable modem status register interrupt
1=enable modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER

The XR-16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the XR-16C452 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

Priority level	Bit-2	Bit-1	Bit-0	Source of the interrupts
1	1	1	0	LSR A/B (Receiver Line Status Register)
2	1	0	0	RXRDY A/B (Received Data Ready)
3	0	1	0	TXRDY A/B (Transmitter holding register empty)
4	0	0	0	MSR A/B (Modem Status Register)
0	0	0	1	No interrupts

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0 parity bit is forced to "1" in the transmitted and received data
LCR BIT-5=1 and LCR BIT-4=1 parity bit is forced to "0" in the transmitted and received data

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TXA/B) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTA/B output control.
0=INTA/B outputs disabled
1=INTA/B outputs enabled

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (RXA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. XR-16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the XR-16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. It is equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. It is equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

SCRATCHPAD REGISTER

XR-16C452 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	36	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

The XR-16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC to 16 MHz and dividing it by any divisor from 2 to 2^{16}-1. Customized Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the Baud Rate Generator.

$$\text{divisor value (decimal)} = \frac{\text{input frequency}}{\text{baud rate X 16}}$$

$$\text{EXAMPLE: } \frac{1.8432 \times 10^6}{1200 \text{ (baud)}} = 96 \text{ (decimal)}$$

96 decimal = 0060 HEX
Divisor MSB = 00
Divisor LSR = 60

XR-16C452 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	**RHR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**THR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**IER**	0	0	0	0	modem status interrupt	receive line status	transmit holding register	receive holding register
0	1	0	**ISR**	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	**LCR**	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	**MCR**	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	**LSR**	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	**MSR**	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	**SPR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**DLL**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**DLM**	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	(PS/2 only) I/O SELECT REGISTER*	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

** Reading the status register will reset the INTP output.*

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
X	0	x x x x x x x x exp. AA Hex	OUTPUT
X	0	10101010	INPUT
0	1	x x x x x x x x	OUTPUT
1	1	x x x x x x x x	INPUT

PORT REGISTER

Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0= ERROR~ input is in low state
1= ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK~ input state.
0= ACK~ input is in low state
1= ACK~ input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0= STROBE~ pin is in high state
1= STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0= AUTOFDXT~ pin is in high state
1= AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0= SLCTIN~ pin is in high state
1= SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0= STROBE~ output is set to high state
1= STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0= AUTOFDXT~ output is set to high state
1= AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0= SLCTIN~ output is set to high state
1= SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5 (PS/2 only):
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER (PS/2 only)

Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"

Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or any other value for output.

XR-16C452 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IERA/B IERA/B	BITS 0-7=0
ISRA/B ISRA/B	BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals
CR	CR BIT 4=0

SIGNALS	RESET STATE
TXA/B	High
RTSA/B~	High
DTRA/B~	High
INTA/B	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0=0
STROBE~	Output mode, high
AUTOFDXT~	Output mode, high
INIT	Output mode, low
SLCTIN~	Output mode, high

XR-16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt AT = only 0= Interrupt (PS/2 only)		

COMMAND REGISTER (READ ONLY)

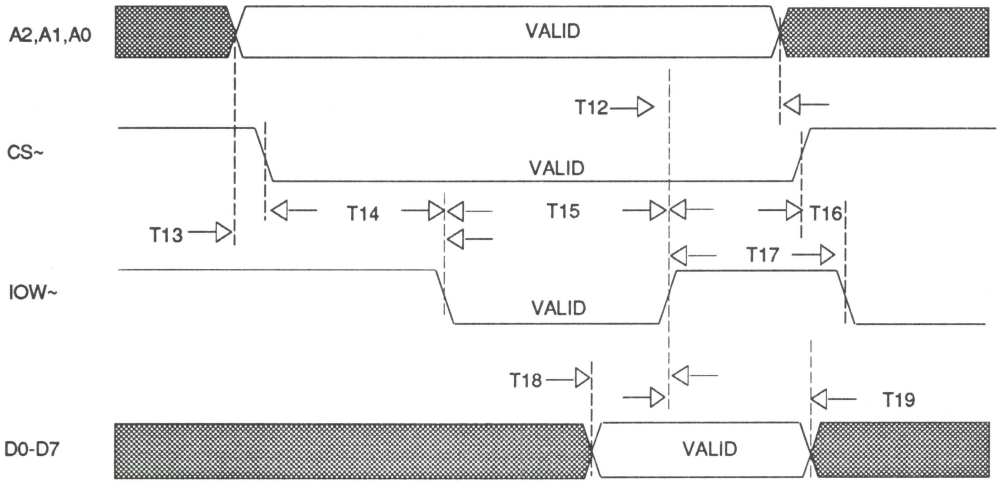
D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT FDXT~	AUTO-	STROBE~
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

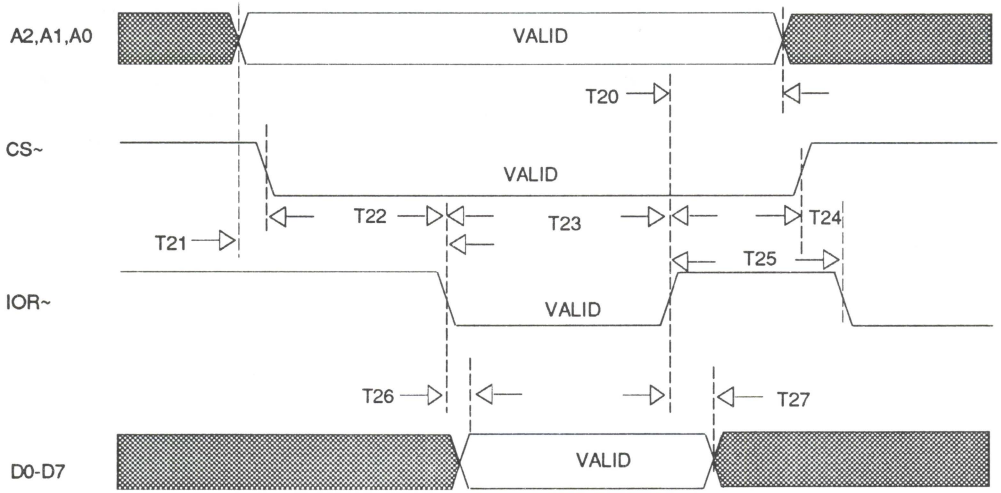
D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
		0=Output (PS/2 only) 1=Input X=AT only	0=INTP output disabled 1=INTP output enabled				

TIMING DIAGRAM

WRITE CYCLE TIMING

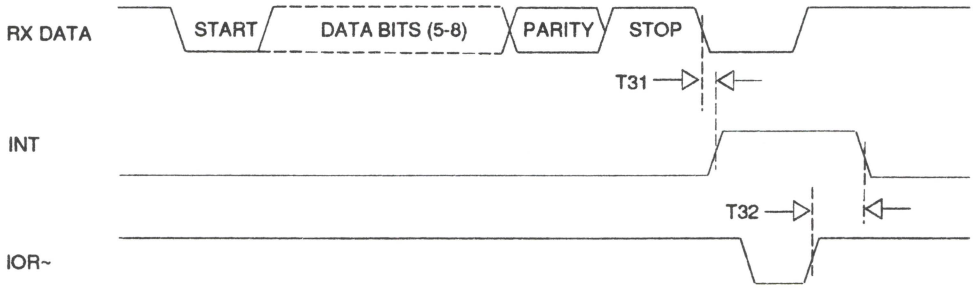


READ CYCLE TIMING

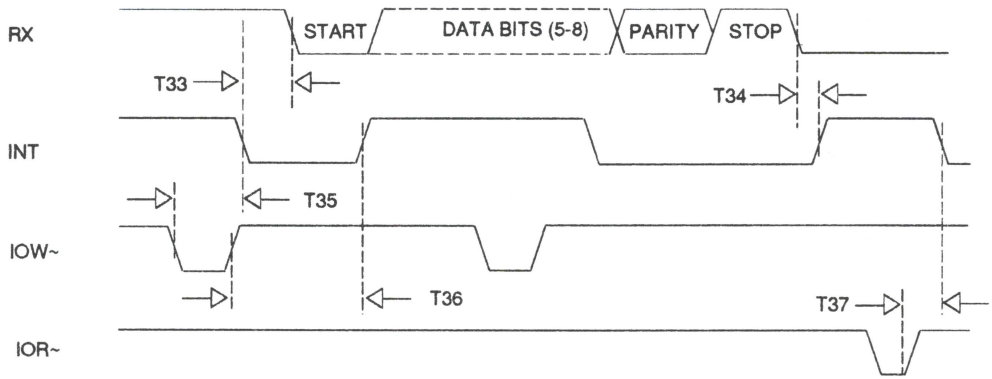


TIMING DIAGRAM

RECEIVER TIMING

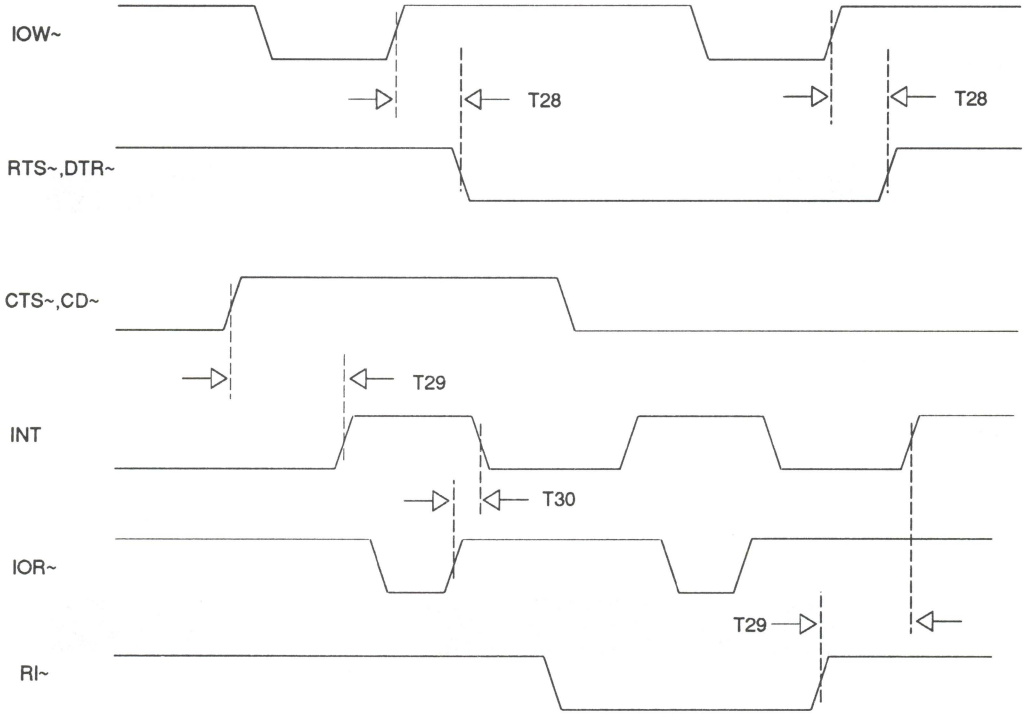


TRANSMITTER TIMING



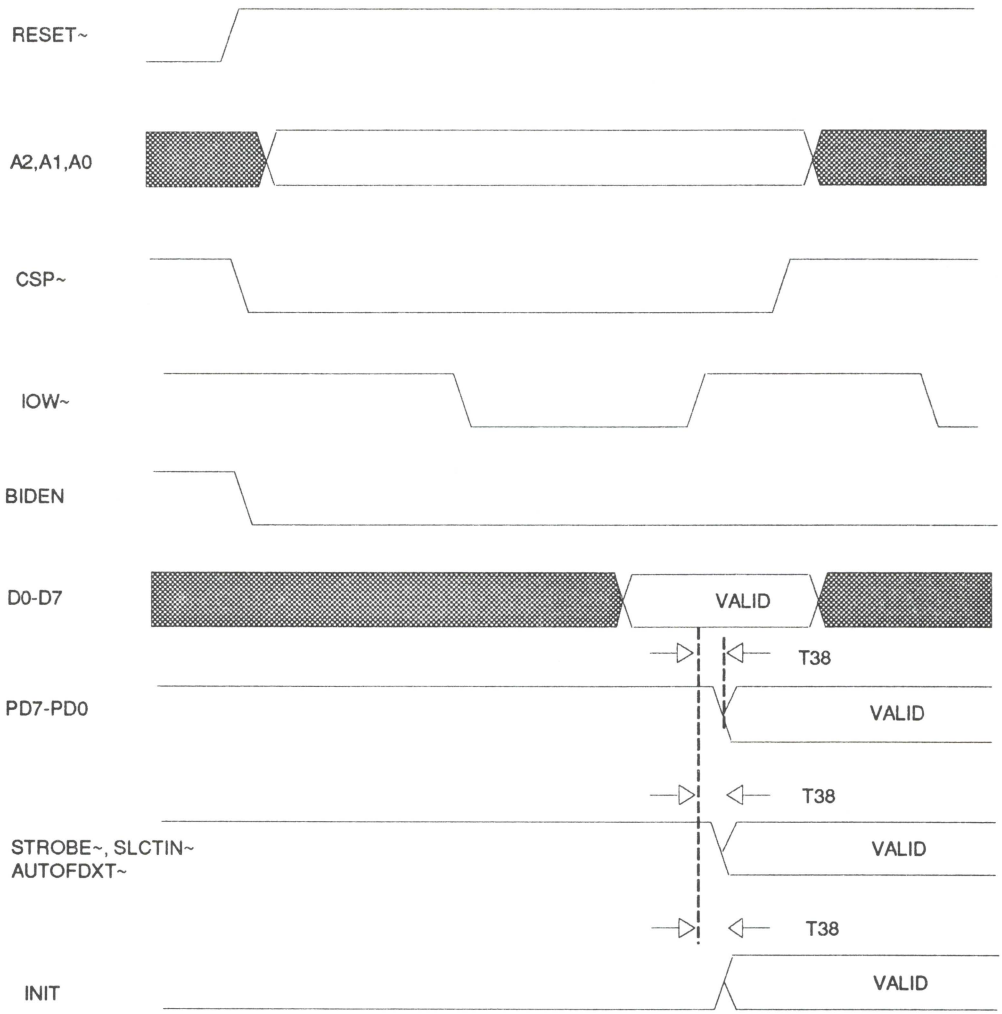
TIMING DIAGRAM

MODEM TIMING



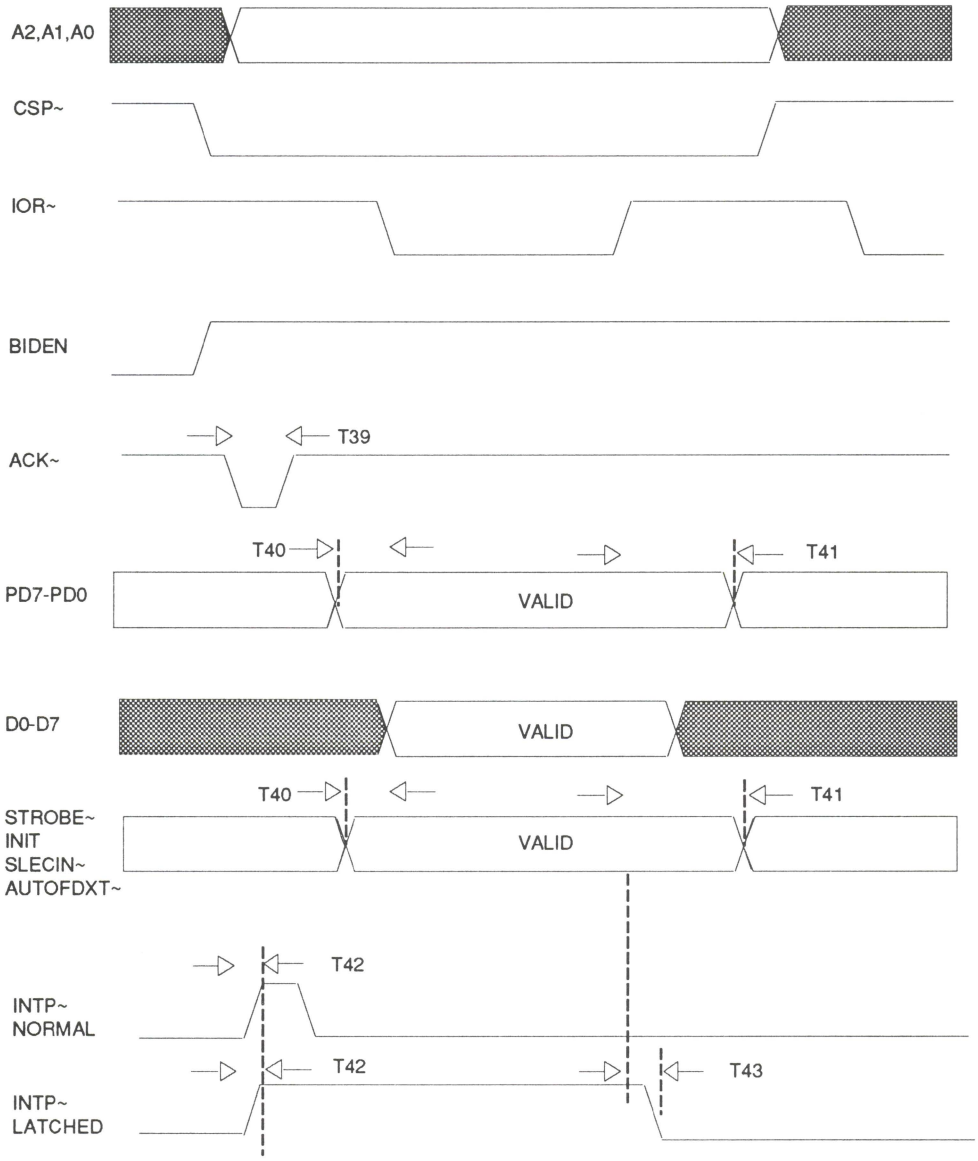
TIMING DIAGRAM

PRINTER WRITE OPERATION



TIMING DIAGRAM

PRINTER READ OPERATION





NOTES



Universal Asynchronous Receiver / Transmitter with FIFOs

GENERAL DESCRIPTION

The XR-16C550 is a universal asynchronous receiver and transmitter with an on-chip FIFO and modem control signal compatibility. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 112kHz. The XR-16C550 is fabricated on an advanced 1.2 µm CMOS process to achieve low power consumption and high operation speed .

FEATURES

Pin to pin and functional compatibility to VL16C550
Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
16 byte programmable FIFO for transmit and receive sections
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs and outputs
448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
Enhanced current drive capability on all I/O ports

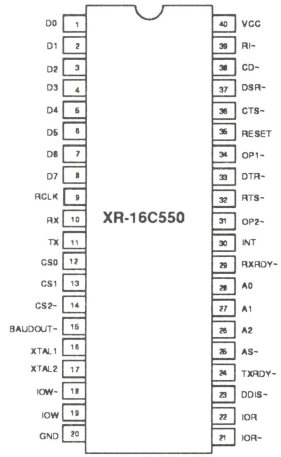
APPLICATIONS

RS232 receiver or transmitter
Serial to parallel/parallel to serial converter
Modem handshaking
IBM PS/2 serial port
Multimedia Systems

ABSOLUTE MAXIMUM RATINGS

Operating Supply Range	5 Volts ± 5%
Voltage at any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +150°C
Package Dissipation	500 mW

PIN ASSIGNMENT



Please refer to page 19 for PLCC Pin Assignment

ORDERING INFORMATION

Part number	Package	Operating Temperature
XR-16C550CP	Plastic	0°C to + 70°C
XR-16C550CJ	PLCC	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-16C550 is an improved version of the VL16C550 UART with higher operating speed and lower access time. The XR-16C550 performs the parallel to serial and serial to parallel conversion on the data characters received from a CPU or MODEM. The on chip status registers will provide the error conditions, as well as the type and status of the transfer operations being performed. Also included in the XR-16C550 is a complete MODEM control capability, and a processor interrupt system. The latter may be software tailored to the user's requirements thereby allowing the user to minimize the computing time required to service the communications link. The on-chip 16 byte FIFO (plus 3 bits of error data per byte in the RX-FIFO) and two DMA signaling functions are provided to also assist in minimizing system computing overhead and maximizing system efficiency.The XR-16C550 also provides an internal loop-back capability for on-board diagnostic testing.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25° C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
VILCK	Clock input low level	-0.5		0.6	V	
VIHCK	Clock input high level	3.0		VCC	V	
VIL	Input low level	-0.5		0.8	V	
VIH	Input high level	2.2		VCC	V	
VOL	Output low level			0.4	V	IOL= 6 mA on all outputs
VOH	Output high level	2.4			V	IOH= -6 mA
ICC	Avg power supply current			6	mA	
IIL	Input leakage			±10	µA	
ICL	Clock leakage			±10	µA	

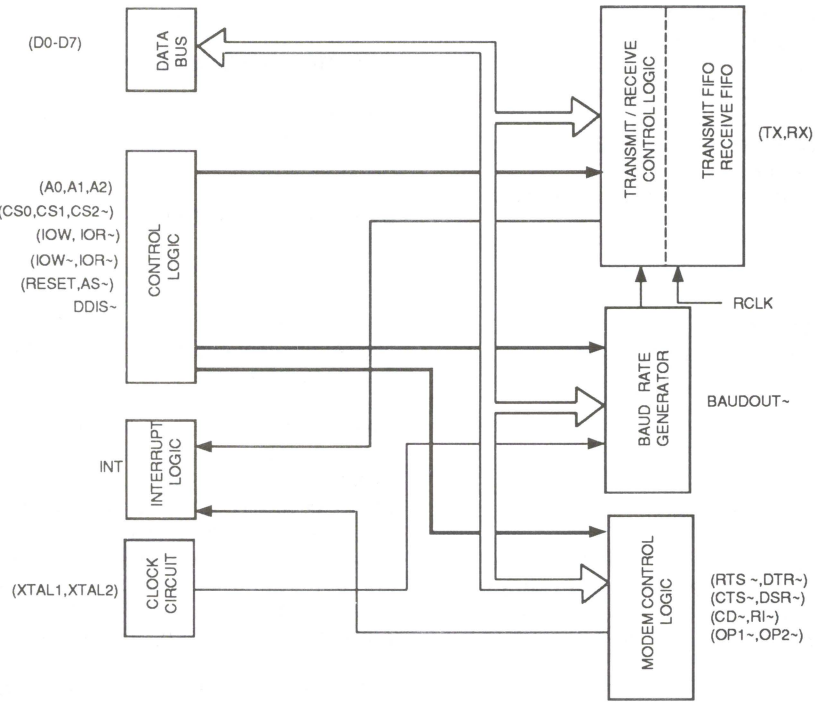


Figure 1. Block Diagram

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T1	Clock high pulse duration	55			ns	
T2	Clock low pulse duration	55			ns	External clock
T3	Clock rise/fall time					
T5	Address strobe width	30			ns	
T6	Address setup time	30			ns	
T7	Address hold time	5			ns	
T8	Chip select setup time	25			ns	
T9	Chip select hold time	0			ns	
T11	IOR~ to drive disable delay			35	ns	100 pF load
T12	Address hold time from IOW~	20			ns	Note: 1
T13	IOW~ delay from address	25			ns	Note: 1
T14	IOW~ delay from chip select	10			ns	Note: 1
T15	IOW~ strobe width	50			ns	
T16	Chip select hold time from IOW~	5			ns	Note: 1
T17	Write cycle delay	55			ns	
Tw	Write cycle=T15+T17	135			ns	
T18	Data setup time	20			ns	
T19	Data hold time	25			ns	
T20	Address hold time from IOR~	0			ns	Note: 1
T21	IOR~ delay from address	10			ns	Note: 1
T22	IOR~ delay from chip select	10			ns	Note: 1
T23	IOR~ strobe width	75			ns	
T24	Chip select hold time from IOR~	0			ns	Note: 1
T25	Read cycle delay	50			ns	
Tr	Read cycle=T23+T25	135			ns	
T26	Delay from IOR~ to data		75		ns	100 pF load
T27	IOR~ to floating data delay	0	50		ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VCC = 5.0 V ± 5% unless otherwise specified

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
MODEM CONTROL						
T28	Delay from IOW~ to output			50	ns	100 pF load
T29	Delay to set interrupt from MODEM input			70	ns	100 pF load
T30	Delay to reset interrupt from IOR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		$2^{16}-1$		
T4	Baud out negative edge delay			100	ns	100 pF load
T4	Baud out positive edge delay			100	ns	100 pF load
RECEIVER						
T31	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T32	Delay from IOR~ to reset interrupt			200	ns	100 pF load
TRANSMITTER						
T33	Delay from initial INT reset to transmit start	8		24	*	
T34	Delay from stop to interrupt			100	ns	
T35	Delay from IOW~ to reset interrupt			125	ns	
T36	Delay from initial Write to interrupt	16		24	*	
T37	Delay from IOR~ to reset interrupt			75	ns	100 pF load

*Note 1: Applicable only when AS~ is tied low
Baudout~ cycle

PIN DESCRIPTION

Pin#	Symbol	Type	Description
1-8	D0-D7	I/O	**Bidirectional Data Bus.** Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
9	RCLK	I	**Receive Clock Input.** The external clock input to the XR-16C550 receiver section.
10	RX	I	**Serial Data Input.** The serial information (data) received from MODEM or RS232 to XR-16C550 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
11	TX	O	**Serial Data Output.** The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
12	CSO	I	**Chip Select 1 (active high).** A high at this pin (while CS1=1 and CS2~=0) will enable the UART / CPU data transfer operation.
13	CS1	I	**Chip Select 2 (active high).** A high at this pin (while CS0=1 and CS2~=0) will enable the UART / CPU data transfer operation.
14	CS2~	I	**Chip Select 3 (active low).** A low at this pin (while CS0=1 and CS1=1) will enable the UART / CPU data transfer operation.
15	BAUDOUT~	O	**Baud Rate Generator Clock Output.** This output provides the 16x clock of the internal selected baud rate.
16	XTAL1	I	**Crystal Input 1 or External Clock Input.** A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
17	XTAL2	I	**Crystal Input 2.** See XTAL1.
18	IOW~	I	**Write Strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the addressed register.
19	IOW	I	**Write Strobe (active high).** Same as IOW~, but uses active high input. Note that only an active IOW~ or IOW input is required to transfer data from CPU to XR-16C550 during write operation (while CS0=1, CS1=1 and CS2~=0). The unused pin should be tied to VCC or GND (IOW = GND or IOW~=VCC) .
20	GND	O	**Signal and Power Ground.**

Pin#	Symbol	Type	Description
2I	IOR~	I	**I/O Read Strobe (active low).** A low level on this pin (while CS0=1, CS1=1 and CS2~=0) will transfer the contents of the XR-16C550 data bus to the CPU.
22	IOR	I	**Read Strobe (active high).** Same as IOR~, but uses active high input. Note that only an active IOR~ or IOR input is required to transfer data from XR-16C550 to CPU during read operation (while CS0=1, CS1=1 and CS2~=0). The unused pin should be tied to VCC or GND (IOR=GND or IOR~=VCC) .
23	DDIS~	O	**Drive Disable (active low).** This pin goes low when the CPU is reading data from the XR-16C550 to disable the external transceiver or logics.
24	TXRDY~	O	**Transmit Ready (active low).** This pin goes low when the transmit FIFO of the XR-16C550 is full. It can be used as a single or multitransfer DMA.
25	AS~	I	**Address Strobe (active low).** A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS~ input permanently low.
26	A2	I	**Address Line 2.** To select internal registers.
27	A1	I	**Address Line 1.** To select internal registers.
28	A0	I	**Address Line 0.** To select internal registers.
29	RXRDY~	O	**Receive Ready (active low).** This pin goes low when the receive FIFO is full. It can be used as a single or multitransfer DMA.
30	INT	O	**Interrupt Output (active high).** This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
31	OP2~	O	**General Purpose Output (active low).** User defined output. See bit-3 modem control register.
32	RTS~	O	**Request to Send (active low).** To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high.
33	DTR~	O	**Data Terminal Ready (active low).** To indicate that the XR-16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" to the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after a reset.
34	OP1~	O	**General Purpose Output (active low).** User defined output. See bit-2 of modem control register.

Pin#	Symbol	Type	Description
35	RESET	I	**Master Reset (active high).** A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
36	CTS~	I	**Clear to Send (active low).** The CTS~ signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS~ has no effect on the transmitter output.
37	DSR~	I	**Data Set Ready (active low).** A low on this pin indicates the MODEM is ready to exchange data with the UART.
38	CD~	I	**Carrier Detect (active low).** A low on this pin indicates the carrier has been detected by the modem.
39	RI~	I	**Ring Detect Indicator (active low).** A low on this pin indicates the modem has received a ringing signal from the telephone line.
40	VCC	I	**Power Supply Input.**

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
x	0	1	0	Interrupt Status Register	FIFO Control Register
x	0	1	1		Line Control Register
x	1	0	0		Modem Control Register
x	1	0	1	Line Status Register	
x	1	1	0	Modem Status Register	
x	1	1	1	Scratchpad Register	Scratchpad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

XR-16C550 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	**RHR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**THR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**IER**	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	**FCR**	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	**ISR**	0/ FIFOs enabled	0/ FIFOs enabled	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	**LCR**	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	**MCR**	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	**LSR**	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	**MSR**	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	**SPR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**DLL**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**DLM**	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

Transmit and Receive Holding Register

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register will transfer the contents of the data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO Polled Mode Operation

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the XR-16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift registers are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

Programmable Baud Rate Generator

The XR-16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC to 16 MHz and dividing it by any divisor from 2 to 2^{16} -1. The output frequency of the Baudout~ is equal to 16X of the transmission baud rate (Baudout~=16 x Baud Rate). Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The XR-16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the XR-16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in XR-16C450 mode. BIT 6-7: are set to "1" in XR-16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	World length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable(DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high.
1=force DTR~ output to low.

MCR BIT-1:
0=force RTS~ output to high.
1=force RTS~ output to low.

MCR BIT-2:
0=set OP1~ output to high.
1=set OP1~ output to low.

MCR BIT-3:
0=set OP2~ output to high.
1=set OP2~ output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS~, DSR~, CD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OP1~ and OP2~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. The character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=a break signal was received by the receiver (RX was low for one character time frame). In the FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. XR-16C550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the XR-16C550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD~ input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

XR-16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

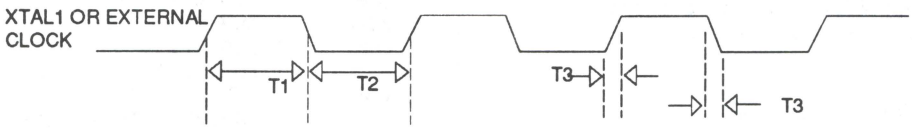
XR-16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

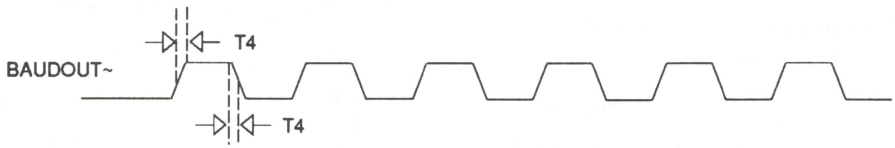
SIGNALS	RESET STATE
TX	High
OP1~	High
OP2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

TIMING DIAGRAM

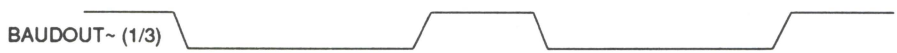
CLOCK TIMING



BAUDOUT~TIMING



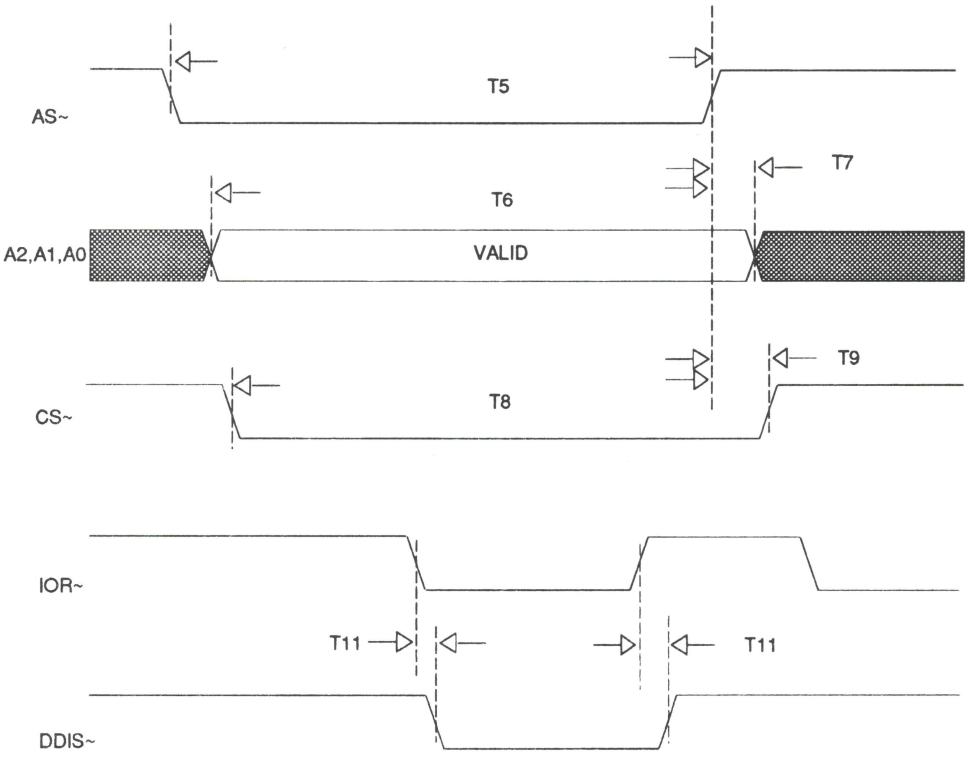






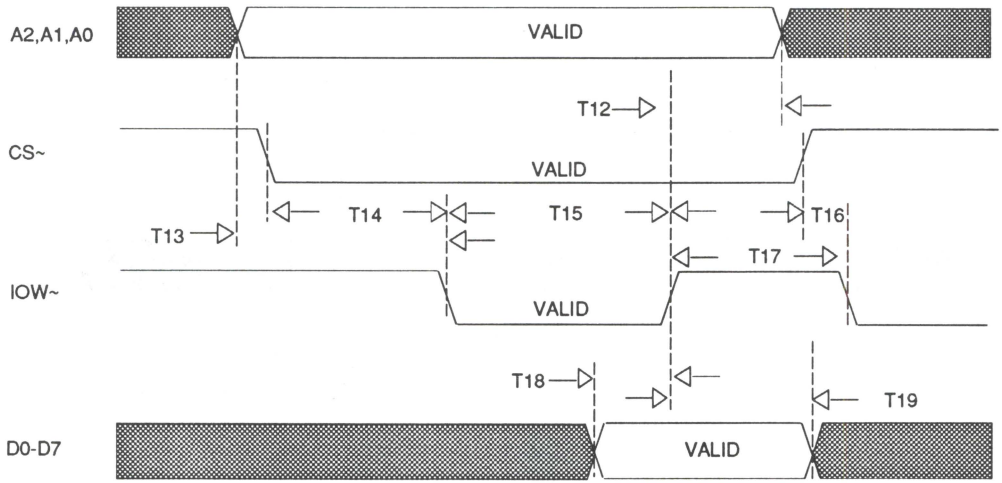
TIMING DIAGRAM

GENERAL TIMING

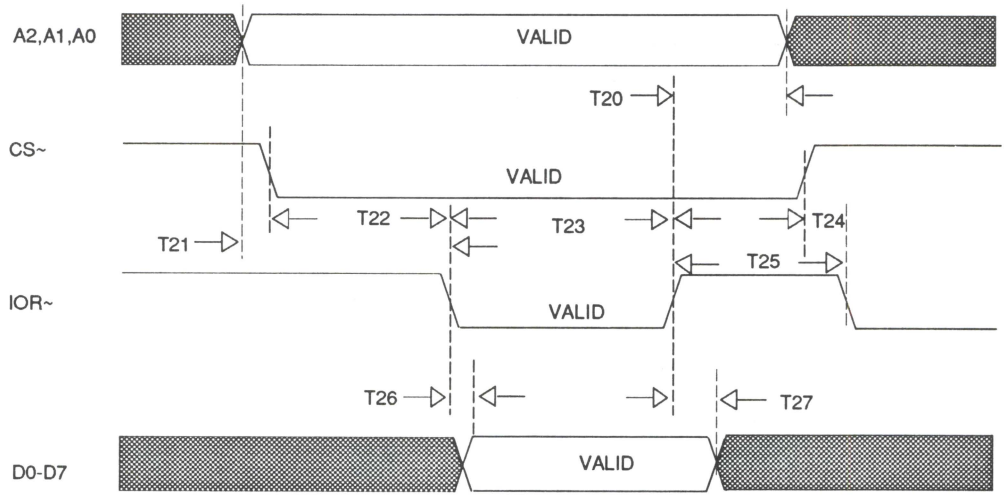


TIMING DIAGRAM

WRITE CYCLE TIMING

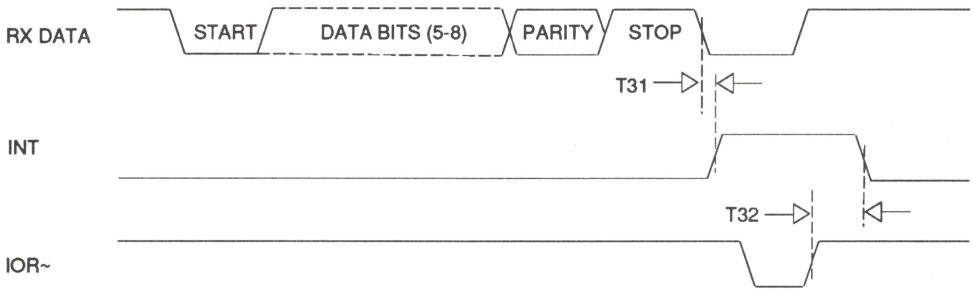


READ CYCLE TIMING

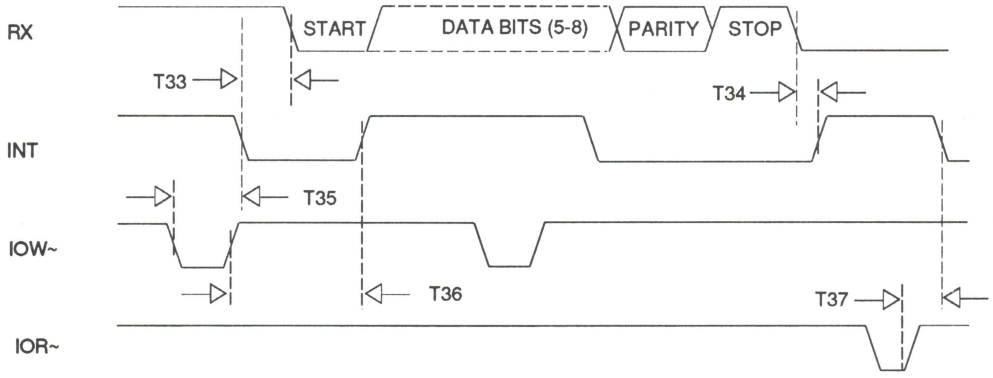


TIMING DIAGRAM

RECEIVER TIMING

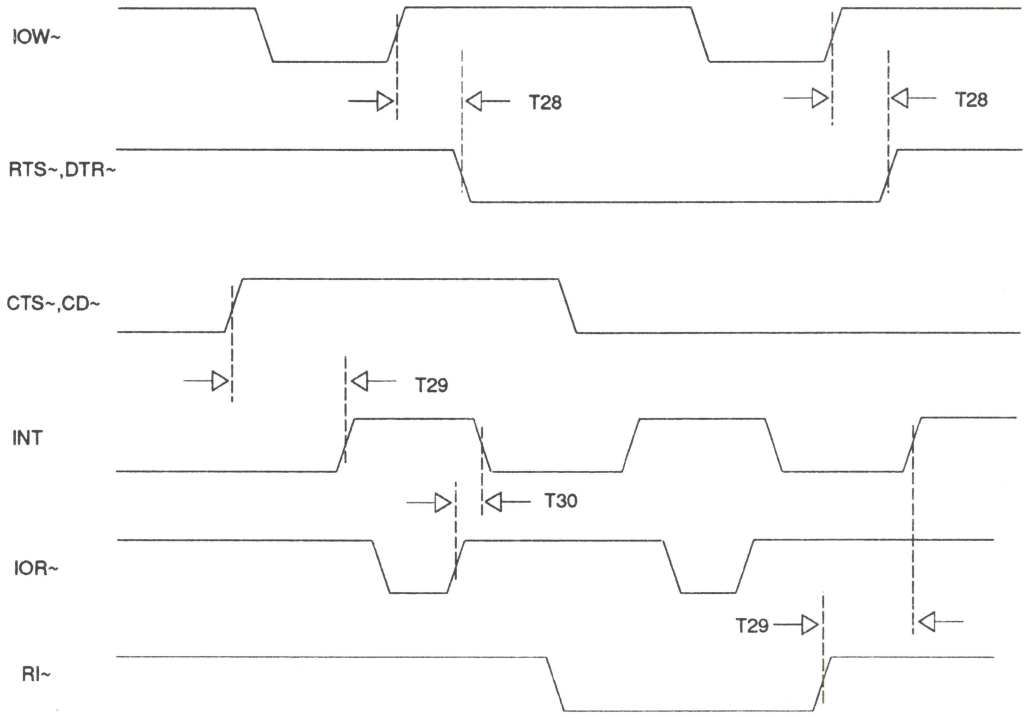


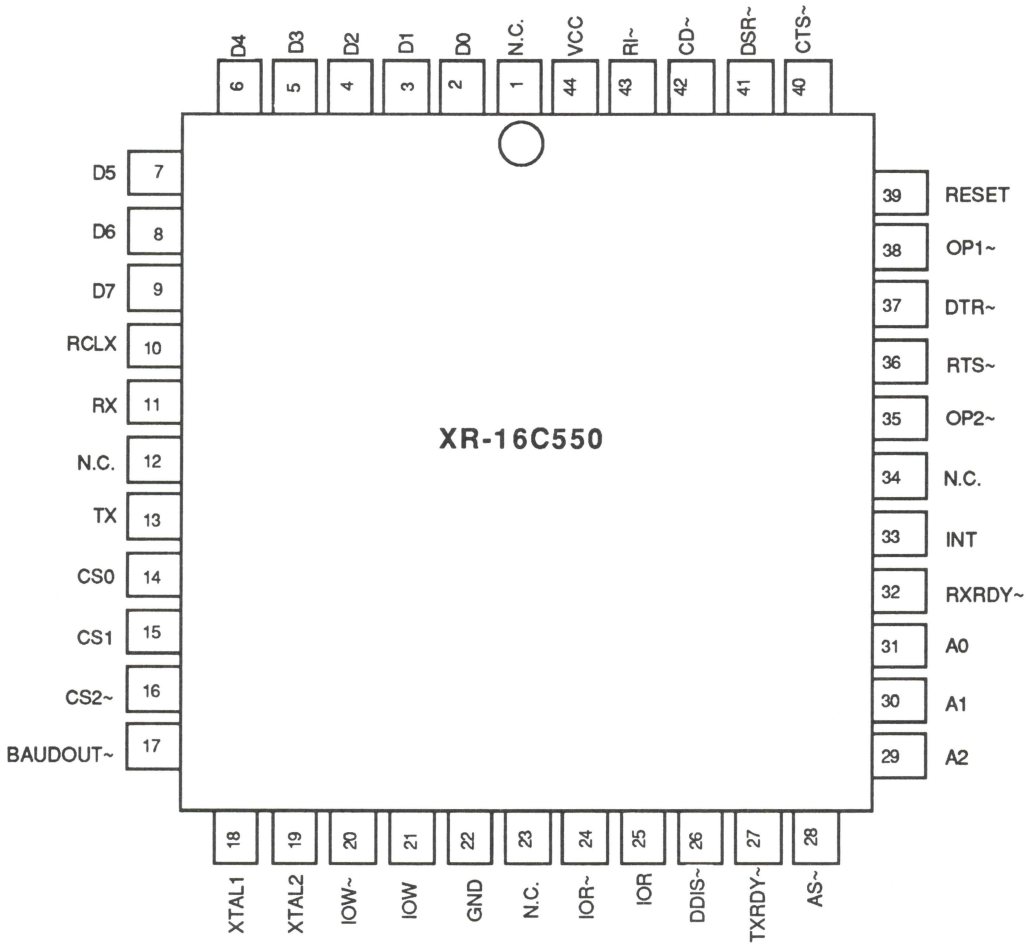
TRANSMITTER TIMING



TIMING DIAGRAM

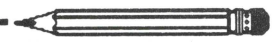
MODEM TIMING




D4 6
D3 5
D2 4
D1 3
D0 2
N.C. 1
VCC 44
RI~ 43
CD~ 42
DSR~ 41
CTS~ 40
D5 7
D6 8
D7 9
RCLX 10
RX 11
N.C. 12
TX 13
CS0 14
CS1 15
CS2~ 16
BAUDOUT~ 17
XR-16C550
39 RESET
38 OP1~
37 DTR~
36 RTS~
35 OP2~
34 N.C.
33 INT
32 RXRDY~
31 A0
30 A1
29 A2
18 XTAL1
19 XTAL2
20 IOW~
21 IOW
22 GND
23 N.C.
24 IOR~
25 IOR
26 DDIS~
27 TXRDY~
28 AS~



NOTES



Dual Universal Asynchronous Receiver and Transmitter with FIFO and Parallel Printer Port

GENERAL DESCRIPTION

The XR-16C552 is a dual universal asynchronous receiver and transmitter with FIFO, a bidirectional CENTRONICS type parallel printer port, and modem control signed capability. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The XR-16C552 is fabricated on an advanced 1.2µm CMOS process to achieve low power consumption and high speed operation.

FEATURES

Pin-to-pin and functionally compatible to VL16C552
Fully compatible with all new bidirectional PS/2 printer port
Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
16 byte programmable FIFO for transmit and receive sections
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection Status report register
Independent transmit and receive control
TTL compatible inputs, outputs
Direct replacement of logic for PC/XT/AT
High data transfer rate
448 kHz transmit / receive operation with 7.372 MHz external clock source
Enhanced current drive capability on all I/O ports.

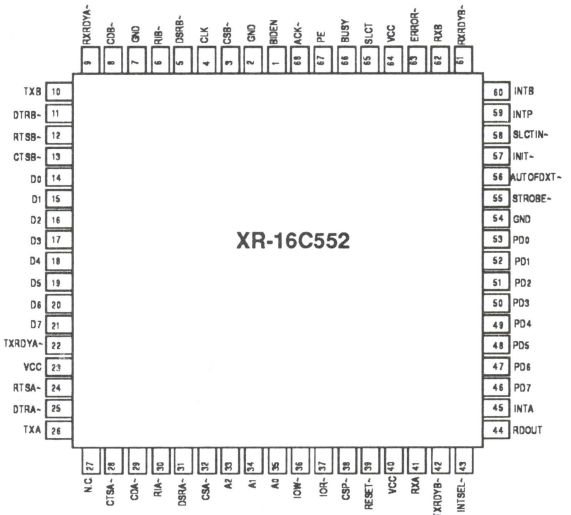
APPLICATIONS

Dual serial receiver and/or transmitter
Serial to parallel / parallel to serial converter
Modem handshaking
CENTRONICS printer port
IBM PS/2 bidirectional printer port
External bidirectional I/O
IBM PC/XT/AT upgrade printer port
Multimedia Systems.

ABSOLUTE MAXIMUM RATINGS

Operating Supply Range	7 Volts ±5%
Voltage at any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +150°C
Package Dissipation	500 mW

PIN ASSIGNMENT



ORDERING INFORMATION

Part number	Package	Operating Temperature
XR-16C552CJ	PLCC	0°C to +70°C

SYSTEM DESCRIPTION

The XR-16C552 is an improved version of the VL16C552 with higher operating speed and lower access time. The XR-16C552 performs the parallel to serial/serial to parallel conversion on the data characters received from a CPU or the MODEM. The XR-16C552 also provides the user with a bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on chip status registers will provide the error conditions, type and status of the transfer operations being performed. The XR-16C552 also has a complete MODEM control capability, and a processor interrupt system. The latter may be software tailored to the user's requirements thereby allowing the user to minimize the computing time required to service the communications link. The on-chip 16 byte FIFO (plus 3 bits of error data per byte is the RX-FIFO), are provided to also assist in minimizing computing overhead and maximizing system efficiency. The XR-16C552 also provides an internal loopback feature for on-board diagnostics testing.

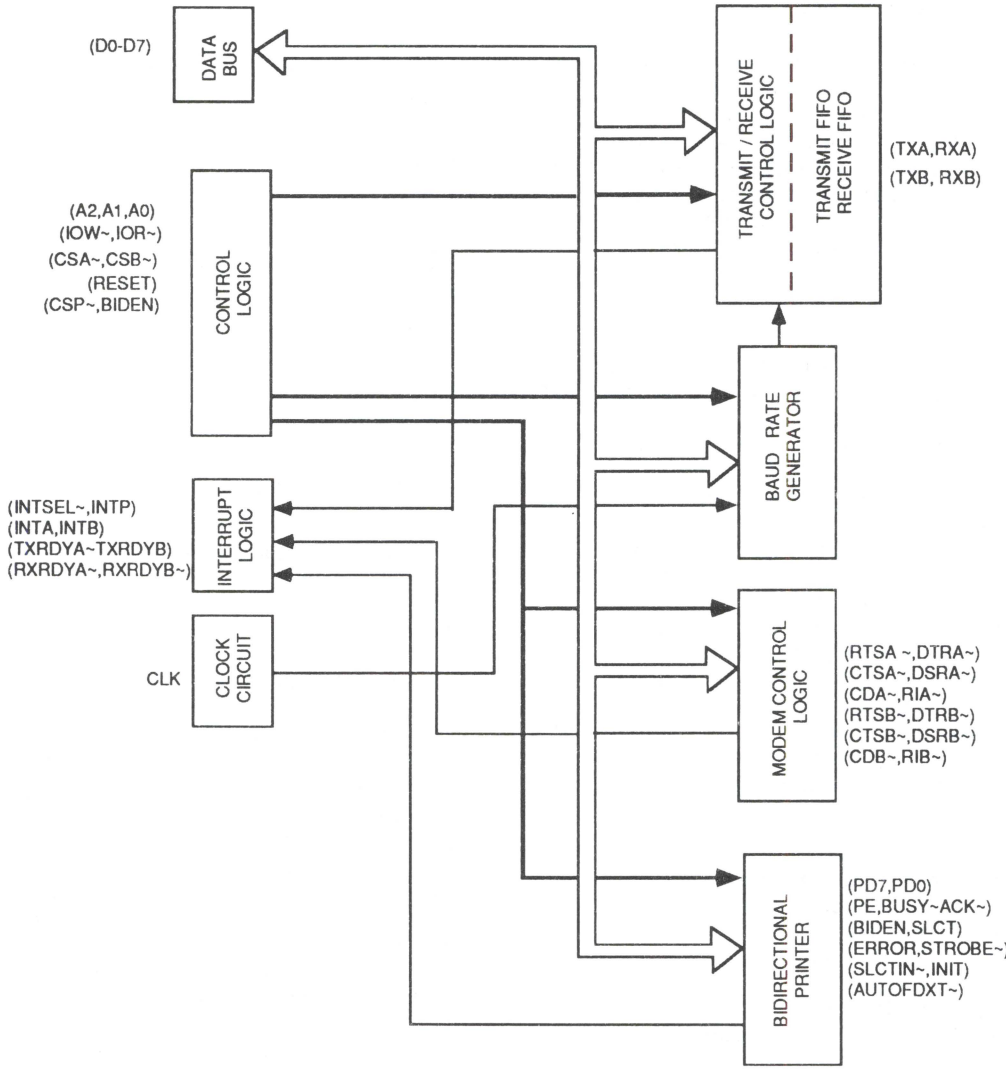


Figure 1. Block Diagram

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ±5% unless otherwise specified.

Symbol	Parameter	Limit			Units	Conditions
		min	typ	max		
VILCK	Clock input low level	-0.5		0.6	V	
VIHCK	Clock input high level	3.0		VCC	V	
VIL	Input low level	-0.5		0.8	V	
VIH	Input high level	2.2		VCC	V	
VOL	Output low level			0.4	V	IOL= 6.0 mA D7-D0 IOL= 20.0 mA PD7-PD0 IOL= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ IOL= 6.0 mA on all other outputs
VOH	Output high level	2.4			V	IOH= -6.0 mA D7-D0 IOH= -12.0 mA PD7-PD0 IOH= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ IOH= -6.0 mA on all other outputs
ICC	Avg power supply current			20	mA	
IIL	Input leakage			±10	µA	
ICL	Clock leakage			+10	µA	

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limit			Units	Conditions
		min	typ	max		
T1	Clock high pulse duration	60			ns	
T2	Clock low pulse duration	60			ns	External clock
T3	Clock rise/fall time			100	ns	
T12	Address hold time from IOW~	20			ns	
T13	IOW~ delay from address	25			ns	
T14	IOW~ delay from chip select	10			ns	
T15	IOW~ strobe width	50			ns	
T16	Chip select hold time from IOW~	5			ns	
T17	Write cycle delay	55			ns	
TW	Write cycle=T15+T17	135			ns	
T18	Data setup time	20			ns	
T19	Data hold time	25			ns	
T20	Address hold time from IOR~	0			ns	
T21	IOR~ delay from address	10			ns	
T22	IOR~ delay from chip select	10			ns	
T23	IOR~ strobe width	75			ns	
T24	Chip select hold time from IOR~	0			ns	
T25	Read cycle delay	50			ns	
TR	Read cycle=T23+T25	135			ns	
T26	Delay from IOR~ to data			75	ns	100 pF load
T27	IOR~ to floating data delay	0		50	ns	100 pF load

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limit			Units	Conditions
		min	typ	max		
MODEM CONTROL						
T28	Delay from IOW~ to output			50	ns	100 pF load
T29	Delay to set interrupt from MODEM input			70	ns	100 pF load
T30	Delay to reset interrupt from IOR~			70	ns	100 pF load
RECEIVER						
T31	Delay from stop to set interrupt			1 Rclk	ns	100 pF load
T32	Delay from IOR~ to reset interrupt			200	ns	100 pF load
TRANSMITTER						
T33	Delay from initial INT reset to transmit start	8		24	*	
T34	Delay from stop to interrupt			100	ns	
T35	Delay from IOW~ to reset interrupt			125	ns	
T36	Delay from initial Write to interrupt	16		24	*	
T37	Delay from IOR~ to reset interrupt			75	ns	100 pF load
PRINTER PORT						
T38	Delay from rising IOW~ to output data.	5			ns	
T39	ACK~ pulse width	75			ns	
T40	PD7 - PD0 setup time	10			ns	
T41	PD7 - PD0 hold time	25			ns	
T42	Delay from ACK~ low to interrupt high.	5			ns	
T43	Delay from IOR~ to reset interrupt	5			ns	

* Baud rate cycle

PIN DESCRIPTION

Pin#	Symbol	Type	Description
1	BIDEN	I	**Printer Direction Select.** A high puts the parallel port in the software controlled mode (input/output). A low puts the parallel port in the out mode.
3	CSB~	I	**Chip Select B (active low).** A low at this pin (while CSA~ and CSP~=1) will enable the UARTB / CPU data transfer operation.
4	CLK	I	**External Clock Input.** An external clock can be used to clock the internal circuit and the baud rate generator for custom and standard transmission rates.
5	DSRB~	I	**Data Set Ready B (active low).** A low on this pin indicates that MODEM B is ready to exchange data with UARTB.
6	RIB~	I	**Ring Detect B Indicator (active low).** A low on this pin indicates that MODEM B has received a ringing signal from the telephone line.
8	CDB~	I	**Carrier Detect B (active low).** A low on this pin indicates that carrier has been detected by the MODEM B.
9	RXRDYA~	O	**Receive Ready A (active low).** This pin goes low when the receive FIFO of the XR-16C552 A section is full. It can be used as a single or multi-transfer DMA .
10	TXB	O	**Serial Data Output B.** The serial data is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
11	DTRB~	O	**Data Terminal Ready B (active low).** To indicate that XR-16C552 is ready to receive data. This pin can be controlled via the modem control register (MCRB bit-0).Writinga "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
12	RTSB~	O	**Request to Send B (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
13	CTSB~	I	**Clear to Send B (active low).** The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
14-21	D0-D7	I/O	**Bidirectional Data Bus.** Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (LSB) of the data bus and the first serial data bit to be received or transmitted.

Pin#	Symbol	Type	Description
22	TXRDYA~	O	**Transmit Ready A (active low).** This pin goes low when the transmit FIFO of the XR-16C552 A section is full. It can be used as a single or multi-transfer DMA.
24	RTSA~	O	**Request to Send A (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.
25	DTRA~	O	**Data Terminal Ready A (active low).** To indicate that XR-16C552 is ready to receive data. This pin can be controlled via the modem control register (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
26	TXA	O	**Serial Data Output A.** The serial data is transmitted via this pin with additional start , stop and parity bits. The TXA will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
28	CTSA~	I	**Clear to Send A (active low).** The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
29	CDA~	I	**Carrier Detect A (active low).** A low on this pin indicates that a carrier has been detected by the MODEM A.
30	RIA~	I	**Ring Detect A Indicator (active low).** A low on this pin indicates that MODEM A has received a ringing signal from the telephone line.
31	DSRA~	I	**Data Set Ready A (active low).** A low on this pin indicates that MODEM A is ready to exchange data with UART A.
32	CSA~	I	**Chip Select A (active low).** A low at this pin (while CSB~ and CSP~=1) will enable the UART A / CPU data transfer operation.
33	A2	I	**Address Line 2.** To select internal registers.
34	A1	I	**Address Line 1.** To select internal registers.
35	A0	I	**Address Line 0.** To select internal registers.
36	IOW~	I	**Write Strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the addressed register.
37	IOR~	I	**Read Strobe (active low).** A low level on this pin will transfer the contents of the XR-16C552 data bus to the CPU.

Pin#	Symbol	Type	Description
38	CSP~	I	**Chip Select P (active low).** To enable the XR-16C552 printer operation, this pin has to go low while CSA~ and CSB~ are high.
39	RESET~	I	**Master Reset (active low).** A low on this pin will reset all the outputs and internal registers. The parallel port of the XR-16C552 will be set to output mode, the transmitter output and the receiver input will be disabled during reset time.
41	RXA	I	**Serial Data Input A.** The serial information (data) received from MODEM or RS232 to XR-16C552 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode RXA input is disabled from external connection and connected to the TXA output internally.
42	TXRDYB~	O	**Transmit Ready B (active low).** This pin goes low when the transmit FIFO of the XR-16C552 B section is full. It can be used as a single or multi-transfer DMA.
43	INTSEL~	I	**Interrupt Select (active low).** The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to VCC, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
44	RDOUT	O	**Read Select Out.** A high on this pin indicates that the chip is being read by the CPU.
45	INTA	O	**UART A Interrupt Output (three state).** This pin goes high when enabled by (MCRA BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
46-53	PD7-PD0	I/O	**Bidirectional Parallel Ports (three state).** To transfer data in or out of the XR-16C552 parallel port. PD7-PD0 are latched during output mode.
55	STROBE~	I/O	**General Purpose I/O or Strobe Output (open drain active low).** To transfer latched data to the external peripheral or printer.
56	AUTOFDXT~	I/O	**General Purpose I/O or Line Printer Autofeed (open drain active low).** To signal the printer for continuous form feed.
57	INIT~	I/O	**General Purpose I/O or Line Printer Initialize (open drain active low).** To signal the line printer to enter internal initialization routine.
58	SLCTIN~	I/O	**General Purpose I/O or Line Printer Select (open drain active low).** To select the line printer.
59	INTP	O	**Printer Interrupt Output (high).** To signal the state of the printer port.

Pin#	Symbol	Type	Description
60	INTB	O	**UART B Interrupt Output (three state).** This pin goes high when enabled by (MCRB BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
61	RXRDYB~	O	**Receive Ready B (active low).** This pin goes low when the receive FIFO of the XR-16C552 B section is full. It can be used as a single or multi-transfer DMA .
62	RXB	I	**Serial Data Input B.** The serial information (data) received from MODEM or RS232 to XR-16C552 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loop-back mode the RXB input is disabled from external connection and connected to the TXB output internally.
63	ERROR~	I	**General Purpose Input or Line Printer Error (active low).** This is an output from the printer to indicate an error by holding it low during error condition.
65	SLCT	I	**General Purpose Input or Line Printer Selected (active high).** This is an output from the printer to indicate that the line printer has been selected.
66	BUSY	I	**General Purpose Input or Line Printer Busy (active high).** An output from the printer to indicate printer is not ready to accept data.
67	PE	I	**General Purpose Input or Line Printer Paper Empty (active high).** An output from the printer to indicate out of paper.
68	ACK~	I	**General Purpose Input or Line Printer Acknowledge (active low).** An output from the printer to indicate that data has been accepted successfully.
2,7,	GND	O	**Signal and Power Ground.** 27,54 All pins must be tied to ground.
23,40,	VCC	I	**Power Supply Input.** All 64 pins must be tied to +5V.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	FIFO Control Register A
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	FIFO Control Register B
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

REGISTER FUNCTIONAL DESCRIPTIONS

Transmit and Receive Holding Register

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input.

Receiver status codes will be posted in the Line Status Register A/B.

FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occur when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO Polled Mode Operation

When FCR BIT-0=1; resetting (IER BIT 3-0) to zero puts the XR-16C552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

Programmable Baud Rate Generator

The XR-16C552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC to 16 MHz and dividing it by any divisor from 2 to 2^{16} -1. Custom Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the baud rate generator.

INTERRUPT ENABLE REGISTER

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0=disable receiver ready interrupt
1=enable receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable modem status register interrupt
1=enable modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER

The XR-16C552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the XR-16C552 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Priority level				Source of the interrupts
P	D2	D1	D0	
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero in ST16C450 mode. BIT 6-7: are set "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0 parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1 parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TXA/B) to go low to alert the communication terminal.
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTA/B output control.
0=INTA/B outputs disabled
1=INTA/B outputs enabled

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (RXA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. XR-16C552 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the XR-16C552 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. It is equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. It is equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

SCRATCHPAD REGISTER

XR-16C552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	36	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

XR-16C552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IERA/B	IERA/B BITS 0-7=0
ISRA/B	ISRA/B BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0,
MSRA/B	BITS 4-7=input signals
CR	CR BIT 4=0

SIGNALS	RESET STATE
TXA/B	High
RTSA/B~	High
DTRA/B~	High
INTA/B	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0=0
STROBE~	Output mode, high

XR-16C552 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	**RHR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**THR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**IER**	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	**FCR**	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	**ISR FIFOs**	0/ FIFOs enabled	0/ enabled	0	0	0 priority	int priority bit-1	int status bit-0	int
0	1	1	**LCR**	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	**MCR**	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	**LSR**	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	**MSR**	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	**SPR**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	**DLL**	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	**DLM**	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0	PORT MODE
X	0	xxxxxxxx exp. AA Hex	OUTPUT
X	0	10101010	INPUT
0	1	xxxxxx	OUTPUT
1	1	xxxxxxx	INPUT

REGISTER DESCRIPTIONS

PORT REGISTER

Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the status of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0= ERROR~ input is in low state
1= ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK~ input state.
0= ACK~ input is in low state
1= ACK~ input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0= STROBE~ pin is in high state
1= STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0= AUTOFDXT~ pin is in high state
1= AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0= SLCTIN~ pin is in high state
1= SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0= STROBE~ output is set to high state
1= STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0= AUTOFDXT~ output is set to high state
1= AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0= SLCTIN~ output is set to high state
1= SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one" Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or any other value for output.

XR-16C552 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt		

COMMAND REGISTER(READ ONLY)

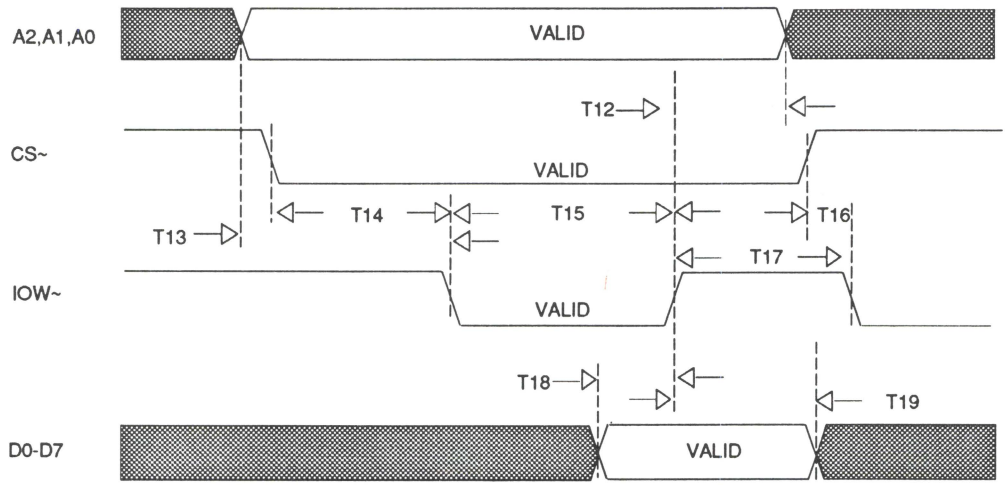
D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

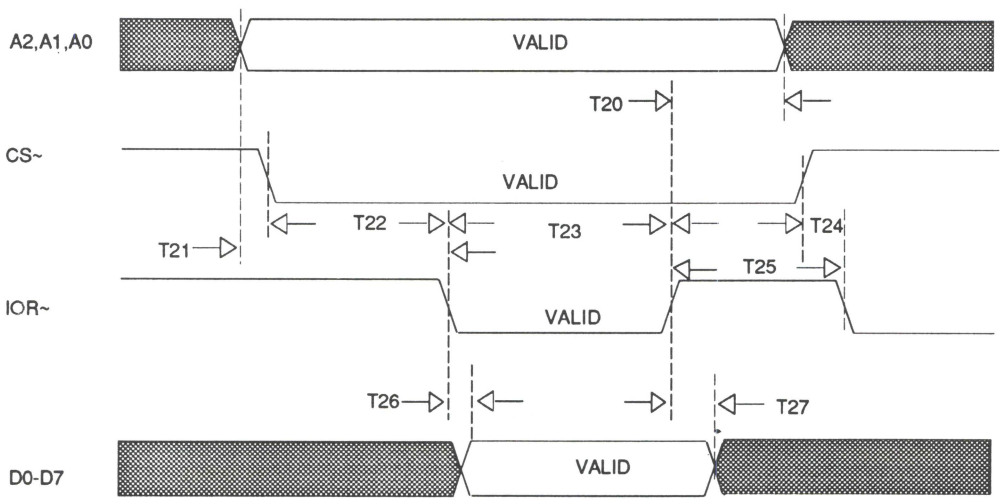
D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
	0=Output 1=Input		0=INTP output disabled 1=INTP output enabled				

TIMING DIAGRAM

WRITE CYCLE TIMING

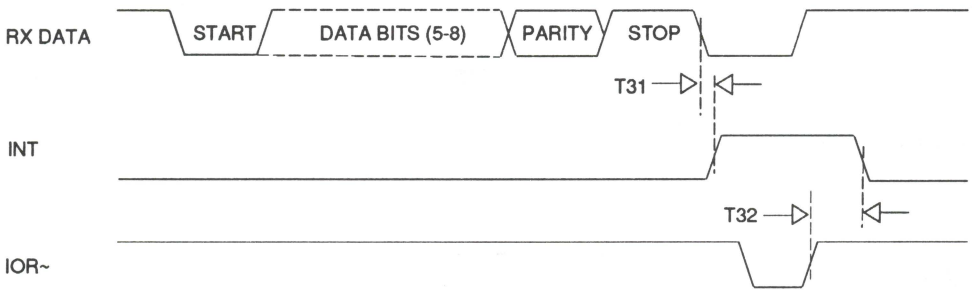


READ CYCLE TIMING

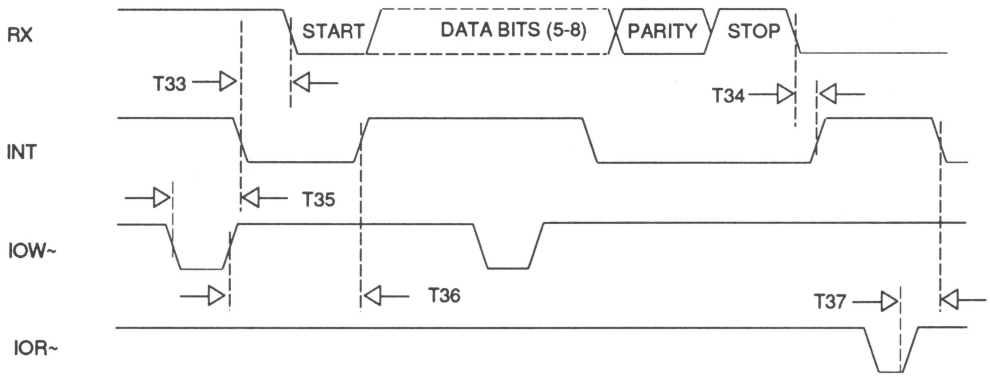


TIMING DIAGRAM

RECEIVER TIMING

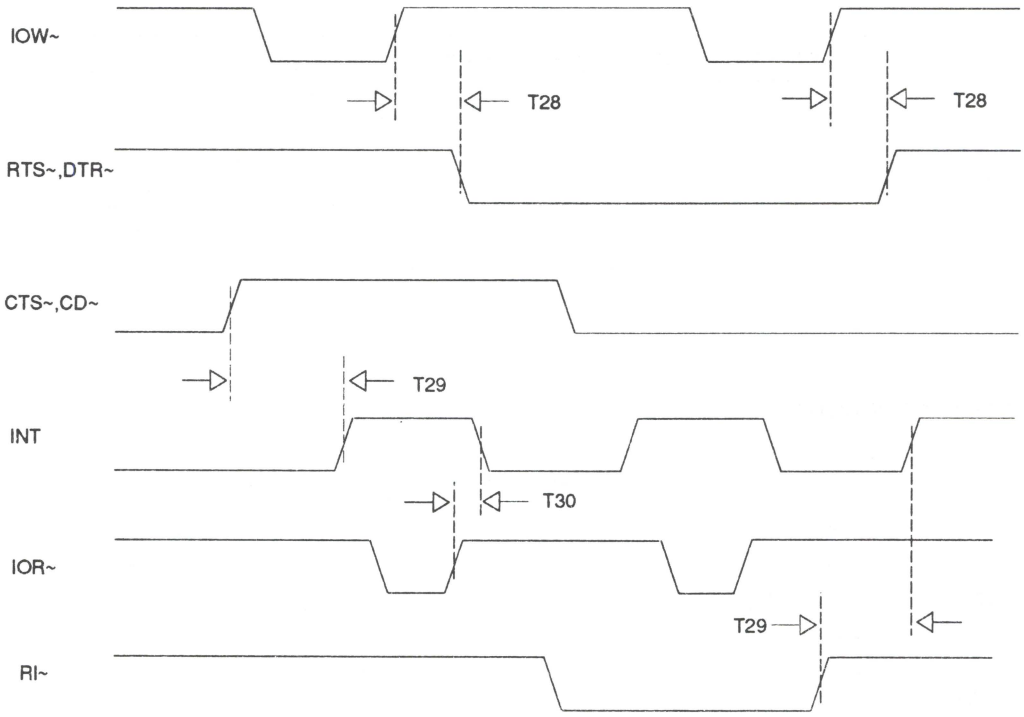


TRANSMITTER TIMING



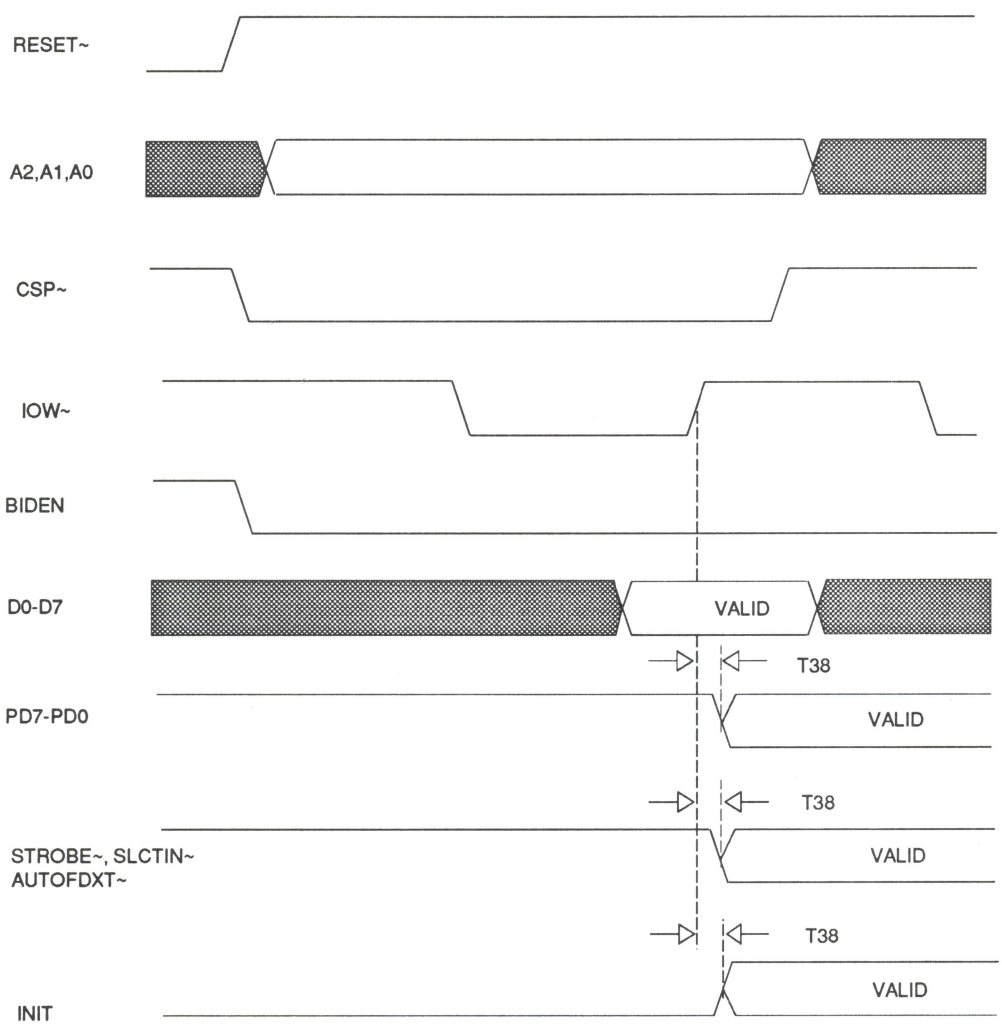
TIMING DIAGRAM

MODEM TIMING



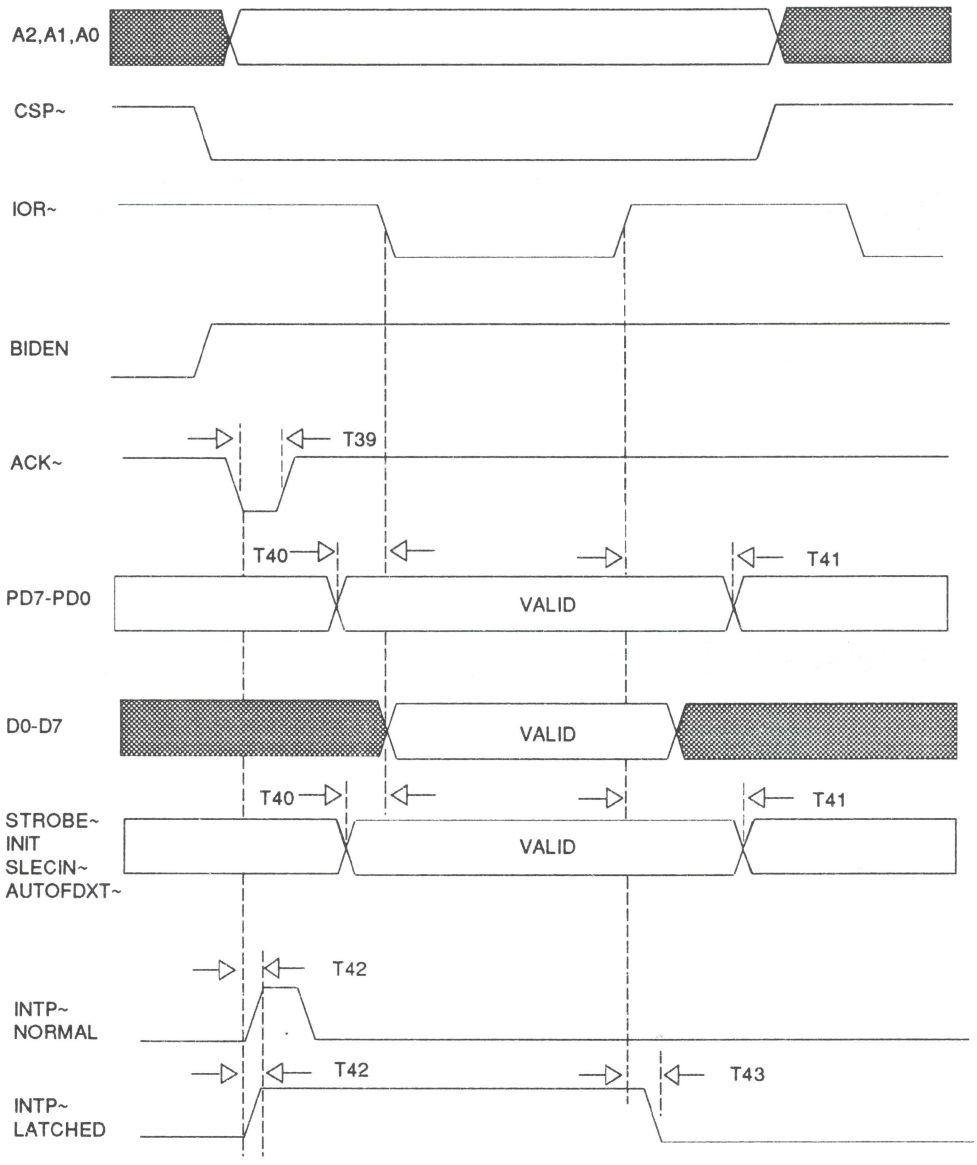
TIMING DIAGRAM

PRINTER WRITE OPERATION



TIMING DIAGRAM

PRINTER READ OPERATION



CMOS Dual Channel UART (DUART)

GENERAL DESCRIPTION

The EXAR Dual Univeral Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communications channels in a single package. The DUART is designed for use in microprocessor bases systems and may be used in a polled or interrupt driven environment.

Two basic versions of the DUART are available, each optimized for use with various microprocessor families: XR- 88C681 for 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx family based systems, and the XR-68C681 for 68000 family based systems. A programmable mode of the XR- 88C681 version provides an interrupt daisy chain capability for use in Z80 and Z8000 based systems. However, the bus interfaces are general enough to allow interfacing with other microprocessors and microcontrollers. The XR-88C681 and XR-68C681 are enhanced versions of the Signetics, Motorola 2681 and 68681 respectively with tighter electrical specifications, and are pin and function compatible with those devices.

The DUART is fabricated using advanced two-layer metal high density CMOS process to provide high performance and low power consumption and is packaged in a 40 pin DIP. The XR-88C681 is also available in a 28 pin DIP.

FEATURES

Full Duplex, Dual Channel, Asynchronous Receiver and Transmitter
Quadruple-Buffered Receiver, Dual-Buffered Transmitter
Stop Bits Programmable in 1/16-bit Increments
Internal Bit Rate Generator with 23 Bit Rates
Independent Bit Rate Selection for Each Receiver and Transmitter
Maximum Bit Rate: 1x Clock - 1 Mb/Sec, 16x Clock - 125Kb/Sec
Normal, Autoecho, Local Loopback, and Remote Loopback Modes
Multi-Function 16-Bit Counter/Timer
Interrupt Output with Eight Maskable Interrupting Cond.
Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
Up to 15 I/O Pins (Depending on Package and Version)
Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On-Chip Oscillator for Crystal
Standby Mode to Reduce Operating Power
Advanced CMOS Low Power Technology

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	65°C to + 150°C
All Voltages with Respect to Ground	0.5 V to + 7.0 V

ORDERING INFORMATION

XR-88C681/40XX,XR-88C681/28XX,XR-88C681/24XX* and XR-68C681XX are offered in the following packages:

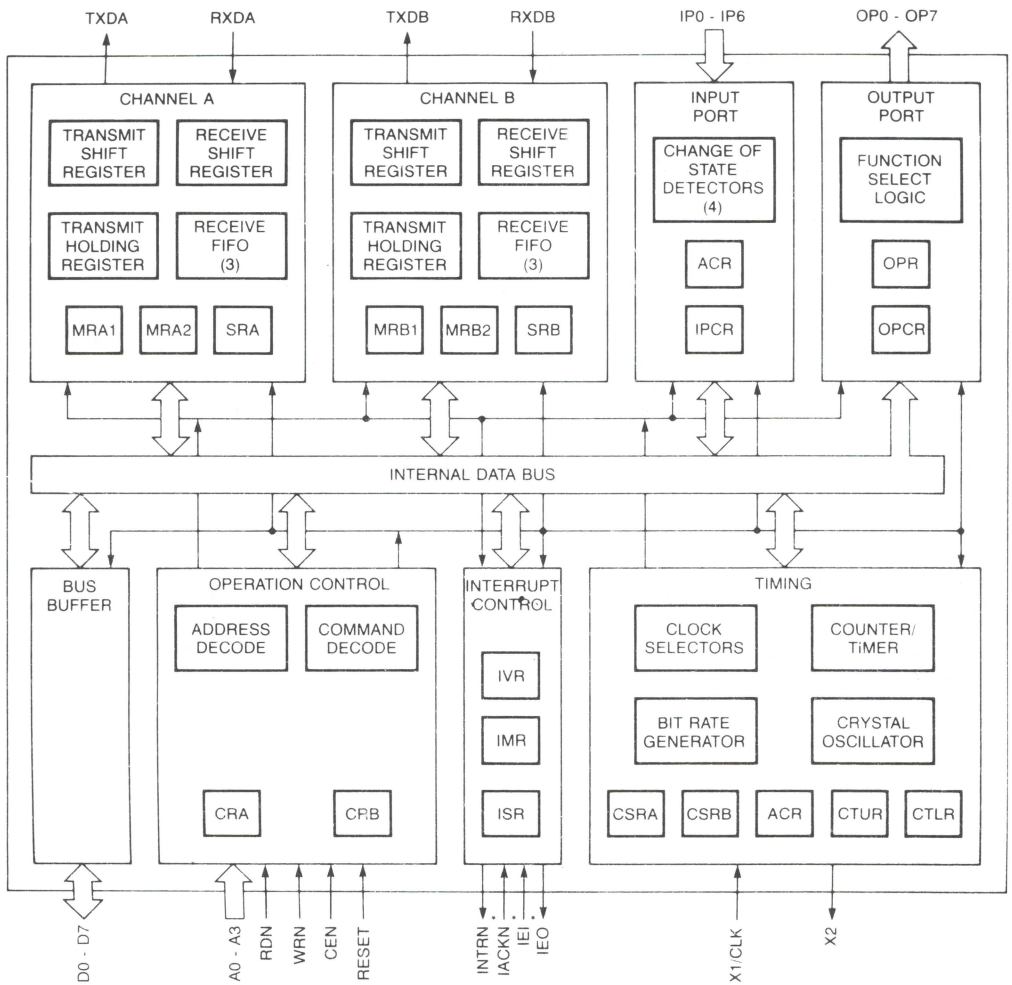
XX=Suffix	Package	Operating Temperature
CN	Ceramic	0°C to + 70°C
N	Ceramic	-40°C to + 85°C
M	Ceramic	-55°C to + 125°C
CP	Plastic	0°C to 70°C
P	Plastic	-40°C to 85°C
CJ	PLCC	0°C to 70°C
J	PLCC	-40°C to 85°C

For pin assignments, refer to the end of this datasheet

SYSTEM DESCRIPTION

Each channel of the DUART may be independently programmed for operating mode and data format. The operating speed of each receiver and transmitter can be selected from one of 23 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an external 1x or 16x clock. The bit rate generator can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the DUART attractive for split-speed channel applications such as clustered terminal systems.

BLOCK DIAGRAM - XR-88C681

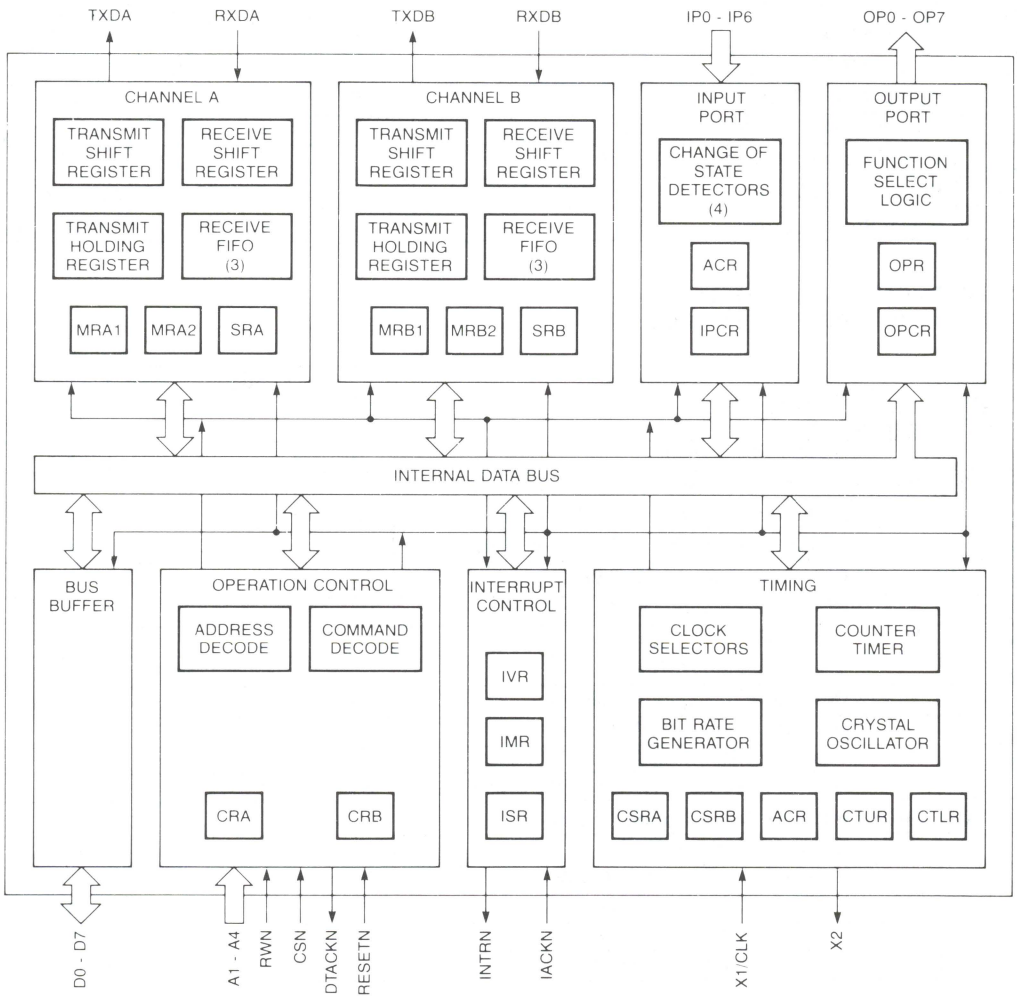


* ALTERNATE FUNCTIONS FOR IP4 - IP6

Received data is quadruple-buffered in an on-chip FIFO to minimize the risk of receiver overrun or to reduce overhead in interrupt-driven applications. The DUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving DUART is full, thus preventing loss of data.

The DUART also provides a general purpose 16-bit counter/timer (which may also be used as a programmable bit rate generator), a multi-purpose input port and a multipurpose output port. These ports can be used as general purpose I/0 ports or can be assigned specific functions such as clock inputs or status/interrupt outputs under program control.

BLOCK DIAGRAM - XR-68C681



DC ELECTRICAL CHARACTERISTICS

TA = 0°C to + 70°C, V_{CC} = 5.0V + 5% [3, 4, 15] unless otherwise specified

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max		
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage (except X1/CLK)	2.0		V_{CC}	V	
V_{IH}15	Input High Voltage	2.2				T_A= -55°C to 125°C
V_{IHI}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage (except open drain outputs)	2.4			V	I_{OH} = -400 µA
I_{IL}	Input Leakage Current (except X1 /CLK, X2)	-10		10	µA	V_{IN} = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		-4		mA	V_{IN} = 0
I_{X2L}	X2 Input Low Current		-30		µA	V_{IN} = V_{CC}
I_{X1H}	X1 Input High Current		0.2		mA	V_{IN} = V_{CC}
I_{X2H}	X2 Input High Current		30		µA	V_{IN} = V_{CC}
I_{LL}	Data Bus 3-State Leakage Current	-10		10	µA	V_O = 0 to V_{cc}
I_{OC}	Open Drain Output Leakage Current	-10		10	µA	V_O = 0 to V_{cc}
I_{CCA}	Power Supply Current [5]		7	10	mA	Active mode
I_{CCS}	Power Supply Current [5]		6	10	mA	Standby mode

AC ELECTRICAL CHARACTERISTICS

TA = 0°C to +70°C, V_{CC} = 5.0V 1 5% [3, 4, 6]

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
Reset Timing (Figure 4)					
t_{RES}	RESET Pulse Width	1.0			µs
XR88C681 Read and Write Cycle Timing (Figures 5 and 6) [7]					
t_{AS}	A0-A3 Setup Time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 Hold Time from RDN, WRN High	0			ns
t_{CS}	CEN Setup Time to RDN, WRN Low	0			ns
t_{CH}	CEN Hold Time form RDN, WRN High	0			ns
t_{RW}	RDN, WRN Pulse Width	200			ns
t_{DD}	Data Valid from RDN Low			160	ns
t_{DF}	Data Bus Floating form RDN High	10		90	ns
t_{DS}	Data Setup Time to WRN High	90			ns
t_{DH}	Data Hold Time for WRN High	5			ns
t_{RWD}	High Time Between Reads and/or Writes 8,9	180			ns
XR88C681 Z-mode Interrupt Cycle Timing (Figure 6)					
t_{DIO}	IEO Delay Ti me from IEI			90	ns
t_{IAS}	IACKN Setup Time to RDN Low	Note 10			ns
t_{IAH}	IACKN Hold Time for RDN High	0			ns
t_{EIS}	IEI Setup Time to RDN Low	45			ns
t_{EOD}	IEO Deay me from INTRN Low			90	ns

Notes: See page 23

AC ELECTRICAL CHARACTERISTICS continued

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% 3,4,6

Symbol	Parameter	Limits Min.	Typ.	Max.	Units
XR68C681 Read, Write and Interrupt Cycle Timing (Figures 7, 8, 9)					
t_{AS}	A1-A4 Setup Time to CSN Low	10			ns
t_{AH}	A1-A4 Hold Time from CSN High	0			ns
t_{RWS}	RWN Setup Time to CSN Low	0			ns
t_{RWH}	RWN Hold Time from CSN High	0			ns
t_{CSW}	CSN High Pulse width 9, 11	90			ns
t_{CSD}	CSN or IACKN High from DTACKN Low 12	10			ns
t_{DD}	Data Valid from CSN or IACKN Low			160	ns
t_{DF}	Data Bus Floating from CSN or IACKN High	10		90	ns
t_{DS}	Data Setup Time to CLK High	90			ns
t_{DH}	Data Hold Time from CSN High	0			ns
t_{DAL}	DTACKN Low from Read Data Valid	0			ns
t_{DCR}	DTACKN Low (Read Cycle) from CLK High			110	ns
t_{DCW}	DTACKN Low (Write Cycle) from CLK High			110	ns
t_{DAH}	DTACKN High from CSN or IACKN High			90	ns
t_{DAT}	DTACKN High Impedance from CSN or IACKN High			110	ns
t_{CSC}	CSN or IACKN Setup Time to High 13	80			ns
Port Timing (Figure 10) 7					
t_{PS}	Port Input Setup Time to RDN/CSN Low	0			ns
t_{PH}	Port Input Hold Time from RDN/CSN High	0			ns
t_{PD}	Port Output Valid from WRN/CSN High			350	ns
Interrupt Output Timing (Figure 11)					
t_{IR}	INTRN or OP3-OP7 When Used As Interrupts High from:				
	Clear of Interrupt Status Bit in ISR or IPCR			270	ns
	Clear of Interrupt Mask Bit in IMR			270	ns
Clock Timing (Figure 12)					
t_{CLK}	X1/CLK (External) High or Low Time	100			ns
t_{CLK}	X1/CLK Crystal or External Frequency	2.0	3.6864	4.0	MHz
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2)	100			ns
f_{CTC}	Counter/Timer External Clock Frequency (IP2)	0		4.0	MHz
t_{RTX}	RXC and TXC (Eternal) High or Low Time 14	220			ns
f_{RTX}	RXC and TXC (External) Frequency				
	16x	0		2.0	MHz
	1x	0		1.0	MHz
Transmitter Timing (Figure 13)					
t_{TXD}	TXD Output Delay from TXC External) Low			315	ns
t_{TCS}	TXD Output Delay from TXC (Internal) Output Low	0		135	ns
Receiver Timing (Figure 14)					
t_{RXS}	RXD Data Setup Time to RXC (External High)	210			ns
t_{RXH}	RXD Data Hold Time from RXC (External) High	180			ns

Note: See page 23

PIN DESCRIPTIONS - XR-88C681

Mnemonic	Type	Description
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and the DUART take place over this bus. The bus is three-stated when the CEN input is high, except during an IACKN cycle in the Z-mode.
A0-A3	I	**Address Inputs.** These inputs select the DUART register or port for the current read/write operation.
CEN	I	**Chip Enable.** Active low. The data bus is three-stated when CEN is high. Transfers between the CPU and the DUART via D0-D7 are enabled when CEN is low.
WRN	I	**Write Strobe.** Active low. A low on this input while CEN is also low writes the contents of the data bus into the addressed destination. The transfer occurs on the rising edge of WRN.
RDN	I	**Read Strobe.** Active low. A low on this input while CEN is also low places the contents of the addressed source on the data bus. The transfer begins on the talling edge of RDN.
RESET	I	**Master Reset.** A high on this pin clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to OFH, stops the counter/timer, puts OP0-OP7 in the high state, and places both serial channels in the inactive state with the TXDA and TXDB outputs marking (high).
INTRN	O	**Interrupt Request.** Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
X1/CLK	I	**Crystal or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used (see figure 12). If the oscillator is not used, an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used a capacitor must also be connected from this pin to ground. This pin may be connected to ground or left open if an external clock is supplied at X1/CLK.
RXDA,RXDB	I	**Receiver Serial Data Inputs.** The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXDA,TXDB	O	**Transmitter Serial Data Outputs.** The least significant bit is transmitted first. Held in the marking (high) state when the transmitter is idle or disabled or when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.
OP0	O	**Output 0.** Can be programmed as a general purpose output or as the channel A request-to-send output (RTSAN). Active low.
OP1	O	**Output 1.** Can be programmed as a general purpose output or as the channel B request-to-send output (RTSBN). Active low.

Mnemonic	Type	Description
OP2	O	**Output 2.** Can be programmed as a general purpose output, the channel A transmitter 1x or 16x clock output, or the channel A receiver 1x clock output. Active low. (40-pin package only).
OP3	O	**Output 3.** Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or an open drain counter/timer low. (40-pin package only).
OP4	O	**Output 4.** Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output. Active low.(40-pin package only).
OP5	O	**Output 5.** Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output. Active low. (40-pin package only).
OP6	O	**Output 6.** Can be programmed as a general purpose output or as an open drain channel A TXRDY output. Active low. (40-pin package only).
OP7	O	**Output 7.** Can be programmed as a general purpose output or as an open drain channel B TXRDY output. Active low. (40-pin package only).
IP0	I	**Input 0.** General purpose input or CTSAN, the channel A active low clear-to-send input. (40-pin package only).
IP1	I	**Input 1.** General purpose input or CTSBN, the channel B active low clear-to-send input. (40-pin package only).
IP2	I	**Input 2.** In the 40-pin package version, when configured in 1-mode, IP2 is a general purpose input or the counter/timer external clock input. When configured in Z-mode, IP2 is a general purpose input, the counter/timer external clock input, or the channel B transmitter and receiver external clock input. In the 28-pin package version, IP2 is a multi-purpose input. It can be used as a general purpose input, the channel A and B receiver and transmitter external clock input, or as the external clock input for the counter/timer.
IP3	I	**Input 3.** When configured in 1-mode, IP3 is a general purpose input or the channel A transmitter external clock input. When configured in Z-mode, IP3 is a general purpose input or the channel A transmitter and receiver external clock input. (40-pin package only).
IP4/IEI	I	**Input 4 or Interrupt Enable Input.** When configured in I-mode, this pin is a general purpose input or the channel A receiver external clock input (IP4). When configured in Z-mode, this pin is the interrupt enable active high input (IEI). (40-pin package only).
IP5/IEO	I/O	**Input 5 or Interrupt Enable Output.** When configured in I-mode, this pin is a general purpose input or the channel B transmitter external clock input (IP5). When configured in Z-mode, this pin is the interrupt enable active high output (IEO). (40-pin package only).
IP6/IACKN	I	**Input 6 or Interrupt Acknowledge Input.** When configured in I-mode, this pin is a general purpose input or the channel B receiver external clock input (IP6). When configured in Z-mode, this pin is the interrupt acknowledge active low input (IACKN). (40-pin package only).
V_{CC}	I	**+5 Volt Power Input.**
GND	I	**Signal and Power Ground.**

PIN DESCRIPTIONS - XR-68C681

Mnemonic	Type	Description
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and the DUART take place over this bus. The bus is three-stated when the CSN input is high, except during an IACKN cycle.
A1-A4	I	**Address Inputs.** These inputs select the DUART register or port for the current read/write operation.
CSN	I	**Chip Select.** Active low. The data bus is three-stated when CSN is high. Transfers between the CPU and the DUART via D0-D7 are enabled when CSN is low.
R/WN	I	**Read/Write.** A high input while CSN is low indicates a read cycle while a low input while CSN is also low indicates a write cycle.
DTACKN	O	**Data Transfer Acknowledge.** Three-state, active low. Assertion of DTACKN indicates that data is present on the bus during a read or interrupt acknowledge cycle and that the data from the bus has been written into the addressed destination during a write cycle.
RESETN	I	**Master Reset.** A low on this pin clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to OFH, stops the counter/timer, puts OP0-OP7 in the high state, and places both serial channels in the inactive state with the TXDA and TXDB outputs marking (high).
INTRN	O	**Interrupt Request.** Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
IACKN	I	**Interrupt Acknowledge.** Active low. Assertion of IACKN indicates that the current bus cycle is an interrupt acknowledge cycle. If the DUART has an interrupt active, it responds by placing the interrupt vector on the data bus and asserting DTACKN.
X1/CLK	I	**Crystal or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used (see figure 12). If the oscillator is not used an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used a capacitor must also be connected from this pin to ground. This pin may be connected to ground or left open if an external clock is supplied at X1/CLK.
RXDA,RXDB	I	**Receiver Serial Data Inputs.** The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXDA,TXDB	O	**Transmitter Serial Data Outputs.** The least significant bit is transmitted first. Held in the marking (high) state when the transmitter is idle or disabled or when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.

Mnemonic	Type	Description
OP0	O	**Output 0.** Can be programmed as a general purpose output or as the channel A request-to-send output (RTSAN). Active low.
OP1	O	**Output 1.** Can be programmed as a general purpose output or as the channel B request-to-send output (RTSBN). Active low.
OP2	O	**Output 2.** Can be programmed as a general purpose output, the channel A transmitter 1x or 16x clock output, or the channel A receiver 1x clock output. Active low.
OP3	O	**Output 3.** Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or as an open drain counter/timer ready output. Active low.
OP4	O	**Output 4.** Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output. Active low.
OP5	O	**Output 5.** Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output. Active low
OP6	O	**Output 6.** Can be programmed as a general purpose output or as an open drain channel A TXRDY output. Active low.
OP7	O	**Output 7.** Can be programmed as a general purpose output or as an open drain channel B TXRDY output. Active low.
IP0	I	**Input 0.** General purpose input or CTSAN, the channel A active low clear-to-send input.
IP1	I	**Input 1.** General purpose input or CTSBN, the channel B active low clear-to-send input.
IP2	I	**Input 2.** General purpose input, counter/timer external clock input. or channel B receiver external clock input.
IP3	I	**Input 3.** General purpose input or channel A transmitter external clock input.
IP4	I	**Input 4.** General purpose input or channel A receiver external clock input.
IP5	I	**Input 5.** General purpose input or channel B transmitter external clock input.
V_{CC}	I	**+5 Volt Power Input.**
GND	I	**Signal and Power Ground.**

PRINCIPLES OF OPERATION

As illustrated in the block diagram, the DUART consists of the following major blocks:

Data Bus Buffer
Operation Control
Interrupt Control
Timing Circuits
Input Port
Output Port
Serial Channels A and B

Data Bus Buffer

The data bus buffer provides the interface between the internal and exernal data busses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the DUART.

Operation Control

The operation control logic receives operating commands from the CPU and generates signals to various sections of the DUART to appropriately control the device's operation. It contains address decoding and read and write circuits to permit communications with the microprocessor and registers to store configuration commands and device status.

The XR-68C681 version includes a data transfer acknowledge (DTACKN) output which is asserted during data transfer cycles to verify that the requested operation has been completed. It indicates that the input data has been latched during a write cycle, that the requested data is on the data bus during a read cycle, or that the interrupt vector is on the data bus during an interrupt acknowledge cycle.

The addressing of the internal elements of the DUART is described in Table 1. Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers, The pointer is set to point to MR1x by a hardware reset or by invoking a 'reset pointer' command to the appropriate channel via its command register, Any read or write operation to the mode register while the pointer is pointing at MR1x switches the pointer to point to MR2x. The pointer then remains pointing to MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset as described above.

Interrupt Control

An interrupt request output signal (INTRN) is provided which may be programmed to be asserted upon the occurrence of any of the following events:

Transmit holding register A or B empty
Receive holding register A or B ready
Receive FIFO A or B full
Start or end of received break, channel A or B
Counter terminal Count reached
Change of state on input pins IP0, IP1, IP2 or IP3

Associated with the interrupt system are the interrupt status register (ISR), the interrupt mask register (IMR),

Table 1. DUART Port and Register Addressing

A3	A2	A1	A0	Read	Write
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Interrupt Status Register, Masked (ISR)	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register, Unmasked (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper Byte (CTU)	Counter/Timer Upper Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte (CTL)	Counter/Timer Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	RESERVED	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Configuration Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Note: in XR68C681 version, replace A3-A0 above with A4-A1 respectively.

and the interrupt vector register (IVR). The ISR indicates the current state of all the potential interrupting conditionslisted above. The IMR may be programmed to select only certain of these conditions to assert the, INTRN output. The ISR can be read by the CPU either masked or unmasked by the IMR. If read masked by the IMR, only the state of the conditions which have been programmed to cause an interrup is output. If read unmasked, the state of all condtions, whether programmed to cause an interrupt or not, is output.

The XR-88C681/40 version may be programmed to operate in two modes to accommodate different CPU interface requirements. In the 'I-mode', which is the default mode after a hardware reset, interrupt prioritiation and interrupt vector 'generation, if required, are implemented using external hardware. In this mode, the on-chip interrupt vector register is not utilized and is available for use as an auxiliary read/write register for any purpose.

In the 'Z' mode, which is invoked via a command to command register B, pins 37, 38 and 39 are designated interrupt acknowledge input (IACKN), interrupt enable output (IEO) and interrupt enable input (IEI) respectively. IEI and IEO are the input and output of an interrupt daisy chain, as illustrated in Figure 1. IEI high means that the DUART may generate an interrupt request. A device with IEI high which is requesting an interrupt sets its IEO low to inhibit lower priority devices from generating their own interrupt requests. A device with its IEI low is inhibited from generating an interrupt and must also keep its IEO output low.

Sometime after the interrupt request is issued, the CPU will respond with an interrupt acknowledge cycle, asserting the IACKN and RDN inputs as shown in Figure 1. Assertion of IACKN must precede assertion of RDN. The time between the assertion of IACKN and the assertion of RDN allows the daisy chain to stabilize. The DUART is inhibited from issuing a new interrupt request while IACKN is asserted.

If the DUART is requesting an interrupt and its IEI is high when the leading edge of RDN is received, it is

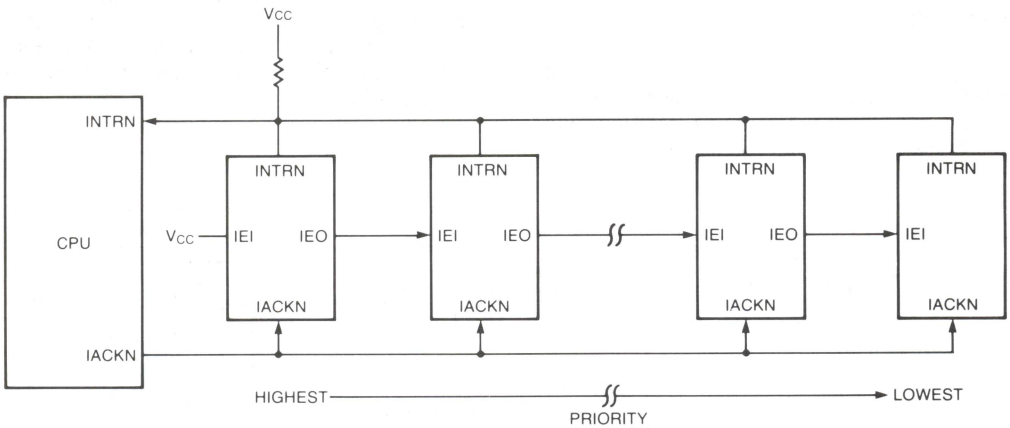


Figure 1A. Daisy chained Interrupt Block Diagram

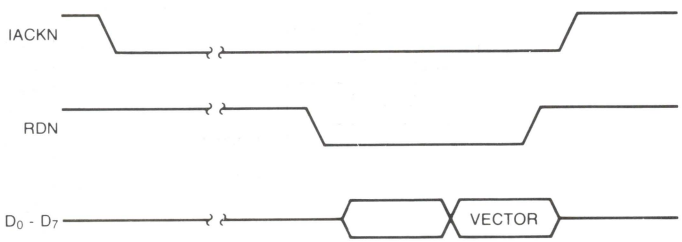


Figure 1B. Daisy chained Interrupt Timing

the highest priority device making the request. It sets its internal 'interrupt under service' (IUS) latch, which keeps its IEO negated regardless of what happens to the interrupt request (which may be negated, for example, by the read of the RHR). It also places the vector from the IVR on the data bus. Keeping IEO low prevents lower priority devices in the daisy chain from requesting an interrupt until the higher priority interrupt has been serviced. Upon completing the service routine, the CPU must issue a 'reset IUS latch' command to the chip, which resets the latch and returns the daisy chain to its normal condition.

In the XR-68C681 version, if the DUART has its interrupt request axtive, it responds to assertion of its IACKN input by placing the, vector from the IVR on the data bus and asserting DTACKN. Otherwise, it ignores IACKN.

In either version, outputs OP3-OP7 can be, programmed to provide separate open drain interrupt requests for transmitters A and B, receivers A and B, and the counter/ timer. See pin description.

Timing Circuits

The timing block contains a crystal oscillator, a bit rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors. A detailed block diagram of this section is shown in Figure 2.

Crystal Oscillator

The crystal oscillator operates from a crystal connected between the X1/CLK and X2 pins. A crystal frequency of 3.6864 MHz is required for generation of standard bit rates by the bit rate generator (see Table 5). If an external clock is available, it may be connected to X1/CLK, with X2 left open or connected to ground. The output of the oscillator is used by the BRG, the C/T and other internal circuits. This requires that a clock within the specified limits always be supplied to the DUART.

Bit Rate Geneator

The BRG uses the crystal oscillator or external clock as an input and generates the clock for 23 commonly used data communicaitons bit rates ranging from 50 to 115.2K bits per second. The actual clock frequencies output from the BRG are at 16 times these rates. The counter/timer can also be used as a programmable bit rate generator to produce a 16x clock for any bit rate not provided by the BRG. The four clock select multiplexers allow each receiver and transmitter to independently select its operating frequency as one of the outputs from the BRG, the output of the couner/timer, or an external clock. Table 4 defines the input pins for external clocking for the three version of the DUART.

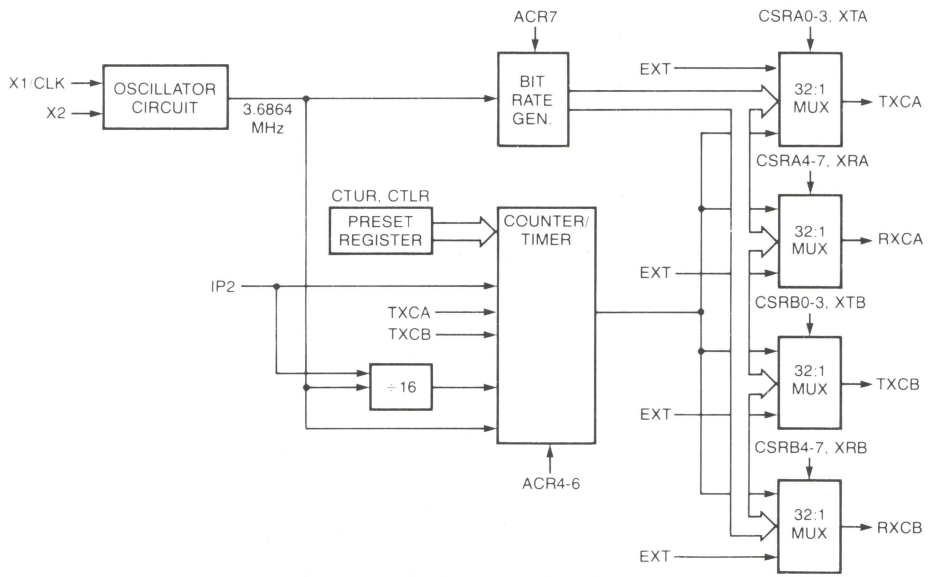


Figure 2. Timing Circuits Block Diagram

Counter/Timer

The C/T is a programmable 16-bit down-counter which can use one of several timing sources as its input. The CIT output is available to the clock selectors for use as a programmable bit rate for any receiver or transmitter, can be programmed to generate an interrupt each time it reaches its terminal count of OOOOH, and can also be programmed as an output at OP3.

In the timer mode, the C/T acts as a programmable divider and generates a square wave whose period is twice the value (in clock periods) of the contents of the counter/timer registers CTUR and CTLR. The contents of these registers may be changed at any time, but will only begin to take effect at the next half cycle of the square wave. The C/T begins operation using the values in CTUR/CTLR upon receipt of a 'startcounter' command (see Table 1). The C/T then runs continuously. A subsequent 'start counter' command causes the C/T to terminate the current timing cycle and to begin a new timing cycle using the current values in CTUR and CTLR. The counter ready status bit (ISR [3]) is set once each cycle of the square wave. This allows use of the C/T as a periodic interrupt generator if the condition is programmed to generate an interrutpt via the interupt mask register. The status bit can be reset by issuing a 'stop counter' command (see Table 1). In this mode, however, the command does not actually stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses written into CTUR/CTLR, beginning at the receipt of a 'start counter' command. The counter ready status bit (ISR[3]) is set upon reaching the count of OOOOH. The C/T will continue to count past this (with the next count being FFFFH) until it is stopped by the CPU via a 'stop counter' command. If OP3 is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time the output goes low. OP3 returns to the high state and ISR [3] is cleared when the counter is stopped, A 'start counter' command while the counter is running restarts the counter with the values in CTUR/CTLR. The CPU may change CTUR or CTLR at any time but the new count takes effect only on the next start counter command. If new values are not programmed, the previous values are preserved and used for the next cycle.

In counter mode, the current value in the C/T may be read by the CPU by reading the upper and lower halves of the C/T separately (see Table 1), stopping the counter when it is read is recommended in order to prevent potential problems which may occur if a carry from the lower half to the upper half occurs between the times that the two halves are read. However, note that a new start counter command will cause the counter to begin counting using the values in CTUR/CTLR.

Input Port

The current state of the inputs to this unlatched port can be read by the CPU by performing a read as described in Table 1. A high input results in a logic "1" while a low input results in a logic "0". The pin description tables describe the alternate uses for the input pins, such as clock inputs and interrupt control signals. A read of the input port will show the state at the pin, regardless of its programmed function. When the port is read, bit 7 will always read as a logic "1" in both versions of the DUART, and D6 will reflect the state of IACKN in the XR-68C681 version, Change of state detectors are provided for inputs IPO-IP3. These inputs are sampled by the 38.4 kHz, output of the BRG (2.4 Kbps x 16). A high-to-low or low-to-high transition at these input lasting at least two clock periods (approximately 50 µs) will guarantee that the corresponding bit in the input port change register (IPCR) will be set, although it may be set by a change of state as short as 25 µs, The status bits in the IPCR are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt.

Output Port

The 8-bit output port can be used as a general purpose output port or can be used to output timing and status signals by appropriate programming of the mode registers (MR 1 A, MR2A, MR1B, MR2B) and with output port configuration register, When used to output status signals the pins are open drain, which allows their use in a wire-OR interrupt scheme.

When used as a general purpose output port, the outputs are the complements of the output port register (OPR). $OPR_{(n)}$ = 1 results in $OP_{(n)}$ low while $OPR_{(n)}$ = 0 results in $OP_{(n)}$ high. Bits of OPR can be set and reset individually. A bit is set by the address-triggered 'set output port bits' command (see Table 1) with the accompanying data specifying the bits to be set (1 = set, 0 = no change). A bit is reset by the address-triggered 'reset output port bits' command (see Table 1) with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Serial Channels A and B

Each serial channel of the DUART comprises a full duplex asynchronous receiver and transmitter. The two channels can independently select their operating frequency (from the BRG, the C/T, or an external clock) as well as operating mode. Besides the normal mode in which the receiver and transmitter of each channel operate independently, the DUART can be configured to operate in various looping modes, which are useful for local and remote diagnostics, as well as in a wake-up mode used for multi-drop applications.

Note: In the descriptions which follow, the transmitter and receiver are described for either channel. References to in-. put and output pins and control and status bits and registers apply to either channel unless otherwise noted.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream at the TXD pin, adding start, stop and optional parity bits as required by the asynchronous protocol.

The DUART is conditioned to transmit data when the transmitter is enabled via the command register. It indicates that it is ready to accept a character from the CPU for serialization by setting the TXRDY bit in the status register. This condition can be programmed to assert an interrupted request via the INTRN output and can also be programmed to assert the OP6 output (channel A) or the OP7 output (channel B). These conditions are negated when the CPU loads a character into the transmit holding register (THR). Data is transferred from the THR to the transmit shift register (TSR) immediately if the TSR is idle, or when it completes serialization of the previous character. The TXRDY condition is then asserted again. Thus, one full character time of buffering is provided. Note that the THR will not accept characters while the transmitter is disabled.

The transmitter sends a start bit followed by the programmed number of data bits (least significant bit first), an optional parity bit, and the programmed number of stop bits and then begins transmission of the next character if one has been loaded into the THR. Otherwise, the TXD output will remain high and the TXEMT status bit will be set following the transmission of the stop bits. Transmission resumes and the TXEMTstatus bit is cleared when the CPU loads a new character into the THR. The transmitter can be forced to send a continuous low at TXD by invoking a 'send break' command.

If the transmitter is disabled, it continues operating until the character currently being serialized, and any in the THR, are completely sent out. The transmitter can be reset by a software command. In this case, operation ceases immediately and the transmitter must be re-enabled before resuming operation.

Setting MR2[4] of the appropriate channel programs its transmitter to begin transmission of a character only if the channel's clear-to-send input pin (IPO for channel A, IP1 for channel B) is low. If CTSN goes high in the middle of a transmission, the transmission of the current character is completed but TXD remains high and the next character will not be sent until CTSN is low again. Setting MR2151 of the appropriate channel programs the transmitter to automatically deactivate its request-to-send output pin (OPO for channel A, OP1 for channel B). If so programmed, and the transmitter has been disabled, the RTSN output will be negated one bit time after the characters in the TS and THR (if any) are completely sent.

Receiver

The receiver accepts serial data at its RXD pin, checks for a proper start bit, converts the serial input to parallel form, checks the parity bit (if parity is specified), checks for presence of a stop bit, performs several other tests on the received data, and sends the assembled character to the CPU.

Each receiver is conditioned to receive data when it is enabled via the command register. It looks for a high to low (mark to space) transition indicating a start bit at the RXD input. If a transition is detected, the state of RXD is sa pied each 16x clock for 7= clocks (16x clock mode) or at the next rising edge of the bit time clock (x clock If RXD is detected high at these sample times, the start bit is invalid and the search for a start bit begins again. If RXD remains low, a valid start bit is assumed and the receiver continues to sample the data at one bit time intervals, at the theoretical center of the bit, until the programmed number of data bits (LSB first), the parity bit (if any), and one stop bit have been assembled. The data is then transferred to the receive holding register (RHR) with the most significant unused bits set to zero. The status conditions (parity error, framing error, overrun error, and break received) are set to indicate to the CPU that a character is available to be read, Setting of RXRDY can be programmed to generate an interrupt request via INTRN and to assert OP4 (channel A) or OP5 (channel B).

After the stop bit position is sampled, the receiver will immediately begin to look for the start bit of the next

character. However, if a non-zero character was received without a stop bit (framing error) and RXD remains low for half a bit time after sampling of the stop bit, the receiver operates as if a new start bit transition had been detected at that point (half a bit time after the sampling of the stop bit).

If a break is received (an all zeroes character including the first stop bit), only a single character consisting of all zeroes will be loaded into the FIFO and the break received status bit will be set, no matter how long the break condition persists. RXD must return to a high condition for at least half a bit time before the search for a new start bit begins again.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the topmost empty position in the FIFO, RXRDY is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. Either of these bits can be selected to assert an interrupt. A read of the R H R outputs the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data.

In addition to the data word, three status bits are appended to each character position in the FIFO. These are parity error, framing error, and received break. Status can be provided in two ways, as programmed by MR1[5] in the channel's mode register. In the 'character' mode status is provided on a character by character basis: the status applies only to the character at the top of the FIFO. In the block mode, these three bits in the status register are the cumulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode, reading the status register does not affect the FIFO. The FIFO is popped only when the RHR is read. Therefore, the status register should be read prior to reading the RHR. Also note that PE, FE and received break status bits are valid only when RXRDY in the status register is asserted.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If a new start bit is detected while this condition exists, the character previously in the shift register is lost and the overrun error status bit is set. The contents of the FIFO are not affected when this occurs.

If the receiver is disabled, the contents of the FIFO are maintained and can be read by the CPU. Resetting the receiver initializes the FIFO pointers and clears the status bits immediately. In either case, any character currently being assermbled is lost and operation does not resume until the receiver is re-enabled.

Setting MR[7] of the appropriate channel programs the receiver to automatically control de-activation of the request-to-send output (OP0 for channel A, OP1 for channel B). If so programmed, RTSN will be negated when a valid start bit is received while the FIFO is full, and will automatically be re-asserted when a FIFO position becomes available for that character. This feature can be used to prevent an overrun in the receiver by connecting the RTSN output to the CTSN input of the transmitting device.

Multidrop (8051 9-bit) Mode

Each serial channel of the DUART can be configured to operate in a wake-up mode useful for multidrop or multiprocessor applications. This mode is compatible with the serial 'Nine-bit Mode' of 8051-family microcomputers. In this mode of operation a master station, connected to a maximum of 256 slave stations, transmits an address character followed by a block of data characters targeted for the addressed slave station. The slave stations normally have their receivers disabled. However, in this mode, the slave receivers monitor the incoming data stream and wake up the CPU (by asserting RXRDY) when any address character is detected. The slave station CPU then compares the received address to its own assigned address and enables the receiver, if it wishes, to receive the subsequent block of data, or leaves the receiver disabled if it does not. Upon completion of reception of the block of data, the receiver is disabled to re-initiate the process.

The multidrop mode is selected by programming MR [4:3] of the channel to '11'. In this mode, a transmitted character consists of a start bit, the programmed number of data bits, an addresss/data flag bit (A/D), and the programmed number of stop bits. A/D = 0 indicates that the character is data, while A/D = 1 identifies it as an address. The CPU controls the state of A/D in the transmitted character by programming MR 1 [2] of the channel prior to loading the data bits into the THR. MR1[2] = 0 results in A/D = 0 and MR1[2] = 1 results in A/D = 1.

In the multidrop mode, the receiver continuously looks at RXD whether enabled or not. When disabled, it loads a character into the RHR and sets RXRDY if its A/D bit is one (address flag) but discards the character if its A/D bit is zero (data flag). If the receiver is

enabled, all characters received are transferred to the RHR. In either case, the received data bits are loaded into the RHR while the A/D bit is loaded into SR[5] , the status register position normally used for parity error. Framing error, overrun error, and break detect status bits operate normally.

Standby Mode

The DUART may be placed in a standby mode to conserve power when its operation is not required. Upon reset the DUART will be in the 'active operation' mode. A 'set stand-by mode' command issued via the channel A command register disables all clocks on the device except for the crystal oscillator, which significantly reduces the operating current, In this mode the only functions which will operate correctly are reading the input port, writing the output port and the 'Set active mode' command. The latter, also invoked via the channel A command register, restores the device to normal operation within 25µs. Resetting the transmitters and receivers and writing 00H into the interrupt mask register before going into the standby mode is recommended to prevent any spurious interrupts from being generated. The chip should be reprogrammed after the 'set active mode' command since register contents are not guaranteed to remain stable during the standby mode. Active operation can also be restored via hardware reset.

PROGRAMMING

Operation of the DUART is programmed by writing control words into the appropriate registers, while operational feed- back is provided by status registers which can be the CPU. Register addressing is shown in Table 1.

A hardware reset clears the contents of SRA, SRB, IMR, ISR, OPR and OPCR and initializes the IVR to OFH. During operation, care should be exercised if the contents of control registers are to be changed, since certain changes may result in improper operation. For example, changing the number of bits per character while data is being received may result in reception of an erroneous character. In general, changes to registers which control receiver or transmitter operation should be made only while the transmitter or receiver are disabled, and certain changes to the ACR should be made only when the C/T is stopped.

Mode, command, clock select, and status registers are duplicated for each channel to provide totally independent operation. Table 2 illustrates the bit assignments for each register.

Note: In the descriptions which follow, registers which are duplicated for each channel are described generically. References to input and output pins and control and status bits and registers apply to each channel unless otherwise noted.

MR1A, MR1B - Channel A/B Mode Register 1

MR1 for each channel is accessed when the channel's MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command invoked via the channel's command register. After reading or writing MR1, the pointer will point to MR2.

MR1[7] - Receiver Request-to-Send Control

This bit controls the negation of the RTSN output (OPO for channel A, OP1 for channel B) by the receiver. RTSN is normally asserted by setting OP0 or OP1 for channels A and B respectively, and negated by resetting the same bit. MR1[7] = 1 causes RTSN to be negated automatically upon receipt of a valid start bit if the channel's FIFO is full and to be re-asserted again when an empty FIFO position becomes available. This flow control feature can be used to prevent overrun of the receiver by using the RTSN output to control transmission of characters to the DUART.

MR1[6] - Receiver Interrupt Select

This bit selects either the RXRDY status bit or the FFULL status bit of the channel to be used for CPU interrupts. It also causes the selected bit to be output on 0P4 (channel A) or 0P5 (channel B) if the pin is programmed as an interrupt output via the OPCR.

MR1[5] - Error Mode Select

This bit controls the operation of the three FIFOed status bits (PE, FE, received break) for the channel. In the character mode these status bits apply only to the character currently at the top of the FIFO. In the block mode these bits are the cummulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command for the channel was issued.

MR1[4:3] - Parity Mode Select

If 'with parity' or :force parity' operation is programmed a parity bit is added to the transmitted characters and the receiver performs a parity check on received characters. See OPERATION section for description of multidrop mode operation.

Table 2. Register Bit Formats

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Rx RTS Control	**Rx Int Select**	**Error Mode**	**Parity Mode**		**Parity Type**	**Bits Per Char.**	
MR1A	0 = no	0 = RXRDY	0 = char	00 = With Parity		0 = even	00 = 5	
MR1B	1 = yes	1 = FFULL	1 = block	01 = Force Parity		1 = odd	01 = 6	
				10 = No Parity			10 = 7	
				11 = Multi-drop Mode			11 = 8	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Channel Mode		**Tx RTS Control**	**CTS Enable Tx**	**Stop Bit Length***			
MR2A	00 = Normal		0 = no	0 = no	0 = 0.563	4 = 0.813	8 = 1.563	C = 1.813
MR2B	01 = Auto Echo		1 = yes	1 = yes	1 = 0.625	5 = 0.875	9 = 1.625	D = 1.875
	10 = Local Loop				2 = 0.688	6 = 0.938	A = 1.688	E = 1.938
	11 = Remote Loop				3 = 0.750	7 = 1.000	B = 1.750	F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/character.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CSRA	**Receiver Clock Select**				**Transmitter Clock Select**			
CSRB	See Table 3				See Table 3			

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Miscellaneous Commands				**Disable Tx**	**Enable Tx**	**Disable Rx**	**Enable Rx**
CRA	See Text				0 = no	0 = no	0 = no	0 = no
CRB					1 = yes	1 = yes	1 = yes	1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	Received Break	**Framing Error**	**Parity Error**	**Overrun Error**	**TXEMT**	**TXRDY**	**FFULL**	**RXRDY**
SRA	0 = no	0 = no	0 = no	0 = no	0 = no	0 = no	0 = no	0 = no
SRB	1 = yes *	1 = yes *	1 = yes *	1 = yes	1 = yes	1 = yes	1 = yes	1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	OP7	**OP6**	**OP5**	**OP4**	**OP3**		**OP2**	
OPCR	0 = OPR[7]	0 = OPR[6]	0 = OPR[5]	0 = OPR[4]	00 = OPR[3]		00 = OPR[2]	
	1 = TXRDYB	1 = TXRDYA	1 = RXRDY/ FFULLB	1 = RXRDY/ FFULLA	01 = C/T Output		01 = TXCA (16X)	
					10 = TxCB (1X)		10 = TXCA (1X)	
					11 = RxCB (1X)		11 = RXCA (1X)	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BRG Set Select	**Counter/Timer Mode and Source**			**Delta IP3 Int**	**Delta IP2 Int**	**Delta IP1 Int**	**Delta IP0 Int**
ACR	0 = Set1	See Table 6			0 = Off	0 = Off	0 = Off	0 = Off
	1 = Set2				1 = On	1 = On	1 = On	1 = On

Table 2. Register Bit Formats (continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IPCR	Delta IP3	Delta IP2	Delta IP1	Delta IP0	IP3	IP2	IP1	IP0
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR	Input Port Change	Delta Break B	RXRDY/ FFULLB	TXRDYB	Counter Ready	Delta Break A	RXRDY/ FFULLA	TXRDYA
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR	Input Port Change Int	Delta Break B Int	RXRDY/ FFULLB Int	TXRDYB Int	Counter Ready Int	Delta Break A Int	RXRDY/ FFULLA Int	TXRDYA Int
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTU	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTL	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IVR	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

MR1[2] - Parity Type Select

This bit selects odd or even parity if 'with parity' mode is programmed and the state of the forced parity bit if the 'force parity' mode is programmed. In the Muiltidrop mode it selects the state of the A/D flag bit. This bit has no effect if 'no parity' mode is programmed.

MR1[1:0] - Bits per Character Select

Selects the number of bits to be transmitted and received in the data field of the character. This does not include start, parity and stop bits.

MR2A, MR2B - Channel A/B Mode Register 2

MR2 for each channel is accessed when the channel's MR Pointer points to MR2, which occurs after any access to the channel's MR1. Reading or writing MR2 does not change the pointer.

MR2[7:6] - Channel Mode Select

Each channel can operate in one of four modes. MR2[7:6] = 00 in the normal mode where the receiver and transmitter operate independently.

MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions apply while in this mode:

1. Received data is transmitted on the channel's TXD output.

2. The receiver must be enabled but the transmitter not be enabled.

3. The channel's TXRDY and TXEMT status bits are inactive.

4. The received parity is checked but is not regenerated for transmission. Thus, transmitted parity is as received.

5. Character framing is checked but the stop bits are retransmitted as received.

6. A received break is echoed as received until the next valid start bit is detected.

7. CPU to receiver communications operate normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. The first is the local loopback mode, selected by MR2[7:6] In this mode:

1. The transmitter output is internally connected to the receiver input.

2. The transmit clock is used for the receiver.

3. The Channel's TXD output is held marking (high).

4. The channl's RXD input is ignored.

5. The transmitter is enabled, but the receiver need not be enabled.

6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is transmitted on the channel's TXD output.

2. Received data is not sent to the CPU and the error status conditions are not checked.

3. Parity and framing (stop bits) are transmitted as received.

4. The receiver must be enabled.

5. A received break is echoed as received until the next valid start bit is detected.

Care must be taken when switching into and out of the various modes. The selected mode will be activated immediately after it is programmed even if this occurs in the middle of transmitting or receiving a character. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RXRDY), and the transmitter is enabled, the transmitter will remain in autoecho or remote loopback mode until one entire stop bit has been transmitted.

MR2[5] - Transmitter Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B) by the transmitter RTSN is normally asserted by setting OP0 or OP1 for channels A and B respectively, and negated by resetting the same bit. MR2[5] = 1 causes OP0 (channel A) or OP1 (channel B) to be reset automatically one bit time after the characters in the channel's transmit shift register and THR, if any, are completely transmitted, including the programmed number of stop bit, if the transmitter has been disabled. This feature can be used to automatically negate RTSN at the conclusion of a message as follows:

1. Program auto-reset mode (MR2[5] = 1).

2. Enable transmitter and assert the channel's RTSN output by setting the appropriate bit in the output port register.

3. Send message.

4. Disable the transmitter after the last character of the message is loaded into the THR.

MR2[4] - Clear-to-Send Control

If this bit is a 0, the channel's CTSN input (IP0 for channel A, IP1 for channel B) has no effect on the transmitter. If the bit is a 1, the transmitter checks the state of its CTSN each time it is ready to send a character. If CTSN is low, the character is transmitted. If CTSN is high, TXD remains in the marking state, and the transmission of the next character is delayed untill CTSN goes low. Changes in CTSN while a character is being serialized do not affect transmission of that character.

MR2[3:0] -Stop Bit Length

This field programs the duration of the stop bit appended to each transmitted character. Stop bit durations of 9/16 to 1 bit time a 1-9/16 to 2 bit times, in increments of 1/16 bit, can be programmed for character lengths of 6, 7 and 8 bits. For a 5-bit character, the stop bit duration can be programmed from 1-1/16 to 2 bit times.

If an external 1x clock is programmed for the transmitter MR2(3) = 0 selects a stop bit duration of

one bit time and MR2[3] = 1 selects a duration of two bit times for transmission.

The receiver only checks for a mark condition at the center of the first stop bit (that is, one bit time after the last data or parity bit is sampled) regardless of the programmed transmitted stop bit length.

CSRA, CSRB - Channel A/B Clock Select Register

CSR[7:4] and CSR[3:0] of each channel operate in conjunction with ACR[7] and the channel's 'set/clear BRG select extend' command's to allow independent selection of the bit rates for the receiver and transmitter respectively. The BRG can generate 23 different bit rates, of which 22 are available simultaneously. The set of 22 is selected by programming ACR [7]. The bit rates generated when using a 3.6864 MHz crystal or an external clock of the same frequency are shown in Table 3, where 'X' refers to the current state of the extend bit. Note that the actual outputs from the BRG are at 16x the bit rates shown in the table. See Table 4 for the source of EXT (external clock) for the three DUART versions.

CRA, CRB - Channel A/B Command Register

Each channel of the DUART has a command register used to supply commands to the respective channel. Multiple commands may be invoked simultaneously be a single write to the command register as long as the commands are non-conflicting.

CR[7:4] - Miscellaneous Commands

The encoded value of this field specifies a single command as follows:

0 0 0 0 - Null Command.

0 0 0 1 - Reset MR Pointer - causes the channel's MR pointer to point to MR1.

0 0 1 0 - Reset Receiver - resets the receiver as if a hardwdre reset had been applied. The receiver is disabled and the FIFO is flushed.

0 0 1 1 - Reset Transmitter - resets the transmitter as if a hardware. reset had been applied. The TXD output is forced to a high level.

Table 3. CSR [3:0] Bit Rate Selection

Field				Bit Rate			
CSR[7:4]				ACR[7] = 0		ACR[7] = 1	
CSR[3:0]				X = 0	X = 1	X = 0	X = 1
0	0	0	0	50	75	75	50
0	0	0	1	110	110	110	110
0	0	1	0	134.5	134.5	134.5	134.5
0	0	1	1	200	150	150	200
0	1	0	0	300	3600	300	3600
0	1	0	1	600	14.4K	600	14.4K
0	1	1	0	1200	28.8K	1200	28.8K
0	1	1	1	1050	57.6K	2000	57.6K
1	0	0	0	2400	115.2K	2400	115.2K
1	0	0	1	4800	4800	4800	4800
1	0	1	0	7200	1800	1800	7200
1	0	1	1	9600	9600	9600	9600
1	1	0	0	38.4K	19.2K	19.2K	38.4K
1	1	0	1	Timer	Timer	Timer	Timer
1	1	1	0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1	1	1	1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

Table 4. External Clock Source Input Pin

Function	XR88C681/28	XR88C681/40 **I-mode**	XR88C681/40 **Z-mode**	XR68C681
Transmitter A	IP2	IP3	IP3	IP3
Transmitter B	IP2	IP5	IP2	IP5
Receiver A	IP2	IP4	IP3	IP4
Receiver B	IP2	IP6	IP2	IP2
Counter/Timer	IP2	IP2	IP2	IP2

0 1 0 0 - Reset Error Status - clears the received break, parity error, framing error and overrun error status bits, SR [7:3]. Used in character mode to clear the OE status bit (although the RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0 1 0 1 - Reset Break Change Interrupt - clears the channel's break change interrupt status bit.

0 1 1 0 - Start Break - forces the TXD output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. It the transmitter is active, the break begins when the transmission of that character in the THR is completed, viz., TXEMT must be true before the break will begin.

0 1 1 1 - Stop Break - the TXD line will go high within two bit times. TXD will remain high for one bit time before the next character, if any, is transmitted.

1 0 0 0 - Sat Rx BRG Select Extend Bit - sets the receiver BRG select extend bit for the channel to 1.

1 0 0 1 - Clear Rx BRG Select Extend Bit - clears the receiver BRG select extend bit for the channel to 0.

1 0 1 0 - Set Tx BRG Select Extend Bit - sets the transmitter BRG select extend bit for the channel to 1.

1 0 1 1 - Clear Tx BRG Select Extend Sit - clears the transmitter BRG select extend bit for the channel to 0.

1 1 0 0 - Set Standby Mode (A)/Reset IUS Latch (B)

When this commnand is invoked via the channel A command register, power is removed from the transmitters, receivers, counter/timer and additional circuits to place the DUART in the standby mode, Normal operation is restored by a hardware reset or by invoking the 'set active mode' command.

When this command is invoked via the channel B command register, and the DUART (XR-88C681 version) is operating in Z-mode, it causes the interrupt-under-service latch to be reset.

1 1 0 1 - Set Active Mode (A)/Set Z-mode (B).

When this command is invoked via the channel A command register the DUART is removed from the standby mode and resumes normal operation.

When this command is invoked via the channel B command register, the DUART is conditioned to operate in the Z- mode. This applies only to the XR-88C681 version.

1 1 1 0 - Reserved - do not invoke during operation.

1 1 1 1 - Reserved - do not invoke during operation.

CR (3) - Disable Transmitter

This command terminates operation of the channel's transmitter and resets the TXRDY and TXEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before going into the inactive state.

CR (2) - Enable Transmitter

This command enables operation of the channel's transmitter and asserts the TXRDY status bit.

CR [1] - Disable Receiver

This command immediately terminates operation of the channel's receiver. Any character being received will be, lost. The command has no effect on the receiver status bits or on any other control registers, If the multi-drop mode is programmed, the receiver operates even it it is disabled. See OPERATION section.

CR [0] - Enable Receiver.

This command enables operation of the receiver. If not in the multidrop mode, it also forces the receiver to start searching for the start bit.

SRA, SRB - Channel A/B Status Register

SR [7] - Received Break

This bit indicates that an all zero character of the programmed length was received without a stop bit. Only a single FIFO position is occupied when a break is received. Additional transfers into the FIFO are inhibited until the RXD line returns to the marking state for at least half a bit time. This is defined as two successive edges of the internal or external 1 x clock.

When this bit is set, the channel's change in break status bit in the ISR is set. The bit in the ISR is also set when the end of the break condition, as defined above, is detected.

SR [6] - Framing Error

When set, this bit indicates that RXD was low when the stop bit of the character is in the FIFO was sampled. The stop bit check is made in the middle of the first stop bit position (one bit time after sampling the last data bit or the parity bit at its midpoint) regardless of the stop bit length programmed.

SR [5] - Parity Error

This bit is set when the 'with parity' or 'force parity' modes are programmed if the corresponding character in the data FIFO was received with incorrect parity.

In the multidrop mode, this status bit indicates the state of received address/data (A/D) flag bit.

SR [4] - Overrun Error

If set, this bit indicates that one or more characters in the received data stream have been lost, It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its error status) is overwritten.

This bit is cleared by a 'reset error status' command.

SR [3] - Transmitter Empty (TXEMT)

This bit is set when the transmitter underruns. It is set after transmission of the last stop bit of a character if there is no character is the THR awaiting transmission. It is reset when the THR is loaded by the CPU and when the transmitter is disabled.

SR [2] - Transmitter Ready (TXRDY)

This bit, when set, indicates that the THR is empty and ready to accept a character. The bit is cleared when the THR is loaded by the CPU and is set when that character is transferred to the transmit shift register. TXRDY is set when the transmitter is initially enabled and is reset when the transmitter is disabled. Characters loaded into the THR while the transmitter is disabled will not be transmitted.

SR [1] - FIFO Full (FFULL)

This bit is set when a character is transferred from the receive shift register to the FIFO and the transfer causes it to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SR [0] - Receiver Ready (RXRDY)

This bit indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when a character is transferred from the receive shift register to the FIFO and reset when the CPU reads the last character currently stored in the FIFO.

OPCR - Output Port Configuration Register

This register programs the output port to provide alternate functions. Note that when an output is programmed as an interrupt, it is not masked by the contents of the IMR.

Table 5. Bit Rate Generator Characteristics
Crystal or Clock Input = 3.6864 MHz

Nominal Rate (bps)	Actua Clock (KHz)	Error (Percent)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3 2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.26
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
3600	57.6	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
14.4K	230.4	0
19.2K	307.2	0
28.8K	460.8	0
38.4K	614.4	0
57.6K	921.6	0
115.2K	1843.2	0

Table 6 ACR [6:4] Field Definition

ACR[6:4]			Mode	Clock Source
0	0	0	Counter	External-IP2 Input
0	0	1	Counter	TXCA - 1x Clock of Channel A Tx
0	1	0	Counter	TXCB - 1x Clock of Channel B Tx
0	1	1	Counter	X1/CLK Input Divided by 16
1	0	0	Timer	External - IP2 Input
1	0	1	Timer	Eternal Divided by 16 - IP2 Input
1	1	0	Timer	X1/CLK Input
1	1	1	Timer	X1/CLK Input Divided by 16

OPCR [7] - OP7 Output Select

This bit programs the OP7 output to provide one of the following:

0 - The complement of OPR [7]

1 - The channel B transmitter interrupt output, TXRDYB. which is the complement of SRB [2]. In this mode, OP7 is an open drain output.

OPCR [6] - OP6 Output Select

This bit programs the OP6 output to provide one of the following:

0 - The complement of OPR [6].

1 - The channel A transmitter interupt output, TXRDYA, which is the complement of SRA[2]. In this mode OP6 is an open drain output.

OPCR [5] - OP5 Output Select

This bit programs the OP5 output to provide one of the, following:

0 - The complement of OPR [5]

1 - The channel B receiver interrupt output which is the complement of ISR [5]. In this mode OP5 is an open drain output.

OPCR [4] - OP4 Output Select

This bit programs the OP4 output to provide one of the following:

0 - The complement of OPR [4].

1 - The channel A receiver interrupt output, which is the complement of ISR [1]. In this mode OP4 is an open drain output.

OPCR [3:2] - OP3 Output Select

These bits program the OP3 output to provide one of the following:

00 - The complement of OPR [3].

01 - The counter/timer output, in which case OP3 is an open drain output. In the timer mode the output is a square wave at the programmed frequency. In counter mode the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.

10 - The 1x clock which shifts the output data for the channel B transmitter. A free running 1x clock is output if data is not being transmitted.

11 - The Ix clock which samples the input data for the channel B receiver. A free running ix clock is output if data is not being received.

OPCR [1:0] - OP2 Output Select

These bits program the OP2 output to provide one of the following:

00 - The complement of OPR[2].

01 - The 16x clock selected for the channel A transmitter by CSRA [3:0]. This will be a 1x clock if external 1x clock is programmed.

10 - The 1x clock which shifts the output data for the channel A transmitter. A free running 1x clock is out put if data is not being transmitted.

11 - The 1x clock which samples the input data for the channel A receiver. A free running 1x clock is output if data is not being received.

ACR - Auxiliary Control Register

ACR [7] - Bit Rate Set Select

This bit selects one of two sets of bit rates to be generated by the BRG. The bit rates provided are selected by the channel A and B receiver and transmitter as described in the Clock Select Register description. Bit rate generator characteristics are shown in Table 5.

ACR [6:4] - Counter/Timer Mode and Clock Source Select

This field selects the operating mode and clock source for the counter/timer. See Table 6.

ACR [3:0] - Change of State Interrupt Enables

These bits select which bits of the input port cause the input port change bit in the interrupt status register (ISR [7]) to be set. If one of these bits is 'on', the setting of the corresponding bit in the IPCR by a change of state on the input will set ISR [7], and will also cause the

interrupt request pin to be asserted if IMR [7] is set. However, if the bit is 'off', the setting of the corresponding bit in the IPCR has no effect on ISR [7].

IPCR - Input Port Change Register

IPCR [7:4] - IP3, IP2, IPI, IP0 Change of State

These bits are set when a change of state occurs at the respective input pins (see Input Port section). The bits are cleared when the CPU reads the IPCR.

The setting of these bits can be programmed to cause an interrupt to the CPU via ACR [3:0], ISR [7] and IMR [7].

IPCR [3:0] - IP3, IP2, IP1, IP0 Current State

These bits indicate the current state of the respective inputs at the time the IPCR is read.

ISR - Interrupt Status Register

This register provides the current status of all possible interrupt conditons. If a bit in the ISR is a '1' and the corresponding bit in the interrupt mask register (IMR) is also a '1' the interrupt request output will be asserted. If the corresponding bit in the IMR is a 'O' the state of the bit in the ISR has no effect on the interrupt request output. The contents of this register can be read by the CPU either unmasked or masked by the IMR. See Table 1.XR-88C681/68C681

ISR [7] - Input Port Change Status

This bit is a '1' when a change of state has occurred at the IP0, IPI, IP2 or IP3 inputs and that event has been programmed to cause an interrupt via ACR [3:0]. It is cleared when the CPU reads the IPCR.

ISR [6] - Channel B Change in Break

This bit indicates that the channel B receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel B 'reset break change interrupt' command.

ISR [5] - Channel B Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the receive shift register to the FIFO if that transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR [4] - Channel B Transmitter Ready

This bit is a duplicate of TXRDYB, SRB[2].

ISR [3] - Counter Ready

In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a 'stop counter' command.

In the timer mode, this bit is set once each cycle of the generated square wave. It is also set each time a 'start counter' command is issued if the output is, at that time, in the second (high) half of the square wave cycle. The bit is reset by a 'stop counter' command. The command, however, does not stop the C/T.

ISR [2] - Channel A Change in Break

This bit indicates that the channel A receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel A 'reset break change interrupt' command.

ISR [1] - Channel A Receiver Ready or FIFO Full

The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO if that transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR(0) - Channel A Transmitter Ready

The bit is duplicated of TXRDYA, SRA(2).

IMR - Interrupt Mask Register

This register selects which bits in the ISR cause an interrupt to be asserted. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0', the state of the bit in the ISR has no effect on the interrupt request output. Note that the IMR does not mask the programmable interrupt outputs, OP3-OP7.

CTUR/CTLR - Counter/Timer Registers

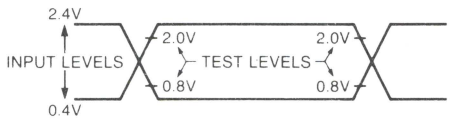
The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used the the counter/timer in both of its modes of operation. The minimum value which may be loaded into CTUR/CTLR is 0001H. These registers are write-only and cannot be read by the CPU.

IVR-Interrupt Vector Register

The IVR holds the value which the DUART places on the data bus in response to assertion of the interrupt acknowledge input. This applies to the XR-68C681 and to the XR- 88C68I when operating in Z-mode. The register is not used for any function when the XR-88C681 operates in I-mode but remains writeable and readable by the CPU, and can be used for any purpose. The contents of this register are initialized to 9FH by a hardware reset.

NOTES:

1. Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage large, than the rated maxima.
3. Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25°C, VCC = 5V and typical processing parameters.
4. All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 3.
5. Measured operating with a 3.6864MHz crystal and with all outputs open.
6. AC test condition for outputs: CL = 150pF, except interrupt outputs: CL = 50pF, RL = 2.7K ohm to VCC.
7. For the XR88C681, timing is illustrated and referenced to the RDN and WRN inputs. The device may also be operated using CEN as the 'strobing' input. In this case, all specifications apply referenced to the failing and rising edges of CEN.
8. If CEN is used as the strobing input, this parameter defines the minimum high time between CENs.
9. Consecutive write operations to the same register require at least three edges of the X1 clock between writes.
10. This parameter is system dependent. For any DUART in the daisy chain, tIAS must be greater than the sum of EOD for the highest priority device in the daisy chain, tEIS for the DUART, and tDIO for each device separating them in the daisy chain.
11. This specification imposes a 6MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle, A higher 68000 clock can be used if this is not the case.
12. This specification imposes a lower bound on CSN and IACKN low, guaranteeing that they will be low for at least one CLK period.
13. This parameter is specified only to insure that DTACKN is asserted with respect to the rising edge of X1/CLK as shown in the timing diagram, not to guarantee operation of the part. If the specified setup time is violated, DTACKN may be asserted as shown or may be asserted one clock cycle later.
14. The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's RX is operating in external 1 x clock mode.
15. For prime grade N, P. J, L, M, ML, VCC = 5 V ±10%.



AC testing inputs are driven at o.4V for a logic '0' and 2.4V for a logic '1' except for -40 to 85°C and -55 to 125°C, logic '1' shall be 2.6V. Timing measurements are made at 0.8V for a logic '0' and 2.0V for a logic '1'.

Figure 3. Input and Output Levels for Timing Measurements

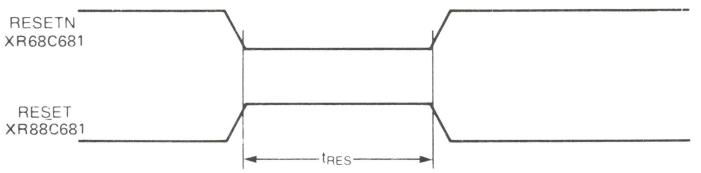


Figure 4. Reset Timing

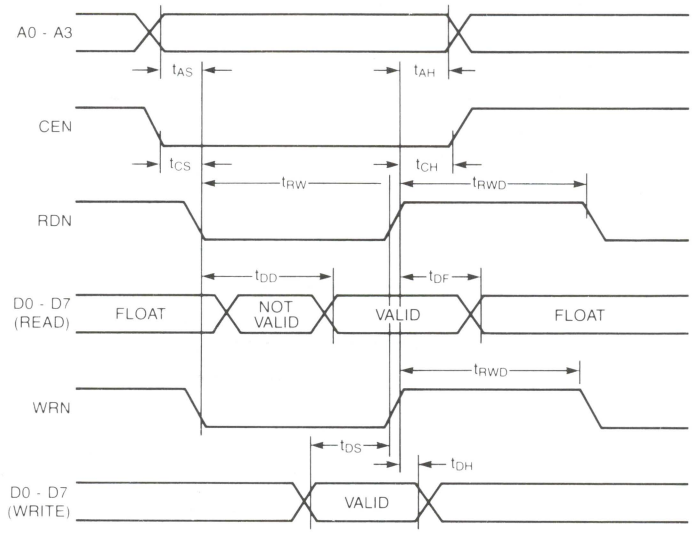


Figure 5. XR-88C681 Read and Write Cycle Timing

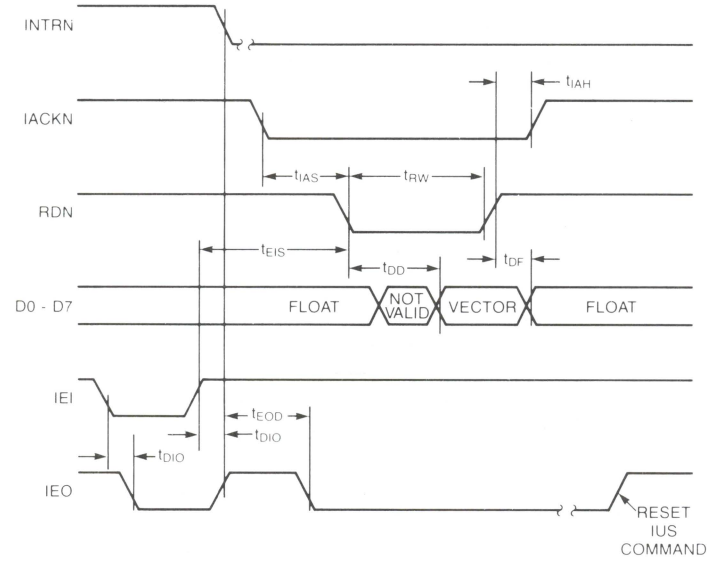


Figure 6. XR-88C681 Z-mode Interrupt Cycle Timing

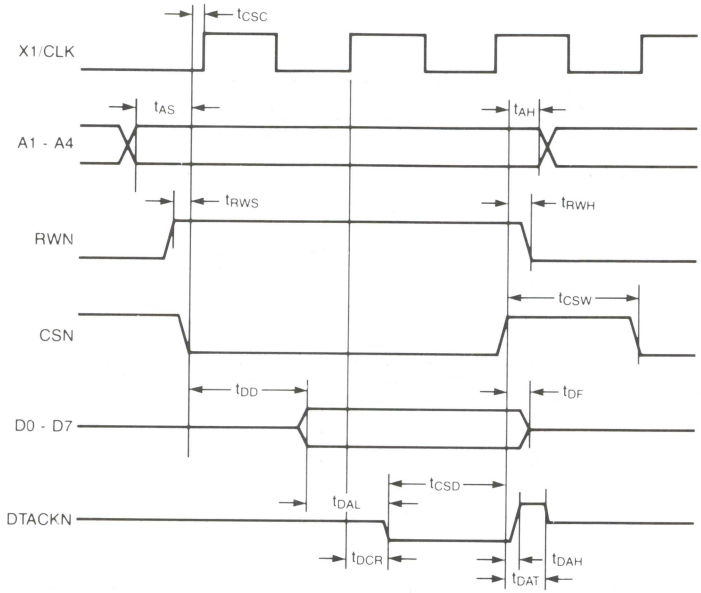


Figure 7. XR-68C681 Read Cycle Timing

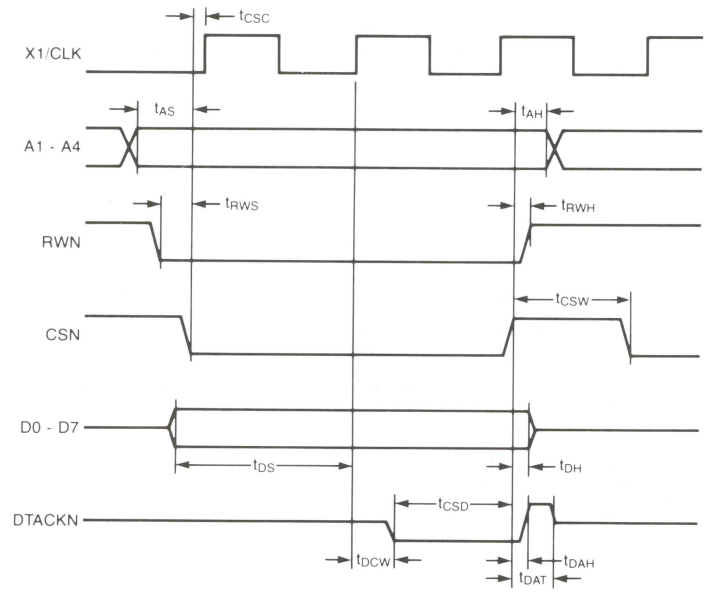


Figure 8. XR-68C681 Write Cycle Timing

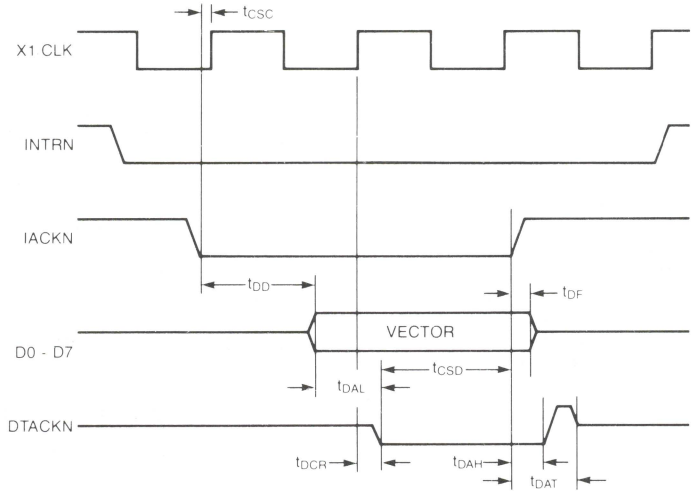


Figure 9. XR-68C681 Interrupt Cycle Timing

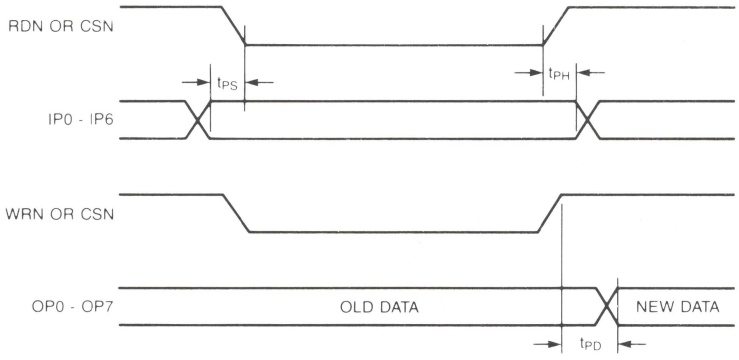
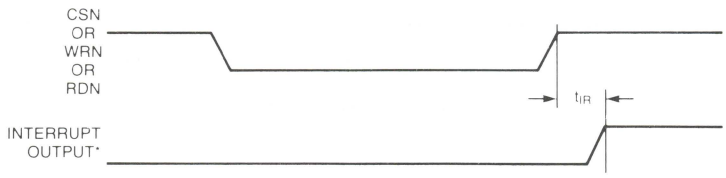


Figure 10. Port Timing



*INTRN or OP3 - OP7 when used as interrupt outputs.

Figure 11. Interrupt Timing

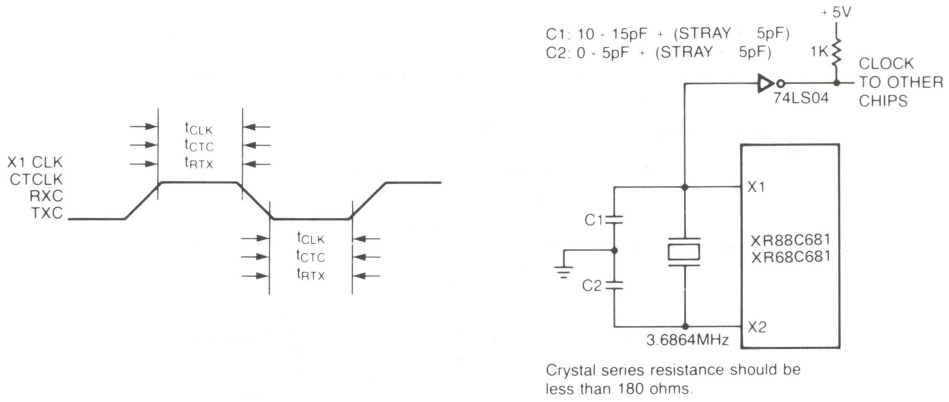


Figure 12. Clock Timing

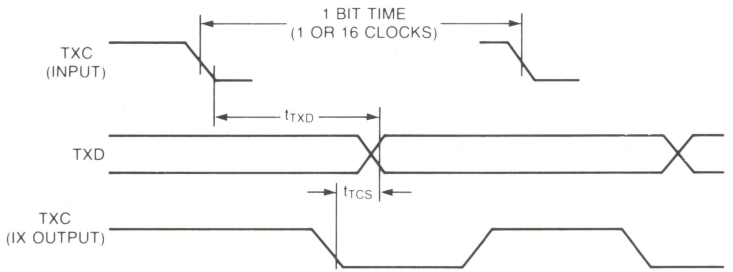


Figure 13. Transmitter Timing

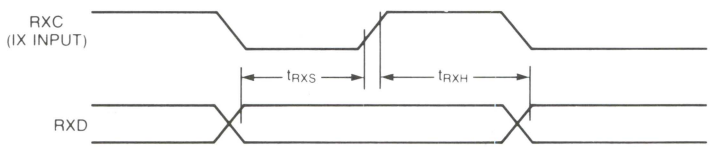
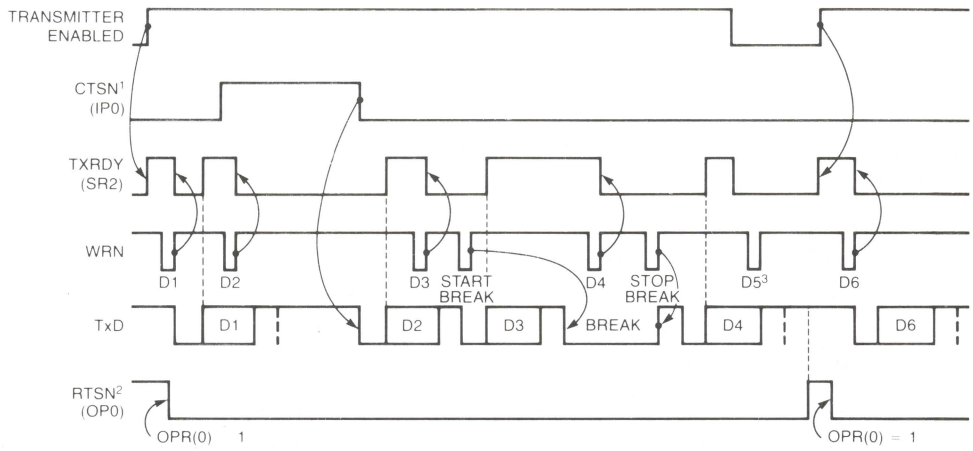
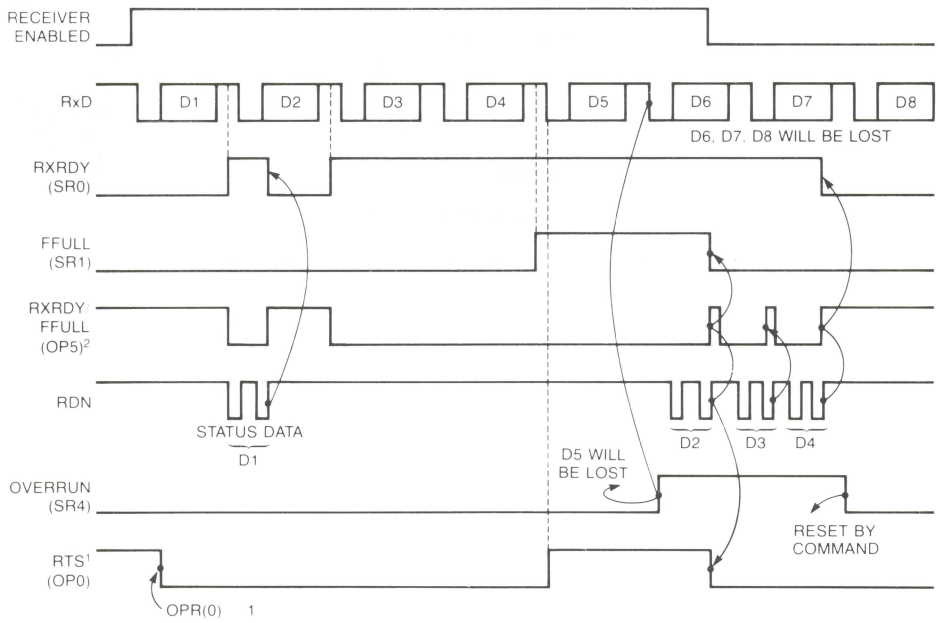


Figure 14. Receiver Timing



NOTES
1. Operation shown for MR2(4) = 1
2. Operation shown for MR2(5) = 1
3. D5 will not be transmitted

Figure 15. Transmitter Operation



NOTES
1. Operation shown for MR1(7) = 1
2. Shown for OPCR(4) = 1 and MR1(6) = 0

Figure 16. Receiver Operation

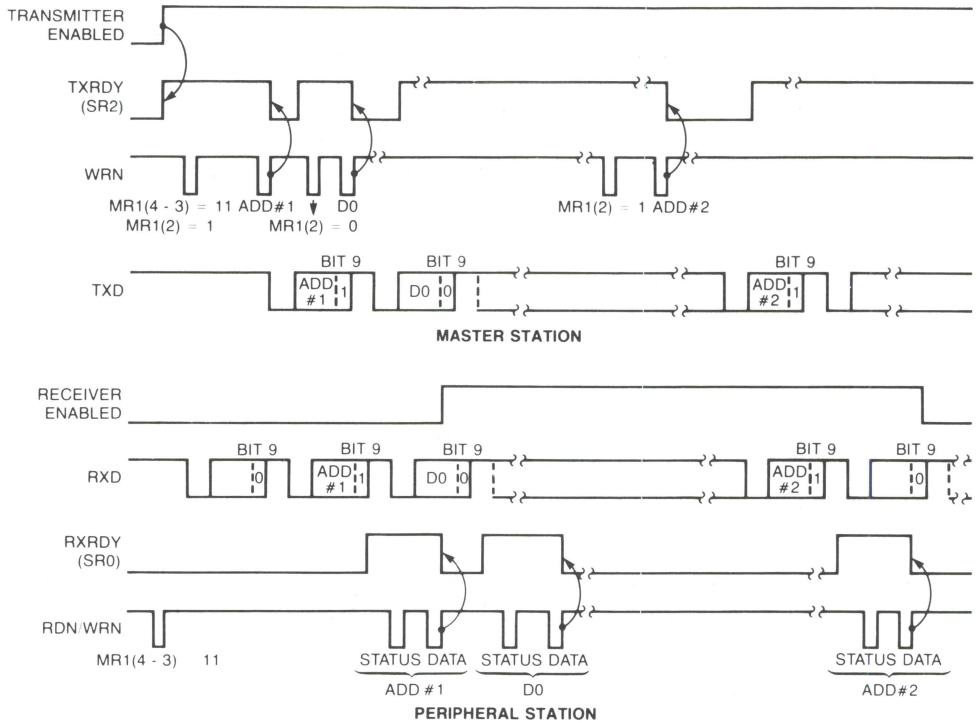
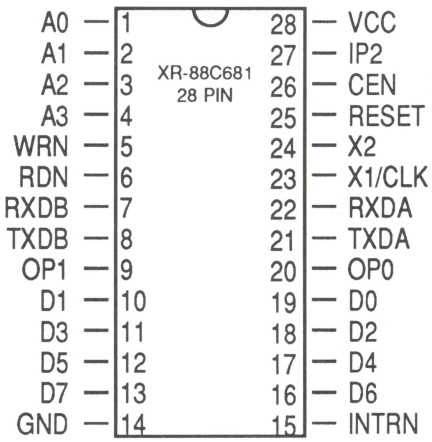
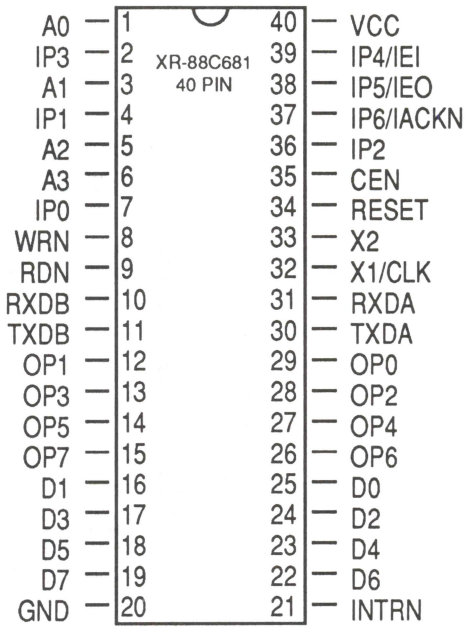
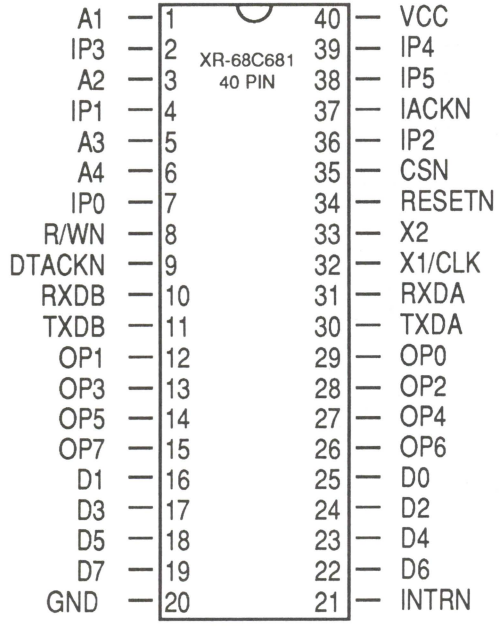
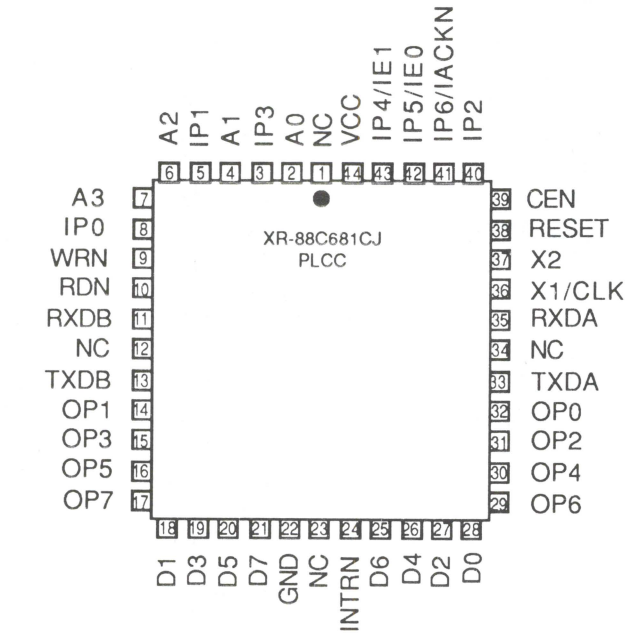


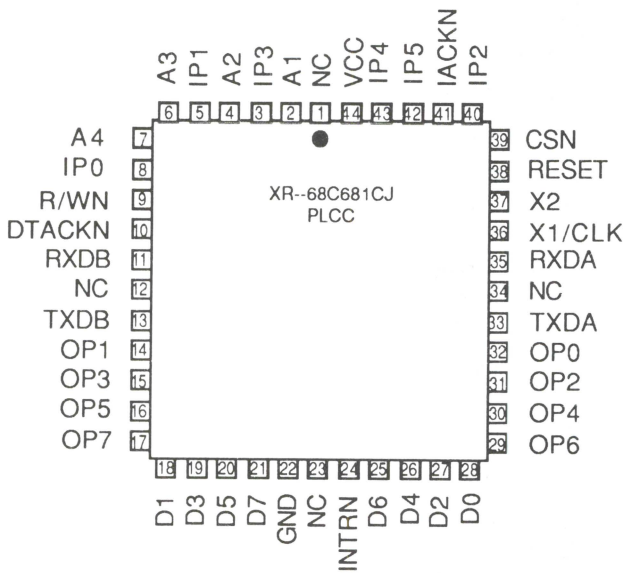
Figure 17. Transmitter and Receiver Operation in Multidrop Mode


XR-88C681
28 PIN
A0 1
A1 2
A2 3
A3 4
WRN 5
RDN 6
RXDB 7
TXDB 8
OP1 9
D1 10
D3 11
D5 12
D7 13
GND 14
28 VCC
27 IP2
26 CEN
25 RESET
24 X2
23 X1/CLK
22 RXDA
21 TXDA
20 OP0
19 D0
18 D2
17 D4
16 D6
15 INTRN


XR-88C681
40 PIN
A0 1
IP3 2
A1 3
IP1 4
A2 5
A3 6
IP0 7
WRN 8
RDN 9
RXDB 10
TXDB 11
OP1 12
OP3 13
OP5 14
OP7 15
D1 16
D3 17
D5 18
D7 19
GND 20
40 VCC
39 IP4/IEI
38 IP5/IEO
37 IP6/IACKN
36 IP2
35 CEN
34 RESET
33 X2
32 X1/CLK
31 RXDA
30 TXDA
29 OP0
28 OP2
27 OP4
26 OP6
25 D0
24 D2
23 D4
22 D6
21 INTRN


XR-68C681
40 PIN
A1 1
IP3 2
A2 3
IP1 4
A3 5
A4 6
IP0 7
R/WN 8
DTACKN 9
RXDB 10
TXDB 11
OP1 12
OP3 13
OP5 14
OP7 15
D1 16
D3 17
D5 18
D7 19
GND 20
40 VCC
39 IP4
38 IP5
37 IACKN
36 IP2
35 CSN
34 RESETN
33 X2
32 X1/CLK
31 RXDA
30 TXDA
29 OP0
28 OP2
27 OP4
26 OP6
25 D0
24 D2
23 D4
22 D6
21 INTRN


A2
IP1
A1
IP3
A0
NC
VCC
IP4/IE1
IP5/IE0
IP6/IACKN
IP2
6 5 4 3 2 1 44 43 42 41 40
A3 7
IP0 8
WRN 9
RDN 10
RXDB 11
NC 12
TXDB 13
OP1 14
OP3 15
OP5 16
OP7 17
XR-88C681CJ
PLCC
39 CEN
38 RESET
37 X2
36 X1/CLK
35 RXDA
34 NC
33 TXDA
32 OP0
31 OP2
30 OP4
29 OP6
18 19 20 21 22 23 24 25 26 27 28
D1
D3
D5
D7
GND
NC
INTRN
D6
D4
D2
D0


A3
IP1
A2
IP3
A1
NC
VCC
IP4
IP5
IACKN
IP2
6 5 4 3 2 1 44 43 42 41 40
A4 7
IP0 8
R/WN 9
DTACKN 10
RXDB 11
NC 12
TXDB 13
OP1 14
OP3 15
OP5 16
OP7 17
XR--68C681CJ
PLCC
39 CSN
38 RESET
37 X2
36 X1/CLK
35 RXDA
34 NC
33 TXDA
32 OP0
31 OP2
30 OP4
29 OP6
18 19 20 21 22 23 24 25 26 27 28
D1
D3
D5
D7
GND
NC
INTRN
D6
D4
D2
D0

Preliminary Information

CMOS Quad Channel UART (QUART)

GENERAL DESCRIPTION

The EXAR Quad Universal Asynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full duplex asynchronous communications channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR-82C684 offers a single IC solution for various microprocessor families. The 88 and 68 modes can be selected by tying SEL pin to VDD or VSS.

The QUART is fabricated using advanced two layer metal, with a high density EPI/CMOS 1.8µ process to provide high performance and low power consumption.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	7V
Storage Temperature	-65°C to150°C
All Voltages with respect to ground	-0.5 V to +7V

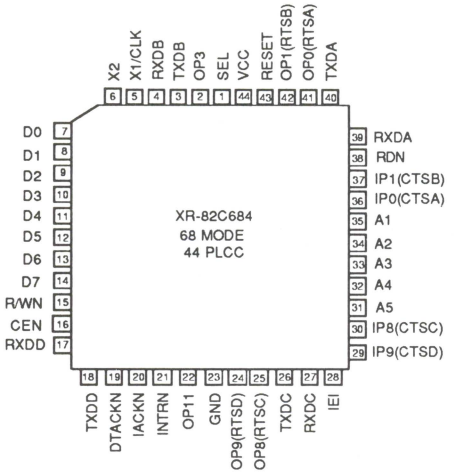
ORDERING INFORMATION

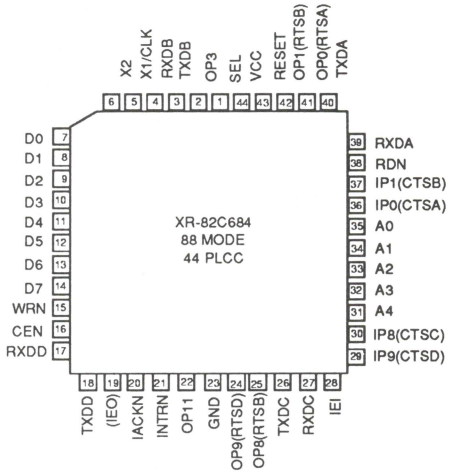
Part number	Package	Operating Temperature
XR-82C684CJ/44	PLCC44 PIN	0°C to 70°C
XR-82C684J/44	PLCC44 PIN	-40°C to 85°C
XR-82C684CJ	PLCC68 PIN	0°C to 70°C
XR-82C684J	PLCC68 PIN	-40 C to 85°C

FEATURES

- Four Full Duplex, Independent Channels
- Asynchronous Receiver and Transmitter
- Quadruple Receive and Transmit Buffer
- Programmable Stop Bits in 1/16 Bit Increments
- Pin Selectable 88 and 68 mode
- Four Independent Internal Bit Rate Generators with more than 33 Bit Rates
- Independent Bit Rate Selection for each Transmitter and Receiver
- External Clock Capability
- Normal, Autoecho, Local Loop Back and Remote Loopback Modes
- Two Multifunction 16-Bit Counter/ Timer
- Interrupt Output with Sixteen Maskable Interrupt Conditions
- Prioritized Interrupt Vector Output on Acknowledge
- Programmable Interrupt Daisy Chain
- 16 General Purpose Outputs
- 16 General Purpose Inputs with Eight Change of State Detectors on Inputs
- Multidrop Mode Compatible with 8051 Nine-Bit Mode
- On Chip Oscillator for Crystal
- Stand-by Mode to Reduce Operating Power

For other pin assignments, refer to the end of this datasheet





SYSTEM DESCRIPTION

Each channel of the QUART may be independently programmed for operating mode and data format. The operating speed of each receiver and transmitter may be selected from one of 33 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an external 1x or 16x clock. The bit rate generator can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the QUART attractive for split speed channel applications such as clustered terminal systems

Receiver and transmitter data are quadruple-buffered in an on chip FIFO to minimize the risk of receiver or transmitter overrun and to reduce overhead in interrupt driven applications. The QUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving QUART is full, thus preventing loss of data.

The QUART also provides two general purpose16 bit counter/timers (which may also be used as programmable bit rate generators), two multi-purpose input ports and two multi-purpose output ports.

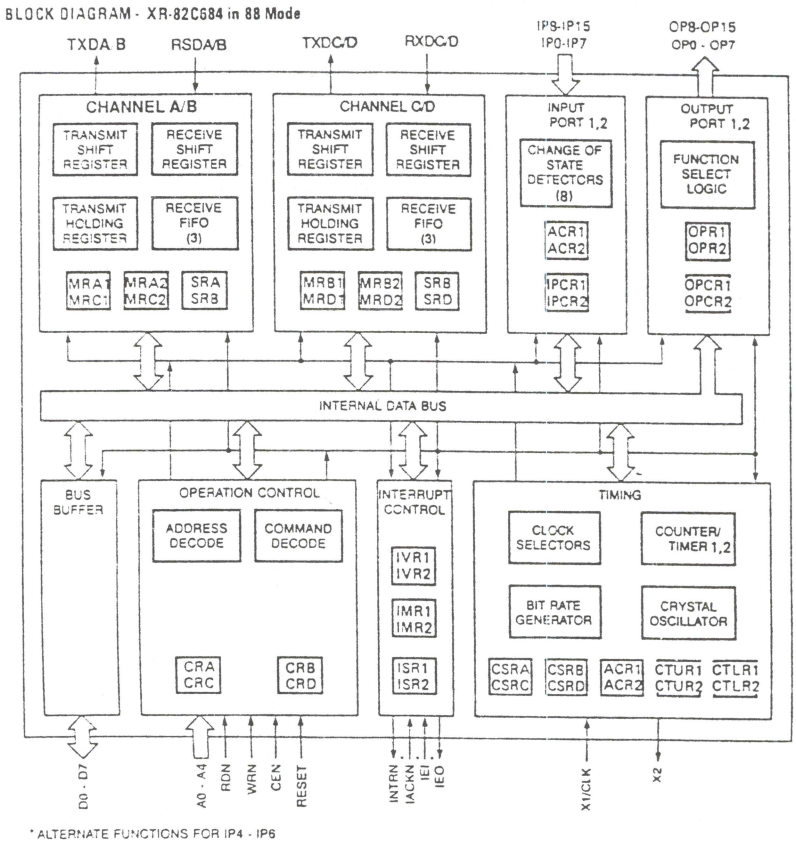


Figure 1. Block Diagram XR-82C684 in 88 Mode

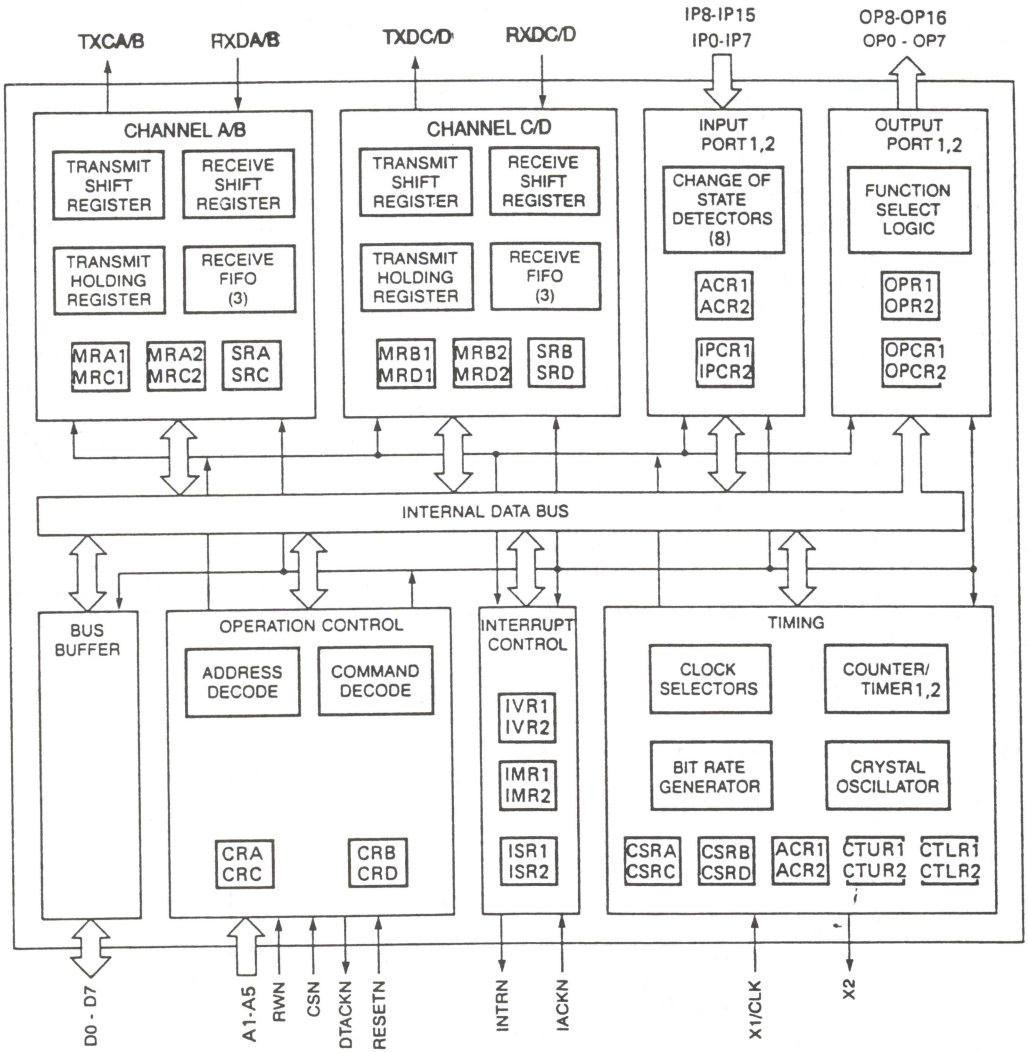


Figure 2. Block Diagram XR-82C684 in 68 Mode

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A= 25° C, V_{CC} = 5.0V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH15}	Input High Voltage	2.0		V_{CC}	V	
V_{IH}	Input High Voltage	2.2			V	-55°C to 125° C
V_{IH1}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage (Except Open Drain Port)	2.4			V	I_{OH} = -400 µA
I_{IL}	Input Leakage Current	-25		25	µA	V_{IN} = 0 to V_{CC}
I_{ILSEL}	Select Pin Leakage Current	-30		+30	µA	V_{IN} = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		-20		µA	V_{IN} = 0
I_{X2L}	X2 Input Low Current		-7		mA	0
I_{X1H}	X1 Input High Current		20		µA	V_{IN} = V_{CC}
I_{X2H}	X2 Input High Current		20		µA	V_{IN} = V_{CC}
I_{LL}	Data Bus Tri-State Leakage Current	-10		10	µA	V_O = 0 to V_{CC}
I_{OC}	Open Drain Output Leakage Current`	-10		10	µA	V_O = 0 to V_{CC}
I_{CCA}	Power Supply Current		6	15	mA	Active Mode
I_{CCS}	Power Supply Current		3	10	mA	Standby Mode

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 5.0 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Reset Timing (Figure 4)						
t_{RES}	Reset Pulse Width	1.0			µs	
XR-82C684 Read and Write Cycle Mode (Figure 5 & 6)[7]						
t_{AS}	A0-A4 Setup Time to RD, WR Low	10			ns	
t_{AH}	A0-A4 Hold Time from RD, WR High	0			ns	
t_{CS}	CS Setup Time to RD, WR Low	0			ns	
t_{CH}	CS Hold Time from RD, WR High	0			ns	
t_{RW}	RD, WR Pulse Width	225			ns	
t_{DD}	Data Valid from RD Low		60	175	ns	
t_{DF}	Data Bus Floating from RD High	10		100	ns	
t_{DS}	Data Setup Time to WR High	100			ns	
t_{DH}	Data Hold Time from WR High	5			ns	
t_{RWD}	High Time Between Reads and/or Writes[8,9]		100		ns	
XR-82C684 Z-mode Interrupt Cycle Timing (Figure 6)						
t_{DIO}	IEO Delay Time from IEI			100	ns	
t_{IAS}	IACK Setup Time to RD Low		Note 10		ns	
t_{IAH}	IACK Hold Time from RD High		0		ns	
t_{EIS}	IEI Setup Time to RD Low		50		ns	
t_{EOD}	IEO Delay Time from INTR Low			100	ns	

XR-82C684 Read, Write and Interrupt Cycle Timing 68 Mode (Figure 7, 8, 9)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	A1-A5 Setup Time to CS Low	10			ns	
t_{AH}	A1-A5 Hold Time from CS High	0			ns	
t_{RWS}	R/W Setup Time to CS Low	0			ns	
t_{RWH}	R/W Setup Time from CS High	0			ns	
t_{CSW}	CS High Pulse Width 9,11	90			ns	
t_{CSD}	CS or IACK High from DTACK Low12	20			ns	
t_{DD}	Data Valid from CS or IACK Low			175	ns	
t_{DF}	Data Bus Floating from CS or IACK High	10		100	ns	
t_{DS}	Data Setup Time to CS Low	0			ns	
t_{DH}	Data Hold Time from CS Low	125			ns	
t_{DAL}	DTACK Low from Read Data Valid	0			ns	
t_{DAH}	DTACK High from CS or IACK High			100	ns	
t_{DAT}	DTACK High Impedance from CS or IACK High			125	ns	
Port Timing 82C684 (Figure 10)7						
t_{PS}	Port Input Setup Time to RD/CS Low	0			ns	
t_{PH}	Port Input Hold Time from RD/CS High	0			ns	
t_{PD}	Port Output Valid from WR/CS High			400	ns	
Interrupt Output Timing 82C684 (Figure11)						
t_{IR}	INTR or OP3-OP7/OP10-OP15 When Used As Interrupts High from:					
	Clear of Interrupt Status Bits in ISR or IPCR			300	ns	
	Clear of Interrupt Mask in IMR			300	ns	
Clock Timing 82C684 (Figure 12)						
t_{CLK}	X1/ CLK (External) High or Low Time	100			ns	
t_{CLK}	X1/ CLK Crystal or External Frequency	2.0	3.684	7.372	MHz	
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2 / IP10)	100			ns	
t_{CTC}	Counter/Timer External Clock Frequency	0		7.372	MHz	
t_{RTX}	RXC and TXC (External) High or Low Time14	220			ns	
fRTX	RXC and TXC (External) Frequency					
	16x	0		16.0	MHz	
	1x	0		1.0	MHz	
Transmitter Timing 82C684 (Figure 13)						
t_{TXD}	TXD Output Delay - TXC (External) Low			350	ns	
t_{TCS}	TXD Output Delay - TXC (Internal) Output Low			150	ns	
Receiver Timing 82C684 (Figure 14)						
t_{RXS}	RXD Data Setup Time to RXC (External) High	240			ns	
tRXH	RXD Data Hold Time from RXC (External) High	200			ns	

PIN DESCRIPTIONS XR-82C684

SYMBOL	TYPE	DESCRIPTION
D0-D7	I/O	**8-bit Bidirectional Three-state Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All transfers between the CPU and QUART take place over this bus. The bus is three-stat ed when the CS input is high, except during an IACK cycle or in the Z-mode.
A1-A5	I	**Address Inputs.** These inputs select the QUART registers or port for the current read / write operation.
CS	I	**Chip Select low.** The data bus is three-stated when CS is high. Transfers between the CPU and the QUART via D0-D7 are enabled when CS is low.
WR	I	**Write Strobe.** (88 mode) Active low. A low on this input while CS is also low writes the contents of the data bus into the addressed register.The transfer occurs on the rising edge of WR.
R/W	I	**Read / Write.** (68 mode) A high input while CS is low indicates a read cycle while a low input while CS is low indicates a write cycle.
RD	I	**Read Strobe.** (88 mode) Active low on this input while CS is also low places the contents of the addressed source on the data bus. The transfer begins on the falling edge of RD.
RESET	I	**Master Reset.** (Active high for 88 mode and Active low for 68 mode). Clears internal registers SRn, ISRn, IMRn, OPRn, OPCRn and initializes the IVRn to 0FH, stops the counter / timer, puts OP0-OP15 in the high state, and places both serial channels in the inactive state with the TXDA, TXDB, TXDC and TXDD outputs marking (high).
INTRN	O	**Interrupt Request.** Active low, open drain. INTRN is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions.
IACK	I	**Interrupt Acknowledge.** (68 mode) Active low. Assertion of IACK indicates that the current bus cycle is an interrupt acknowledge cycle. If the QUART has an interrupt active, it responds by placing the interrupt vector on the data bus and asserting DTACK.
IEI	I	**Interrupt Enable Input.** (88 mode) Active high.
IEO	O	**Interrupt Enable Output.** (88 mode) Active high.
DTACK	O	**Data Transfer Acknowledge** (68 mode) Three state, active low. Assertion of DTACK indicates that data is present on the bus during a read or interrupt acknowledge cycle and that the data from the bus has been written into the addressed destination during a write cycle.
X1 / CLK	O	**Crystal Output or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used. If the oscillator is not used, an external clock signal must be supplied at this input.
X2	I	**Crystal Input.** Connection for other side of the crystal. If the oscillator is used, a capac itor must also be connected from this pin to ground. This pin must be left open if an external clock is supplied at X1 / CLK.

SYMBOL	TYPE	DESCRIPTION
RXD-A RXD-B RXD-C RXD-D	I	**Receive Serial Data Inputs**. The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
TXD-A TXD-B TXD-C TXD-D	O	**Transmitter Serial Data Outputs**. The least significant bit is transmitted first. Held in the high (marking) state when the transmitter is idleordisabled and also when the channel operates in local loopback mode. If external transmitter clock is specified, the data is shifted out on the falling edge of the clock.
OP0	O	**Output 0.** Active low. Can be programmed as a general purpose output or as the chan nel A request-to-send output (RTS-A).
OP1	O	**Output 1.** Active low. Can be programmed as a general purpose output or as the chan nel B request-to-send output (RTS-B).
OP2	O	**Output 2.** Active low. Can be programmed as a general purpose output, the channel A transmitter 16x or 1x clock output, or the channel A receiver 1x clock output.
OP3	O	**Output 3.** Active low. Can be programmed as a general purpose output, the channel B transmitter 1x clock output, the channel B receiver 1x clock output, or an open drain counter / timer 1 ready output.
OP4	O	**Output 4.** Active low. Can be programmed as a general purpose output or as an open drain channel A RXRDY/FFULL output.
OP5	O	**Output 5.** Active low. Can be programmed as a general purpose output or as an open drain channel B RXRDY/FFULL output.
OP6	O	**Output 6.** Active low. Can be programmed as a general purpose output or as an open drain channel A TXRDY output.
OP7	O	**Output 7.** Active low. Can be programmed as a general purpose output or as an open drain channel B TXRDY output.
OP8	O	**Output 8.** Active low. Can be programmed as a general purpose output or as the chan nel C request-to-send output (RTS-C).
OP9	O	**Output 9.** Active low. Can be programmed as a general purpose output or as the chan nel D request-to-send output (RTS-D).
OP10	O	**Output 10.** Active low. Can be programmed as a general purpose output, the channel C transmitter 16x or 1x clock output, or the channel C receiver 1x clock output.
OP11	O	**Output 11.** Active low. Can be programmed as a general purpose output, the channel D transmitter 1x clock output, the channel D receiver 1x clock output, or an open drain counter / timer 2 ready output.
OP12	O	**Output 12.** Active low. Can be programmed as a general purpose output or as an open drain channel C RXRDY/FFULL output.

SYMBOL	TYPE	DESCRIPTION
OP13	O	**Output 13.** Active low. Can be programmed as a general purpose output or as an open drain channel D RXRDY/FFULL output.
OP14	O	**Output 14.** Active low. Can be programmed as a general purpose output or as an open drain channel C TXRDY output.
OP15	O	**Output 15.** Active low. Can be programmed as a general purpose output or as an open drain channel D TXRDY output.
IP0	I	**Input 0.** General purpose input or CTS-A, the channel A active low clear-to-send input.
IP1	I	**Input 1.** General purpose input or CTS-B, the channel B active low clear to send input.
IP2	I	**Input 2.** General purpose input or the counter/timer 1 external clock input.
IP3	I	**Input 3.** General purpose input or the channel A transmitter external clock input.
IP4	I	**Input 4.** General purpose input or the channel A receiver external clock input.
IP5	I	**Input 5.** General purpose input or the channel B transmitter external clock input.
IP6	I	**Input 6.** General purpose input or the channel B receiver external clock input.
IP7	I	**Input 7.** General purpose input.
IP8	I	**Input 8.** General purpose input or CTS-C, the channel C active low clear-to-send input.
IP9	I	**Input 9.** General purpose input or CTS-D, the channel D active low clear-to-send input.
IP10	I	**Input 10.** General purpose input or the counter/timer 2 external clock input.
IP11	I	**Input 11.** General purpose input or the channel C transmitter external clock input.
IP12	I	**Input 12.** General purpose input or the channel C receiver external clock input.
IP13	I	**Input 13.** General purpose input or the channel D transmitter external clock input.
IP14	I	**Input 14.** General purpose input or the channel D receiver external clock input.
IP15	I	**Input 15.** General purpose input.
SEL	I	**Mode Select.** 88 mode can be selected by tying this pin to ground; connecting this pin to Vcc will select the 68 mode.
VCC	I	**+5 Volt Power Input**
GND	I	**Signal and Power Ground**

PRINCIPLES OF OPERATION

As illustrated in the block diagram, the QUART consists of the following major blocks:

Bus Buffer
Operation Control
Interrupt Control
Timing
Input Ports
Output Ports
Serial Communication Channels A, B, C and D

BUS BUFFER

The data bus buffer provides the interface between the internal and external data buses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the QUART.

OPERATION CONTROL

The control logic receives operating commands from the CPU and generates proper signals to the various sections of the QUART. It contains address decoding and read/write circuits to permit communication with the microprocessor and internal registers, to set configuration commands and to monitor device status.

In the 68 mode (68000 Microprocessor Family), the QUART includes a data transfer acknowledge (DTACK) output which is asserted during data transfer cycle to verify that the requested operation has been completed. It indicates that the input data has been latched during a write cycle, that the requested data is on the data bus during a read cycle, or that the interrupt vector is on the data bus during an interrupt acknowledge cycle.

When using a 6800 family processor, the QUART should be used in the 88 mode. This can be readily achieved by implementing the minor external logic change as shown in the figure below:

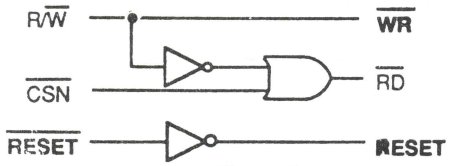


Figure 3

Note: This is required for 6800 based microprocessors and is not necessary for 68000 based machines.

The addressing of the internal registers of the QUART is described in Table 1. The mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The MR1n pointer is set by a hardware reset or by 'reset pointer' command from command register (CRn bit4-7). Any read or write operation to the mode register while the pointer is pointing at MR1n switches the pointer to MR2n and remains there such that any subsequent accesses are always to MR2n unless the pointer is reset back to MR1n.

INTERRUPT CONTROL

An interrupt request output signal (INTRN) is provided which may be programmed to be asserted upon the occurrence of any of the following events:

Transmit Hold register A,B,C or D ready.
Receive Hold register A,B,C or D ready.
Receive FIFO A,B,C or D Full.
Start or End of received Break A,B,C or D
End of Counter/Timer count reached.
Change of State on input pins IP0,
IP1, IP2, IP3, IP8, IP9, IP10 or IP11

Associated with the interrupt system are the interrupt status register (ISRn), the interrupt mask register (IMRn), and the interrupt vector register (IVRn).The ISRn indicates the current state of all the potential interrupting conditions listed above. The IMRn may be programmed to select only certain of these conditions to assert the INTR output.

In the 88 mode, the QUART may be programmed to operate in two modes to accommodate different CPU interface requirements.

In the "I mode", which is the default mode, after a hardware reset, interrupt prioritization and interrupt vector generation, if required, are implemented using external hardware. In this mode, the on-chip interrupt vector register is not utilized and is available for use as an auxiliary read/write register for any purpose.

In the "Z mode", which is invoked via a command to command register B three pins are designated as an interrupt acknowledge (IACK), interrupt enable input (IEI) and interrupt enable output (IEO). IEI and IEO are the input and output of an interrupt daisy chain, as illustrated in Figure 1A. IEI high means that the QUART may generate an interrupt request.

Counter/Timer (either DUART 1 or 2 as need.ed), and last the change of state on the inputs IP0, IP1, IP2, IP3, IP8, IP9, IP10 or IP11 (either DUART 1or 2 and sequence as shown).

Sometime after the interrupt request, the CPU will respond with an interrupt acknowledge cycle, followed by a RD cycle (Figure 1B). The time between IACK and RD allows the daisy chain to stabilize. Also as long as IACK is asserted, the QUART is inhibited from issuing a new interrupt request. The device making the request sets its internal 'interrupt under service' (IUS) latch and places the vector from the IVR (Interrupt Vector Register) on the data bus. Upon completion, the CPU must issue a reset IUS latch command to the chip, which resets the latch and returns the daisy chain to its normal condition. In the 68 mode, the QUART has its interrupt request active and responds to the IACK input by placing the vector from the IVR on the data bus and asserting DTACK. Otherwise, it ignores IACK.

In either mode, outputs OP3-OP7 and OP11-OP15 can be programmed to provide separate open drain interrupt requests for transmitters A,B,C and D, receivers A,B,C and D, and the timer/counter 1, 2. See pin description.

TIMING

The timing block as illustrated in Figure 2 contains a crystal oscillator, a bit rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors.

The crystal oscillator operates from a parallel crystal connected between the X1/CLK and X2 pins. A crystal frequency of 3.6864 or 7.3728 MHz is required for generation of standard bit rates by the bit rate generator (see Table 3). A crystal clock or an external TTL clock signal on the X1/CLK pin can be used either directly or it can be divided by two before being used to generate the internal system clock. After reset, the device is in the divide by two mode. To select direct system clock, write "CO" in channel C of the command register. If an external clock is available, it may be connected to X1/CLK, with X2 left open.

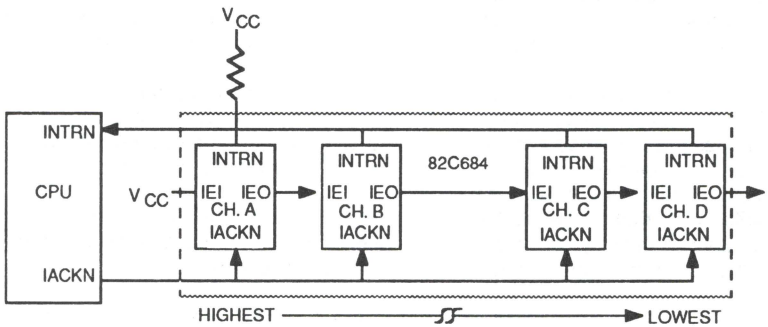


Figure 4A. Daisy Channel Interrupt Block Diagram

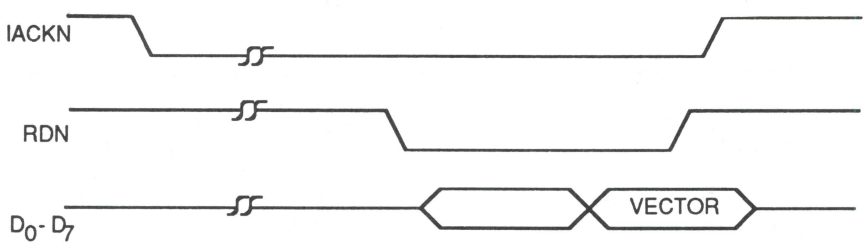


Figure 4B. Daisy Chained Interrupt Timing

The output of the oscillator is used by the BRG, the C/T and other internal circuits. This requires that a clock within the specified limits always be supplied to the QUART.

Bit Rate Generator

The BRG uses the crystal oscillator or external clock as an input and generates the clock for 33 commonly used data communications bit rates ranging from 50 to 230.4K bits per second. The actual clock frequencies output from the BRG are at 16 times these rates. The counter/timer can also be used as a programmable bit rate generator to produce a 16x clock for any bit rate not provided by the BRG. The four clock select multiplexers/per channel allow each receiver and transmitter to independently select its operating frequency as one of the outputs from the BRG, the output of the counter/timer, or an external clock. (See Input Port Selection in the Pin Description Table, page 8)

Counter /Timer

Each C/T is a programmable 16-bit down-counter which can use one of several timing sources as their input. The C/T outputs are available to the clock selectors for use as a programmable bit rate for any receiver or transmitter (note that counter/timer 1 is used for A/B receiver and transmitter, counter/timer 2 is used for C/D receiver and transmitter), each can be programmed to generate an interrupt each time it reaches its terminal count of OOOOH, and can also be programmed as an output at OP3 and OP11.

In the timer mode, the C/T acts as a programmable divider and generates a square wave whose period is twice the value (in clock periods) of the contents of the counter/timer registers CTUR and CTLR. The contents of these registers may be changed at any time, but will only begin to take effect at the next half cycle of the square wave. The C/T begins operation using the values in CTUR/CTLR upon receipt of a 'start counter' command (see Table 1).

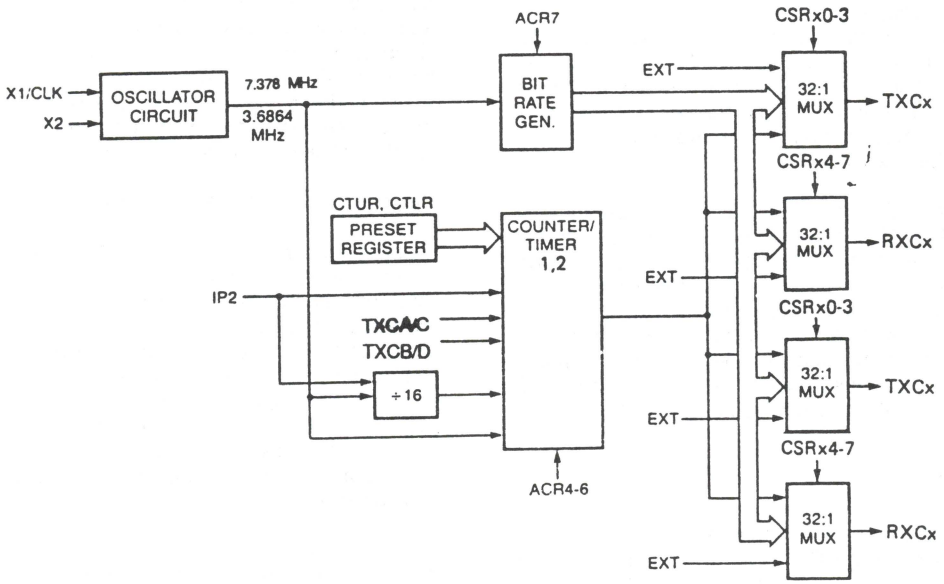


Figure 5. Half of QUART Timing Circuit Block Diagram

The C/T then runs continuously. A subsequent 'start counter' command causes the C/T to terminate the current timing cycle and begin a new timing cycle using the current values in CTUR and CTLR. The counter ready status bit (ISRn) is set once each cycle of the square wave. This allows use of the C/T as a periodic interrupt generator if the condition is programmed to generate an interrupt via the interrupt mask register. The status bit can be reset by issuing a 'stop counter' command (see Table 1). In this mode, however, the command does not actually stop the C/T. The generated square wave is output on OP3 or OP11 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses written into CTUR/CTLR, beginning at the receipt of a 'start counter' command. The counter ready status bit (ISR [3]) is set upon reaching the count of OOOOH. The C/T will continue to count past this (with the next count being FFFFH) until it is stopped by the CPU via a 'stop counter' command. If OP3 or OP11 is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time the output goes low. It then returns to the high state and ISR[3] is cleared when the counter is stopped. A 'start counter' command while the counter is running restarts the counter with the values in CTUR/CTLR. The CPU may change CTUR or CTLR at any time but the new count takes effect only on the next start counter command. If new values are not programmed, the previous values are preserved and used for the next cycle.

In counter mode, the current value in the C/T may be read by the CPU by reading the upper and lower halves of the C/T separately (see Table 1). Stopping the counter when it is read is recommended in order to prevent potential problems which may occur if a carry from the lower half to the upper half occurs between the times that the two halves are read. However, note that a new start counter command will cause the counter to begin counting using the values in CTUR/CTLR.

INPUT PORT

The current state of the inputs to this unlatched port can be read by the CPU by performing a read as described in Table 1. A high input results in a logic "1" while a low input results in a logic "0". The pin description tables describe the alternate uses for the input pins, such as clock inputs and interrupt control sampled by the 38.4 kHz output of the BRG (2.4 Kbps x 16). A high-to-low or low-to-high transition at these inputs lasting at least two clock periods (approximately 50 µs) will guarantee that the corresponding bit in the input port change register (IPCR) will be set, although it may be set by a change of state as short as 25 µs. The status bits in the IPCR are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt.

OUTPUT PORT

The output ports can be used as a general purpose output or can be used to output timing and status signals by appropriately programming of the mode registers (MR1A-D, MR2A-D) and also the output port configuration registers. When used to output status signals the pins are open drain, which allows their use in a wire OR interrupt scheme.

When used as a general purpose output port, the outputs are the complements of the output port register (OPR). $OPR_{(n)}$ = 1 results in $OP_{(n)}$ low while $OPR_{(n)}$ = 0 results in $OP_{(n)}$ high. Bits of OPR can be set and reset individually. A bit is set by the address-triggered 'set output port bits' command (see Table 1) with the accompanying data specifying the bits to be set (1 = set, 0 = no change). A bit is reset by the address-triggered 'reset output port bits' command (see Table 1) with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

SERIAL CHANNELS A, B, C and D

Each serial channel of the QUART comprises a full duplex asynchronous receiver and transmitter. The four channels can independently select their operating frequency (from the BRG, the C/T, or an external clock) as well as operating mode. Besides the normal mode in which the receiver and transmitter of each channel operate independently, the QUART can be configured to operate in various looping modes, which are useful for local and remote diagnostics, as well as in a wake-up mode used for multidrop applications.

Note: In the descriptions which follow, the transmitter and receiver are described for either channel. References to input and output pins and control and status bits and registers apply to either channel unless otherwise noted.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream at the TXD pin, adding start, stop and optional parity bits as required by the asynchronous protocol.

The QUART is conditioned to transmit data when the transmitter is enabled via the command register. It indicates that it is ready to accept a character from the CPU for serialization by setting the TXRDY bit in the status register. This condition can be programmed to assert an interrupt request via the INTRN output and can also be programmed to assert the OP6/14 output (channel A/C) or the OP7/15 output (channel B/D). These conditions are negated when the CPU loads a character into the transmit holding register (THR). Data is transferred form the THR to the transmit shift register (TSR) immediately if the TSR is idle or when it completes serialization of the previous character. The TXRDY condition is then asserted again. Thus, one full character time of buffering is provided. Note that the THR will not accept characters while the transmitter is disabled.

The transmitter sends a start bit followed by the programmed number of data bits (least significant bit first), an optional parity bit, and the programmed number of stop bits and begins transmission of the next character if one has been loaded into the THR. Otherwise, the TXD output will remain high and the TXEMT status bit will be set following the transmission of the stop bits. Transmission resumes and the TXEMT status bit is cleared when the CPU loads a new character into the THR. The transmitter can be forced to send a continuous low at TXD by invoking a 'send break' command.

If the transmitter is disabled, it continues operating until the character currently being serialized, and any in the THR, are completely sent out. The transmitter can be reset by a software command. In this case, operation ceases immediately and the transmitter must be re-enabled before resuming operation.

Setting MR2n[4] of the appropriate channel programs its transmitter to begin transmission of a character only if the channels clear-to-send input pin (IP0 for channel A, IP1 for channel B, IP8 for channel C and IP9 for channel D) is low. If CTSN goes high in the middle of a transmission, the transmission of the current character is completed but TXD remains high and the next character will not be sent until CTSN is low again. Setting MR2[5] of the appropriate channel programs the transmitter to automatically deactivate its request-to-send output pin (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D). If so programmed, and the transmitter has been disabled, the RTSN output will be negated one bit time after the characters in the TSR and THR (if any) are completely sent.

Receiver

The receiver accepts serial data at its RXD pin, checks for a proper start bit, converts the serial input to parallel form, checks the parity bit (if parity is specified), checks for presence of a stop bit, performs several other tests on the received data, and sends the assembled character to the CPU.

Each receiver is conditioned to receive data when it is enabled via the command register. It looks for a high to low (mark to space) transition indicating a start bit at the RXD input. If a transition is detected, the state of RXD is sampled each 16x clock for 7 1/2 clocks (16x clock mode) or at the next rising edge of the bit time clock (1x clock mode). If RXD is detected high at these sample times, the start bit is invalid and the search for a start bit begins again. If RXD remains low, a valid start bit is assumed and the receiver continues to sample the data at one bit time intervals, at the theoretical center of the bit , until the programmed number of data bits (LSB first), the parity bit (if any), and one stop bit have been assembled. The data is then transferred to the receive holding register (RHR) with the most significant unused bits set to zero. The status conditions (parity error, framing error, overrun error, and break received) are set to indicate to the CPU that a character is available to be read. Setting of RXRDY can be programmed to generate an interrupt request via INTRN and to assert OP4 (channel A), OP5 (channel B), OP12 (channel C) and OP13 (channel D).

After the stop bit position is sampled, the receiver will immediately begin to look for the start bit of the next character. However, if a non-zero character was received without a stop bit time after sampling of the stop bit, the receiver operates as if a new start bit transition had been detected at that point (half a bit time after the sampling of the stop bit).

If a break is received (an all zeroes character including the first stop bit), only a single character consisting of all zeroes will be loaded into the FIFO and the

break received status bit will be set, no matter how long the break condition persists. RXD must return to a high condition for at least half a bit time before the search for a new start bit begins again.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the topmost empty position in the FIFO. RXRDY is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. Either of these bits can be selected to assert an interrupt. A read of the RHR outputs the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data.

In addition to the data word, three status bits are appended to each character position in the FIFO. These are parity error, framing error, and received break. Status can be provided in two ways, as programmed by MR1[5] in the channels mode register. In the 'character' mode, status is provided on a character by character basis: the status applies only to the character at the top of the FIFO. In the block mode, these three bits in the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode, reading the status register does not affect the FIFO. The FIFO is popped only when the RHR is read. Therefore, the status register should be read prior to reading the RHR. Also note that PE, FE and received break status register is asserted.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If a new start bit is detected while this condition exists, the character previously in the shift register is lost and the overrun error status bit is set. The contents of the FIFO are not affected when this occurs.

If the receiver is disabled, the contents of the FIFO are maintained and can be read by the CPU. Resetting the receiver initializes the FIFO pointers and clears the status bits immediately. In either case, any character currently being assembled is lost and operation does not resume until the receiver is re-enabled.

Setting MR[7] of the appropriate channel programs the receiver to automatically control de-activation of the request-to-send output (OP0 for channel A, OP1 for channel B). If so programmed, RTSN will be negated when a valid start bit is received while the FIFO is full, and will automatically be re-asserted when a FIFO position becomes available for that character. This feature can be used to prevent an overrun in the receiver by connecting the RTSN output to the CTSN input of the transmitting device.

Multidrop (8051 9-bit) Mode

Each serial channel of the QUART can be configured to operate in a wake-up mode useful for multidrop or multiprocessor applications. This mode is compatible with the serial 'Nine-bit Mode' of 8051-family microcomputers. In this mode of operation a master station, connected to a maximum of 256 slave station, transmit an address character followed by a block of data characters targeted for the addressed slave station. The slave stations normally have their receivers disabled. However, in this mode, the slave receivers monitor the incoming data stream and wake up the CPU (by asserting RXRDY) when any address character is detected. The slave station CPU then compares the received address to its own assigned address and enables the receiver, if it wishes, to receive the subsequent block of data, or leaves the receiver disabled if it does not. Upon completion of reception of the block of data, the receiver is disabled to re-initiate the process.

The multidrop mode is selected by programming MR[4:3] of the channel to '11'. In this mode, a transmitted character consists of a start bit, the programmed number of data bits, and address/data flag bit (A/D), and the programmed number of stop bits. A/D = 0 indicates that the character is data, while A/D = 1 identifies it as an address. The CPU controls the state of A/D in the transmitted character by programming MR1[2] of the channel prior to loading the data bits into the THR. MR1[2] = 0 results in A/D = 0 and MR1[2] =1 results in A/D =1.

In the multidrop mode, the receiver continuously looks at RXD whether enabled or not. When disabled, it loads a character into the RHR and sets RXRDY if its A/D bit is one (address flag) but discards the character if its A/D bit is zero (data flag). If the receiver is enabled, all characters received are transferred to the RHR. In either case, the received data bits are loaded into the RHR while the A/D bit is loaded into SR[5], the status register position normally used for parity error. Framing error, overrun error, and break detect status bits operate normally.

Standby Mode

The QUART may be placed in a standby mode to conserve power when its operation is not required. Upon reset, the QUART will be in the 'active operation' mode. A 'set standby mode' command issued via the channel A command register disables all clocks on the device except for the crystal oscillator, which significantly reduces the operating current. In this mode the only functions which will operate correctly are reading the input port, writing the output port and the 'set active mode' command. The latter, also invoked via the channel A command register, restores the device to normal operation within 25 µs. Resetting the transmitters and receivers and writing 00H into the interrupt mask register before going into the standby mode is recommended to prevent any spurious interrupts from being generated. The chip should be reprogrammed after the 'set active mode' command since register contents are not guaranteed to remain stable during the standby mode. Active operation can also be restored via hardware reset.

PROGRAMMING

Operation of the QUART is programmed by writing control words into the appropriate registers, while operational feedback is provided by status registers which can be read by the CPU. Register addressing is shown in Table 1.

A hardware reset clears the contents of SRA, SRB, IMR, ISR, OPR and OPCR and initializes the IVR to 0FH. During operation, care should be exercised if the contents of control registers are to be changed, since certain changes may result in improper operation. For example, changing the number of bits per character while data is being received may result in reception of an erroneous character. In general, changes to registers which control receiver or transmitter operation should be made only while the transmitter or receiver are disabled, and certain changes to the ACR should be made only when the C/T is stopped.

Mode, command, clock select, and status registers are duplicated for each channel to provide totally independent operation. Table 2 illustrates the bit assignments for each register.

Note: In the descriptions which follow, registers which are duplicated for each channel are described generically. References to input and output pins and control and status bits and registers apply to each channel unless otherwise noted.

Address (HEX)	Reading From The Registers	Writing To The Registers
0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
1	Status Register A (SRA)	Clock Select Register A (CSRA)
2	Masked Interrupt Status Register 1(MISRA)	Command Register A (CRA)
3	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
4	Input Port Change Register 1 (IPCR1)	Auxiliary Control Register A (ACRA)
5	Interrupt Status Register 1 (ISR1)	Interrupt Mask Register 1 (IMR1)
6	Counter/Timer 1 Upper byte (CTU1)	Counter/Timer 1 Upper Register (CTUR1)
7	Counter/Timer 1 Lower byte (CTL1)	Counter/Timer 1 Lower Register (CTLR1)
8	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
9	Status Register B (SRB)	Clock Select Register B (CSRB)
A	RESERVED	Command Register B (CRB)
B	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
C	Interrupt Vector Register A (IVR1)	Interrupt Vector Register 1 (IVR1)
D	Input Port A (IP1)	Output Port Configuration Register 1 (OP0-OP7), (OPCRA)
E	Start Counter/Timer 1 (SCC1)	Set Output Port Bits Command 1 (SOPBC1)
F	Stop Counter/Timer Command 1 (STC1)	Reset Output Port Bits Command 1 (ROPBC1)
10	Mode Register C (MR1C, MR2C)	Mode Register C (MR1C, MR2C)
11	Status Register C (SRC)	Clock Select Register C (CSRC)
12	Masked Interrupt Status Register 2(MILSRB)	Command Register C (CRC)
13	Rx Holding Register C (RHRC)	Tx Holding Register C (THRC)
14	Input Port Change Register 2 (IPCR2)	Auxiliary Control Register B (ACRB)
15	Interrupt Status Register 2 (ISR2)	Interrupt Mask Register B (IMR2)
16	Counter/Timer 2 Upper byte (CTU2)	Counter/Timer 2 Upper Register (CTUR2)
17	Counter/Timer 2 Lower byte (CTL2)	Counter/Timer 2 Lower Register (CTLR2)
18	Mode Register D (MR1D, MR2D)	Mode Register D (MR1D, MR2D)
19	Status Register D (SRD)	Clock Select Register D (CSRD)
1A	RESERVED	Command Register D (CRD)
1B	Rx Holding Register D (RHRD)	Tx Holding Register D (THRD)
1C	Interrupt Vector Register B (IVR2)	Interrupt Vector Register 2 (IVR2)
1D	Input Port B (IP2)	Output Port Configuration Register 2 (OP8-OP15), (OPCRB)
1E	Start Counter/Timer 2 (SCC2)	Set Output Port Bits Command 2 (SOPBC2)
1F	Stop Counter/Timer Command 2 (STC2)	Reset Output Port Bits Command 2 (ROPBC2)

TABLE 1. QUART PORT AND REGISTER ADDRESSING

MODE REGISTER 1 (Channels A - D)

MR1 for each channel is accessed when the channel's MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command invoked via the channel's command register. After reading or writing MR1, the pointer will point to MR2.

MR1(7) - Receiver Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D) by the receiver. RTSN is normally asserted by setting the respective output bit (OP 1/2/8/9 for channels A/B/C/D), and negated by resetting the same bit. MR1(7) = 1 causes RTSN to be negated automatically upon receipt of a valid start bit if the channel's FIFO is full and to be re-asserted again when an empty FIFO position becomes available. This flow control feature can be used to prevent overrun of the receiver by using the RTSN output to control transmission of characters to the QUART.

MR1(6) - Receiver Interrupt Select

This bit selects either the RXRDY status bit or the FFULL status bit of the channel to be used for CPU interrupts. It also causes the selected bit to be output on OP4 channel A, OP5 channel B, OP12 channel C or OP13 channel D.

MR1(5) - Error Mode Select

This bit controls the operation of the three FIFO status bits (PE, FE, received break) for the channel. In the character mode these status bits apply only to the character currently at the top of the FIFO. In the block mode these bits are the cumulative logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command for the channel was issued.

MR1(4:3) - Parity Mode Select

If 'with parity' or 'force parity' operation is programmed, a parity bit is added to the transmitted characters and the receiver performs a parity check on received characters. See OPERATION section for description of multidrop mode operation.

MR1(2) - Parity Type Select

This bit selects odd or even parity if 'with parity' mode is programmed and the state of the forced parity bit if the 'force parity' mode is programmed. In the multidrop mode it selects the state of the A/D flag bit. This bit has no effect if 'no parity' mode is programmed.

MR1(1:0) - Bits per Character Select

Selects the number of bits to be transmitted and received in the data field of the character. This does not include start, parity and stop bits

MODE REGISTER 2 (Channels A-D)

MR2 for each channel is accessed when the channel's MR pointer points to MR2, which occurs after any access to the channel's MR1. Reading or writing MR2 does not change the pointer.

MR2(7:6) - Channel Mode Select

Each channel can operate in one of four modes. MR2(7:6) = 00 in the normal mode where the receiver and transmitter operate independently.

MR2(7:6) = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions apply while in this mode:

1. Received data is transmitted on the channel's TXD output.
2. The receiver must be enabled but the transmitter need not be enabled.
3. The channel's TXRDY and TXEMT status bits are inactive.
4. The received parity is checked but is not regenerated for transmission. Thus, transmitted parity is as received.
5. Character framing is checked but the stop bits are transmitted as received.
6. A received break is echoed as received until the next valid start bit is detected.
7. CPU to receiver communications operate normally, but the CPU to transmitter link is disabled.

MR1A-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Rx RTS Control	Rx Int Select	Error Mode	Parity Mode		Parity Type	Bits Per Char.	
0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multi-drop Mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

MR2A-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Channel Mode		Tx RTS Control	CTS Enable Tx	Stop Bit Length*			
00 = Normal 01 = Auto Echo 10 = Local Loop 11 = Remote Loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/character.

CSRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Receiver Clock Select				Transmitter Clock Select			
See Table 3				See Table 3			

CRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Miscellaneous Commands				Disable Tx	Enable Tx	Disable Rx	Enable Rx
See Text				0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

SRA-D

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Received Break	Framing Error	Parity Error	Overrun Error	TXEMT	TXRDY	FFULL	RXRDY
0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

OPCR1,2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OP7/OP15	OP6/OP14	OP5/OP13	OP4/OP12	OP3/OP11		OP2/OP10	
0 = OPR[7/15] 1=TXRDYB/D	0 = OPR[6/14] 1=TXRDYA/C	0 = OPR[5/13] 1 = RXRDY/ FFULLB/D	0 = OPR[4/12] 1 = RXRDY/ FFULLA/C	00 = OPR[3/11] 01 = C/T Output 10 = TxCB/D(1X) 11 = RxCB/D(1X)		00 = OPR[2/10] 01 = TXCA/C(16X) 10 = TXCA/C(1X) 11 = RXCA/C(1X)	

ACR1,2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BRG Set Select	Counter/Timer Mode and Source			Delta IP3/IP11	Delta IP2/IP10	Delta IP1/IP9	Delta IP0/IP8 Int
0 = Set1 1 = Set2	See Table 6			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IPCR1,2	Delta IP3/IP11	Delta IP2/IP10	Delta IP1/IP9	Delta IP0/IP8	IP3 IP11	IP2 IP10	IP1 IP9	IP0 IP8
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR1,2	Input Port Change1, 2	Delta Break B/D	RXRDY/ FFULLB/D	TXRDYB/D	Counter Ready1, 2	Delta Break A/C	RXRDY/ FFULLA/C	TXRDYA/C
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR1,2	Input Port Change Int1, 2	Delta Break B/D Int	RXRDY/ FFULLB/D Int	TXRDYB/D Int	Counter Ready Int1, 2	Delta Break A/C Int	RXRDY/ FFULLA/C Int	TXRDYA/C Int
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTU1,2	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR1,2								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTL1,2	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR1,2								

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IVR1,2	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

Table 2. Register Bit Formats (continued)

MR2(7:6) - Channel Mode Select (cont.)

Two diagnostic modes can also be configured.

The first is the local loopback mode, selected by MR2(7:6) = 10. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The channel's TXD output is held marking (high).
4. The channel's RXD input is ignored.
5. The transmitter is enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2(7:6) = 11. In this mode:

1. Received data is transmitted on the channel's TXD output.
2. Received data is not sent to the CPU and the error status conditions are not checked.
3. Parity and framing (stop bits) are transmitted as received.
4. The receiver must be enabled.

MR2(7:6) - Channel Mode Select (cont.)

5. A received break is echoed as received until the next valid start bit is detected.

Care must be taken when switching into and out of the various modes. The selected mode will be activated immediately after it is programmed even if this occurs in the middle of transmitting or receiving a character. An exception to this is switching out of autoecho or remote loopback modes: if this deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RXRDY), and the transmitter is enabled, the transmitter will remain in autoecho or remote loopback mode until one entire stop bit has been transmitted.

MR2(5) - Transmitter Request-to-Send Control

This bit controls the negation of the RTSN output (OP0 for channel A, OP1 for channel B, OP8 for channel C and OP9 for channel D) by the transmitter. RTSN is normally asserted by setting the respective output port bits (OP1/2/8/9 for channels A/B/C/D) and negated by resetting the same bit. MR2(5) = 1 causes OP1/2/8 or 9 to be reset automatically one bit time after the characters in the channel's transmit shift register and THR, if any, are completely transmitted, including the programmed number of stop bit, if the transmitter has been disabled. This feature can be used to automatically negate RTSN at the conclusion of a message as follows:

1. Program auto-reset mode (MR2[5] =1).

2. Enable transmitter and assert the channel's RTSN output by setting the appropriate bit in the output port register.

3. Send message.

4. Disable the transmitter after the last character of the message is loaded into the THR.

MR2(4) - Clear-to-Send Control

If this bit is a 0, the channels CTSN input (IP0 for channel A, IP1 for channel B, IP8 for channel C and IP9 for channel D) has no effect on the transmitter. Ifthe bit is a 1, the transmitter checks the state of its CTSN each time it is ready to send a character. If CTSN is low, the character is transmitted. If CTSN is high, TXD remains in the marking state and the transmission of the next character is delayed until CTSN goes low. Changes in CTSN while a character is being serialized do not affect transmission of that character.

MR2(3:0) - Stop Bit Length

This field programs the duration of the stop bit appended to each transmitted character. Stop bit durations of 9/16 to 1 bit time a 1-9/16 to 2 bit times, in increments of 1/16 bit, can be programmed for character lengths of 6, 7 and 8 bits. For a 5-bit character, the stop bit duration can be programmed from 1-1/16 to 2 bit times.

If an external 1x clock is programmed for the transmitter, MR2(3) = 0 selects a stop bit duration of one bit time and MR2(3) = 1 selects a duration of two bit times for transmission.

The receiver only checks for mark condition at the center of the first stop bit (that is, one bit time after the last data or parity bit is sampled) regardless of the programmed transmitted stop bit length.

CLOCK SELECT REGISTER (Channels A-D)

CSR (7:4) and CSR (3:0) of each channel operate in conjunction with ACR(7) and the channel's set/clear BRG select extend' commands to allow independent selection of the bit rates for the receiver and transmitter respectively. The BRG can generate 33 different bit rates, of which 22 is selected by programming ACR(7). The bit rates generated when using a 3.6864 MHz crystal or an external clock of the same frequency are shown in Table 3A, where 'X' refers to the current state of the extend bit (see CR [7:4] selection). Note that the actual outputs from the BRG are at 16x the bit rates shown in the table.

COMMAND REGISTER (Channels A-D)

Each channel of the QUART has a command register used to supply commands to the respective channel. Multiple commands may be invoked simultaneously by a single write to the command register as long as the commands are non-conflicting.

CR(7:4) - Miscellaneous Commands
The encoded value of this field specifies a single command as follows:

0 0 0 0 - Null Command.

0 0 0 1 - Reset MR Pointer - causes the channel's MR pointer to point to MR1.

0 0 1 0 - Reset Receiver - reset the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0 0 1 1 - Reset Transmitter - resets the transmitter as if a hardware reset had been applied. The TXD output is forced to a high level.

0 1 0 0 - Reset Error Status - clears the received break (RB), parity error (PE), framing error (FE) and overrun error (OE) status bits, SR(7:3). Used in character mode to clear the OE status bit (although the RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

Field	Bit Rate			
CSR[7:4] CSR[3:0]	ACR[7] = 0		ACR[7] = 1	
	X = 0	X = 1	X = 0	X = 1
0 0 0 0	50	75	75	50
0 0 0 1	110	110	110	10
0 0 1 0	134.5	134.5	134.5	134.5
0 0 1 1	200	150	150	200
0 1 0 0	300	3600	300	3600
0 1 0 1	600	14.4K	600	14.4K
0 1 1 0	1200	28.8K	1200	28.8K
0 1 1 1	1050	57.6K	2000	57.6K
1 0 0 0	2400	115.2K	2400	115.2K
1 0 0 1	4800	4800	4800	4800
1 0 1 0	7200	1800	1800	7200
1 0 1 1	9600	9600	9600	9600
1 1 0 0	38.4K	19.2K	19.2K	38.4K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1 1 1 1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

TABLE 3A CSR [7:4] / [3:0] Bit Rate Selection (3.686 MHz)

Field	Bit Rate			
CSR[7:4] CSR[3:0]	ACR[7] = 0		ACR[7] = 1	
	X = 0	X = 1	X = 0	X = 1
0 0 0 0	100	150	150	100
0 0 0 1	220	220	220	220
0 0 1 0	269	269	269	269
0 0 1 1	400	300	300	400
0 1 0 0	600	7200	600	7200
0 1 0 1	1200	28.8K	1200	28.8K
0 1 1 0	2400	57.6K	2400	57.6K
0 1 1 1	2100	115.2K	4000	115.2K
1 0 0 0	4800	230.4K	4800	230.4K
1 0 0 1	9600	9600	9600	9600
1 0 1 0	14.4K	3600	3600	14.4K
1 0 1 1	19.2K	19.2K	19.2K	19.2K
1 1 0 0	76.8K	38.4K	38.4K	76.8K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	EXT - 16x	EXT - 16x	EXT - 16x	EXT - 16x
1 1 1 1	EXT - 1x	EXT - 1x	EXT - 1x	EXT - 1x

TABLE 3B CSR [7:4] / [3:0] Bit Rate Selection (7.3728 MHz)

0 1 0 1 - Reset Break Change Interrupt - clears the channel's break change interrupt status bit.

0 1 1 0 - Start Break - forces the TXD output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. If the transmitter is active, the break begins when the transmission of that character in the THR is completed, viz., TXEMT must be true before the break will begin.

0 1 1 1 - Stop Break - the TXD line will go high within two bit times. TXD will remain high for one bit time before the next character, if any, is transmitted.

1 0 0 0 - Set Rx BRG Select Extend Bit - sets the receiver BRG select extend bit for the channel to 1.

1 0 0 1 - Clear Rx BRG Select Extend Bit - clears the receiver BRG select extend bit for the channel to 0.

1 0 1 0 - Set Tx BRG Select Extended Bit - sets the transmitter BRG select extend bit for the channel to 1.

1 0 1 1 - Clear Tx BRG Select Extend Bit - clears the transmitter BRG select extend bit for the channel to 0.

1 1 0 0 - Set Standby Mode (Channel A) Reset IUS Latch (Channel B) and Select Direct Systems Clock (Channel C) - when this command is invoked via the channel A command register, power is removed from the transmitters, receivers, counter/timer and additional circuits to place the QUART in the standby mode. Normal operation is restored by a hardware reset or by invoking the 'set active mode' command.

When this command is invoked via the channel B command register, and the QUART (88 Mode) is operating in Z-mode, it causes the interrupt-under-service latch to be reset.

When this command is invoked via the channel C command register, the QUART will generate its internal system clock and take a direct crystal or TTL clock signal to generate a set of standard baud rates described in Table 3A.

1 1 0 1 - Set Active Mode (Channel A) Set Z-mode (Channel B) and Select Divided System Clock (Channel C) - when this command is invoked via the channel A command register the QUART is removed from the stand-by mode and resumes normal operation.

When this command is invoked via the channel B command register, the QUART is conditioned to operate in the Z-mode. This applies only in the 88 mode.

When this command is invoked via the channel C command register, the QUART is set to generate internal system clock after dividing the external clock input frequency by two. In this mode an external 7.3728 MHz clock may be used.

1 1 1 0 - Set Special MR Pointer - this single command, invoked through channel A of the QUART, sets a special pointer which points to all 4 shadow mode registers simultaneously.

1 1 1 1 - Reset Special MR Pointer - this command resets the special mode register pointer and enables access to the normal mode registers.

Note: When writing 'O4H' at the mode register address of the selected channel, this value is written into the selected shadow mode register since the normal mode register address are disabled by the special pointer. In this step the TXFIFO mode bit (bit 2) is set. This procedure can be executed regardless of the state of the normal mode register pointer whose value stays intact throughout the procedure. Note also that the TXFIFO can be activated independently for each channel of the QUART. The lowest two bits (bits 0 and 1) of the shadow mode register are reserved for factory testing and must never be set to 1's.

CR[3] - Disable Transmitter

This command terminates operation of the channel's transmitter and resets the TXRDY and TXEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before going into the inactive state.

CR[2] - Enable Transmitter

This command enables operation of the channel's transmitter and asserts the TXRDY status bit.

CR[1] - Disable Receiver

This command immediately terminates operation of the channel's receiver. Any character being received will be lost. The command has no effect on the receiver status bits or on any other control registers. If the multidrop mode is programmed, the receiver operates even if it is disabled. See OPERATION section.

CR[0] - Enable Receiver

This command enables operation of the receiver. If not in the multidrop mode, it also forces the receiver to start searching for the start bit.

STATUS REGISTER (Channels A-D)

SR[7] - Received Break

This bit indicates that an all zero character of the programmed length was received without a stop bit. Only a single FIFO position is occupied when a break is received. Additional transfers into the FIFO are inhibited until the RXD line returns to the marking state for at least half a bit time. This is defined as two successive edges of the internal or external 1 x clock.

When this bit is set, the channel's change in break status bit in the ISR is set. The bit in the ISR is also set when the end of the break condition, as defined above, is detected.

The chip's break detect logic can detect breaks that begin in the middle of a character. However, the break must persist until the end of the next character time in order for it to be detected.

SR[6] - Framing Error

When set, this bit indicates that RXD was low when the stop bit of the character is the FIFO was sampled. The stop bit check is made in the middle of the first stop bit position (one bit time after sampling the last data bit or the parity bit at its midpoint) regardless of the stop bit length programmed.

SR[5] - Parity Error

This bit is set when the 'with parity' or 'force parity' modes are programmed if the corresponding character in the data FIFO was received with incorrect parity.

In the multidrop mode, this status bit indicates the state of received address/data (A/D) flag bit.

SR[4] - Overrun Error

If set, this bit indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its error status) is overwritten.

This bit is cleared by a 'reset error status' command.

TABLE 5. BIT RATE GENERATOR CHARACTERISTICS
Crystal or Clock Input = 3.6864 MHz or 7.3728 MHz

Nominal Rate (bps)	Actual Clock (KHz)	Error (Percent)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.26
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
3600	57.6	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
14.4K	230.4	0
19.2K	307.2	0
28.8K	460.8	0
38.4K	614.4	0
57.6	921.6	0
115.2K	1843.2	0

TABLE 6. ACR [6:4] FIELD DEFINITIONS

ACR [6:4]	Mode	Clock Source
0 0 0	Counter	External - IP2/10 Input
0 0 1	Counter	TXCA/C 1x Clock of Channel A/CTx
0 1 0	Counter	TXCB/D 1x Clock of Channel B/DTx
0 1 1	Counter	X1/CLK Input Divided by 16
1 0 0	Timer	External - IP2/10 Input
1 0 1	Timer	External Divided by 16 - IP2/10 Input
1 1 0	Timer	X1/CLK Input
1 1 1	Timer	X1/CLK Input Divided by 16

SR[3] - Transmitter Empty (TXEMT)

This bit is set when the transmitter underruns. It is set after transmission of the last stop bit of a character, if there is no character, the THR is awaiting transmission. It is reset when the THR is loaded by the CPU and when the transmitter is disabled.

SR[2] - Transmitter Ready (TXRDY)

This bit, when set, indicates that the THR is empty and ready to accept a character. The bit is cleared when the THR is loaded by the CPU and is set when that character is transferred to the transmit shift register. TXRDY is set when the transmitter is initially enabled and is reset when the transmitter is disabled. Characters loaded into the THR while the transmitter is disabled will not be transmitted.

SR[1] - FIFO Full (FFULL)

This bit is set when a character is transferred from the receive shift register to the FIFO and the transfer causes it to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SR[0] - Receiver Ready (RXRDY)

This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when a character is transferred from the receive shift register to the FIFO and reset when the CPU reads the last character currently stored in the FIFO.

OUTPUT PORT CONFIGURATION REGISTER (1, 2)

This register programs the output port to provide alternate functions. Note that when an output is programmed as an interrupt, it is not masked by the contents of the IMR.

OPCR [7/15] - OP7/OP15 Output Select

This bit programs the OP7/OP15 output to provide one of the following:

0-The complement of OPR[7]/[15].

1-The channel B/D transmitter interrupt TXRDY B/D which is the complement of SRB/D [2]. In this mode, OP7, and/or OP15 are open drain outputs.

OPCR [6/14] - OP6/OP14 Output Select

This bit programs the OP6/OP14 output to provide one of the following:

0-The complement of OPR[6]/[14].

1-The channel A/C transmitter interrupt output, TXRDY A/C which is the complement of SRA/C[2]. In this mode OP6/OP14 are open drain outputs.

OPCR [5/13] - OP5/OP13 Output Select

This bit programs the OP5/OP13 output to provide one of the following:

0-The complement of OPR[5]/[13].

1-The channel B/D receiver interrupt output, which is the complement of ISR[5]. In this mode OP5/OP13 are open drain outputs.

OPCR [4/12] - OP4/OP12 Output Select

This bit programs the OP4/OP12 output to provide one of the following:

0-The complement of OPR[4]/ [12].

1-The channel A/C receiver interrupt output, which is the complement of ISR[5]. In this mode OP5 / OP12 are open drain outputs.

OPCR[3:2] - OP3/OP12 Output Select

These bits program the OP3/OP11 output to provide one of the following:

00-The complement of OPR[3]/[11].

01-The counter/timer output, in which case OP3 / OP11 is an open drain output. In the timer mode the output is a square wave at the programmed frequency. In counter mode the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.

10-The 1x clock which shifts the output data for the channel B/D transmitter. A free running 1x clock is output if data is not being transmitted.

11-The 1x clock which samples the input data for the channel B/D receiver. A free running 1x clock is output if data is not being received.

OPCR [1:0] - OP2/OP10 Output Select

These bits program the OP2/OP10 output to provide one of the following:

00-The complement of OPR[2]/[10].

01-The 16x clock selected for the channel A transmitter by CSRA/C[3:0]. This will be a 1x clock if external 1x clock is programmed.

10-The 1x clock which shifts the output data for the channel A/C transmitter. A free running 1x clock is output if data is not being transmitted.

11-The 1x clock which samples the input data for the channel A/C receiver. A free running clock is output if data is not being received.

AUXILIARY CONTROL REGISTER (1,2)

ACR[7] - Bit Rate Set Select

This bit selects one of two bit rates to be generated by the BRG. The bit rates provided are selected by the channel A through D receiver and transmitter as described in the Clock Select Register description. Bit rate generator characteristics are shown in Table 5.

ACR [6:4] - Counter/Timer Mode and Clock Source Select

This field selects the operating mode and clock source for the counter/timer. See Table 6.

ACR [3:0] - Change of State Interrupt Enables

These bits select which bits of the input port cause the input port change bit in the interrupt status register (ISR[7]) to be set. If one of these bits is 'on', the setting of the corresponding bit in the IPCR by a change of state on the input will set ISR[7], and will also cause the interrupt request pin to be asserted if IMR[7] is set. However, if the bit is 'off', the setting of the corresponding bit in the IPCR has no effect on ISR[7].

INPUT PORT CHANGE REGISTER (1,2)

IPCR [7:4] - IP0 - IP3, IP8 - IP11 Change of State

These bits are set when a change of state occurs at the respective input pins (see Input Port Section). The bits are cleared when the CPU reads the IPCR1,2.

The setting of these bits can be programmed to cause an interrupt to the CPU via ACR[3:0], ISR[7] and IMR[7].

IPCR [3:0] - IP3 - IP0, IP11 - IP8 Current State

These bits indicate the current state of the respective inputs at the time the IPCR is read.

INTERRUPT STATUS REGISTER

This register provides the current status of all possible interrupt conditions. If a bit in the ISR is a '1' and the corresponding bit in the interrupt mask register (IMR) is also a '1' the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0' the state of the bit in the ISR has no effect on the interrupt request output. The contents of this register can be read by the CPU either unmasked or masked by the IMR. See Table 1.

ISR[7] - Input Port Change Status

This bit is a '1' when a change of state has occurred at the IPO - IP3 or IP8 - IP11 inputs and that event has been programmed to cause an interrupt via ACR[3:0]. It is cleared when the CPU reads the IPCR.

ISR[6] - Channel B/D Receiver Ready or FIFO Full

This bit indicates that the channel B or D receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel B/D 'reset break change interrupt' command.

ISR[5] - Channel B/D Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B/D[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[4] - Channel B/D Transmitter Ready

This bit is a duplicate of TXRDYB/D, SRB/D[2]

ISR[3] - Counter Ready

In the counter mode, this bit is set when the counter reaches the terminal count and is reset when the counter is stopped by a 'stop counter' command. The command, however, does not stop the C/T.

ISR[2] - Channel A/C Change in Break

This bit indicates that the channel A/C receiver has detected the beginning or end of a received break. It is reset when the CPU invokes a channel A/C 'reset break change interrupt' command.

ISR[1] - Channel A/C Receiver Ready or FIFO Full

The function of this bit is programmed by MR1A/C[6]. If programmed as receiver ready, it indicates that data is in the FIFO. It is set when a character is transferred from the receive shift register to the FIFO and cleared when the CPU reads the RHR. If there are still more characters in the FIFO after the read operation, the bit will be set again after the FIFO is 'popped.'

If this bit is programmed as FIFO full, it is set when a character is transferred from the receive shift register to the FIFO and the transfer causes the FIFO to become full. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, this bit will be set again after the read operation, when that character is loaded into the FIFO.

ISR[0] - Channel A/C Transmitter Ready

This bit is a duplicate of TXRDYA/C, SRA/C(2).

INTERRUPT MASK REGISTER (1,2)

This register selects which bits in the ISR cause an interrupt to be asserted. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the interrupt request output will be asserted. If the corresponding bit in the IMR is a '0', the state of the bit in the ISR has no effect on the interrupt request output. Note that the IMR does not mask the programmable interrupt outputs, OP3-OP7 and OP11-OP15.

COUNTER/TIMER REGISTERS (CTUR/CTLR)

The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used in the counter/timer in both of its modes of operation. The minimum value which may be loaded into CTUR/CTLR is 0001H.

INTERRUPT VECTOR REGISTER (1,2)

The IVR holds the value which the QUART places on the data bus in response to assertion of the interrupt acknowledge input. In the 88 mode the register is not used for any function when the device operates in I-mode but remains writable and readable by the CPU, and can be used for any purpose. The contents of this register are initialized to OFH by a hardware reset.

The following is a list of features which have been modified or enhanced over the DUART.

1). IEI, IEO and IACK are separate pins, no longer shared with IP4, IP5 and IP6.

2). Address A4/A5 has been added to provide additional internal registers.

3). Two additional inputs have been provided IP7 and IP15.

4). Reset input is debounced for Min of 20 n sec (Min).

5). The QUART is designed to operate with 7.3728 MHz crystal or an external TTL level clock.

6). Buffered system clock is provided to drive additional external logics (bonding option).

7). Since the interrupt is prioritized, channel A has highest priority and channel D has lowest priority. This determines the order of interrupt vector response on interrupt acknowledge cycles.

8). The QUART has a three byte FIFO stack behind the Transmit Hold Register in each channel. After a system reset or when coming out of standby mode, only the THR1 is accessible. This maintains DUART compatibility. The transmitter FIFO can be activated via commands in the Command Register A. Following steps are required to set additional FIFO's for each transmitter. Each channel in the QUART contains a shadow mode register, writing "E0" in the command register A will enable the shadow mode registers (A-D). Writing "04" in each channel will enable the additional FIFO registers, by writing "F0" in the command register A will exit the shadow mode.

NOTES:

1. Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger that the rated maxima.
3. Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25 ° C, V_{CC} = 5V and typical processing parameters.
4. All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 3.
5. Measured operation with a OR7 .3 MHz crystal and with all outputs open.
6. AC test condition for outputs: $C_L = 50_pF$, R_L = 2.7K ohm to V_{CC}.
7. For the 88 mode, timing is illustrated and referenced to the RDN and WRN inputs. The device may also be operated using CEN as the 'strobing' input. In this case, all specifications apply referenced to the falling and rising edges of CEN.
8. If CEN is used as the strobing input, this parameter defines the minimum high time between CENs.
9. Consecutive write operations to the same register require at least three edges of the X1 clock between writes.
10. This parameter is system dependent. For any QUART in the daisy chain, t_{IAS} must be greater than the sum of t_{EOD} for the highest priority device in the daisy chain, t_{EIS} for the QUART, and $_{DIO}$ for each device separating them in the daisy chain.
11. This specification imposes a 6 MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle. A higher 68000 clock can be used if this is not the case.
12. This specification imposes a lower bound on CSN and IACKN low, guaranteeing that they will be low for at least one CLK period.
13. The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's R_X is operation in external !x clock mode.
14. For prime grade N, P, J, L, M, ML $V_{CC,}$ = 5V ± 10%.

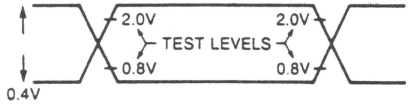


Figure 3. Input and Output levels for Timing Measurements

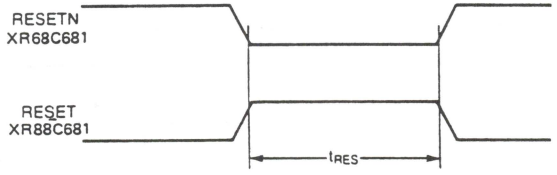


Figure 4. Reset Timing

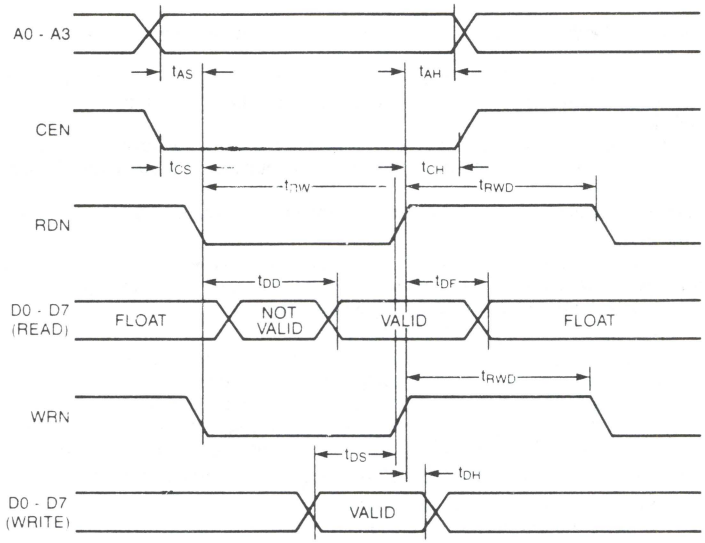
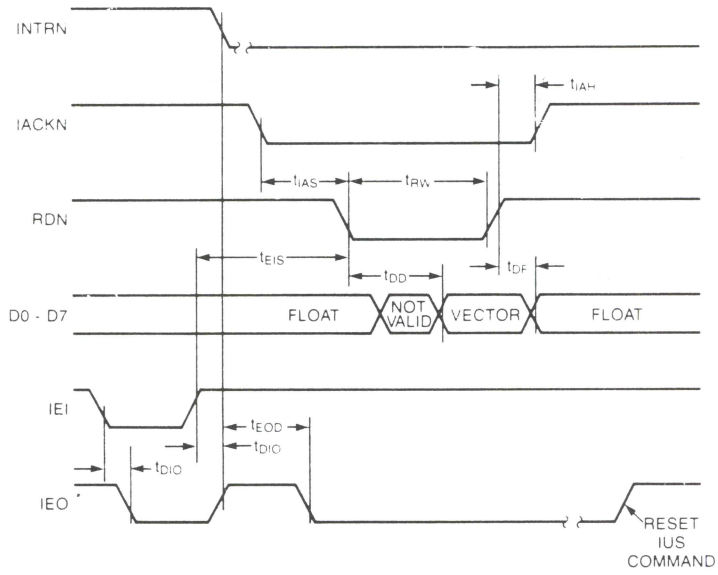


Figure 5. XR 82C684 Read and Write Cycle Timing (88 Mode)



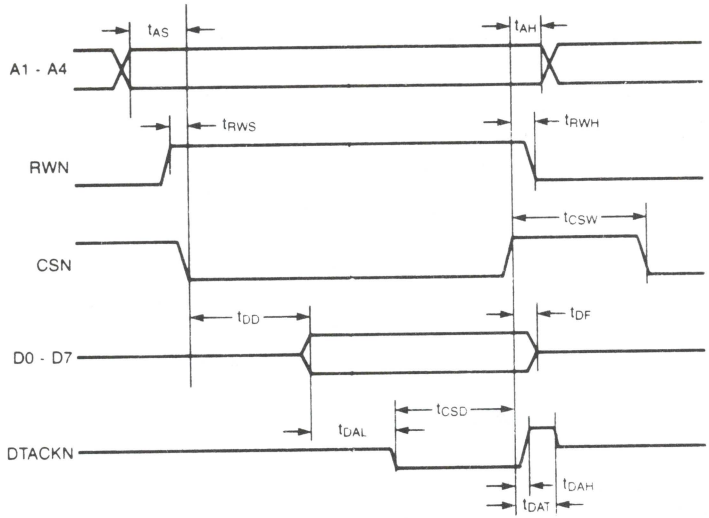
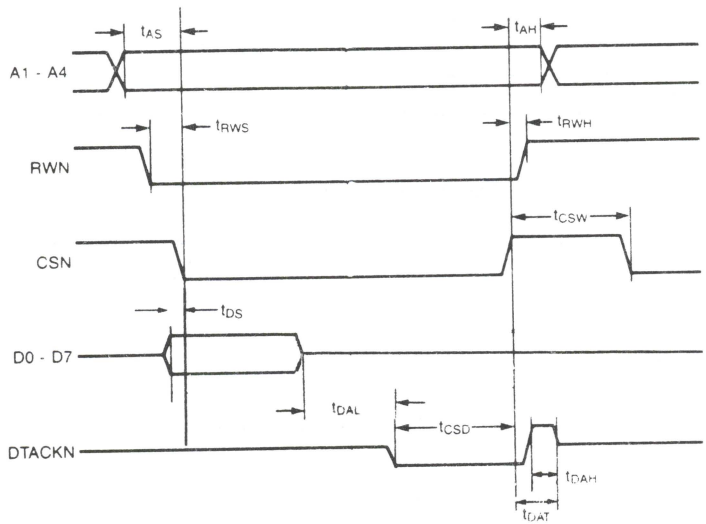


Figure 7. XR 82C684 Read Cycle Timing (68 Mode)



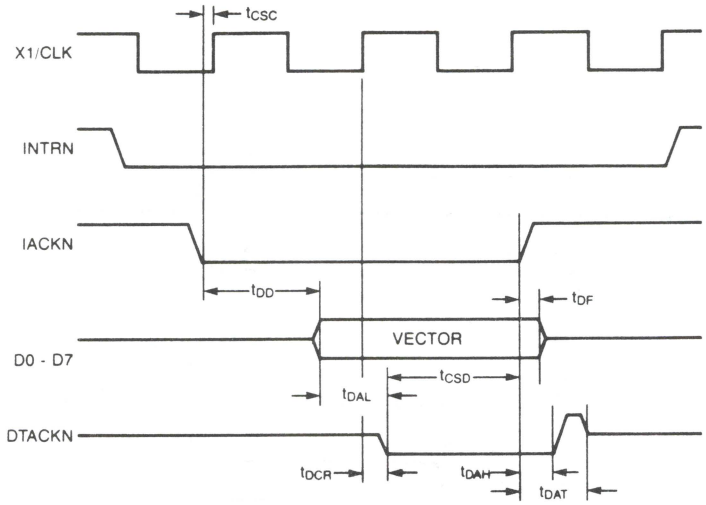


Figure 9. XR 82C684 Interrupt Cycle Timing (68 Mode)

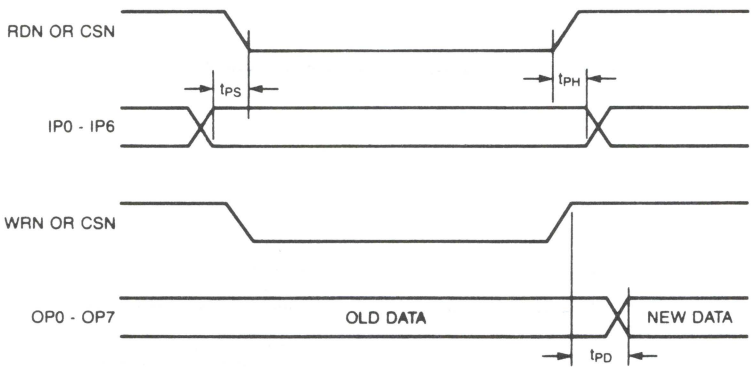
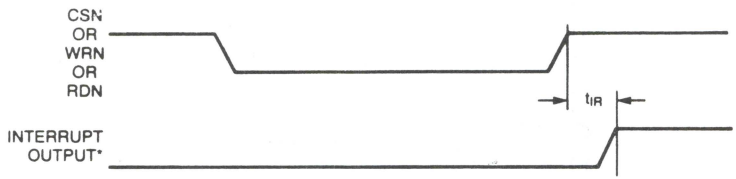


Figure 10. Port Timing



*INTRN or OP3 - OP7 when used as interrupt outputs.

Figure 11. Interrupt Timing

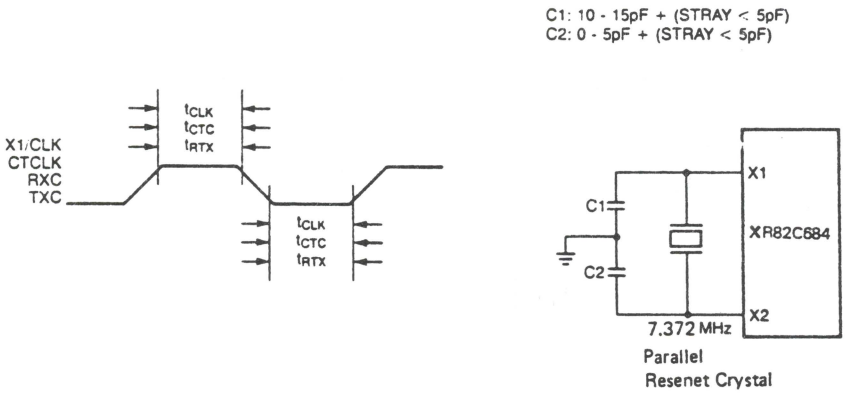


Figure 12. Clock Timing

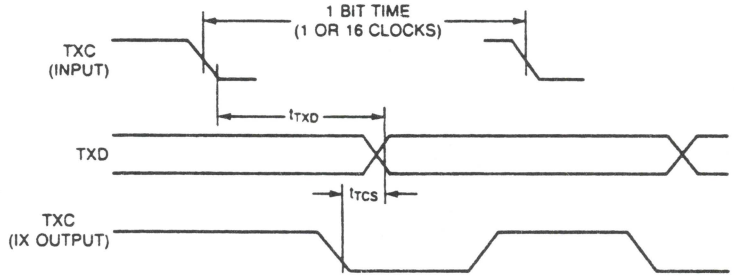


Figure 13. Transmitter Timing

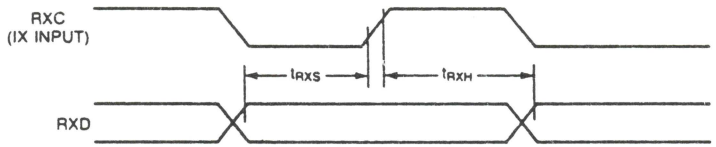


Figure 14. Receiver Timing

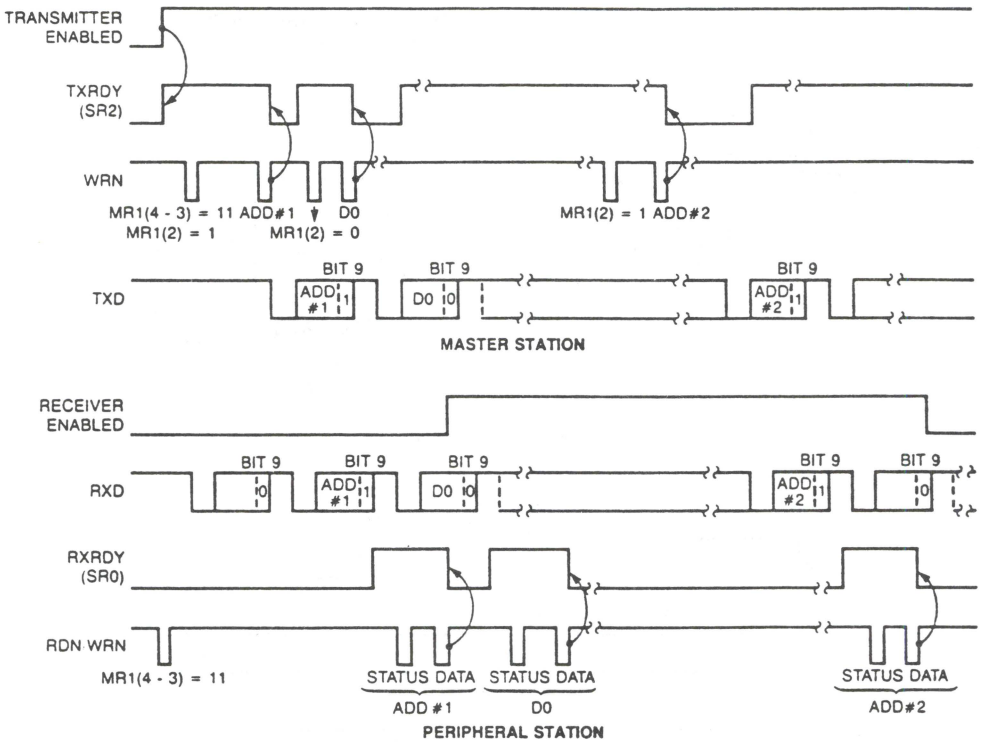
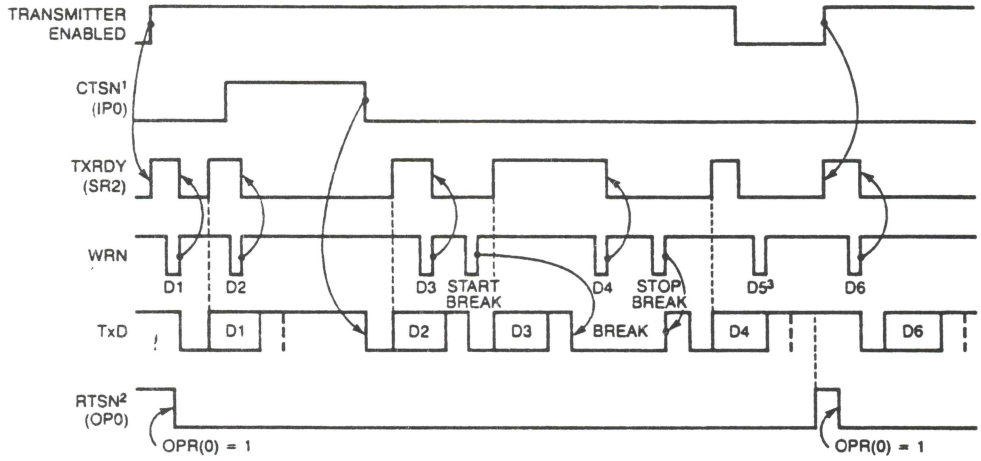
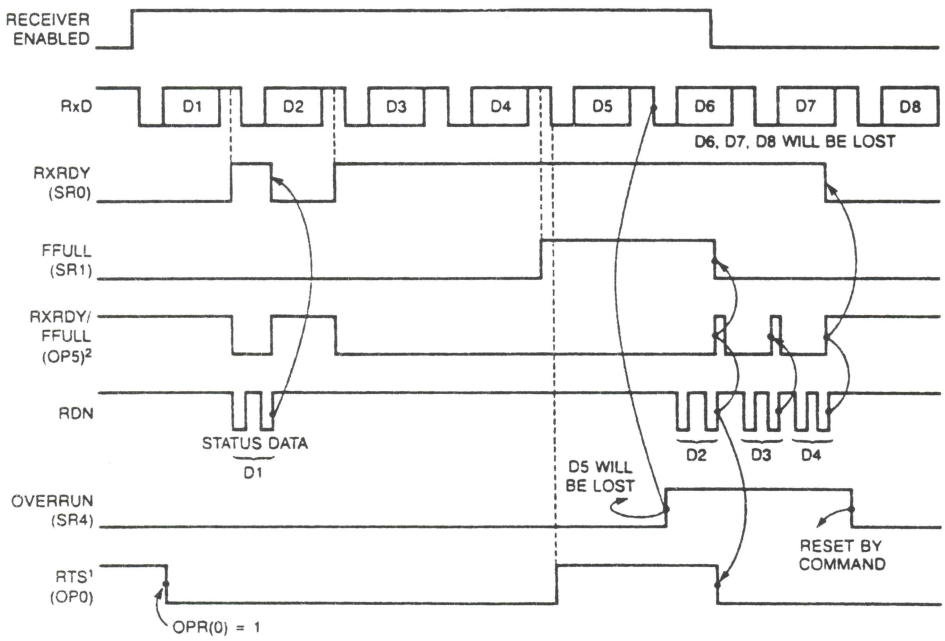


Figure 17. Transmitter and Receiver Operation in Multidrop Mode.



NOTES
1. Operation shown for MR2(4) = 1
2. Operation shown for MR2(5) = 1
3. D5 will not be transmitted

Figure 15. Transmitter Operation



NOTES
1. Operation shown for MR1(7) = 1
2. Shown for OPCR(4) = 1 and MR1(6) = 0

Figure 16. Receiver Operation



NOTES



CMOS DUART

INTRODUCTION

Asynchronous serial data communications is one of the most established, least costly, and easiest to implement means of transferring data from one electronic system to another. It is also the most widely used protocol of data communications today, due primarily to the expanding popularity of low cost microcomputer based products requiring data communications interfacing.

GENERAL DESCRIPTION

The XR-68C681 and XR-88C681 are intended for use in multichannel serial communication applications. They are fabricated using low power silicon gate CMOS process. They are also pin-for-pin and functionally compatible with the NMOS version of Signetics 2681, 68681 and Motorola 68681.

In addition to the two full duplex asynchronous serial channels which they provide, the XR-68C681 and XR-88C681 contain several other versatile system supports such as Timer/counter and I/O functions within the same package.

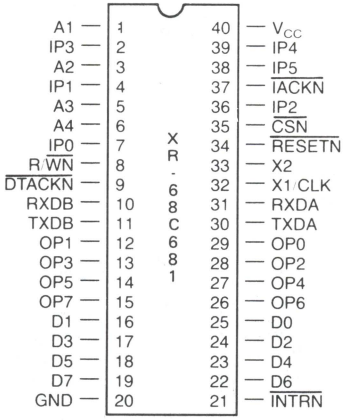
DUART COMPARISON CHART

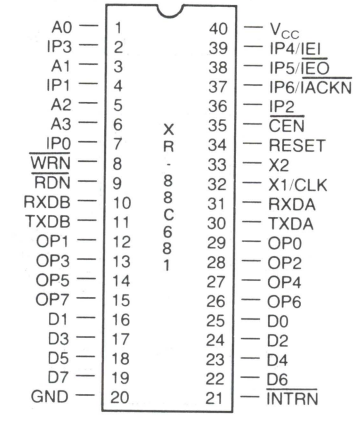
FEATURES	NMOS	CMOS
Predefined internal baud rates	23	28
Bus vector interrupts	No	Yes
Daisy chain interrupt Priority signals	No	Yes
Masked interrupt status register	No	Yes
Multi-drop mode	No	Yes
Standby mode	No	Yes

Two basic versions of the DUART are available, the XR-68C681 and the XR-88C681. Each version is optimized for interfacing with various microprocessors as follows:

EXAR DUART	MICROPROCESSORS
XR-68C681	65xx, 65C0x 65C1x 63xx, 68xx 68000, 68010 68200
XR-88C681	Z80, Z800 Z8000 8048 8080, 8085 8086, 8088 80286, 80286

Both versions of the EXAR DUARTs are provided in a 40 pin DIP and 44 pin PLCC package. The additional option in 24 and 28 pin DIP packages are available for the XR-88C681.

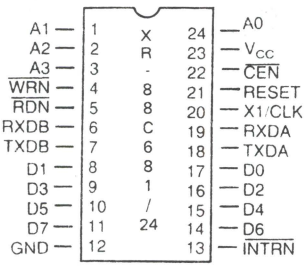


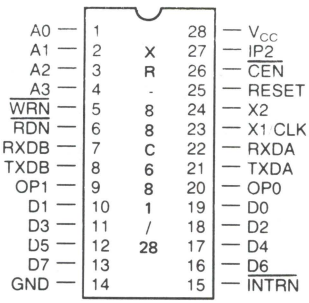


The pin configurations are as follows:

24 Pin	28 Pin	40 Pin
VDD	VDD	VDD
GND	GND	GND
A0-A3	A0-A3	A0-A3
WR	WR	WR
RD	RD	RD
CE	CE	CE
RX A,B	RX A,B	RX A,B
TX A,B	TX A,B	TX A,B
RST	RST	RST
D0-D7	D0-D7	D0-D7
INT	INT	INT
CLK1	CLK1	CLK1
	CLK0	CLK0
	OP0-OP1	OP0-OP1
		OP0-OP7
		IP0-IP1
	IP2	IP2
		IP3-IP6

Other options include extended temperature range and military products.





FUNCTIONAL ENHANCEMENTS OVER THE NMOS DUART

In addition to compatibility and low power, the XR-68C-681 and XR-88C681 features several functional enhancements.

More Bit Rate Selection

The EXAR DUARTs provide additional interal fixed baud rates which are not offered in the Signetics and Motorola versions; these rates are 3.600 KHz, 14.4 KHz, 28.8 KHz, 57.6 KHz, 115.2 KHz. Customized transmission rates can be configured by supplying an external clock to IP2 pin up to 2 MHz.

Bus Vectored Interrupts

The standard procedure of responding to an interrupt is the status polling of all possible interrupting devices. Depending on the application and the number of devices involved, this could consume a substantial amount of time and software code. To alleviate this overhead, some CPUs are capable of receiving an "interrupt vector" on the data bus. This vector causes the program to jump directly to the interrupt routine for the peripheral device which supplied the vector.

The XR-88C681 does not have a separate, dedicated interrupt acknowledge input as does the XR-68C681. Instead, a special mode called "Z mode" can be programmed to designate three of the general pupose inputs to be interrupt control signals. One of these control signals is IACK, the interrupt acknowledge. While in "Z mode", the CPU can respond to a DUART interrupt with an interrupt acknowledge. The DUART will then place the interrupt vector on the data bus when both IACK and RD are asserted.

Daisy Chained Interrupt Priority Signals

When more than one device capable of generating interrupts is used in a system, it is often necessary to implement additional logic that provides prioritization of simultaneous interrupts.

The XR-88C681 DUART has a built in Daisy chained prioritization scheme that is common to many other existing peripheral devices. The Daisy chained prioritization scheme implemented in "Z mode" via the interrupt enable in (IEI) and interrupt enable out (IEO) pins, assures that only the interrupting device with the highest priority responds with the interrupt vector. It also prevents lower priority devices from generating interrupts until the service for the higher priority device has been completed.

Masked Interrupt Status Register

The XR-68C681 and XR-88C681 provide an interrupt mask register (IMR) that can be programmed to mask out any of the eight interrupt conditions from generating interrupts to the CPU via the INTR output. When an interrupt is generated, it is necessary to read the interrupt status register (ISR) to find out which condition caused the interrupt. The ISR register shows all the interrupting conditions regardless of whether they had been masked out or not. The XR-68C681 and XR-88C681 DUARTs provide additional interrupt status registers (MISR) which show only the masked interrupt conditions.

Reading Reserved Addresses Locations

If the user tried to read address 2 Hex and A Hex in the NMOS version of the DUART, it will enter a test mode which will alter the function of its internal timing circuit. Once this is done, the NMOS DUART will not function properly until a hardware reset has been issued. Since the EXAR DUARTs do not use this method to invoke its special test modes, they allow any address to be read without adversely affecting operation.

Mutli-drop Mode -- 8051 Series Compatible

A special multi-drop mode feature in the XR-88C681, compatible with the nine bit mode of the 8051 series microcomputer, allows the implementation of a simplified local area network configuration of up to 256 stations. Current XR-68C681 users can achieve this feature by switching to the XR-88C681 and implementing minor external logic changes as shown below in Figure 1.

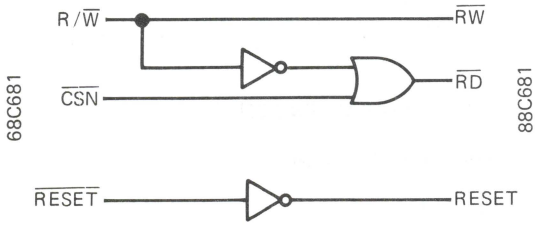


Figure 1.

Standby Mode

The XR-68C681 and XR-88C681 DUART can be programmed to be in standby mode when it is not needed for communications and timer/counter function mode. While it is in standby mode, the input ports and output ports can still be used for general system control. Standby mode is exited by issuing a "set active mode" command which returns the DUART to normal operation within 25 μs.

With the external clock source, the DUART can enter into standby mode by stopping the external clock to the DUART, this approach will not change or affect any of the DUARTs internal registers or programmed functions. This application is useful for portable computers or battery operated communication equipment.

Clock Drive Capability

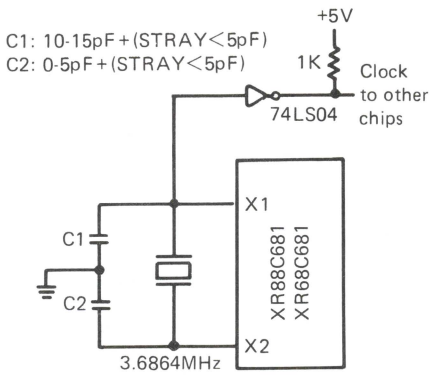
The XR-68C681 and XR-88C681 crystal output can drive an additional DUART crystal input to Daisy chain the clock circuit, and to reduce the additional crystal cost. If additional clock drive is required, it is recommended to use CMOS 4069 or 4049/4050, LS 7404 to buffer the crystal output of the DUART.

The number of DUARTs that can be driven from one crystal for NMOS parts is eight, and for CMOS parts, three.

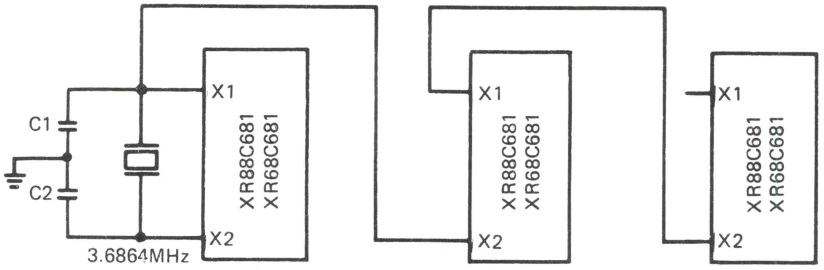
Crystal Information

The XR-68C681 and XR-88C681 DUART uses a standard 3.6864 MHz crystal available from several crystal manufacturers, including Q-Matic, McCoy, M-Tron, Crystek and US Crystal. If other bit rates are necessary, the DUART can derive bit rates from its internal programmable timer or by using external 16x and 1x clock sources through the input port.

KSS Crystal	KR-037	C1,C2 = 19 pF
Crystek	CY3JM	C1 = 18 pF
NYmph	NYP037-20	C1,C2 = 20 pF
MYmph	NYP037	Series



Crystal series resistance should be less than 180 ohms.



DESIGN HINTS FOR NEW USERS

Since XR-68C681 and XR-88C681 are asynchronous devices, read and write cycles are not DUART clock dependent, so only internal gate delays are counted.

If the user does not utilize the DTACK and IACK signals (like 65xx, 68xx CPU's users), the IACK input should be tied to VDD and ignore the DTACK signal output.

The EXAR DUART offers two types of output configurations for genral purpose output pins, push pull or open drain. The table below shows the different types of output configuration.

OPEN DRAIN OUTPUT	PUSH PULL OUTPUT
OP0	General Purpose Channel A RTS Out
OP1	General Purpose Channel B RTS Out
OP2	General Purpose TxA 1x Clock Out TxA 16x Clock Out RxA 1x Clock Out
OP3 Timer/Counter	General Purpose TxB 1x Clock Out RxB 1x Clock Out
OP4 RxRdy A /Ffull A	General Purpose
OP5 RxRdy B /Ffull B	General Purpose
OP6 TxRdy A	General Purpose
OP7 TxRdy B	General Purpose

All outputs will be inverted from Set Output Port Bits Command register or Output Port Configuration register.

INITIALIZATION AND POWER-UP HINTS:

It is possible after power-up to get a character in the transmit and/or Receive Hold Register. This happens after release of the master reset and before it receives a character from the CPU. The way to clear this situation is during the initialization routine. It is recommended to enable the loopback mode after a master reset, load the baud rate generator, wait one character time and then clear the receive buffer by reading it. This will clear any uncertain states of the transmit or receive holding registers. Following this, disable the loopback mode. Programming of the baud rate generator during initialization is also important to assure the correct operation of the RTS/CTS output port pins.

STATUS OF DUART AFTER RESET

All outputs will be set to high state, interrupt registers will be masked, the following registers will be set to "00 Hex", Status register A (SRA), Status register B (SRB), Masked Interrupt Status register (MISR), Stop Counter/Timer Command (SCC), Command register A (CRA), Command register B (CRB), Interrupt Mask register (IMR), Output Port Configuration (OPCR), Reset Output Port Bits (ROPBC), and Interrupt Vector register (IVR) to "0F Hex."

SIMPLE PROGRAMMING STEPS

Programming Timer Mode

LDAA	70	Hex	
STAA	04	Hex	Set Timer Mode
LDAA	04	Hex	
STAA	0D	Hex	Set Timer Output
LDAA	0E	Hex	
STAA	06	Hex	Load Upper Count Value
LDAA	64	Hex	
STAA	07	Hex	Load Lower Count Value
LDAA	00	Hex	
STAA	05	Hex*	Disable All Interrupts
LDAA	0E	Hex	Start The Timer

OP3 will generate 1 KHz square wave output.

Programming Counter Mode

```
LDAA  30  Hex
STAA  04  Hex        Set Counter Mode
LDAA  04  Hex
STAA  0D  Hex        Set Counter Output
LDAA  08  Hex
STAA  05  Hex        Set Counter Interrupt
LDAA  12  Hex
STAA  06  Hex        Load Upper Count Value
LDAA  38  Hex
STAA  07  Hex        Load Lower Count Value
LDAA  0E  Hex        Start The Counter
CLI                  Clear the CPU Interrupt
WAI                  Wait For Interrupt
LDAA  0F  Hex        Stop The Counter
```

Programming Output Port Bits

```
LDAA  00  Hex
STAA  0D  Hex        Make All Output Ports
LDAA  00  Hex
STAA  05  Hex        Disable The Interrupt
LDAA  55  Hex                    LHLHLHLH
STAA  0E  Hex        Set Output To HLHLHLHL
```

Reset The Output Bits

```
LDAA  55  Hex
STAA  0F  Hex        Reset  All  Outputs  to  H
```

Reset All Outputs to H

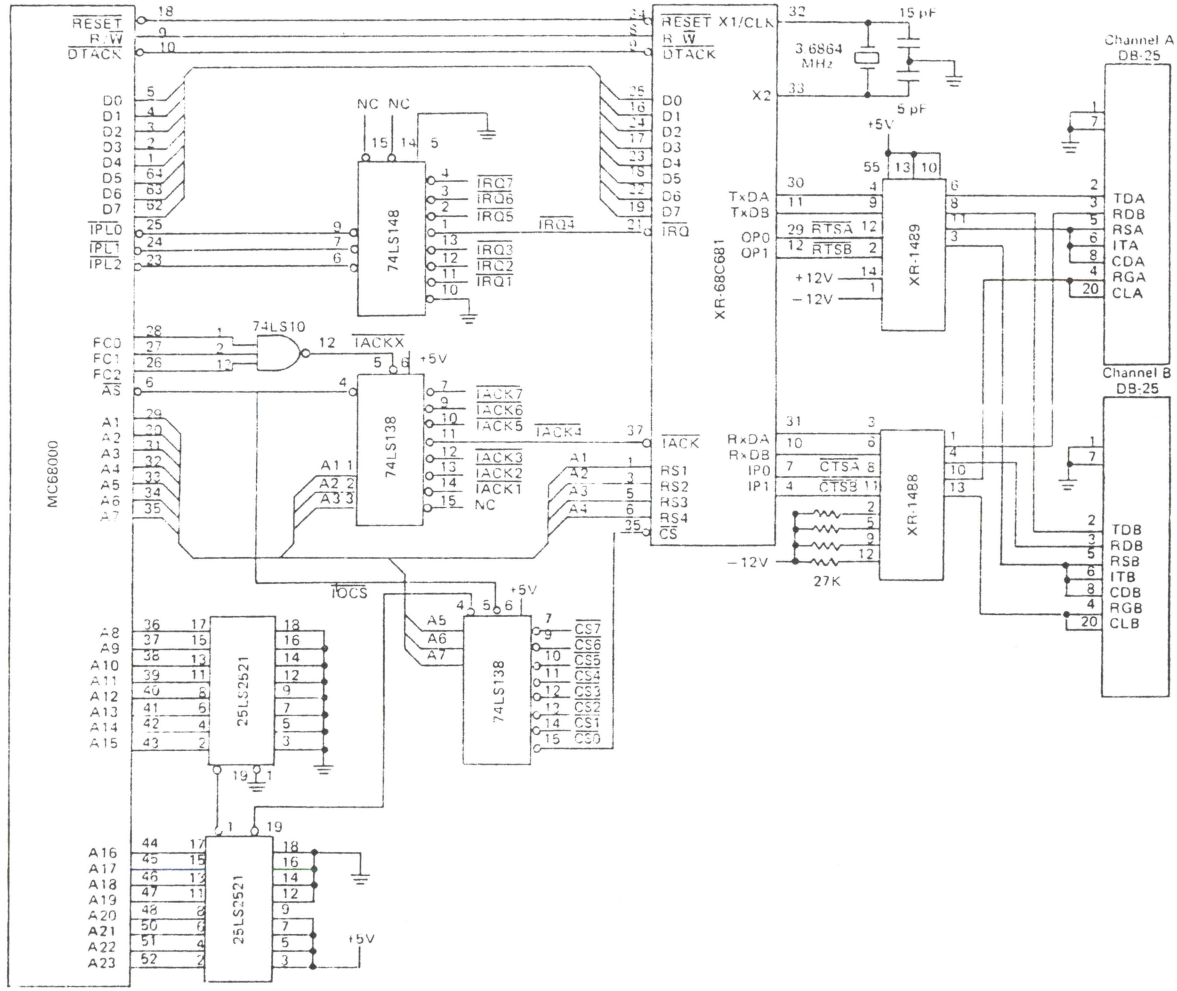
Programming For Transmit Mode A

```
LDAA  92  Hex
STAA  00  Hex        7 Bits/Char, No Parity
LDAA  07  Hex
STAA  00  Hex        1 Stop Bit
LDAA  06  Hex
STAA  01  Hex        Set 1200 Baud Rate
LDAA  42  Hex
STAA  0D  Hex        Set TX Clock Out, TXRDY
LDAA  00  Hex
STAA  04  Hex        Select Standard Baud Rate
LDAA  00  Hex
STAA  05  Hex        Disable The Interrupt
LDAA  04  Hex
STAA  02  Hex        Enable The Transmitter
LDAA  01  Hex  Loop
CMPA  04  Hex        See It TXRDY Is High
BNE   Loop
LDAA  55  Hex
STAA  03  Hex        Load The Data Into THRA
JMP   Loop           Continue
```

Programming for Receive Mode A

The RX Hold Register consists of a First In First Out (FIFO) stack with a capacity of three characters. Data is transferred from the receive shift register into the top most empty position in the FIFO. RxRdy is set whenever one or more characters are in the FIFO, and the FFULL status bit is set if the FIFO is filled with data. A read of the Rx Holding Register outputs, the data at the top of the FIFO and any remaining characters are pushed up, thus freeing a FIFO position for new data. Therefore, the status register must be read prior to reading the Rx Holding Register. With reset FIFO pointers are initialized and old data is still in the FIFO.

```
LDAA  92  Hex
STAA  00  Hex        7 Bits/Char, No Parity
LDAA  03  Hex
STAA  00  Hex        1 Stop Bit
LDAA  60  Hex
STAA  01  Hex        Set To Receive 1200 Baud
LDAA  13  Hex
STAA  00  Hex        RXRDY and RX Clock Out
LDAA  00  Hex
STAA  04  Hex        Select Standard Baud Rate
LDAA  02  Hex
STAA  05  Hex        Enable RXRDY Interrupt
LDAA  01  Hex
STAA  02  Hex        Enable The Receiver
CLI             Loop Clear CPU Interrupt
WAI                  Wait For Interrupt
LDAA  03  Hex        Get The Received Data
JMP             Loop Continue
```



TYPICAL APPLICATION CIRCUIT USING 68000 CPU

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MASS STORAGE PRODUCTS

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XR-9050 Low Power Data Synchronizer / 1,7 RLL ENDEC with Write Precompensation 4-101

XR-9080 Frequency Synthesizer, Data Synchronizer /1,7 RLL ENDEC with Write Precompensation 4-111

Mass Storage Product Selection Guide

Part Number	Description	Technology	Product Features	Supply Voltages	Packages
XR-117 XR-117R	R/W Preamplifier for 3 Terminal Recording Heads,	High Speed Bipolar	2, 4 & 6 Channels Industry Standard 2,4,or 6 Channels	+5, +12	PLCC (J) 28 JEDEC SO (D) 18, 24, 28 DIP (P) 18, 22, 28
XR-501 XR-501R	R/W Preamplifier for 3 Terminal Recording Heads, 6 or 8 Channels	High Speed Bipolar	6 & 8 Channels High Performance	+5, +12	PLCC (J) 28,44 JEDEC SO (D) 28, 32 DIP (P) 28,40
XR-505 XR-505R	Low Power R/W Preamplifier for 3 Terminal Recording Heads, 2 or 4 Channels	High Speed Bipolar	Low Power Operation High Performance Single Supply 2 & 4 Channels	+5	JEDEC SO (D) 16, 20, 24 JEDEC SO (G) 16 DIP (P) 18, 22, 28
XR-507 XR-507R	Low Power R/W Preamplifier for 3 Terminal Recording Heads, 2 or 4 Channels	High Speed Bipolar	Extremely Low Power, Idle, Low Noise, Selectable Low/High Gain, Head Pinout on 1 side of IC	+5	Japanese SO (K) 24
XR-510A XR-510AR	R/W Preamplifier for 3 Terminal Recording Heads, 4, 6, or 8 Channels	High Speed Bipolar	2, 4 & 6 Channels Enhanced Performance Same Pinout as XR-117	+5, +12	PLCC (J) 28 JEDEC SO (D) 18, 24, 28 DIP (P) 18, 22, 28
XR-511 XR-511R	R/W Preamplifier for 3 Terminal Heads 6 or 8 Channels	High Speed Bipolar	2, 4 & 6 Channels Enhanced Performance Same Pinout as XR-501	+5, +12	PLCC (J) 28, 44 JEDEC SO (D) 24, 28, 32 DIP (P) 28, 40
XR-532A	Low Power, High Speed RLL (2, 7) Data Separator	BiCMOS	Low Power Operation (150mW), Improved Speed and Performance	+5	PLCC (J) 28 JEDEC SO (D) 28 PQFP(Q) 32
XR-541	Disk Drive Pulse Detector	High Speed Bipolar	RLL & MFM Compatible High Accuracy (1ns available)	+5, +12	PLCC (J) 28 JEDEC SO (D) 24 DIP (P) 24
XR-4610 XR-4610R	R/W Preamplifier for 2 Terminal Recording Heads	High Speed Bipolar	Low Power Thin Film Heads 2 and 4 Channels	+5	JEDEC SO (D) 16, 20
XR-9010 XR-9010R	Low Power R/W Preamplifier for 3 Terminal Recording Heads	High Speed Bipolar	Reduced Noise Reduced Capacitance from XR-505	+5	JEDEC SO (D) 16, 20
XR-9022	Low Pass Filter with Differentiation and Pulse Slimming	BiCMOS	3-9MHz fc, Serial Interface,Resistor Program, Low Power	+5	JEDEC SO (D) 18 Japanese SO (K) 18

Part Number	Description	Technology	Product Features	Supply Voltages	Packages
XR-9030	R/W Preamplifier for 2 Terminal Recording Heads	High Speed Bipoloar	Enhanced Version of XR-4610 plus Low Noise Low Capacitance	+5	JEDEC SO (D) 16, 20
XR-9040	Disk Drive Pulse Embedded Servo Position Sampler and R/W Preamp Interface	BiCMOS	Complete Pulse Detector Internal Offset Self-Zero Circuit Low Power Integral A to D with Timing Generator Logic	+5	PQFP (Q) 52
XR-9050	Data Synchronization / 1,7 RLL ENDEC with Write Precompensation	BiCMOS	Low Power (150mW) 1,7 RLL ENDEC Improved Speed	+5	PLCC (J) 28 JEDEC SO (D) 28
XR-9080	Data Synchronizer, (1,7) ENDEC, Frequency Synthesizer	BiCMOS	Programmable Loop Filter, Change Pump Current, VCO 24Mbit/sec	+5	PQFP (Q) 52

R/W Preamplifier for 3 Terminal Recording Heads, 2, 4, or 6 Channels

GENERAL DESCRIPTION

The XR-117 is a high speed head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-117 is compatible with 3 1/2" to 14" single and multiple platter drives, and features high bandwidth, large dynamic range, and low noise. Several packaging options extend usefulness to applications requiring two, four, or six center-tapped read/write heads; multiple devices are easily cascaded for drives with more heads.

The XR-117R includes internal damping resistors, facilitating use in circuits requiring minimum external complexity and mass.

The XR-117, manufactured with a high speed bipolar process, operates on +5V and +12V.

FEATURES

Complete Head Interfacing Functions, Read and Write
High Bandwidth and Dynamic Range
Low Noise
Available in Two, Four, and Six Head Versions
Easily Cascaded for Larger Systems
Power Monitor
TTL Compatible Inputs

APPLICATIONS

Hard Disk Drives with MZG, ferrite, or composite heads

ABSOLUTE MAXIMUM RATINGS

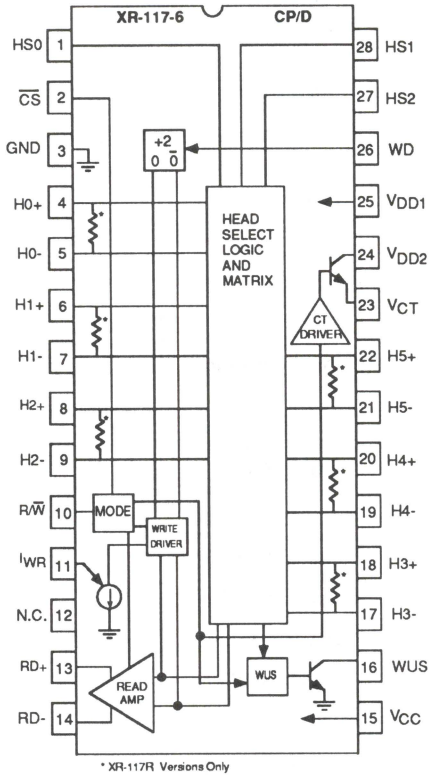
V_{DD1} and V_{DD2}	15 V
V_{CC}	6V
Digital Inputs	-0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to +15°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-117-2CP	18 Pin Plastic	0°C to 70°C
XR-117-4CP	22 Pin Plastic	0°C to 70°C
XR-117-6CP	28 Pin Plastic	0°C to 70°C
XR-117-xD	Surface Mount	0°C to 70°C
XR-117-6CJ	28 Pin PLCC	0°C to 70°C
XR-117R-xCP	Plastic	0°C to 70°C
XR-117R-xD*	Surface Mount	0°C to 70°C
XR-117R-6CJ	28 Pin PLCC	0°C to 70°C

x = 2, 4 or 6, depending on number of heads required
** = contact factory for availability*

PIN ASSIGNMENT



* XR-117R Versions Only

SYSTEM DESCRIPTION

Four major blocks comprise the XR-117: a multiplexer for head selection, write data control circuitry, read signal amplifiers and buffers. Designed for six read/write heads, the XR-117 is also available in smaller packages for systems requiring only two or four heads. The 30 MHz minimum bandwidth facilitates data rates exceeding 25 Mbits per second.

Less than 1.3 nV/√Hz (typical) noise allows error free operation with small input signals. Up to 50 mA of write current output (user selectable) are available.

Cascading multiple XR-117s is accomplished by alternately enabling and disabling devices via the chip select ($\overline{CS}$) pin. Guaranteed write current tolerances allows close write matching between devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C VDD = 12 V, VCC = 5V, R_{IW} = 3.1 kΩ, L_h = 10µH, R_d = 750Ω, CL (R_{D+},R_{D-}), ≤20pF, 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{CC}	Supply Current			25	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			25	mA	V_{DD} = 13.2 V, Idle Mode
				50	mA	V_{DD} = 13.2 V, Read Mode
				30	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
P_D	Power Dissipation			400	mW	V_{CC} - 5.5 V, V_{DD} = 13.2 V, Idle Mode
				600	mW	Read Mode
				700	mW	Write Mode, I_W = 50 mA, RCT = 130Ω
				1050	mW	Write Mode, I_W = 50 mA, RCT = 0Ω
V_{CT}	Center Tap Voltage		4.0		V	Read Mode
			6.0		V	Write Mode
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	IOL = 8mA
I_{OH}	Leakage Current			100	µA	V_{OH} = 5 V
DIGITAL INPUTS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input Current, Low	-0.4			mA	
I_{IH}	Input Current, High			100	µA	
WRITE CHARACTERISTICS						
	Write Current Accuracy	-5		+5	%	Note 1
I_W	Recommended Write Current Range	10	45	50	mA	
	Differential Head Voltage Swing	5.7			Vpeak	
	Unselected Differential Head Current			2	mApeak	
C_O	Differential Output Capacitance			15	pF	
R_O	Differential Output Resistance	10			KΩ	XR-117
		635	750	865	Ω	XR-117R
	WD Rate (Transition Frequency)	125	500	625	kHz	WUS = Unsafe
K_1	Current Source Factor		20			$K_1 = I_W$/(Current Through R_W)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
READ CHARACTERISTICS						
A_V	Differential Voltage Gain	80	100	120	V/V	V_{in} = 1 mVp-p @ 300 kHz R_L+ = R_L- = 1KΩ
	Dynamic Range	-2		2	mV	DC input voltage where gain drops 10%. $V_{in} = V_i$ + 0.5 mVp-p @ 300 kHz.
R_{in}	Differential Input Resistance	2	8		KΩ	XR-117
		500	675	850	Ω	XR-117R
C_{in}	Differential Input Capacitance			23	pF	f = 5 MHz
e_{ni}	Input Noise Voltage		1.3	2.1	nV/√Hz	L_h = 0, R_h = 0, BW = 15 MHz
BW	Bandwidth	30	60		MHz	-3dB point |Zs|< 5Ω, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}
	Channel Separation	45	60		dB	Unselected Channel: Vin = 100 mVp-p at 5 MHz. Selected Channel V_{in} = 0 V
	Output Offset Voltage	-480	±50	480	mV	
V_{CM}	Common Mode Output Voltage	5	6	7	V	
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	µs	Note 2 Write to Read
	Write to Read		0.1	1	µs	Note 3, Note 4
CS	Start-Up Delay		0.1	1	µs	Delay to 90% of IW or to 90% of 100 mV 10 MHz read signal envelope.
	Inhibit Delay		0.1	1	µs	Note 4
	Head Switching Delay		0.1	1	µs	Note 3, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6	2.5	8.0	µs	IW = 50 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	IW = 20 mA, See Figure 2, TD2
IW	Head Current					
	Propagation Delay		4	25	ns	L_h = 0µH, R_h = 0Ω, Note 5
	Asymmetry			2	ns	Note 6. See Figure 1, TD3
	Rise or Fall Time		9	20	ns	10% to 90% or 90% to 10% points

Note 1: Error from $I_W = \frac{140}{R_W} \frac{V}{(\Omega)}$

Note 2: Delay to 90% of I_W

Note 3: Delay to 90% of 100 mVp-p 10 MHz read single envelope

Note 4: Delay to 90% decay of I_W

Note 5: From 50% points

Note 6: Input WD has 50% duty cycle and 1 nS rise and fall times.

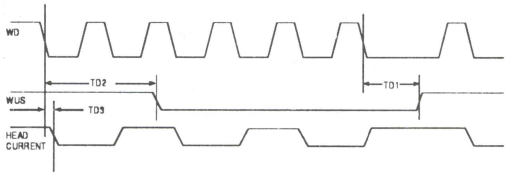


Figure 1. Write Mode Timing Diagram

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode.

Read Mode

Pulling R/$\overline{W}$ high enables the data readback mode. The head signal is amplified by a low noise differentiated stage and output by low impedance drivers.

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-117 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-117R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-117R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-117 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{140{,}000}{I_W}$$

where I_W Is in mA and R_{IW} is in ohms.

The V_{CC} supply monitor disables writing when. V_{CC} drops below about 4V.

Device power dissipation is reduced by a resistor, R_{CT} connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage drop then is across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$RCT = 130\left(\frac{55}{I_W}\right)$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small outline packages. For low write currents, R_{CT} may be deleted, with V_{DD2} directly connected to the supply.

Write center tap circuitry is designed for higher stability than similar devices from other manufacturers. If extreme conditions exist, a ferrite bead around the V_{CT} line to the heads will reduce or eliminate overshoot and ringing.

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low, are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of about 2 KΩ to 10 KΩ is necessary for operation of this open collector output.

Read Mode Design Considerations

The read amp is fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.3nV/ √Hz typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 6 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 µA.

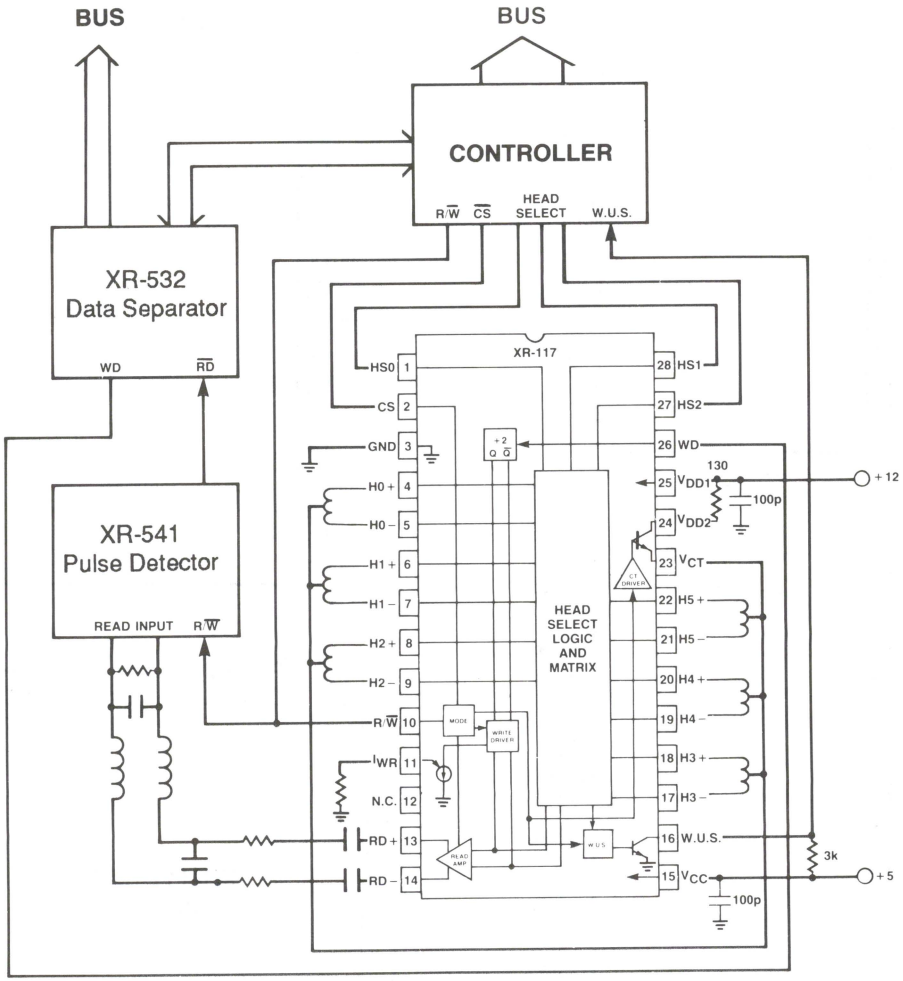


Figure 2. Hard Disk Read/Write Applications Circuit
Note: Circuit shown for XR-117R. Non-R versions require damping resistors across each head.

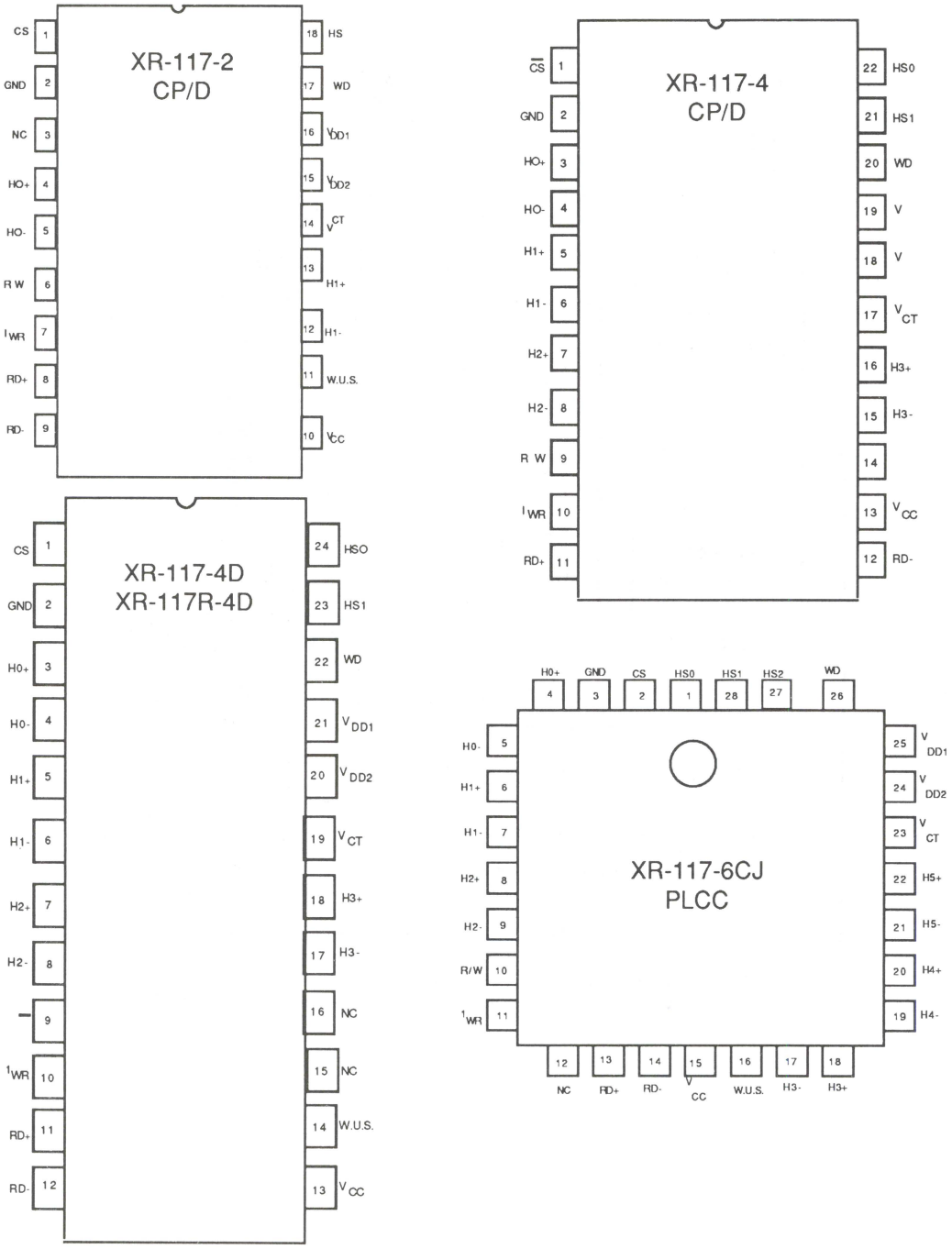


Figure 3. Additional Packages for XR-117(Six head DIP shown in Functional Block Diagram, page 1)

R/W Preamplifier for 3 Terminal Recording Heads, 6 or 8 Channels

GENERAL DESCRIPTION

The XR-501 is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions The XR-501 is compatible with 3 1/2" to 14" multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring six or eight center-tapped read/write heads Multiple devices are easily cascaded for drives with more heads.

The XR-501 features a pinout with all head ports on one side of the circuit. This eases flex cable or PC board layout by eliminating crossovers. The XR-501R option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-501, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Pinout Optimized for Easy Layout
Available in Six and Eight Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs

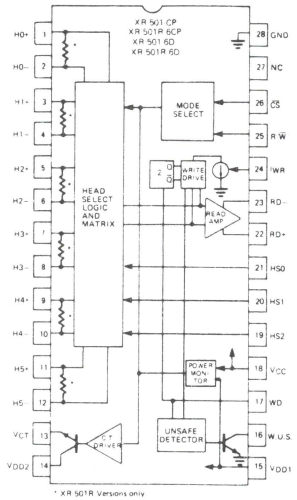
APPLICATIONS

Hard Disk Drives with MIG, ferrite or composite heads

ABSOLUTE MAXIMUM RATINGS

VDD	15V
VCC	6V
Digital Inputs	-0.3 V to VCC +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-501-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-501-6CJ	28 Pin PLCC	0°C to 70°C
XR-501-6D	28 Pin SO	0°C to 70°C
XR-501-8CP	40 Pin Plastic DIP	0°C to 70°C
XR-501-8CJ	44 Pin PLCC	0°C to 70°C
XR-501-8D	32 Pin SO	0°C to 70°C
XR-501R-6CP*	28 Pin Plastic DIP	0°C to 70°C
XR-501R-6CJ	28 Pin PLCC	0°C to 70°C
XR-501R-6D	28 Pin SO	0°C to 70°C
XR-501R-8CP*	40 Pin Plastic DIP	0°C to 70°C
XR-501R-8CJ	44 Pin PLCC	0°C to 70°C
XR-501R-8D	32 Pin SO	0°C to 70°C

**Contact Factory for availability*

SYSTEM DESCRIPTION

The XR-501 consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of eight heads, and associated control and monitoring functions. Less than 1.0 nV/ √Hz (typical) noise allows error free operation with small input signals. Over 50 mA of write current output (user adjustable) are available.

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C V_{CC}=5V, V_{DD} =12 V, I_W = 40 mA, R_D =750Ω, C_L (R_{D+}, R_{D-}) ≤20 pF, Data Rate= 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current			25	mA	V_{CC} = 5.5 V, Read or Idle Mode
				26	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			20	mA	V_{DD} = 13.2 V, Idle Mode
				40	mA	V_{DD} = 13.2 V, Read Mode
				20	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
PD	Power Dissipation			400	mW	Idle Mode - V_{CC} = 5.5V, V_{DD} = 13.2V
				600	mW	Read Mode-V_{CC}=5.5V, V_{DD}=13.2V
				750	mW	I_W = 50 mA,,R_{CT}=160Ω
				1050	mW	I_W=50 mA, R_{CT} = 0Ω
VCT	Center Tap Voltage		4.5		V	Read Mode
			6.5		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	µA	V_{OH}=5V
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0		V		All digital inputs
I_{IL}	Input Low Current	-0.4		mA		All digital inputs, V_{IL} = 0.8V
I_{IH}	Input High Current			100	µA	All digital inputs, V_{IH} = 2.0V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-7		7	%	Error from IW=$\frac{140}{RW}$
	Recommended Write Current Range	10		50	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak(Inductive Load)
	Unselected Differential Head Current			85	µA	
	Unselected Transient Current			2	mA	Peak
	Differential Output Capacitance			15	pF	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
WRITE CHARACTERISTICS (cont.)						
	Differential Output Resistance	10			KΩ	XR-501
		635	750	865	Ω	XR-501R
	WD Rate/Transistion Freq.	125	500		KHz	
K_I	Current Source Factor		20			$K_I = I_W/(\text{Current through } R_W)$
K	Write Current Constant	129	140	151	V	$I_W = K/R_W$
	Write Protection Leakage Current -200	-200		200	µA	Per Side, V_{CC}- ≤3.7 V V_{DD}- ≤8.7V
V	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	-50		50	µA	Write or Idle Mode, $R_D+ = R_D- = 6$ V
READ MODE						
A_V	Differential Voltage Gain	80		120	V/V	V_{IN} = 1 mVp-p at 300 kHz, $R_L+ = R_L- = 1$ kΩ
	Dynamic Range	-3		+3		DC input voltage where gain drops 10%. $V_{IN} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2	8		KΩ	XR-501
		530	650	790	Ω	XR-501R
C_{IN}	Differential Input Capacitance			23	pF	
e_{ni}	Input Noise Voltage		**1.0**	1.5	nV/√Hz	$L_h = 0$, $R_h = 0$, BW = 15 MHz
BW	Bandwidth	30	60		MHz	-3dB Point, $\lvert Z_s \rvert$- ≤5ΩV_{in} = 1 mVp-p
I_B	Input Bias Current		10	100	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}
	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0 V
	Output Offset Voltage	-480	±50	480	mV	
V_{CM}	Common Mode Output Voltage	5.0	6.2	7	V	
	Head Current Leakage	-200		200	µA	Per Side

4

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
READ MODE (cont.)						
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	0.6	µs	Note 1
	Write to Read		0.1	0.6	µs	Note 1,3
CS	Start-up Delay		0.1	0.6	µs	Note 1,2
	Inhibit Delay		0.1	0.6	µs	Note 3
	Head Switching Delay		0.1	0.6	µs	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6		8.0	µs	I_W = 50 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	I_W = 20 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay			30	ns	Note 4, See Figure 1, TD3
	Asymmetry			2	ns	Note 5
	Rise or Fall Time			20	ns	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0H, R_h = 0Ω
Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

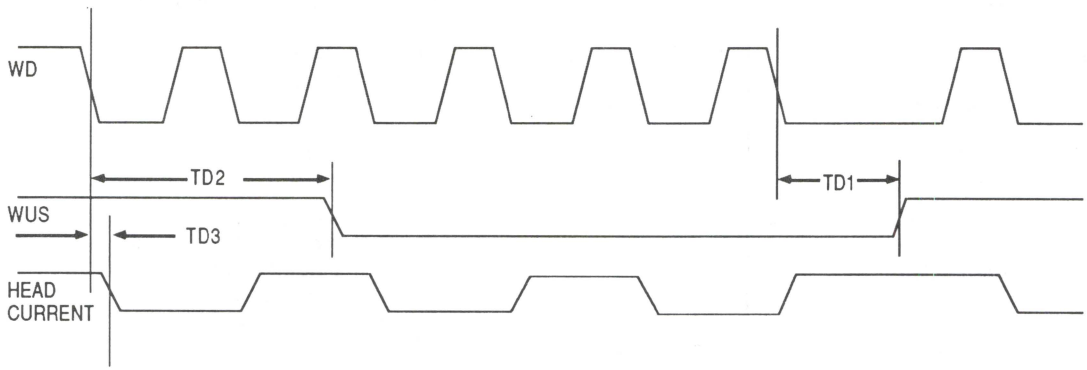


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (W.U.S.) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/W high enables the data readback mode. A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well by passed. The XR-501 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-501R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-501R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-501 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$RIW = \frac{140{,}000}{I_W}$$

where I_W is in mA and R_{IW} is in Ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130\left(\frac{55}{IW}\right)$$

where R_{CT} is in Ohms and IW is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. All XR-501 packages are suitable for continuous operation under worst case conditions without requiring R_{CT}. If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1}.

Write center tap circuitry is designed for higher stability than similar devices from other manufacturers. If extreme conditions exist, a ferrite bead around the V_{CT} line to the heads will reduce overshoot and ringing.

Write Unsafe Indicator (WUS)

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS This output is for indication only, intended for signaling a controller, and does not stop the write operation. A pull-up resistor of from 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable,

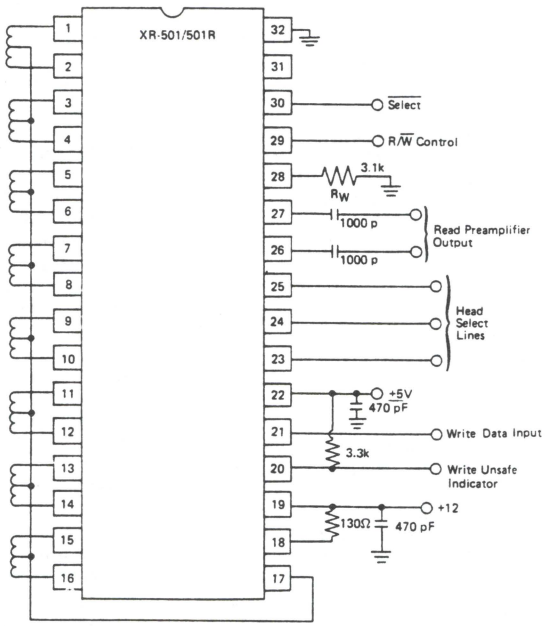
Device operation at standard voltages (V_{CC} = 5 V ± 10%, V_{DD1} = 12 V 1 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

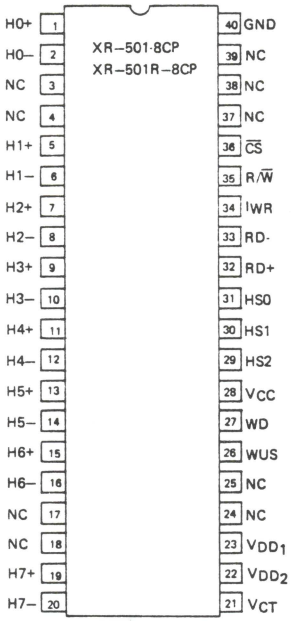
The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz band- width and low noise characteristics (1.0 nV/ √Hz typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.5 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 µA.

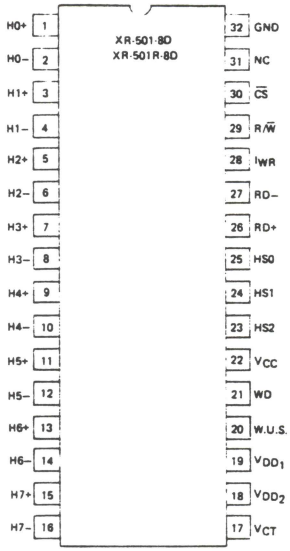
The XR-501 read preamplifier is specially designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time.

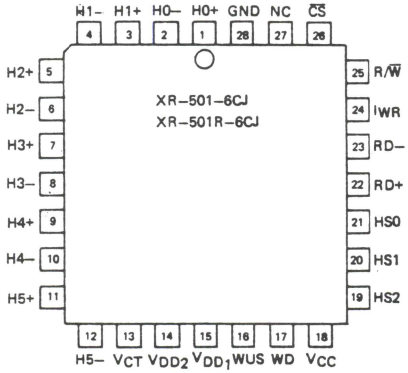


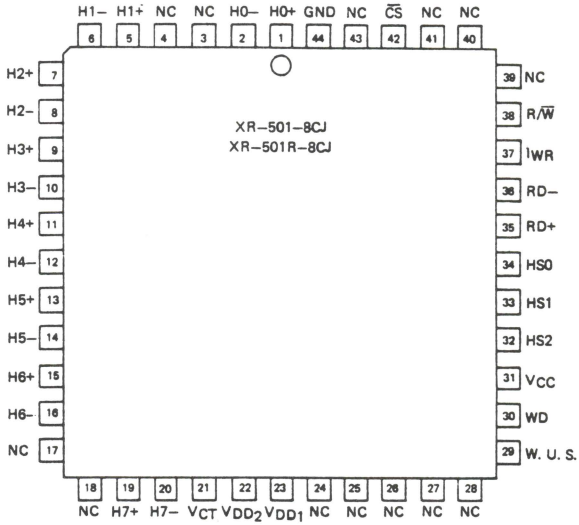
XR-501R Typical Application Circuit

NOTE: Non 'R' Versions Require External Damping Resistors









XR-501-6CP/501R-6CP/501-6D/501R-6D 28 Pin Package Pinout shown on front page.



NOTES



R/W Preamplifier for 3 Terminal Recording Heads, 2, 4, or 6, Channels

GENERAL DESCRIPTION

The XR-510A is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-510A is compatible with 2" to 14" single and multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring from two to six center-tapped read/write heads Multiple devices are easily cascaded for drives with more heads.

The XR-510AR option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-510A, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Available in Two, Four and Six Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs
Optional Internal Damping Resistors
Fast Settling Time

APPLICATIONS

Hard Disk Drives with MIG, ferrite, or composite heads

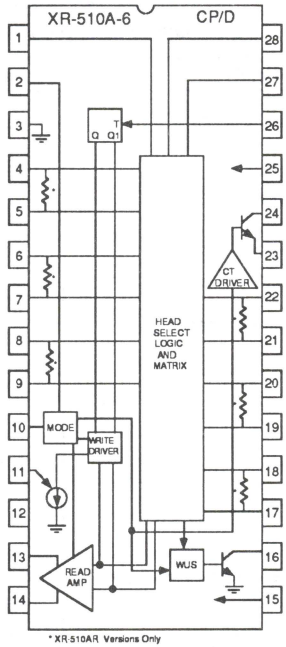
ABSOLUTE MAXIMUM RATINGS

V_{DD}	15 V
V_{CC}	6 V
Digital Inputs	-0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

SYSTEM DESCRIPTION

The XR-510A consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of six heads, and associated control and monitoring functions.

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-510A-2CP	18 Pin Plastic DIP	0°C to 70°C
XR-510A-2D	18 Pin SO	0°C to 70°C
XR-510A-4CP	22 Pin Plastic DIP	0°C to 70°C
XR-510A-4D	24 Pin SO	0°C to 70°C
XR-510A-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-510A-6CJ	28 Pin PLCC	0°C to 70°C
XR-510A-6D	28 Pin SO	0°C to 70°C
XR-510AR-2CP	18 Pin Plastic DIP	0°C to 70°C
XR-510AR-2D	18 Pin SO	0°C to 70°C
XR-510AR-4CP	22 Pin Plastic DIP	0°C to 70°C
XR-510AR-4D	24 Pin SO	0°C to 70°C
XR-510AR-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-510AR-6CJ	28 Pin PLCC	0°C to 70°C
XR-510AR-6D	28 Pin SO	0°C to 70°C

Less than 1.0 nV/ Hz (nominal) noise allows error free operation with small input signals. Over 40 mA of write current output (user adjustable) is available. Preamplifier offset voltages are low, aiding use in "wedge" servo drives and in other applications where rapid system settling times are needed.

ELECTRICAL SPECIFICATIONS

Test Conditions: T_A = 25°C, V_{CC} = 5 V, V_{DD} = 12 V, I_W = 40 mA, R_D = 750Ω, C_L (R_{D+},R_{D-})≤20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	Min	TYP	MAX	UNIT	CONDITION
I_{CC}	Supply Current			35	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			20	mA	V_{DD} = 13.2 V, Idle Mode
				40	mA	V_{DD} = 13.2 V, Read Mode
				20	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
PD	Power Dissipation			400	mW	Idle Mode - V_{CC} = 5.5 V, V_{DD} = 13.2 V
				600	mW	Read Mode - V_{CC} = 5.5 V, V_{DD} = 13.2 V
				670	mW	I_W = 40 mA, R_{CT} = 160Ω
				800	mW	I_W = 40 mA, R_{CT} = 0Ω
V_{CT}	Center Tap Voltage		5.0		V	Read Mode
			7.0		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{0L} = 8 mA
I_{OH}	Leakage Current			100	µA	V_{OH} = 5 V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-0.4			mA	V_{IL} = 0.8 V
I_{IH}	Input High Current			100	µA	V_{IH} = 2.0 V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-5		5	%	Error from $I_W = \frac{2.5V}{R_W}$
	Recommended Write Current Range	10		40	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	µA	Peak
	Unselected Transient Current			2	mA	Peak

SYMBOL	PARAMETER	Min	TYP	MAX	UNIT	CONDITION
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			KΩ	XR-510A
		635	750	865	Ω	XR-510AR
	WD Rate/Transistion Freq.	250	500		kHz	
K_I	Current Source Factor		1			$K_I = I_W/(\text{Current through } R_W)$
K	Write Current Constant	2.375	2.50	2.625	V	$K = I_W \cdot R_W$
	Write Protection Leakage Current	-200		200	µA	Per Side, $V_{CC} \leq 3.7$ V and/or $V_{DD} \leq 8.5$ V
V_{OS}	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	-100		100	µA	Write or Idle Mode, RD += $R_{D-} = 6$ V
READ MODE						
A_V	Differential Voltage Gain	85		115	V/V	$V_{IN} = 1$ mVp-p at 300 kHz, $R_L+ = R_L- = 1K\Omega$
	Dynamic Range	-3		+3	mV	DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p at 300 KHz.
R_{IN}	Differential Input Resistance	2			KΩ	XR-510
		500	650	850	Ω	XR-510AR
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	$nV/\sqrt{HZ}$	$L_h = 0$, $R_h = 0$, $B_W = 15$ MHz
BW	Bandwidth	30	60		MHz	-3 dB Point, $\|Z_s\| \leq 5\Omega$, $V_{in} =$ 1 mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT} + 100$ mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}

4

SYMBOL	PARAMETER	Min	TYP	MAX	UNIT	CONDITION
READ MODE (cont.)						
	Channel Separation	45	60		dB	Unselected Channel: V_{IN} - 100 mVp-p at 5 MHz. Selected Channel V_{IN} - 0 V
V_{OS} Out	Output Offset Voltage	-440	-+50	440	mV	
ΔV_{OS}	Output Offset Voltage Change		-+20		mV	Switching between any two heads
V_{CM}	Common Mode Output Voltage	4.5	5.5	6.5	V	
ΔV_{CM}	V_{CM} Change from Write to Read		500		mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	-200		200	µA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/$\overline{W}$	Read to Write		0.1	1	µs	Note 1
	Write to Read		0.1	1	µs	Notes 2,3
$\overline{CS}$	Start-up Delay		0.1	1	µs	Notes 1,2
	Inhibit Delay		0.1	1	µs	Note 3
	Head Switching Delay		0.1	1	µs	Note 2, Switching between any heads.
WUS	Write Unsafe Safe to Unsafe	1.6	2	8.0	µs	I_W = 35 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	I_W = 35 mA, See Figure 1, TD2
I_W	Head Current Propagation Delay		2	25	ns	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	ns	Note 5
	Rise or Fall Time		1	20	ns	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.

Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.

Note 3: Delay to 90% Decay of I_W.

Note 4: From 50% Points. L_h =0µH, R_h = 0Ω.

Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

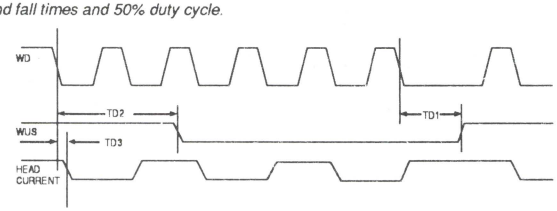


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity. Improved write stability over 117-type devices is achieved by employing a unity gain write current constant.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/ Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude IW, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk oontroller whenever one of six error conditions exist and writing should be discontinued. The six faults are: -open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/W high enables the data readback mode. The head read signal is amplified by the low noise differential stage and is output by low impedance drivers for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency. high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-510A is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-510AR option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-510AR option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-510A lead to a certain degree of electrostatic discharge (ESD) suseptability, so static reducing precautions should be taken.

Write Mode Design Considertions

Write current, I_W. typically between 20 mA and 40 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{2500}{I_W}$$

where I_W is in mA and R_{IW} is in Ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 150\ \frac{(40)}{Iw}$$

where R_{CT} is in Ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. If RCT is not used, VDD2 is directly conneded to VDD1.

Write Unsafe Indicator (WUS)

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exists. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS This output is for indication only, intended for signaling a controller, and does not stop the write operation. A pull-up resistor of from 2K Ω to 10KΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable.

Device operation at standard voltages (V_{CC} = 5 V ±10%, V_{DD1} = 12 V ± 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.0nV/$\sqrt{Hz}$ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.3 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100μA.

The XR-510A read preamplifier is specifically designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time. DC shifts are typically held under 500mV from the 5.3V nominal bias level.

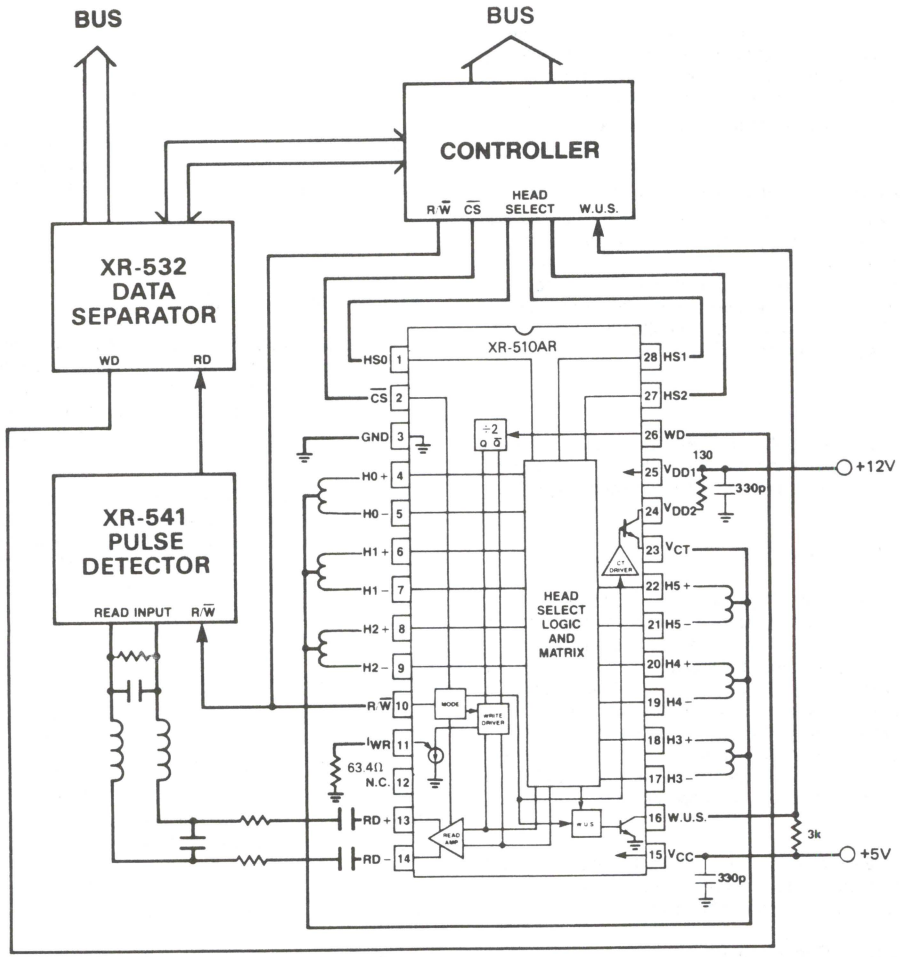


Figure 2. Hard Disk Read/Write Applications Circuit
Note: Circuit shown for XR-510AR . Non-R versions require damping resistors across each head.

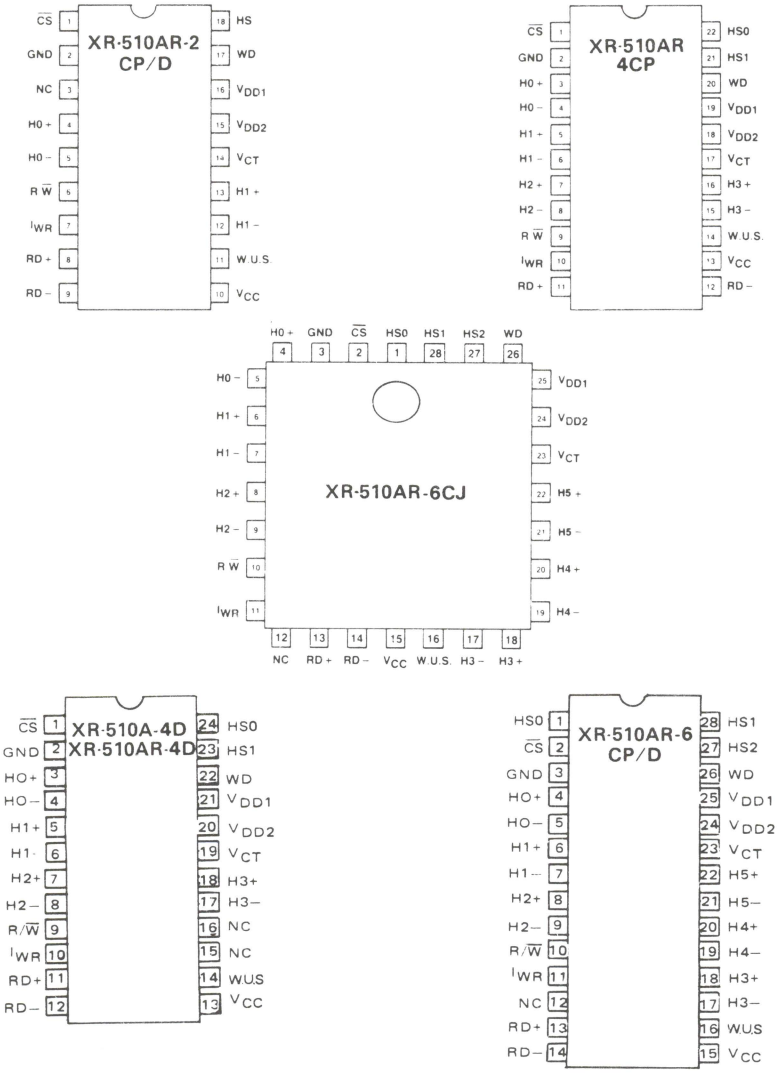


Figure 3. Additional Packages for XR-510A



NOTES



R/W Preamplifier for 3 Terminal Recording Heads, 4, 6, or 8 Channels

GENERAL DESCRIPTION

The XR-511 is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-511 is compatible with 3 1/2" to 14" multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring six or eight center-tapped read/write heads. Multiple devices are easily cascaded for drives with more heads.

The XR-511 features a pinout with all head ports on one side of the circuit. This eases flex cable or PC board layout by eliminating crossovers, The XR-511R option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-511, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Pinout Optimized for Easy Layout
Available in Four, Six and Eight Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs
Optional Internal Damping Resistors

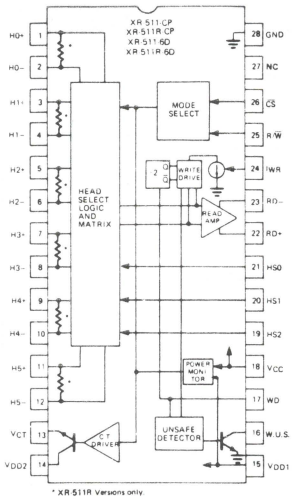
APPLICATIONS

Hard Disk Drives with MIG, ferrite, or composite heads

ABSOLUTE MAXIMUM RATINGS

V_{DD}	15V
V_{CC}	6V
Digital Inputs	-0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-511-4D	24 Pin SO	0°C to 70°C
XR-511-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-511-6CJ	28 Pin PLCC	0°C to 70°C
XR-511-6D	28 Pin SO	0°C to 70°C
XR-511-BCP	40 Pin Plastic DIP	0°C to 70°C
XR-511-8CJ	44 Pin PLCC	0°C to 70°C
XR-511-8D	32 Pin SO	0°C to 70°C
XR-511R-4D	24 Pin SO	0°C to 70°C
XR-511R-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-511R-6CJ	28 Pin PLCC	0°C to 70°C
XR-511R-6D	28 Pin SO	0°C to 70°C
XR-511R-8CP	40 Pin Plastic DIP	0°C to 70°C
XR-511R-8CJ	44 Pin PLCC	0°C to 70°C
XR-511R-8D	32 Pin SO	0°C to 70°C

SYSTEM DESCRIPTION

The XR-511 consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of eight heads, and associated control and monitoring functions. Less than 1.0 nV/√Hz (nominal) noise allows error free operation with small input signals. Over 40 mA of write current are available.

ELECTRICAL SPECIFICATIONS

Test Conditions: TA = 25°C, V_{CC} = 5 V, V_{DD} = 12 V, I_W = 40 mA, R_D = 750Ω, C_L (R_{D+},R_{D-}) ≤ 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{CC}	Supply Current			35	mA	V_{CC} = 5.5 V, Read or Idle Mode
			30	mA		V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			20	mA	V_{DD} = 13.2 V, Idle Mode
				40	mA	V_{DD} = 13.2 V, Read Mode
				20	mA	V_{DD} = 13.2 V, Write Mode, I_W= 0 mA
PD	Power Dissipation			400	mW	Idle Mode - V_{CC} - 5.5 V, V_{DD} = 13.2 V
				600	mW	Read Mode - V_{CC} - 5.5 V. V_{DD} = 13.2 V
				670	mW	I_W = 40 mA, R_{CT} = 160Ω
				800	mW	I_W = 40 mA, R_{CT} = 0Ω
V_{CT}	Center Tap Voltage		5.0		V	Read Mode
			7.0		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL}=8 mA
I_{OH}	Leakage Current			100	µA	V_{OH} = 5 V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-0.4			mA	V_{IL} = 0.8 V
I_{IH}	Input High Current			100	µA	V_{IH} = 2.0 V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-5		5	%	Error from $I_W = \frac{2.5V}{R_W}$
	Recommended Write Current Range	10		40	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	µA	
	Unselected Transient Current			2	mA	Peak

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
WRITE CHARACTERISTICS						
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			KΩ	XR-511
		635	750	865	Ω	XR-511R
	WD Rate/Transistion Freq.	125	500		KHz	WUS = Unsafe
K_I	Current Source Factor		1			K_I I_W/(Current through R_W)
K	Write Current Constant	2.375	2.50	2.625	V	$K = I_W \cdot R_W$
	Write Protection Leakage Current	-200		200	µA	Per Side, $V_{CC} \leq 3.7$ V $V_{DD} \leq 8.5$ V
V_{OS}	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	-100		100	µA	Write or Idle Mode, R_D += R_D- = 6 V
READ MODE						
A_V	Differential Voltage Gain	85		115	V/V	V_{IN} = 1 mVp-p at 300 kHz. R_L+ = R_L- = 1kΩ
	Dynamic Range	-3		+3		DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2	8		KΩ	XR-511
		530	650	790	Ω	XR-511R
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	nV/√Hz	L_h = 0, R_h = 0, BW = 15 MHz
BW	Bandwidth	30	60		MHz	-3 dB Point, $\|Z_s\| \leq 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	V_{CM} - V_{CT} + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}

4

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
READ MODE (cont)						
	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0 V
	Output Offset Voltage	-440	-+50	440	mV	
V_{CM}	Common Mode Output Voltage	4.5	5.5	6.5	V	
Δ_{VCM}	VCM Change from Write to Read		500		mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	-200		200	µA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	µs	Note 1
	Write to Read		0.1	1	µs	Notes 2,3
CS	Start-up Delay		0.1	1	µs	Notes 1,2
	Inhibit Delay		0.1	1	µs	Note 3
	Head Switching Delay		0.1	1	µs	Note 2, Switching between any heads.
WUS	Write Unsafe Safe to Unsafe	1.6		8.0	µs	I_W = 35 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	I_W = 35 mA, See Figure 1, TD2
I_W	Head Current Propagation Delay		2	25	ns	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	ns	Note 5
	Rise or Fall Time		1	20	ns	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.

Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope,

Note 3: Delay to 90% Decay of I_W.

Note 4: From 50% Points. L_h = 0µH, R_h = 0Ω.

Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

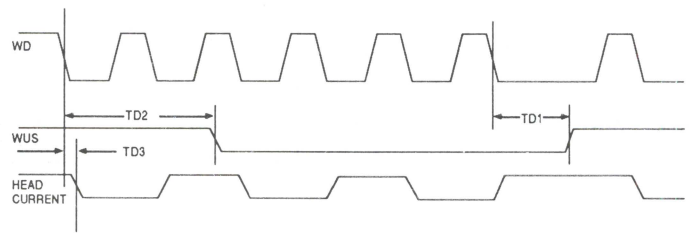


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity. Improved write stability over 501-type devices is achieved by employing a unity gain write current constant.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select (LS) and Read/ Write (R/W) must be pulled low. The desired head, selected by HSO to HS2, is driven by a differential current sink of magnitude I_W, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: -open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/W high enables the data readback mode, A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-511 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-511R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-511R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-511 lead to a certain degree of electrostatic discharge (ESD) susceptability. so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 40 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{2500}{I_W}$$

where I_W is in mA and R^{IW} is in Ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = \frac{130\ (55)}{I_W}$$

where R_{CT} is in Ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. All XR-511 packages are suitable for continuous operation under worst case conditions without requiring R_{CT}. If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1}.

Write Unsafe Indicator (WUS)

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exists. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not stop the write operation. A pull-up resistor of from 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V andlor V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable,

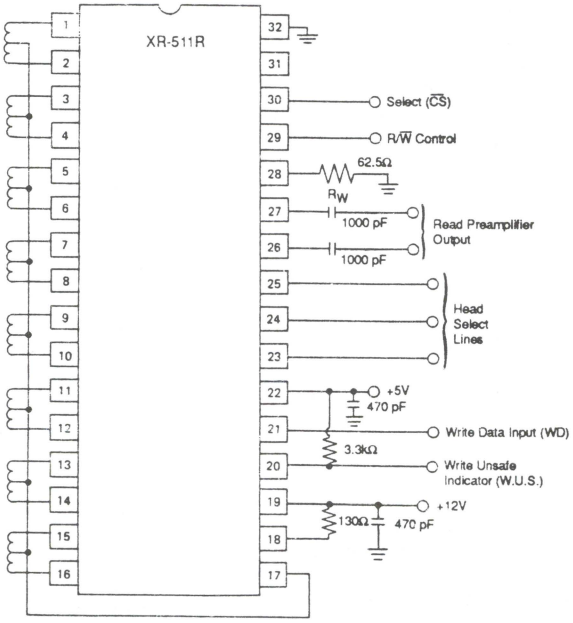
Device operation at standard voltages (V_{CC} = 5 V ± 10%, V_{DD1} = 12 V ± 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

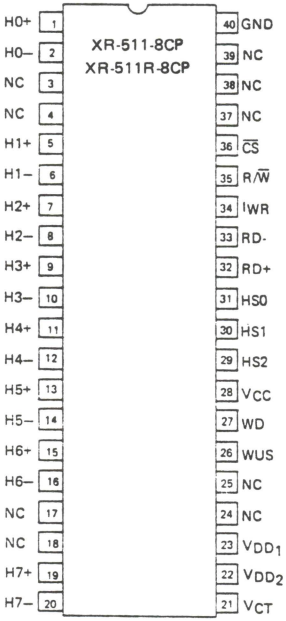
The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.0nV/√HZ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.5 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 µA.

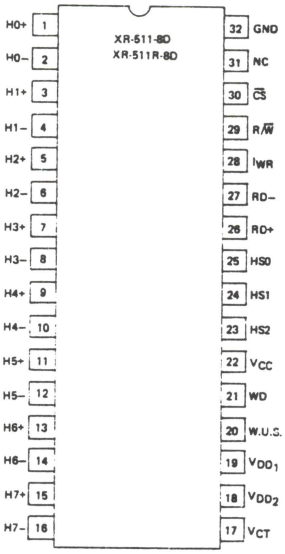
The XR-511 read preamplifier is specially designed to minimize output common mode voltage changes between writs mode and read mode, thus reducing switching transients that slow write to read recovery time. DC shifts are typically held under 500 mV from the 5.5 V nominal bias level.

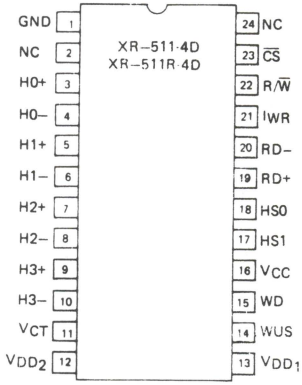


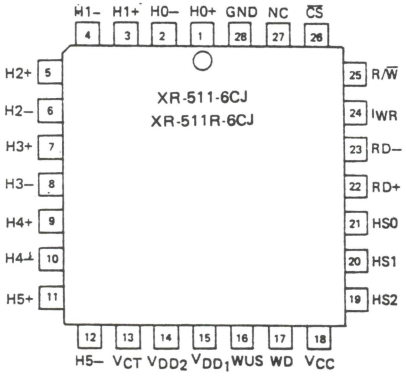
XR 511R Typical Application Circuit

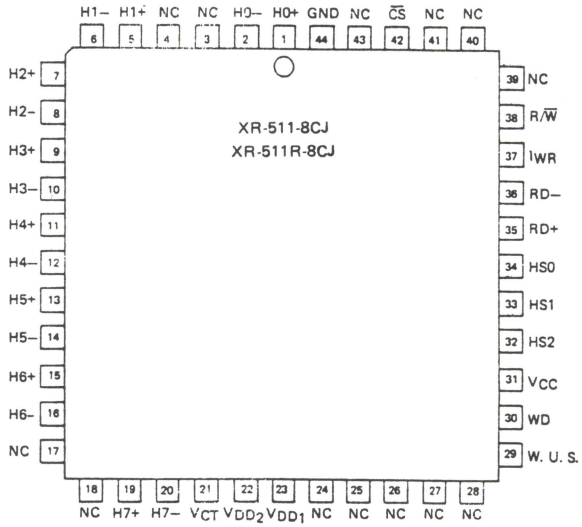
NOTE: Non 'R' Versions Require External Damping Resistors











XR-511-6CP/511R-6CP/511-6D/511R-6D 28 Pin Package Pinout shown on front page.



NOTES



5V R/W Preamplifier for 3 Terminal Recording Heads, 2 or 4 Channels

GENERAL DESCRIPTION

The XR-505 is a monolithic disk drive integrated circuit providing read mode preamplification, write current control, and head selection. It requires a single +5V power supply and consumes far less power than similar devices.

Up to four read/write heads can be switched with one device; multiple devices are cascadable. A low noise read signal preamplifier provides two user selectable gain levels.

All digital controls are TTL compatible. The XR-505 is available in 16, 20 and 24 pin SO packages. A 24 Pin DIP version is available for evaluation.

FEATURES

Complete Head Interface Functions, Read and Write
Low Power, Single +5V Operation
High Bandwidth and Dynamic Range
Low Noise Preamplifier
Error Preventing Power Monitor
Pinout Designed for Layout Ease
Digitally Selectable Preamplifier Gain
Digitally Selectable Write Current

APPLICATIONS

Battery operated Winchester disk drives
Low power disk drives
High density floppy disk drives
Digital tape drives
Dedicated servo read/write

ABSOLUTE MAXIMUM RATINGS

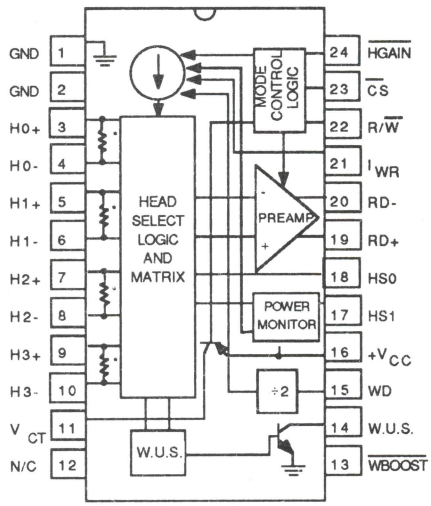
V_{CC}	8 Volts
Digital Inputs	-0.3V to V_{CC} +0.3V
Write Current	70mA
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C

SYSTEM DESCRIPTION

The XR-505 is a low power four channel Winchester Disk Drive Read/Write Amplifier ideally suited for laptop computer system drives and other applications where power consumption is important. Similar in function to other Exar Read/Write amplifiers, the XR-505 provides equivalent or superior performance at one-fourth the power consumption and requires only a single +5V power supply.

The read preamplifier section consists of a 55MHz bandwidth 1nV/ Hz noise level differential amplifier. Preamplifier gain of either 100 V/V or 200 V/V is digitally selectable. The write driver controls up to 5OmA of write current. A full featured power monitor circuit positively disables write mode operation during low voltage fault conditions to preserve data integrity.

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-505-4D	24 JEDEC SO	0°C to 70°C
XR-505R-4D	24 JEDEC SO	0°C to 70°C
XR-505R-4AD	20 JEDEC SO	0°C to 70°C
XR-505R-4BD	20 JEDEC SO	0°C to 70°C
XR-505R-2AD	16 JEDEC SO	0°C to 70°C
XR-505-2BD	16 JEDEC SO	0°C to 70°C
XR-505R-2AD	16 JEDEC SO	0°C to 70°C
XR-505R-2BD	16 JEDEC SO	0°C to 70°C
XR-505R-2AG	16 JEDEC SO	0°C to 70°C
XR-505R-2BG	16 JEDEC SO	0°C to 70°C
XR-505-4CP	24 DIP	0°C to 70°C

(other versions and packages available upon request)

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 4.5V to 5.5V (5.0V nominal), I_W = 25 mA, R_D = 75OΩ, C_L (R_{D+}, R_{D-}) ≤ 20 pF, Lh = 10 µH, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current		25	35	mA	V_{CC} = 5.5V, Read
			20	30	mA	V_{CC} = 5.5V, Write Mode I_W = 0
P_D	Power Dissipation		0.5	1	mW	Idle Mode. V_{CC} = 5.5V
			125	170	mW	Read Mode. V_{CC} = 5.5V,
			100	150	mW	Write Mode: I_W = 0mA. V_{CC} = 5.5V
V_{CT}	Center Tap Voltage		2.1		V	Read Mode. V_{CC} = 5V
			4.5		V	Write Mode. V_{CC} = 5V
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL} = 8mA
I_{OH}	Leakage Current			100	µA	V_{OH} = 5V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-0.4			mA	V_{IL} = 0.8V
I_{IH}	Input High Current			100	µA	V_{IH} = 2.0V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-7	±2	7	%	Error from $I_W = \frac{0.47V}{R_W}$ See Fig.2
	Recommended Write Current Range	10		40	mA	
WBOOST	Write Current Boost Factor	1.20	1.25	1.30	I/I	$\overline{\text{WBOOST}}$ = Low
	Differential Head Voltage Swing	7.0	8.2		V	Peak (Inductive Load), L_h =10µH Iw = 40mA
	DC Swing	3.5	4		V	DC Load, One Side
	Unselected Differential Head Current			85	µA	
	Unselected Transient Current			2	mA	Peak
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			kΩ	XR-505
		635	750	865	Ω	XR-505R
WUS	WD Rate/Transition Freq.	125			kHz	
K_I	Current Source Factor		1			$K_I = I_W$/(Current through R^W^)
K	Write Current Constant	440	470	500	mV	K = 1000 $I_w \cdot R_w$
	Write Protection Shut-off Leakage Current	-200		+200	µA	Per Side, V_{CC} ≤ 3.7V
V_{OS}	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CM}	Preamplifier Output Common Mode Voltage		1.5		V	Write Mode
	Preamplifier Output Leakage Current	-100		+100	µA	Write or Idle Mode, $R_D+ = R_D- = 6V$
READ MODE						
A_V	Differential Voltage Gain	85	100	115	V/V	$\overline{HGAIN}$= High, V_{IN} = 1mVp-p at 300 kHz, $R_L+ = R_L- = 1k\Omega$
		170	200	230	V/V	$\overline{HGAIN}$ = Low
	Dynamic Range	-3		+3	mV	DC input voltage where gain drops 10% $V_{in} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2	8		kΩ	XR-505
		500	650	850	Ω	XR-505R
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	$nV/\sqrt{Hz}$	$L_h = 0$, $R_h = 0$, BW = 15MHz
BW	Bandwidth	30	60		MHz	-3dB Point, $\lvert Z_s \rvert \pm 5\Omega$, V_{in}= 1mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	60	80		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5MHz
PSRR	Power Supply Rejection Ration	60	80		dB	100mVp-p at 5 MHz Superimposed on V_{CC}
	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel $V_{IN} = 0$
V_{OS}	Output Offset Voltage	-200	150	+200	mV	
ΔV_{OS}	Output Offset Voltage Change	-100	120	+100	mV	Switching Between Any Two Heads
V_{CM}	Common Mode Output Voltage	1.25	1.50	1.75	V	
ΔV_{CM}	V_{CM} Change from Write to Read	-200	+100	+200	mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	-200		+200	µA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	µS	Note 1
	Write to Read		0.1	1	µS	Notes 2,3
CS	Start-up Delay		0.1	1	µS	Notes 1,2
	Inhibit Delay		0.1	1	µS	Note 3
	Head Switching Delay		0.1	1	µS	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6		8.0	µS	I_W = 25 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µS	I_W = 25 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay		2	25	nS	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	nS	Note 5
	Rise or Fall Time		1	20	nS	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.

Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.

Note 3: Delay to 90% Decay of I_W.

Note 4: From 50% Points. L_h = 0H, R_h =0Ω

Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

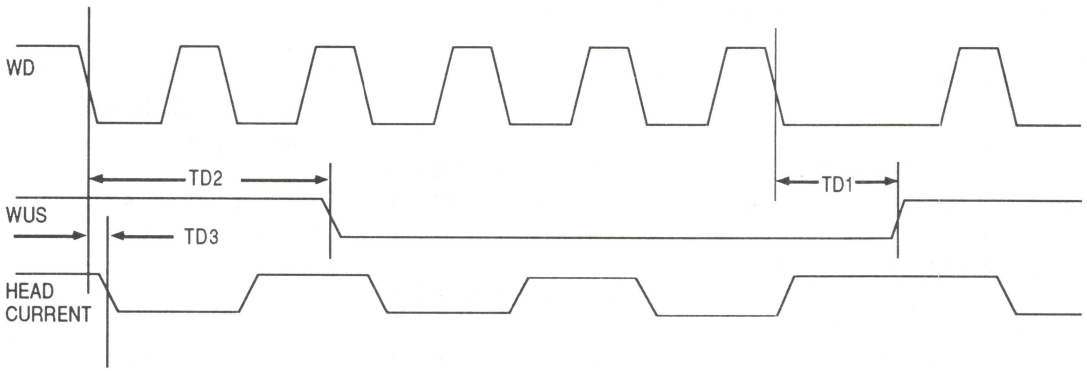


Figure 1. Write Mode Timing Diagram

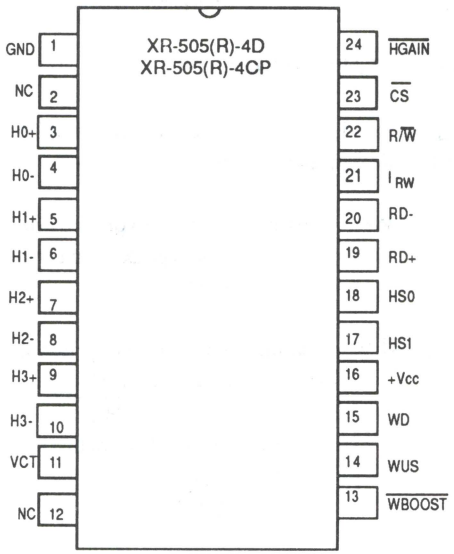
XR-505 PIN DESCRIPTION

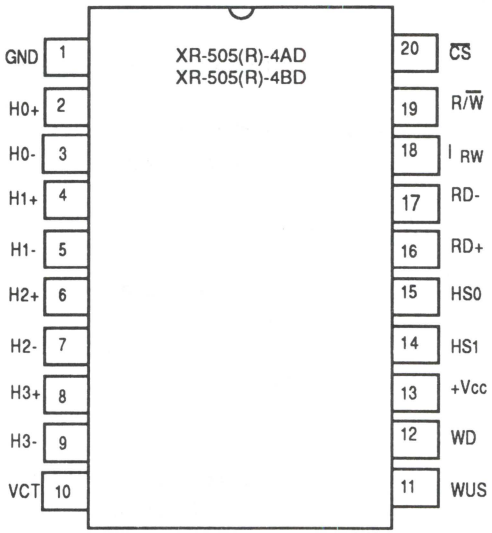
PIN	SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select	Low enables device operation
R/$\overline{W}$	Read/Write Select	High selects read mode Low selects write mode
WD	Write Data Input	
$\overline{HGAIN}$	High Gain Select	Low selects preamp gain of 200V/V High selects preamp gain of 100V/V
WUS	Write Unsafe Output	Open collector output. High indicates write fault condition
HS0, HS1	Head Select	Selects head for Read/Write operation
V_{CC}	+5V Supply Input	
R_{D+}, R^D-	Read Preamplifier	Differential preamplifier output
I_{WR}	Write Current	Resistor to ground programs peak write current level
$\overline{WBOOST}$	Write Current Boost	Low Selects, I_W Boost of $I_W = 1.25 \cdot \frac{0.47}{R_W}$ High Selects Nominal $I^W = \frac{0.47}{R^W}$

4

XR-505 DIGITAL CONTROLS

CONTROL PIN						FUNCTION
$\overline{CS}$	R/$\overline{W}$	$\overline{HGAIN}$	$\overline{WBOOST}$	HS1	HS0	
1	X	X	X	X	X	Device Disabled
0	0	X	0	0	0	Write Mode, Head 0, Iw = Boost
0	0	X	0	0	1	Write Mode, Head 1, Iw = Boost
0	0	X	0	1	0	Write Mode, Head 2, Iw = Boost
0	0	X	0	1	1	Write Mode, Head 3, Iw = Boost
0	0	X	1	0	0	Write Mode, Head 0, Iw = Normal
0	0	X	1	0	1	Write Mode, Head 1, Iw = Normal
0	0	X	1	1	0	Write Mode, Head 2, Iw = Normal
0	0	X	1	1	1	Write Mode, Head 3, Iw = Normal
0	1	0	X	0	0	Read Mode, Head 0, Preamp A^V = 200
0	1	0	X	0	1	Read Mode, Head 1, Preamp A^V = 200
0	1	0	X	1	0	Read Mode, Head 2, Preamp A^V = 200
0	1	0	X	1	1	Read Mode, Head 3, Preamp A^V = 200
0	1	1	X	0	0	Read Mode, Head 0, Preamp A^V = 100
0	1	1	X	0	1	Read Mode, Head 1, Preamp A^V = 100
0	1	1	X	1	0	Read Mode, Head 2, Preamp A^V = 100
0	1	1	X	1	1	Read Mode, Head 3, Preamp A^V = 100

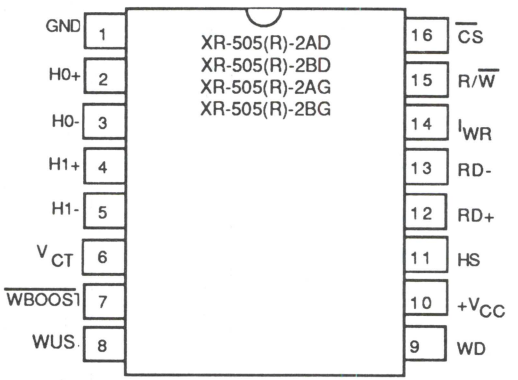




XR-505 Packaging Options

Device	HGain	WBoost	Package
XR-505(R)-4D	100/200	1.0/1.25	24 SO
XR-505(R)-4AD	100	1.0	20 SO
XR-505(R)-4BD	200	1.0	20 SO
XR-505(R)-2AD	100	1.0/1.25	16 SO
XR-505(R)-2BD	200	1.0/1.25	16 SO
XR-505(R)-2AG	100	1.0/1.25	16 SO
XR-505(R)-2BG	200	1.0/1.25	16 SO
XR-505(R)-4CP	100/200	1.0/1.25	24 DIP

"G" Package is 150 mil JEDEC SO



5V R/W Preamplifier for 3 Terminal Recording Heads, 2 or 4 Channels

GENERAL DESCRIPTION

The XR-507 is a monolithic disk drive integrated circuit providing read mode preamplification, write current control, and head selection. It requires a single +5V power supply and consumes far less power than similar devices.

Up to four read/write heads can be switched with one device; multiple devices are cascadable. A low noise read signal preamplifier provides two user selectable gain levels.

All digital controls are TTL compatible. The XR-507 is available in 16, 20 and 24 pin SO packages. A 24 Pin DIP version is available for evaluation.

FEATURES

Complete Head Interface Functions, Read and Write
Low Power, Single +5V Operation
High Bandwidth and Dynamic Range
Low Noise Preamplifier
Error Preventing Power Monitor
Pinout Designed for Layout Ease
Digitally Selectable Preamplifier Gain
Digitally Selectable Write Current

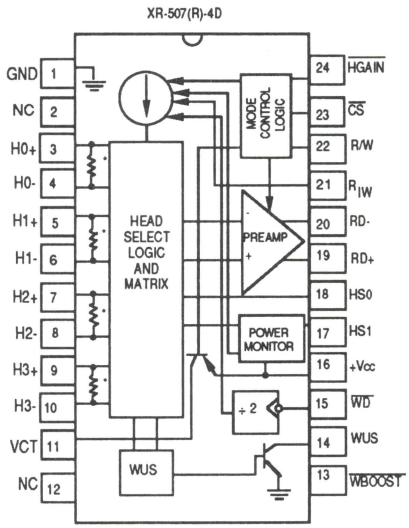
APPLICATIONS

Battery operated Winchester disk drives
Low power disk drives
High density floppy disk drives
Digital tape drives
Dedicated servo read/write

ABSOLUTE MAXIMUM RATINGS

VCC	8 Volts
Digital Inputs	-0.3V to VCC +0.3V
Write Current	70mA
Junction Temperature	150° C
Storage Temperature	-65° C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-507R-4CK	24 SOP	0°C TO 70°C

SYSTEM DESCRIPTION

The XR-507 is a low power four channel Winchester Disk Drive Read/Write Preamplifier ideally suited for laptop computer system drives and other applications where power consumption is important. Similar in function to other Exar Read/Write amplifiers, the XR-507 provides equivalent or superior performance at one-fourth the power consumption and requires only a single +5V power supply.

The read preamplifier section consists of a 60MHz bandwidth 1.0nv/$\sqrt{Hz}$ noise level differential amplifier. Preamplifier gain of either 100 V/V or 200 V/V is digitally selectable. The write driver controls up to 50mA of write current. A full featured power monitor circuit positively disables write mode operation during low voltage fault conditions to preserve data integrity.



NOTES



5V, R/W Preamplifier for 2 Terminal Recording Heads, 2 or 4 Channels

GENERAL DESCRIPTION

The XR-4610/4610R are bipolar monolithic integrated circuits commonly used in two terminal thin film recording head applications. The circuitry on the device includes a low noise preamplifier, write current control circuitry and data protection for both two and four channel applications. Power supply fault detection circuitry present on the device disables the write current generator in various power down modes. The read recovery time is improved by control of the read channel common mode output shift when in write mode. The read write device is also available in the XR-4610R option which offers internal 700 Ohm damping resistors.

The XR-4610/4610R operate on a single 5V power supply making them ideal for low power applications. They are available in a variety of low profile packaging options.

FEATURES

5V Supply Voltage Only
Low Power Device (150mW TYP in Read mode)
High Performance Circuitry
- -Low Input Noise = 0.70nV/$\sqrt{Hz}$ max
- -Read Mode Gain = 230V/V
- -Input Capacitance = 48pF max
- -Write Current Range = 10-35mA

Programmable Write Current Source
Write Unsafe Detect/Indicator
Power Supply Fault Protection
Head Short to Ground Protection
Enhanced Write to Read Recovery Time
Designed for Use With Two Terminal Thin Film Heads

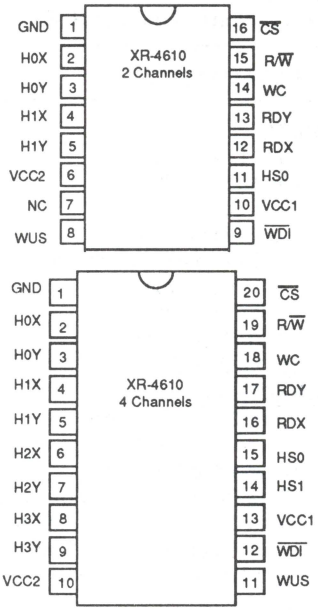
APPLICATIONS

Thin Film Recording Heads in Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3 to +7 VDC
Write Current IW	80mA
Digital Input Voltage	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	-0.3 to VCC2 +0.3 VDC
Output Current Maximum	
Pins: RDX, RDY	±10mA
WUS	+12mA
Storage Temperature Range	-65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4610/4610R-4CD	20 Pin SOP	0°C to 70°C
XR-4610/4610R-2CD	16 Pin SOP	0°C to 70°C
XR-4610/4610R-4CU	20 Pin SSOP	0°C to 70°C

SYSTEM DESCRIPTION

The XR-4610/4610R is a low power four channel hard disk drive Read / Write preamplifier for thin film (2 terminal) heads. The XR-4610/4610R provides superior recording performance, and uses only a +5V power supply. Its low power consumption suits it for drives used in battery powered laptop computers.
The read amplifier consists of a 55 MHz bandwidth 0.50 nV/$\sqrt{Hz}$ input noise (both typical) differential amplifier with a fixed gain of 230 V/V. The write driver has a current range of 10 to 35 mA and is disabled automatically when a voltage fault is detected. The write mode also has a write unsafe detection circuit.

ELECTRICAL CHARACTERISTICS

Test Conditions: L_H = 1.0µH R_H = 30 Ω, I_W = 20mA, f(Data) = 5MHz, $V_{CC1} = V_{CC2}$ = 5V ±5%

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INPUTS						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-400			µA	VIL = 0.8V
I_{IH}	Input High Current			100	µA	VIH = 2.0V
WUS VOL	WUS Output Low Voltage			0.5	V	I_{OL} = 2mA
VF	VCC1 Fault Voltage Fault to No Fault			4.2	V	Note 1
VF	VCC1 Fault Voltage No Fault to Fault	3.8			V	
WRITE CHARACTERISTICS						
VWC	Write Current Voltage	1.15		1.35	V	
	Differential Head Voltage Swing	3.4			V	
	Unselected Head Current			1	mA pk	
	Head Differential Load Capacitance			25	pF	
	Head Differential Load Resistance	560	700	950		R Option
	Head Differential Load Resistance	4K				
	WDI Transition Frequency	1			MHz	I_W = 5mA
IW	Write Current Range	10		35	mA	
READ CHARACTERISTICS Recommended operating conditions apply, unless otherwise stated. R_L(RDX,RDY) = 1KΩ, C_L(RDX,RDY) <20 pF, f = 5MHz						
Av	Differential Voltage Gain	180	230	260	V/V	
BW	Bandwidth -3dB	35	55		MHz	
eni	Equivalent Input Noise		0.50	0.70	nV/√Hz	BW= 15 MHz L_H= 0, R_H = 0
C_{IN}	Differential Input Capacitance			48	pF	
R_{IN}	Differential Input Resistance	835	2K		Ω	
R_{IN}	Differential Input Resistance		700		Ω	R Option
	Dynamic Range to 90% of Gain	3			mV pp	
CMRR	Common Mode Rejection Ratio	45			dB	
PSRR	Power Supply Rejection Ration	40			dB	100mV_{pp} 5MHz sin on V_{CC}
	Channel Rejection Ratio	45			dB	Unselected channels driven with100mV_{pp} 5MHz sin
	Output Offset Voltage	-300		300	mV	
R_O	Single Ended Output Resistance			40	Ω	
I_O	Output Current	1.4			mA	AC coupled load, RDX to RDY
V_{CM}	Common Mode Output Voltage	2		3.5	V	

DC CHARACTERISTICS

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
$I_{CC}1$	VCC1 Supply Current			33	mA	READ Mode
				27	mA	WRITE Mode
				12	mA	IDLE Mode
$I_{CC}2$	VCC2 Supply Current			11	mA	READ Mode
				10+ IW	mA	WRITE Mode
				400	µA	IDLE Mode
P_D	Power Dissipation			230	mW	READ Mode
				190+4IW	mW	WRITE Mode
			35	45	mW	IDLE Mode

Note 1: On the Fault to No Fault transition, all devices will be No Fault at 4.2V.
On the No Fault to Fault transition, all devices will be Fault at 3.8V.

4

SWITCHING CHARACTERISTICS - Recommended operating conditions apply unless otherwise specified.
Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω, f(Data) = 5 MHz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	R/$\overline{W}$ Read to Write		0.1	1.0	µs	R/$\overline{W}$ to 90% of write current
	Write to Read		0.5	1.0	µs	R/$\overline{W}$ to 90% of 100mV 10 MHz Read signal envelope
	$\overline{CS}$ Unselect to Select		0.4	1.0	µs	$\overline{CS}$ to 90% of write current or to 90% of 100mV 10MHz Read signal envelope
	Select to Unselect		0.4	1.0	µs	$\overline{CS}$ to 10% of write current
	HS0,1 to any Head		0.2	1.0	µs	To 90% of 100mV 10MHz Read signal envelope
TD1	WUS: Safe to Unsafe	0.6	2.0	3.6	µs	
TD2	Unsafe to Safe		0.2	1.0	µs	
	Head Current:					Lh = 0, Rh = 0
TD3	$\overline{WDI}$ to Ix - Iy			32	ns	from 50% level
	Asymmetry			1.0	ns	$\overline{WDI}$ has 1 ns rise/fall time

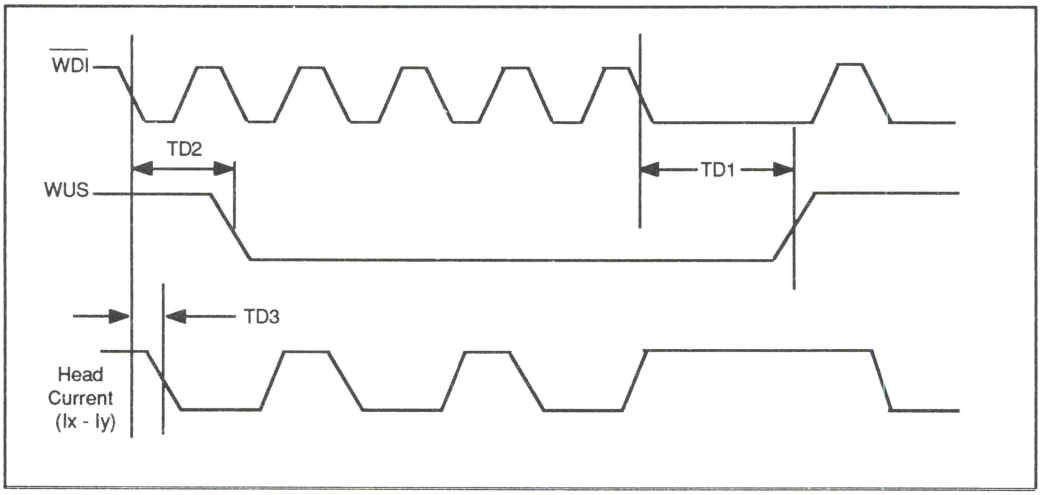


Figure 1. Write Mode Timing Diagram

PIN DESCRIPTION

Name	I/O	Description
HS0,HS1	I	Head Select. Select one of four heads.
$\overline{CS}$	I	Chip Select. High inhibits the chip.
R/$\overline{W}$	I	Read/$\overline{Write}$. High selects Read mode.
WUS *	O	Write Unsafe. High indicates an unsafe writing condition.
$\overline{WDI}$	I	$\overline{Write\ Data\ In}$. Changes the direction of the current in the recording head.
H0X-H3X; H0Y-H3Y	I/O	X,Y Head Connections
RDX, RDY *	O	X,Y Read Data. Differential read data output.
WC		Write Current. Used to set the magnitude of the write current.
VCC1	I	+5V Supply
VCC2	I	+5V Supply for Write current drivers.
GND	I	Ground

* These signals can be wire OR'ed.

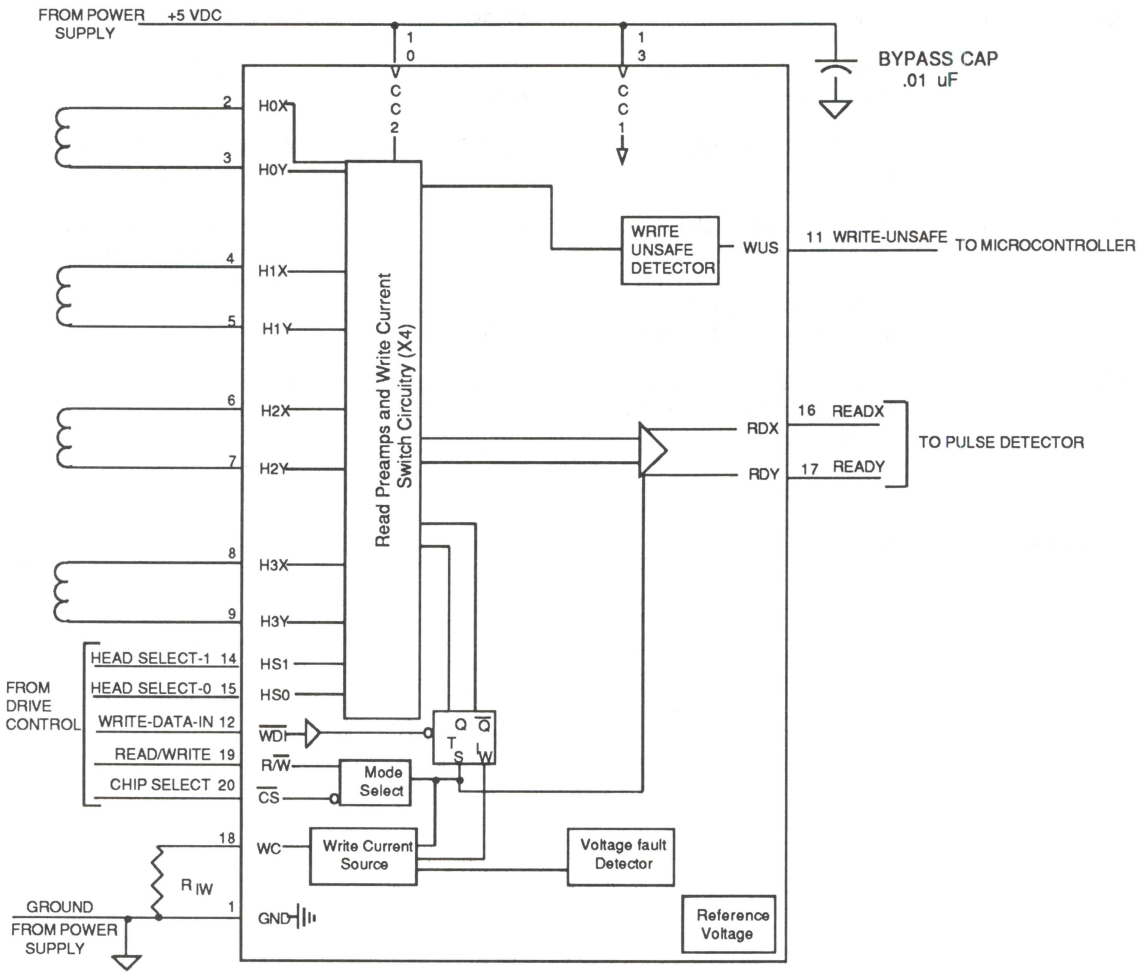


Figure 2. IC Interconnection and Block Diagram

CIRCUIT OPERATION

The XR-4610 read/write device is intended for use in thin film head hard disk drives with up to four heads. Head selection and mode selection instructions are shown in Tables 1 and 2 respectively. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ protect from accidental write current by internal pull up resistors. HS0 and HS1 have internal pull down resistors. The pin descriptions are shown on page 4.

Read Mode

In read mode operation, the low noise preamplifier circuit reads and amplifies pulses detected on the disk surface caused by magnetic transitions in the media. In this mode write current operations are disabled. RDX and RDY are emitter follower outputs which provide differential read data output pulses. These should be AC coupled to the load. In Write mode and in Idle mode these outputs go into a high impedance state. This allows wire-oring of these outputs in multi-chip applications where more than four head capability is required.

Write Mode

Write mode is selected when both R/$\overline{W}$ and $\overline{CS}$ are taken low. The head current direction of the selected head is toggled by each negative going transition on the write data input pin, $\overline{WDI}$. A preceding read or idle mode select initializes the write data flip-flop to pass current through the X side of the head. This current is set by and external resistor, Rw, where:

$$Iw = \frac{Vwc}{Rw}$$

Rw is connected between the pins WC and GND. The actual head current is also a function of the head resistance and external wire resistance (Rh) and the damping resistance (Rd), so that:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

The write unsafe detector is also activated in this state.
The pin WUS is an open collector output which should be tied to VCC by a 2KΩ to 10KΩ resistor.

Idle Mode

This mode is selected by taking the pin $\overline{CS}$ high. The pins RDX and RDY are placed in a high impedance mode to minimize device power consumption and allow another chip to drive these common lines.

Voltage Fault

The write current function is disabled when either a voltage fault or power startup mode is detected, to avoid going into Write mode and contaminating the disks.
The following conditions will indicate a Write Unsafe, but will not stop the Write operation:

- -Device in Read Mode
- -Chip Disabled
- -$\overline{WDI}$ Frequency too Low
- -No Write Current
- -Head Opened

MODE DESCRIPTION

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

Table 1. Head Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

Table 2. Mode Select



NOTES



5V, Low Power R/W Preamplifier for 3 Terminal Recording Heads, 2 or 4 channels

Advanced Information

GENERAL DESCRIPTION

The XR-9010/9010R are monolithic disk drive integrated circuits providing read mode pre-amplification, write current control, and head selection. They require a single +5V power supply and consume far less power than similar devices.

The XR-9010R option offers internal 750 Ohm damping resistors.

Up to four read/write heads can be switched with one device; multiple devices are cascadable. A low noise read signal preamplifier provides two user selectable gain levels.

All digital controls are TTL compatible. The XR-9010/9010R are available in 16, 20 and 24 pin SO packages. A 24 Pin DIP version is available for evaluation.

FEATURES

Complete Head Interface Functions, Read and Write
Low Power, Single +5V Operation
High Bandwidth and Dynamic Range
Low Noise Preamplifier
Error Preventing Power Monitor
Pinout Designed for Layout Ease
Digitally Selectable Write Current

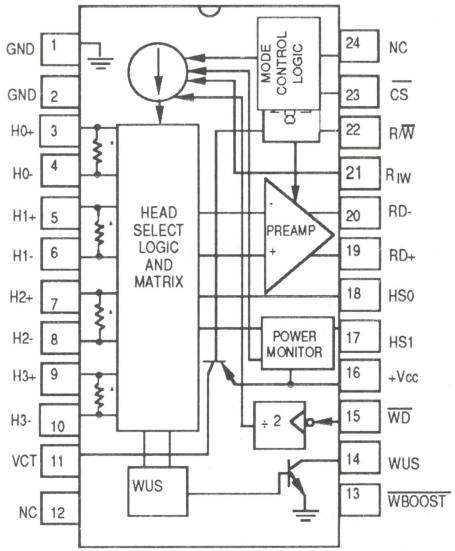
APPLICATIONS

Battery powered Winchester disk drives
High density floppy disk drives
Digital tape drives
Dedicated servo read/write

ABSOLUTE MAXIMUM RATINGS

V_{CC}	8 Volts
Digital Inputs	-0.3V to V_{CC} +0.3V
Write Current	70mA
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C

PIN ASSIGNMENT



(Evaluation SOIC)

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9010(R)-4CD	20 Pin SOP	0°C To 70°C
XR-9010(R)-2CD	16 Pin SOP	0°C To 70°C
XR-9010(R)-4CU	24 Pin SSOP	0°C To 70°C

(other versions and packages available upon request)

SYSTEM DESCRIPTION

The XR-9010/9010R is a low power, up to four channel Winchester Disk Drive Read/Write Amplifier ideally suited for laptop computer system drives and other applications where power consumption is important. Similar in function to other Exar Read/Write amplifiers, the XR-9010/9010R provides equivalent or superior performance at lower power consumption and requires only a single +5V power supply.

The read preamplifier section consists of a 60MHz bandwidth 0.65nV/ $\sqrt{Hz}$ noise level(both typical) differential amplifier. The write driver controls up to 50mA of write current. A full featured power monitor circuit positively disables write mode operation during low voltage fault conditions to preserve data integrity.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 4.5V to 5.5V (5.0V nominal), I_W = 25 mA, R_D = 750Ω, C_L (R_{D+}, R_{D-}) ≤ 20 pF, Lh = 10 µH, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current			35	mA	V_{CC} = 5.5V, Read
				30	mA	V_{CC} = 5.5V, Write Mode I_W = 0
P_D	Power Dissipation			2	mW	Idle Mode. V_{CC} = 5.5V
			125	190	mW	Read Mode. V_{CC} = 5.5V,
			100	165	mW	Write Mode: I_W = 0mA. V_{CC} = 5.5V
V_{CT}	Center Tap Voltage		4.2		V	Write Mode. V_{CC} = 5V
V_{PM}	Power Monitor Protection	3.9	4.1	4.4	V	V_{CC} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL} = 8mA
I_{OH}	Leakage Current			100	µA	V_{OH} = 5V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-0.4			mA	V_{IL} = 0.8V
I_{IH}	Input High Current			100	µA	V_{IH} = 2.0V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-7	±2	7	%	Error from I_W = 50V/R_W See Fig.2
	Recommended Write Current Range	10		50	mA	
$\overline{\text{WBOOST}}$	Write Current Boost Factor	1.20	1.25	1.30	I/I	$\overline{\text{WBOOST}}$ = Low
	Differential Head Voltage Swing	6.0			V	Peak (Inductive Load), L_h =10µH Iw = 40mA
	DC Swing	3.5	4		V	DC Load, One Side
	Unselected Differential Head Current			85	µA	
	Unselected Transient Current			2	mA	Peak
	Differential Output Capacitance			10	pF	
	Differential Output Resistance	10			KΩ	XR-9010
		600	750	960	Ω	XR-9010R
WUS	WD Rate/Transition Freq.	125			KHz	WUS = Unsafe
K_I	Current Source Factor		20			K_I = I_W/(Current through R_W)
K	Write Current Constant		50		V	I_w = K / R_w
	Write Protection Shut-off Leakage Current	-200		+200	µA	Per Side, V_{CC} ≤ 3.7V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CM}	Preamplifier Output Common Mode Voltage		2.3		V	Write Mode
	Preamplifier Output Leakage Current	-200		+200	µA	Write or Idle Mode, $R_{D}+ = R_{D}- = V_{CC}$
READ MODE						
A_V	Differential Voltage Gain	170	200	230	V/V	V_{IN} = 1mVp-p at 300 KHz, $R_L+ = R_L- = 1K\Omega$
	Dynamic Range	-3		+3	mV	DC input voltage where gain drops 10% $V_{in} = V_i + 0.5$ mVp-p at 300 KHz.
R_{IN}	Differential Input Resistance	2	8		KΩ	XR-9010
		500	650	850	Ω	XR-9010R
C_{IN}	Differential Input Capacitance			15	pF	
e_{ni}	Input Noise Voltage		.65	.85	$nV/\sqrt{Hz}$	L_h = 0, R_h = 0, BW = 15MHz
BW	Bandwidth	30	60		MHz	-3dB Point, $\lvert Z_s \rvert \pm 5\Omega$, V_{in}= 1mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	50			dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5MHz
PSRR	Power Supply Rejection Ration	45			dB	100mVp-p at 5 MHz Superimposed on V_{CC}
	Channel Separation	45				Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0
V_{OS}	Output Offset Voltage	-200		+200	mV	
ΔV_{OS}	Output Offset Voltage Change	-100		+100	mV	Switching Between Any Two Heads
V_{CM}	Common Mode Output Voltage		2.3		V	
	Head Current Leakage	-200		+200	µA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	1.5			mA	AC Coupled, Source or Sink

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
SWITCHING CHARACTERISTICS						
R/$\overline{W}$	Read to Write		0.1	1	µs	Note 1
	Write to Read		0.1	1	µs	Notes 2,3
$\overline{CS}$	Start-up Delay		0.1	1	µs	Notes 1,2
	Inhibit Delay		0.1	1	µs	Note 3
	Head Switching Delay		0.1	1	µs	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6		8.0	µs	I_W = 25 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	I_W = 25 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay		2	25	ns	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	ns	Note 5
	Rise or Fall Time		1	20	ns	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.

Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.

Note 3: Delay to 90% Decay of I_W.

Note 4: From 50% Points. L_h = 0µH, R_h =0Ω

Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

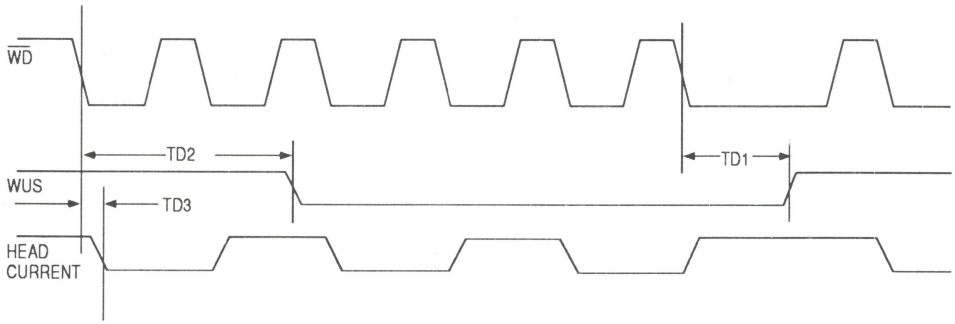


Figure 1. Write Mode Timing Diagram

PIN DESCRIPTION

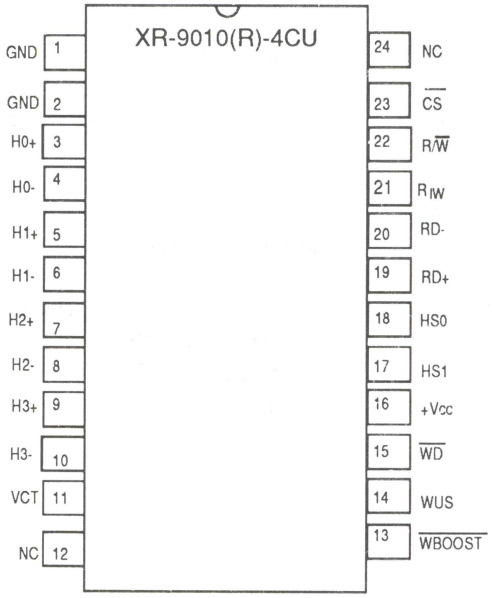
Pin #	Symbol	Description
23	$\overline{CS}$	$\overline{Chip\ Select}$. Low enables device operation.
22	R/$\overline{W}$	Read/$\overline{Write}$ Select. High selects read mode. Low selects write mode.
15	$\overline{WD}$	$\overline{Write\ Data}$ Input.
14	WUS	Write Unsafe Output. Open collector output High indicates write fault condition.
17,18	HS1,HS0,	Head Select. Selects head for Read/Write operation.

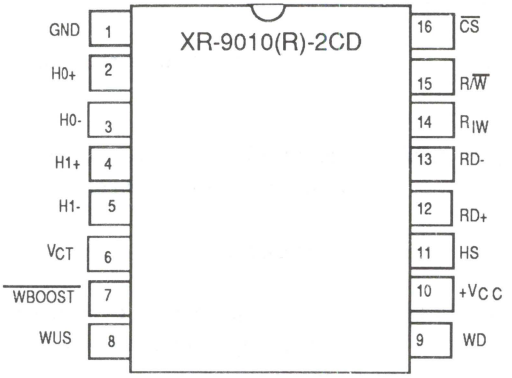
Pin #	Symbol	Description
16	V_{CC}	+5V Supply Input
19,20	R_{D+},R_{D-}	Read Preamplifier. Differential preamplifier output
21	R_{IW}	Write Current. Resistor to ground programs peak write current level
13	$\overline{WBOOST}$	$\overline{Write\ Current\ Boost}$. Low Selects, I_W Boost of $I_W = 1.25\ (K/R_W)$ High Selects Nominal $I_W = K/R_W$

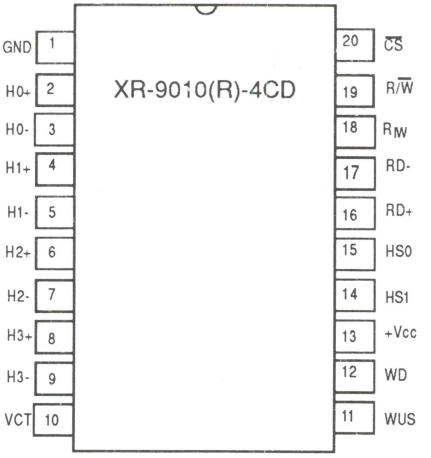
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DIGITAL CONTROLS

CONTROL PIN					FUNCTION
$\overline{CS}$	R/$\overline{W}$	$\overline{WBOOST}$	HS1	HS0	
1	X	X	X	X	Device Disabled
0	0	0	0	0	Write Mode, Head 0, Iw = Boost
0	0	0	0	1	Write Mode, Head 1, Iw = Boost
0	0	0	1	0	Write Mode, Head 2, Iw = Boost
0	0	0	1	1	Write Mode, Head 3, Iw = Boost
0	0	1	0	0	Write Mode, Head 0, Iw = Normal
0	0	1	0	1	Write Mode, Head 1, Iw = Normal
0	0	1	1	0	Write Mode, Head 2, Iw = Normal
0	0	1	1	1	Write Mode, Head 3, Iw = Normal
0	1	X	0	0	Read Mode, Head 0, Preamp A_V = 200
0	1	X	0	1	Read Mode, Head 1, Preamp A_V = 200
0	1	X	1	0	Read Mode, Head 2, Preamp A_V = 200
0	1	X	1	1	Read Mode, Head 3, Preamp A_V = 200







XR-9010 Packaging Options

Device	WBoost	Package
XR-9010(R)-4CD	1.0	20 SO
XR-9010(R)-2CD	1.0/1.25	16 SO

5V, R/W Preamplifier for 2 Terminal Recording Heads, 2 or 4 Channels

GENERAL DESCRIPTION

The XR-9030/9030R are bipolar monolithic integrated circuits commonly used in two terminal thin film recording head applications. The circuitry on the device includes a low noise preamplifier, write current control circuitry and data protection. It is available for both two and four channel applications. Power supply fault detection circuitry present on the device disables the write current generator in various power down modes. The read recovery time is improved by control of the read channel common mode output shift when in write mode. The read write device in the XR-9030R option offers internal 700 Ohm damping resistors.

The XR-9030 operates on a single 5V power supply making it ideal for low power applications. Both versions are available in a variety of low profile packaging options.

FEATURES

5V Supply Voltage Only
Low Power Device (150mW Typ in Read mode)
High Performance Circuitry
- -Low Input Noise = 0.85nV/$\sqrt{Hz}$ max
- -Read Mode Gain = 200V/V
- -Input Capacitance = 35pF max
- -Write Current Range = 2-35mA

Programmable Write Current Source
Write Unsafe Detect/Indicator
Power Supply Fault Protection
Head Short to Ground Protection
Enhanced Write to Read Recovery Time
Designed for Use With Two Terminal Thin Film Heads

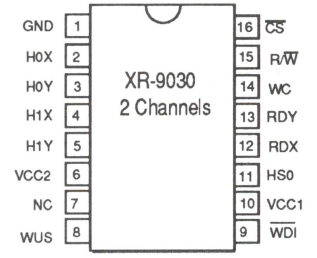
APPLICATIONS

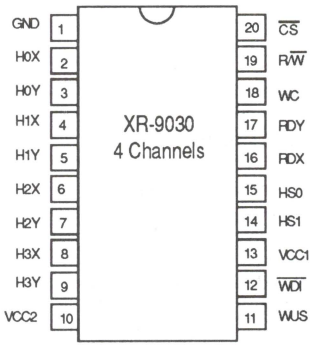
Thin Film Recording Heads in Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3 to +7 VDC
Write Current IW	80mA
Digital Input Voltage	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	-0.3 to VCC2 +0.3 VDC
Output Current Maximum	
Pins: RDX, RDY	±10mA
WUS	+12mA
Storage Temperature Range	-65°C to +150°C

PIN ASSIGNMENT





ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9030/9030R-4D	20 Pin SOP	0°C to 70°C
XR-9030/9030R-2D	16 Pin SOP	0°C to 70°C
XR-9030/9030R-4D	20 Pin SSOP	0°C to 70°C

SYSTEM DESCRIPTION

The XR-9030/9030R is a low power, two or four channel hard disk drive Read / Write preamplifier for thin film (2 terminal) heads. The XR-9030/9030R provides superior recording performance, and uses only a +5V power supply. Its low power consumption suits it for drives used in battery powered laptop computers. The read amplifier consists of a 60 MHz bandwidth 0.55 nV/$\sqrt{Hz}$ input noise (both typical) differential amplifier with a fixed gain of 200 V/V. The write driver has a current range of 2 to 35 mA and is disabled automatically when a voltage fault is detected. The write mode also has a write unsafe detection circuit.

ELECTRICAL CHARACTERISTICS

Test Conditions: L_H = 1.0µH R_H = 30 Ω, I_W = 20mA, f(Data) = 5MHz, $V_{CC1} = V_{CC2}$ = 5V ±5%

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INPUTS						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-400			µA	VIL = 0.8V
I_{IH}	Input High Current			100	µA	VIH = 2.0V
WUS VOL	WUS Output Low Voltage			0.5	V	I_{OL} = 2mA
VF	VCC1 Fault Voltage Fault to No Fault			4.2	V	Note 1
VF	VCC1 Fault Voltage No Fault to Fault	3.8			V	
WRITE CHARACTERISTICS						
Vwc	Write Current Voltage	1.15		1.35	V	
	Differential Head Voltage Swing	3.4			V	
	Unselected Head Current			1	mA pk	
	Head Differential Load Capacitance			25	pF	
	Head Differential Load Resistance	560	700	950		R Option
	Head Differential Load Resistance	4K				
	$\overline{WDI}$ Transition Frequency	1			MHz	I_W = 5mA
Iw	Write Current Range	2		35	mA	
READ CHARACTERISTICS Recommended operating conditions apply, unless otherwise stated. R_L(RDX,RDY) = 1KΩ, C_L(RDX,RDY) <20 pF, f = 5MHz						
Av	Differential Voltage Gain	160	200	240	V/V	
BW	Bandwidth -3dB	35	60		MHz	
eni	Equivalent Input Noise		0.55	0.85	nV/√Hz	BW= 15 MHz L_H= 0, R_H = 0
C_{IN}	Differential Input Capacitance			35	pF	
R_{IN}	Differential input Resistance	835	2K		Ω	
R_{IN}	Differential Input Resistance		700		Ω	R Option
	Dynamic Range to 90% of Gain	3			mV pp	
CMRR	Common Mode Rejection Ratio	45			dB	
PSRR	Power Supply Rejection Ration	40			dB	100mV_{pp} 5MHz sin on V_{CC}
	Channel Rejection Ratio	45			dB	Unselected channels driven with100mV_{pp} 5MHz sin
	Output Offset Voltage	-300		300	mV	
R_O	Single Ended Output Resistance			40	Ω	
I_O	Output Current	1.4			mA	AC coupled load, RDX to RDY
V_{CM}	Common Mode Output Voltage	2		3.5	V	

DC CHARACTERISTICS

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
$I_{CC}1$	VCC1 Supply Current			33	mA	READ Mode
				27	mA	WRITE Mode
				12	mA	IDLE Mode
$I_{CC}2$	VCC2 Supply Current			11	mA	READ Mode
				10+ IW	mA	WRITE Mode
				400	µA	IDLE Mode
P_D	Power Dissipation			230	mW	READ Mode
				190+4IW	mW	WRITE Mode
			35	45	mW	IDLE Mode

Note 1: On the Fault to No Fault transition, all devices will be No Fault at 4.2V.
On the No Fault to Fault transition, all devices will be Fault at 3.8V.

4

SWITCHING CHARACTERISTICS - Recommended operating conditions apply unless otherwise specified.
Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω, f(Data) = 5 MHz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	R/$\overline{W}$ Read to Write		0.1	1.0	µs	R/$\overline{W}$ to 90% of write current
	Write to Read		0.5	1.0	µs	R/$\overline{W}$ to 90% of 100mV 10 MHz Read signal envelope
	$\overline{CS}$ Unselect to Select		0.4	1.0	µs	$\overline{CS}$ to 90% of write current or to 90% of 100mV 10MHz Read signal envelope
	Select to Unselect		0.4	1.0	µs	$\overline{CS}$ to 10% of write current
	HS0,1 to any Head		0.2	1.0	µs	To 90% of 100mV 10MHz Read signal envelope
TD1	WUS: Safe to Unsafe	0.6	2.0	3.6	µs	
TD2	Unsafe to Safe		0.2	1.0	µs	
	Head Current:					Lh = 0, Rh = 0
TD3	$\overline{WDI}$ to Ix - Iy			32	ns	from 50% level
	Asymmetry			1.0	ns	$\overline{WDI}$ has 1 ns rise/fall time
	Rise/Fall Time			12	ns	10% to 90% level

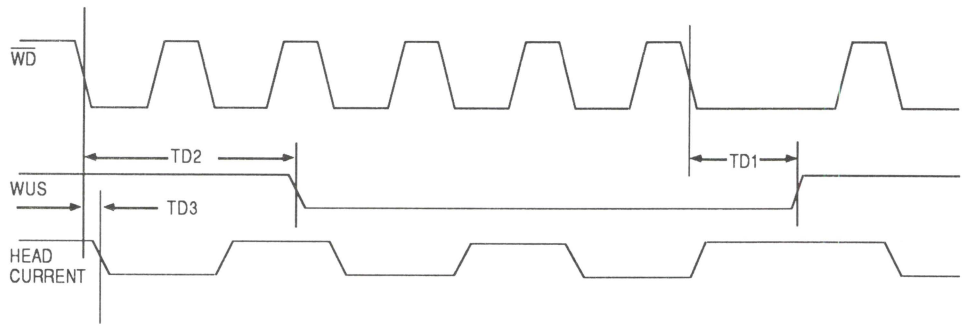


Figure 1. Write Mode Timing Diagram

PIN DESCRIPTION

Pin #	Symbol	I/O	Description
14,15	HS0,HS1	I	Head Select. Select one of four heads.
20	$\overline{CS}$	I	$\overline{\text{Chip Select}}$. High inhibits the chip.
19	R/$\overline{W}$	I	Read/$\overline{\text{Write}}$. High selects Read mode.
11	WUS*	O	Write Unsafe. High indicates an unsafe writing condition.
12	$\overline{WDI}$	I	$\overline{\text{Write Data In}}$. Changes the direction of the current in the recording head.
2,4,6,8 3,5,7,9	H0X-H3X; H0Y-H3Y	I/O	X,Y Head Connections
16,17	RDX, RDY*	O	X,Y Read Data. Differential read data output.
18	WC		Write Current. Used to set the magnitude of the write current.
13	VCC1	I	+5V Supply
10	VCC2	I	+5V Supply for Write current drivers.
1	GND	I	Ground

* *These signals can be wire OR'ed.*

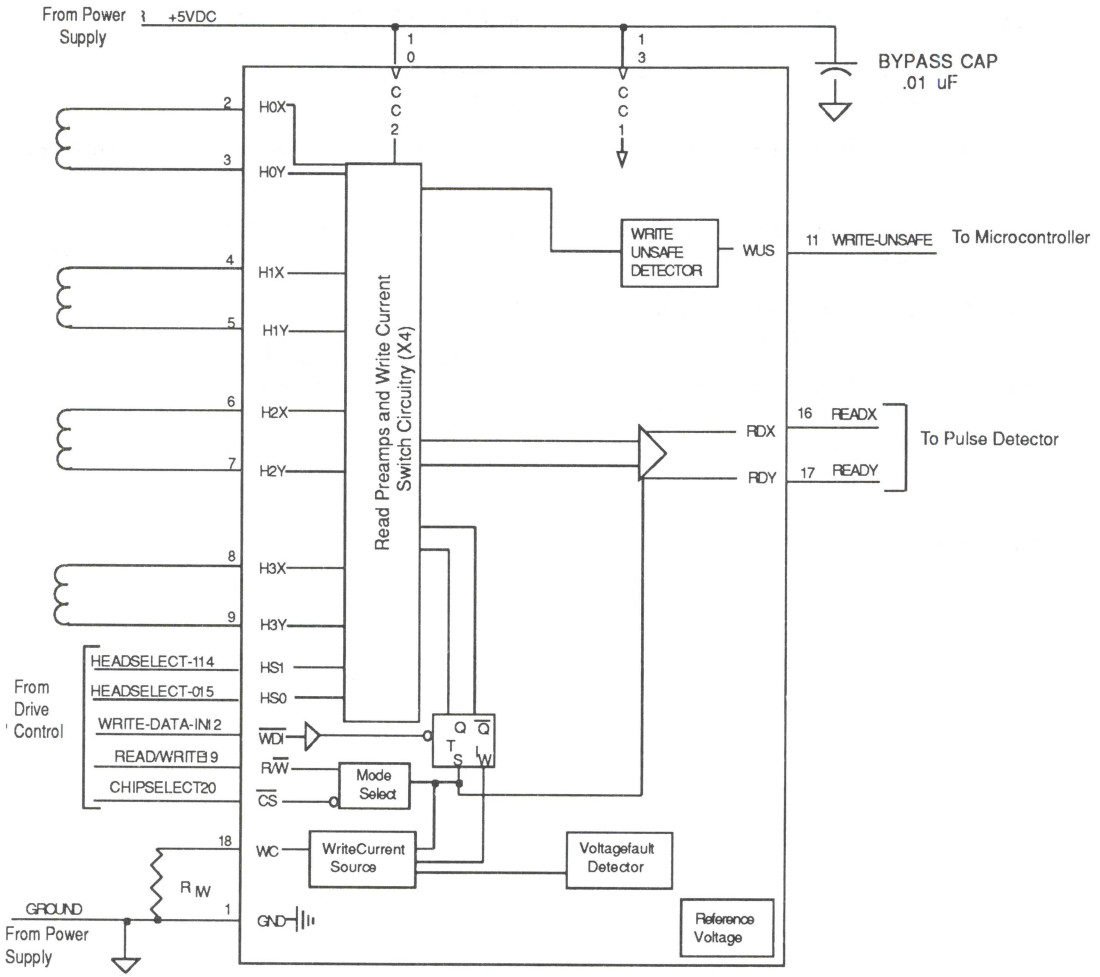


Figure 2. IC Interconnection and Block Diagram

CIRCUIT OPERATION

The XR-9030/9030R read/write device is intended for use in thin film head hard disk drives with up to four heads. Head selection and mode selection instructions are shown in Tables 1 and 2 respectively. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ protect from accidental write current by internal pull up resistors. HS0 and HS1 have internal pull down resistors. The pin descriptions are shown on page 4.

Read Mode

In read mode operation, the low noise preamplifier circuit reads and amplifies pulses detected on the disk surface caused by magnetic transitions in the media. In this mode write current operations are disabled. RDX and RDY are emitter follower outputs which provide differential read data output pulses. These should be AC coupled to the load. In Write mode and in Idle mode these outputs go into a high impedance state. This allows wire-oring of these outputs in multi-chip applications where more than four head capability is required.

Write Mode

Write mode is selected when both R/$\overline{W}$ and $\overline{CS}$ are taken low. The head current direction of the selected head is toggled by each negative going transition on the write data input pin, $\overline{WDI}$. A preceding read or idle mode select initializes the write data flip-flop to pass current through the X side of the head. This current is set by and external resistor, Rw, where:

$$Iw = \frac{Vwc}{Rw}$$

Rw is connected between the pins WC and GND. The actual head current is also a function of the head resistance and external wire resistance (Rh) and the damping resistance (Rd), so that:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

The write unsafe detector is also activated in this state.
The pin WUS is an open collector output which should be tied to VCC by a 2KΩ to 10KΩ resistor.

Idle Mode

This mode is selected by taking the pin $\overline{CS}$ high. The pins RDX and RDY are placed in a high impedance mode to minimize device power consumption and allow another chip to drive these common lines.

Voltage Fault

The write current function is disabled when either a voltage fault or power startup mode is detected, to avoid going into Write mode and contaminating the disks.
The following conditions will indicate a Write Unsafe, but will not stop the Write operation:

- -Device in Read Mode
- -Chip Disabled
- -$\overline{WDI}$ Frequency too Low
- -No Write Current
- -Head Opened

MODE DESCRIPTION

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

Table 1. Head Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

Table 2. Mode Select



NOTES



RLL (2,7) Data Separator

GENERAL DESCRIPTION

The XR-532A is high speed, low power, single +5V supply data separator for disk drive applications. Data Synchronization and RLL (2,7) encoding and decoding are provided. The XR-532A, combined with an Exar Read/Write Preamplifier and Pulse detector, provides a complete Read/Write electronics channel for magnetic storage systems.

The XR-532A is manufactured with a BiCMOS process, providing high speed, accurate timing, and low power consumption. It operates with a single +5V power supply and is available in 3 packaging configurations:

28 Pin PLCC
28 Pin SOIC
32 Pin PQFP

FEATURES

Low Noise, Low Jitter Data Synchronizer
High Speed RLL (2,7) ENDEC
Low Power Operation
Easily Adapted to Zoned Recording Applications
Hard or Soft Sector Compatible
Single +5V Supply
Advanced BiCMOS Technology

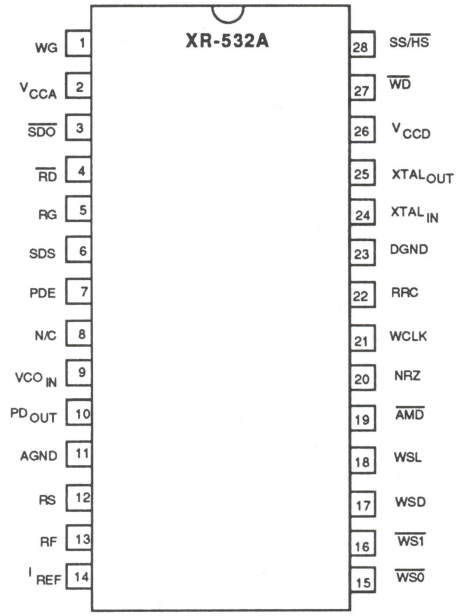
ABSOLUTE MAXIMUM RATINGS

V_{CCA}, V_{CCD}	7V
Digital Inputs	-0.3V to V_{CCD} +0.3V
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-532ACJ	28 Pin PLCC	0°C to 70°C
XR-532ACD	28 Pin SOIC	0°C to 70°C
XR-532ACQ	32 Pin PQFP	0°C to 70°C

PIN ASSIGNMENT (SOIC)



SYSTEM DESCRIPTION

The XR-532A is a 7.5 to 15 Mb/sec RLL (2,7) Data Synchronizer and ENDEC implemented in a low power BiCMOS process. This process allows independent optimization of the linear VCO and charge pump in high performance bipolar technology, while using fine geometry, low power CMOS for the numerous logic functions. The resulting device is faster than similar bipolar-only versions while dissipating less power. Only about 150mW of power is used during read operations.

Either hard sector or soft sector operation is supported.

The XR-532A data rate is adjusted with a single resistor. All necessary internal timings will track each other as this resistor value is changed, accommodating zoned recording applications.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C to 70°C, V_{CC} = 5.0V, 1/ TORC between 7.5 & 15MHz; 1/TVCO between 15 & 30 MHz.

Digital load capacitance limited to 15pF, 4.75 < V_{CC} < 5.25V, unless otherwise specified.

Typicals are measured with T_A = 25°C, V_{CCA} = V_{CCD} = 5.0V, 1/ TORC = 10MHz, 1/ TVCO = 20MHz.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
ICC	Supply Current		30	50	mA	
PD	Power Dissipation		150		mW	
DIGITAL SIGNALS						
VIL	Input "Low" Voltage			0.8	V	
VIH	Input "High" Voltage	2.0			V	
IIL	Input "Low" Current	-0.4			mA	VIL = 0.4V
IIH	Input "High" Current			10	µA	VIH = 2.7V
VOL	Output "Low" Voltage			0.4	V	IOL = 4mA
VOH	Output "High Voltage	2.8	4.8		V	IOH = -0.4mA
READ MODE						
	Maximum data rate	15	20		Mbit/sec	Host NRZ Data Rate
TRD	Read Pulse Width (Data)	20		TORC -40	ns	
TFRD	Read Data Fall Time			15	ns	2.0V to 0.8V
TRRC	Read Clock Rise Time			8	ns	0.8V to 2.0V
TFRC	Read Clock Fall Time			5	ns	2.0V to 0.8V
TPNRZ	NRZ Read Data Prop. Delay	-15		15	ns	
TPAMD	$\overline{AMD}$ Propagation Delay	-15		15	ns	
	1/4 Cell Delay + Timer	-4		4	%	
	1/4 Cell + Timer Delay Stability	0.91 TD	TD	1.09 TD	ns	See Note 1 @ T_A = 25°C V_{CC} = 5V
	1/4 Cell + Timer Delay	0.89 TD		1.11 TD	ns	
WRITE MODE						
TWD	Write Data Pulse Width	TORO/2 -12	TORO/2	TORO/2 +12	ns	
TFWD	Write Data Pulse Fall Time			8	ns	2.4V to 0.8V
TOWC	Write Clock Repetition	TORO -12	TORO	TORO +12	ns	
TRWC	Write Clock Rise Time			10	ns	0.8V to 2.4V
TFWC	Write Clock Fall Time			8	ns	2.4V to 0.8V
	NRZ Set-Up Time	20			ns	
	NRZ Hold Time	7			ns	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DATA SYNCHRONIZER						
TVCO	VCO Center Frequency Period	0.8TO	TO	1.2TO	sec	VCC = 5.0V Note 2
	VCO Frequency Dynamic Range	±25		±40	%	VCC = 5.0V Note 3
KVCO	VCO Control Gain	0.14 ω_o		0.23 ω_o	rad/sec/V	$\omega_o = 2\pi$ / TO Note 3
KD	Phase Detector Gain	0.83KD		1.17KD	A/rad	VCC = 5.0V Note 4
	KVCO x KD Product Accuracy	-28		+28	%	
	VCO Phase Restart Error	-0.5		+0.5	rad	
	Decode Window Centering Accuracy			±(0.01* TORC +2)	ns	
	Decode Window	(TORC/2)-2			ns	
TS1	Decode Window Time Shift Magnitude	0.60*TS1		1.4*TS1	sec	TS1 = 0.015 TORC
TS2	Decode Window Time Shift Magnitude	0.80 TS2		1.2*TS2	sec	TS2 = 0.06 TORC
TS3	Decode Window Time Shift Magnitude	0.80*TS3		1.2*TS3	sec	TS3 = 0.075 TORC
TSA	Decode Window Time Shift Magnitude	0.65*TSA		1.35*TSA	sec	Note 5
SWITCHING CHARACTERISTICS						
	TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set-Up Time	50			ns	
	THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time	20			ns	
	RG, WG, SS/$\overline{HS}$ Time Delay			100	ns	

Notes:

1) TD = 6.14 (R_{REF} + 0.5 KΩ) + 0.170 Rd (Cd +11.5) with Cd from 65pF to 100pF. R_d & R_{REF} in KΩ .
   C_d = 82pf (7.5 ~11MB) and C_d = 65pf (10~15MB) .
2) VCO In = 2.7V, TO = 11.3 (R_{REF} +500Ω) x 10^{-12}.
3) VCO In from 1V to VCC -0.5V.
4) KD = 0.409 / (RREF + 500Ω)
5) TSA = 0.125 TORC $\left[1- \left[\frac{R + 680}{R + 1180} \right] \right]$ R in Ohms, connected between RF/RS and AGND

PIN DESCRIPTION

(Pin # refers toPLCC /SOIC Packages)

Pin #	Name	Description
POWER PINS		
2	V_{CCA}	+5V for Analog Circuitry
26	V_{CCD}	+5V for Digital Circuitry
11	AGND	Analog Ground
23	DGND	Digital Ground
CONTROL PINS		
1	WG	Write Gate Control. Enables write mode. Internal pull-up resistor provided.
5	RG	Read Gate Control. Enables read mode. When low, the internal VCO is locked to the crystal oscillator. When high, the PLL synchronizes to Read Data (RD). Internal pull-up resistor provided.
6	SDS	Sync Detect Set. The R/C node here determines the one-shot timer period used for synchronization detection.
7	PDE	Phase Detector Enable. When low, the VCO free-runs. When high, the VCO receives the phase detector control voltage. Internal pull-up resistor provided.
9	VCO IN	VCO Input Control Voltage. Phase Detector control voltage applied here, determines VCO frequency.
12	RS	Symmetry Adjust Slow Resistor. Resistor from here to AGND (Pin 11) can eliminate window symmetry offset and maximize window margin.
13	RF	Symmetry Adjust Fast Resistor. Resistor from here to AGND (Pin 11) can eliminate window symmetry offset and maximize window margin.
14	IREF	Reference Current Set. A resistor from here to VCCA determines reference current, which sets VCO center frequency and anticipator (1/4 cell) delay.
15	$\overline{WS0}$	When low, this pin digitally provides a 1.5% TORC window shift. Internal pull-up resistor.
16	$\overline{WS1}$	When low, this pin digitally provides a 6% TORC window shift. Internal pull-up resistor.
17	WSD	Window Shift Direction. When low, shifts the window early by an amount determined by $\overline{WS0}$ (Pin 15), and $\overline{WS1}$ (Pin 16). When high, the window is shifted late. Internal pull-up resistor provided.
18	WSL	Window Shift Latch. When high, latches the window shift in the mode determined by WSD (Pin 17), $\overline{WS0}$ (Pin 15), and $\overline{WS1}$ (Pin 16). When window shift is not needed, this pin should be tied low. Internal pull-up resistor provided.

Pin #	Name	Description
24	**XTAL IN**	Crystal Oscillator Input. Also used as the external clock input (TTL compatible).
25	**XTAL OUT**	Crystal Oscillator Driver. When an external clock is employed, this pin must remain open.
28	**SS/$\overline{HS}$**	Soft Sector / $\overline{\text{Hard Sector}}$ Select. When low, hard sector mode is selected. High chooses soft sector mode. Internal pull-up resistor provided.

INPUT/OUTPUT PINS

Pin #	Name	Description
3	**$\overline{SDO}$**	$\overline{\text{Sync Detect Output}}$. Goes low when 3T preamble sync field is detected.
4	**$\overline{RD}$**	$\overline{\text{Read Data Input}}$. TTL level, asserts low. Composite read data from the pulse detector enters here.
10	**PDOUT**	Phase Detector Output. The PLL filter placed here conditions the phase detector output before application to VCO IN.
19	**$\overline{AMD}$**	$\overline{\text{Address Mark Detect Output}}$. In the soft sector mode, successful address mark detection is signaled by a latched low AMD output.
20	**NRZ**	NRZ Data Input/Output Pin. This bidirectional I/O pin inputs write data and outputs read data, depending on device mode. CMOS compatible.
21	**WC**	Write Clock Input. Clock input for NRZ write data.
22	**RRC**	Read Reference Clock Output. In read mode, this is the NRZ read data clock. In the write mode, this output is the crystal reference divided by two.
27	**$\overline{WD}$**	$\overline{\text{Write Data Output}}$. Active low encoded RLL write data, directly compatible with all Exar read/write amplifiers.

RG	WG	Mode
0	0	Idle
0	1	Write
1	0	Read
1	1	Illegal

Table 1. Digital Control Modes

WSD	WS1	WS0	Window Shift
0	0	0	+TS3
0	0	1	+TS2
0	1	0	+TS1
0	1	1	0
1	1	1	0
1	1	0	-TS1
1	0	1	-TS2
1	0	0	-TS3

Table 2. Delayed Data Shift Control

RLL (2,7)	NRZ
0100	10
1000	11
000100	000
100100	010
001000	011
00100100	0010
00001000	0011

Table 3. (2,7) RLL Conversion

GENERAL OPERATION

The XR-532A is designed to perform data recovery and data encoding in disk drives using 2,7 RLL encoding. In the Read Mode the XR-532A performs: Data Synchronization, Clock Recovery, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the XR-532A converts NRZ data into 2,7 RLL, generates the Preamble Field, and inserts Address Marks (as requested).

The XR-532A can operate with data rates ranging from 7.5 to 20 Mbits/sec. This data rate is established by a single external resistor, RREF, connected from IREF to V_{CCA}. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$R_{REF} = \frac{40670}{D} - 500\ (\Omega)$$

with RREF is in Ohms,
where: D = Data Rate in Mbits/sec.

An internal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTALIN and XTALOUT should operate at twice the data rate. Alternatively, an external TTL compatible reference clock may be applied to XTALIN, leaving XTALOUT open.

The XR-532A employs a dual mode phase detector: its operation is harmonic in the read mode and non-harmonic in write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false frequency locking to DLYD DATA in read acquisition is eliminated.

The phase detector incorporates a charge pump that drives the loop filter. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 shows average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

WRITE MODE

In the Write Mode the XR-532A converts NRZ data from the controller to 2,7 RLL formatted data for writing to disk. The XR-532A can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SS/$\overline{HS}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2,7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SS/$\overline{HS}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the XR-532A and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. In many configurations, WCLK can be connected directly to the RRC output.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the XR-532A automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark, the XR-532A changes the '1' in the eleventh position of the 2,7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2,7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the XR-532A automatically generates the 4T (1000) Preamble Field at the Write Data, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11...' input which generates the 4T

'1000...' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The XR-532A needs at least 32 4T (1000) bit groups prior to the data field.

READ MODE

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the RD input and a low level selects the crystal reference oscillator.

In Read Mode the rising edge of the internal signal DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a nominal 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of RD. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay does not influence the accuracy of the decode window.

The relative position of the DYLD DATA pulse can be shifted within the decode window. This powerful capability easily facilitates defect mapping, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In applications not utilizing this feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts of ±1.5%, ±6, or ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late data bit positions within the decode windows respectively, as depicted in Figure 3. If window shifts are selected, the trailing edge of DLYD DATA will not appear phase locked to the falling edge of the VCO clock. See figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC \left[1 - \left[\frac{680 + R}{1180 + R} \right] \right]$$

where: R is in Ohms.

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In non-read modes, the PLL is locked to the crystal reference oscillator. This tunes the VCO at a frequency which is very close to that required for read back of actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment. In this manner (phase error ≤0.5 rads), the acquisition time is substantially reduced.

The XR-532A provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. When RG transitions high, the counter is reset and the XR-532A requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled. See Figure 4.

a). PREAMBLE SEARCH:

After RG is enabled the 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing

capacitor is included on-chip and its timing is externally set by resistor R_{REF}. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time-out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) PLL LOCKING:

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquisition begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

c) ADDRESS MARK DETECTION:

The circuit searches for the occurrence of the 5EAx16 Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the AMD output is latched low, the PLL acquisition sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL input is put back to the crystal reference oscillator, and the RRC output is switched to the crystal reference oscillator divided by 2. PLL acquisition sequence is restarted when the Input Counter reaches count 96. See Figure 4 and 5.

Additionally, if a non-3T pattern is detected during the Address Mark, search another part of the circuit is activated. This circuit expects to find an Address Mark within 24 VCO clocks after detecting the non-3T pattern. If an Address Mark is not detected during this period, the search for AM is aborted and the PLL acquisition sequence is restarted as described above, within three VCO cycles.

HARD SECTOR MODE

In the Hard Sector mode ($SS/\overline{HS}$ = 0) the XR-532A utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read. See Figure 6.

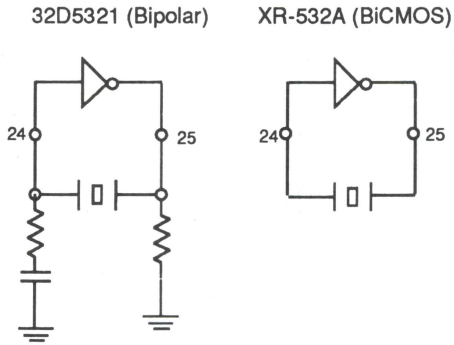
In the Hard Sector Mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

APPLICATION COMPARISON

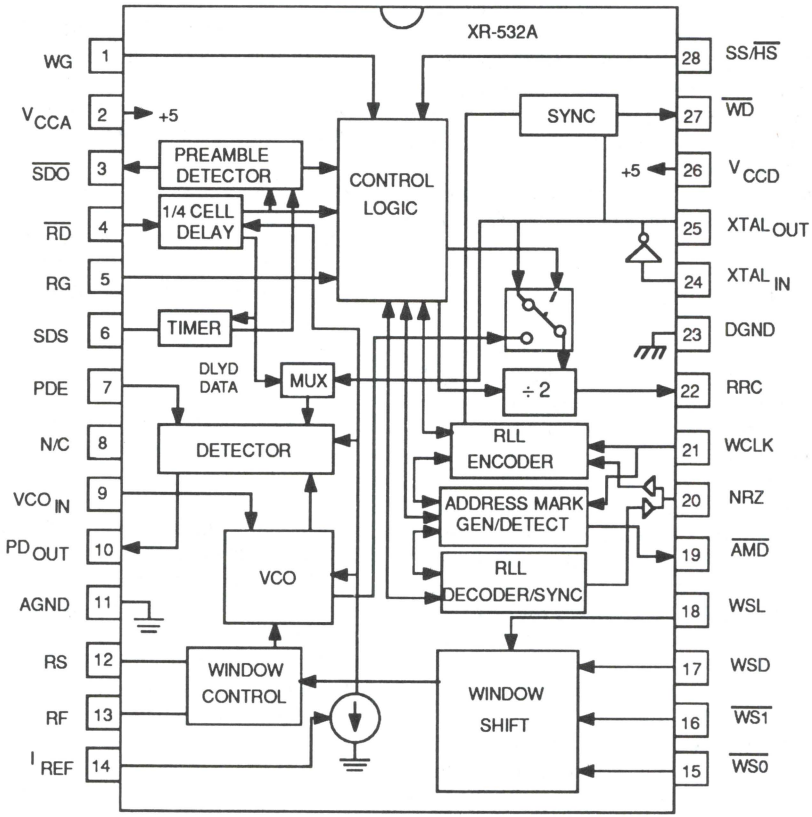
The XR-532A is pin-for-pin compatible with the SSI 32D5321. In most applications, improved performance will result when the XR-532A is employed, without any circuit changes. The XR-532A is a BiCMOS device and the SSI 32D5321 is a bipolar device. Application differences will include:

- XR-532A power consumption is only 150mW at 10MB/sec., compared to the approximately 750mW burned by the 32D5321.

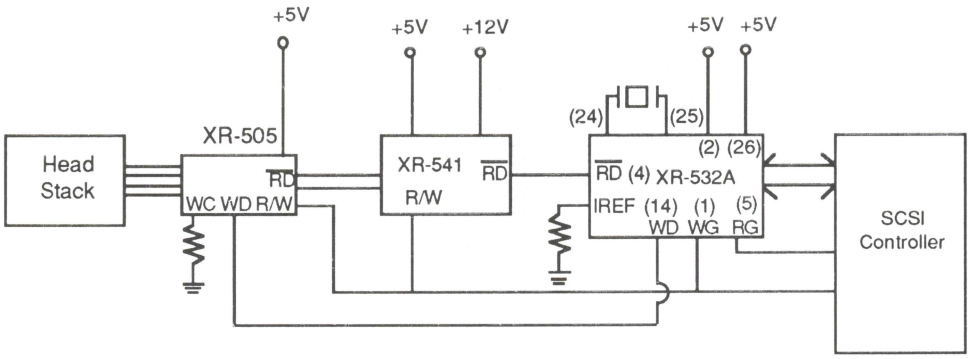
- XR-532A eliminates the need for the two resistor, one capacitor crystal oscillator start-up circuit required for 10MB/sec and faster operation with the 32D5321. This reduces circuit complexity and cost. In fact, these components, if used will cause problems with the higher impedance CMOS inverter, and should be removed (see drawing below). If an external clock is supplied, no change is required (see diagram next page).



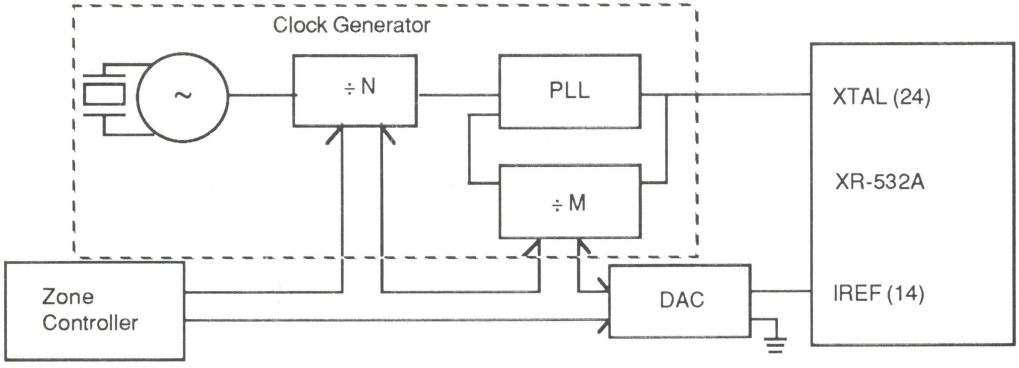
Crystal Oscillator Circuits



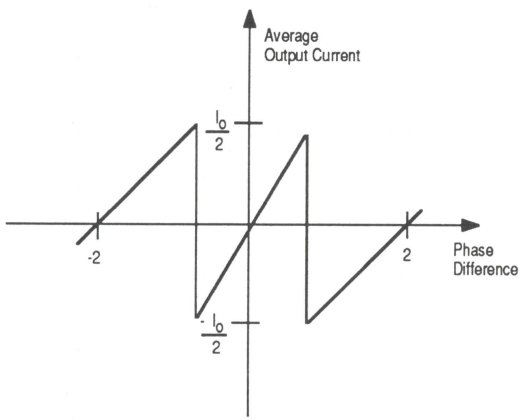
XR-532A Functional Block Diagram



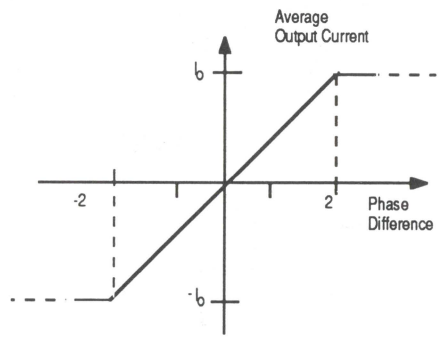
Simple SCSI Disk Drive Read/Write channel with the XR-532A



Zoned Recording Implementation



Harmonic Mode



Non-Harmonic Mode

Notes: 1. Io is the magnitude of the charge pump current
2. Phase error is relative to the VCO period

Figure 1. Phase Detector Transfer Characteristics

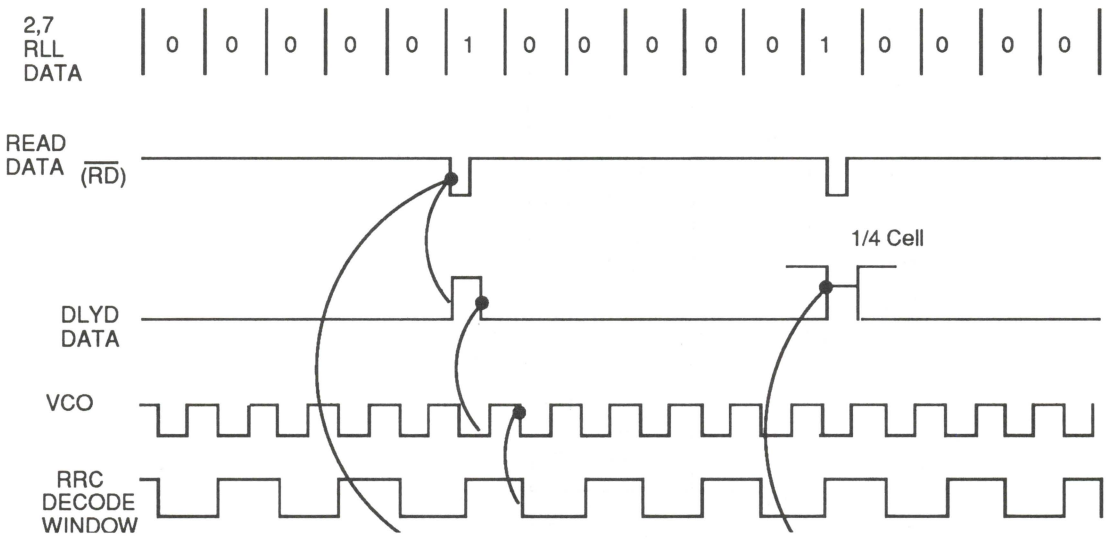
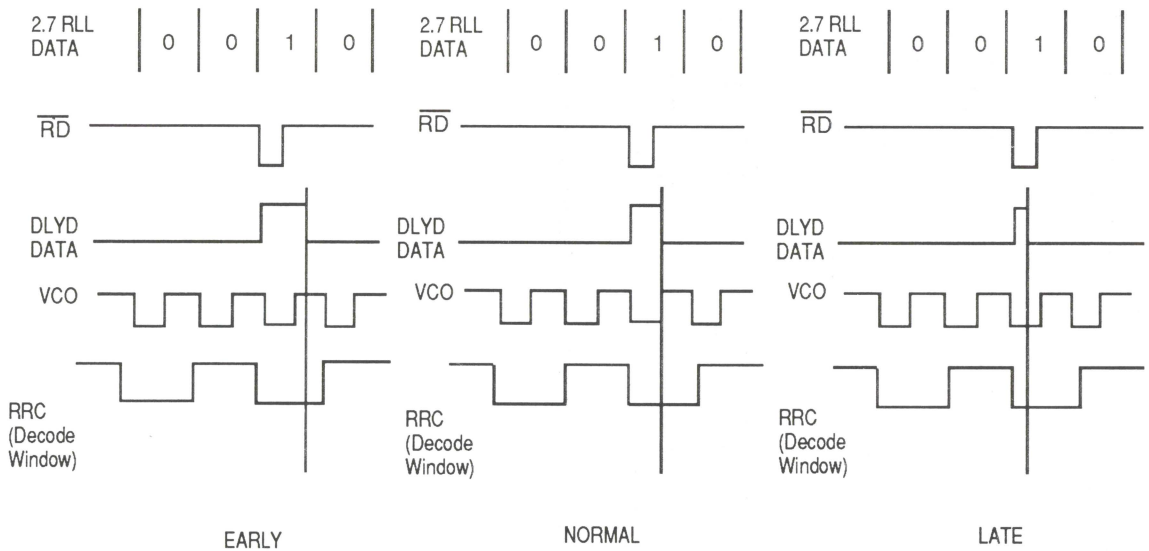
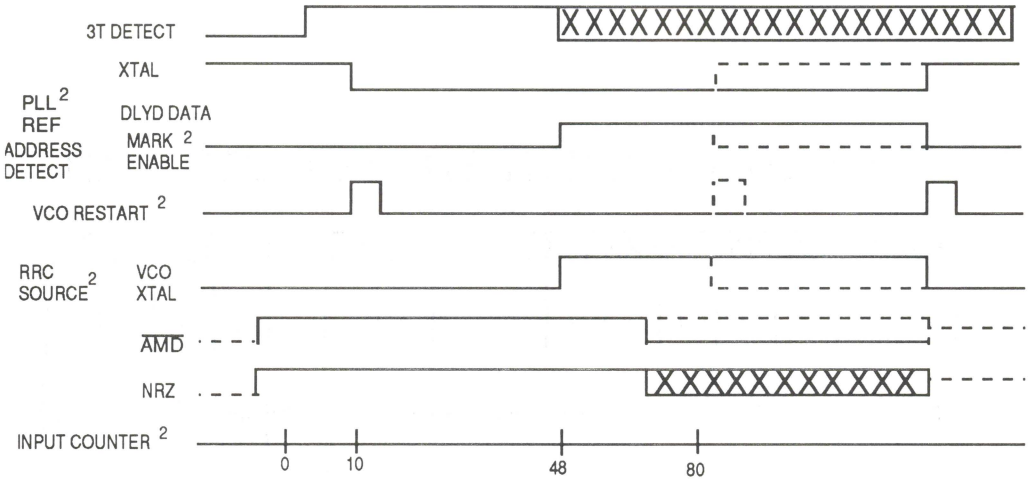


Figure 2. Read Mode Delayed Data / VCO Phase Comparison



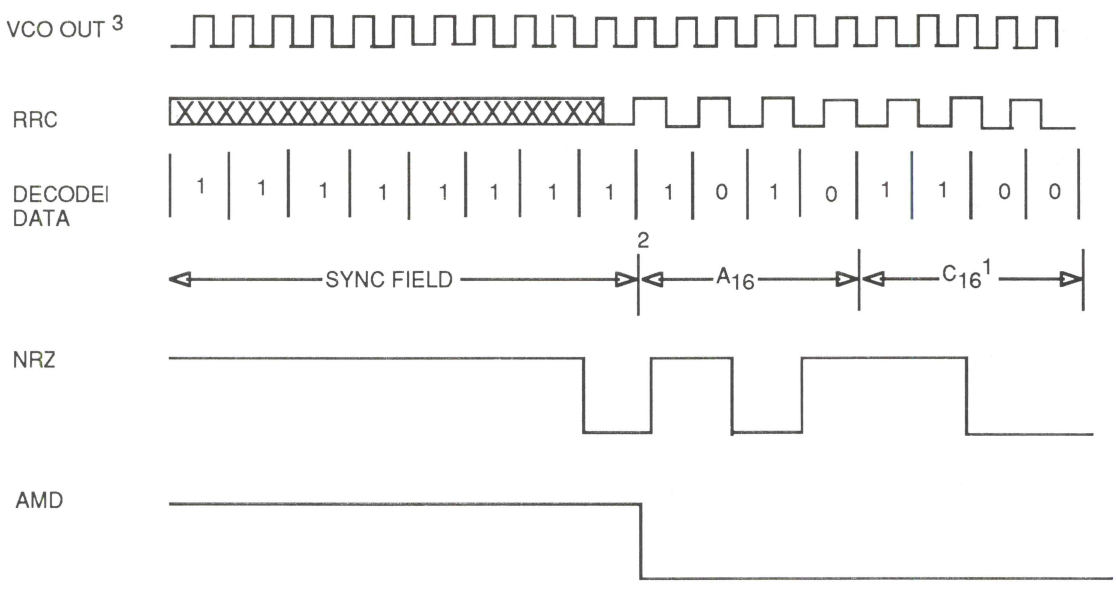
DLYD DATA width is adjusted by Window Shifting.
Width adjustment is exaggerated for clarity.

Figure 3. Decode Window Shifting Using WS* Controls



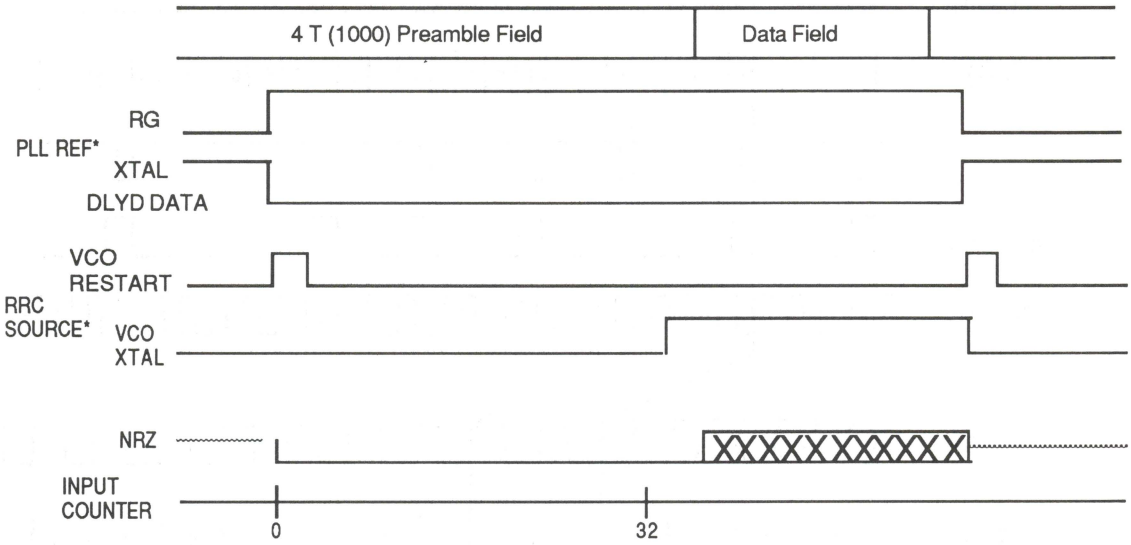
Notes:
1. Dashed lines represent conditions where the Address Mark was not found.
2. Representations of internal signals
3. Dotted lines represent a high impedance output state

Figure 4. Read Mode Soft Sector Preamble Search and Address Mark Detection



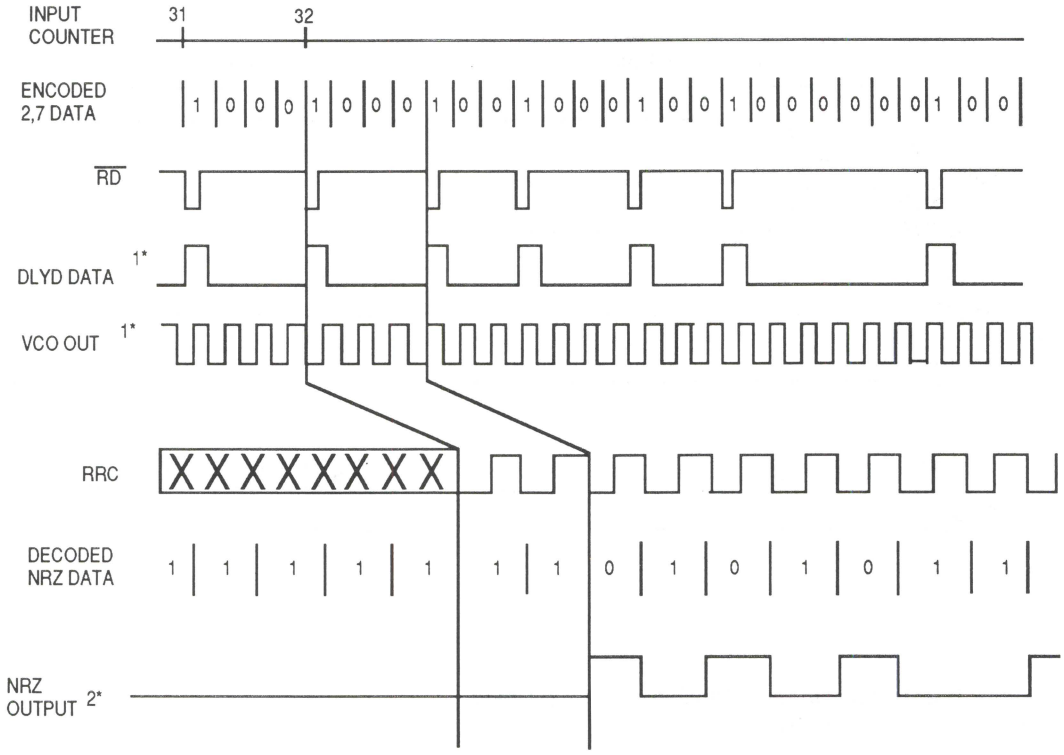
Notes: 1. These four bits can be any combination. C (1100) was selected in this example.
2. The $5E_{16}$ of the $5EAx_{16}$ Address Mark is not read back.
3. Internal signal

Figure 5. Read Mode, Soft Sector Address Mark Detection



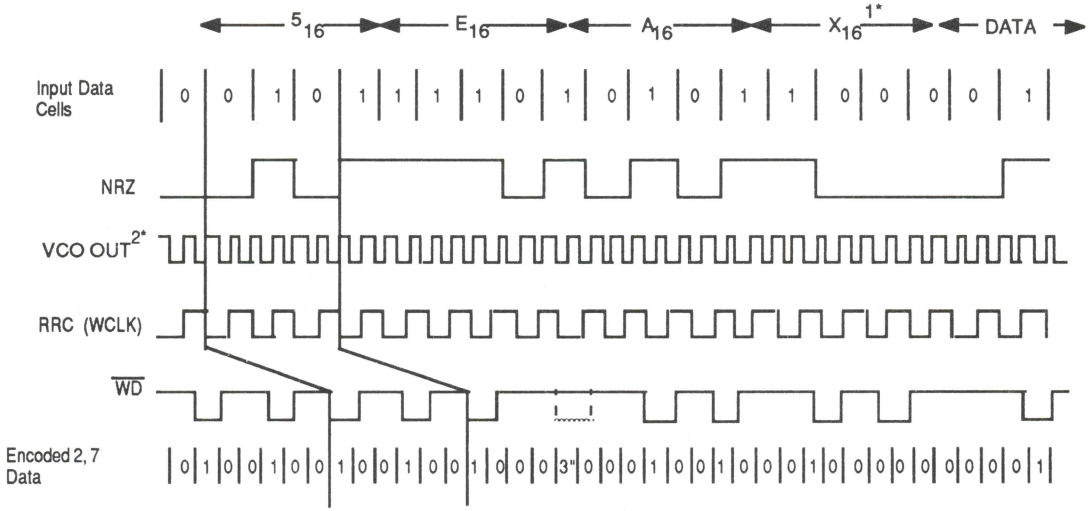
Note: Dashed lines represent a high impedance output state.
* - internal signal

Figure 6. Read Mode Hard Sector PLL Acquisition Sequence



Notes: *1. Representations of internal signals
*2. In hard sector mode the NRZ output is inverted

Figure 7. Read Mode Hard Sector Read Reference Clock Switching



Notes: *1. X16 can be any combination, C16 (1100) was selected in this example
*2. Representations of internal signals
*3. Deleted output pulse to encode Address Mark

Figure 8 Write Mode Soft Sector Address Mark Write Data Encoding

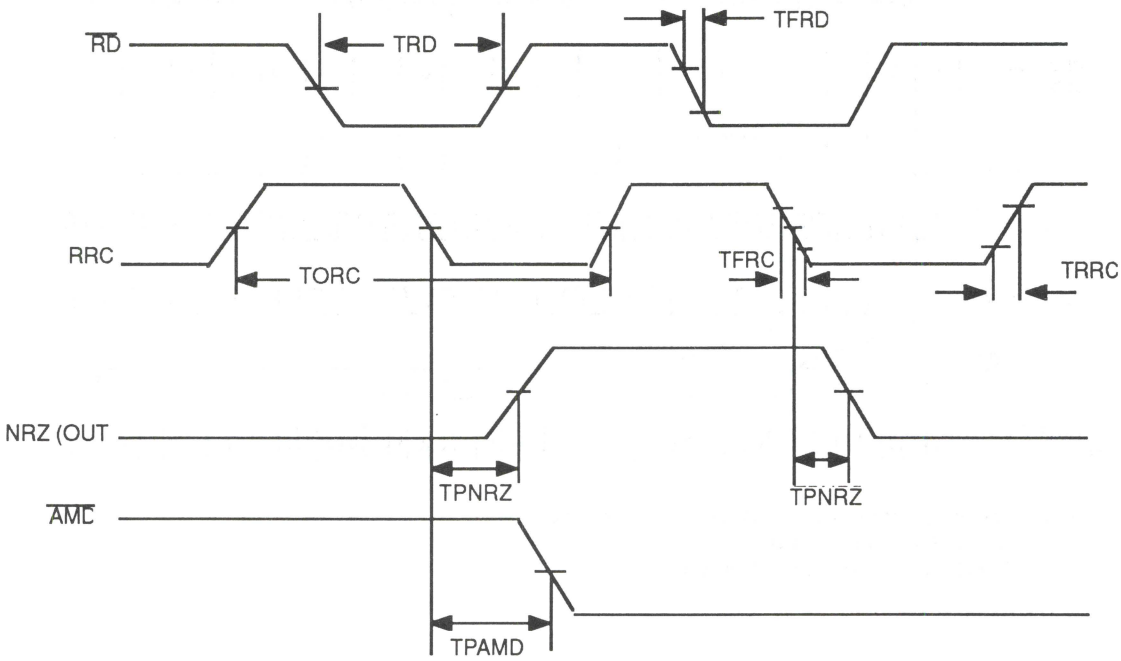


Figure 9. Read Timing Definition

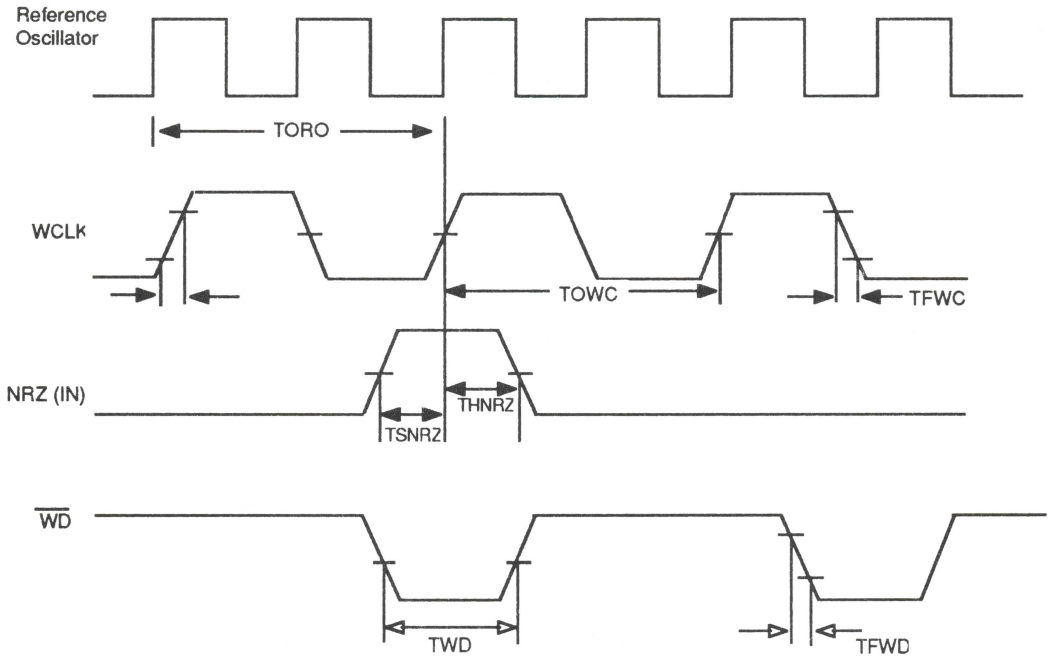


Figure 10. Write Timing Definitions

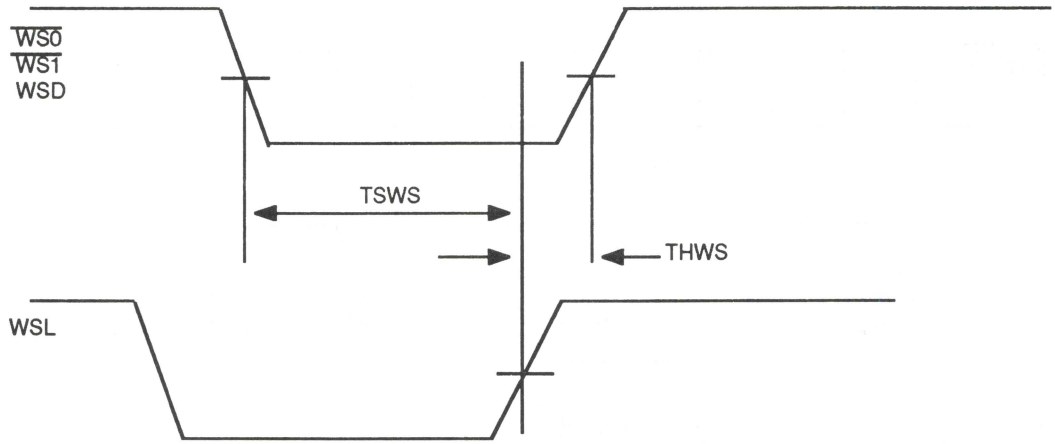
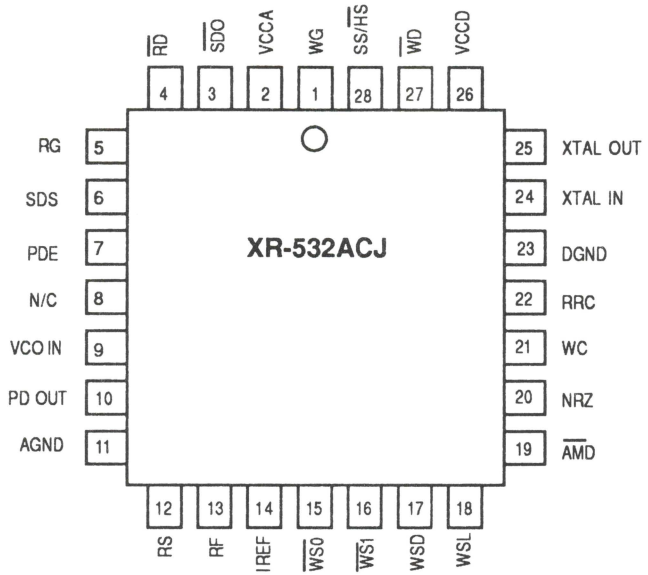
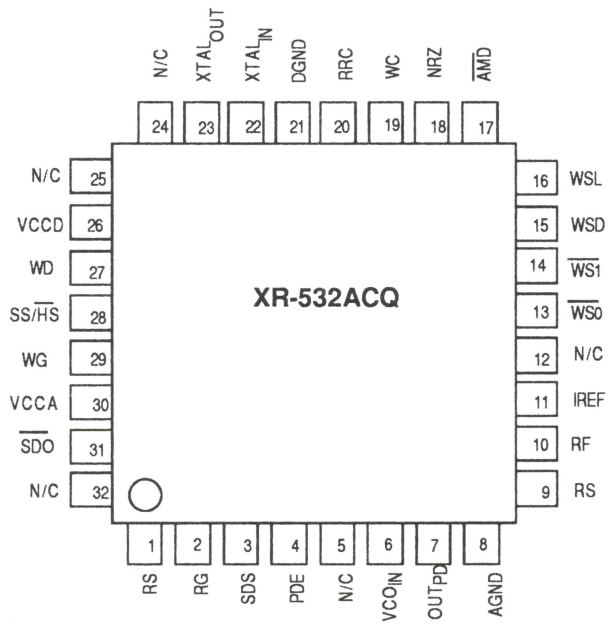


Figure 11. Window Shift Controls Timing Definitions


RD
SDO
VCCA
WG
SS/HS
WD
VCCD
4
3
2
1
28
27
26
RG 5
SDS 6
PDE 7
N/C 8
VCO IN 9
PD OUT 10
AGND 11
25 XTAL OUT
24 XTAL IN
23 DGND
22 RRC
21 WC
20 NRZ
19 AMD
XR-532ACJ
12
13
14
15
16
17
18
RS
RF
IREF
WS0
WS1
WSD
WSL


N/C
XTALOUT
XTALIN
DGND
RRC
WC
NRZ
AMD
24
23
22
21
20
19
18
17
N/C 25
VCCD 26
WD 27
SS/HS 28
WG 29
VCCA 30
SDO 31
N/C 32
16 WSL
15 WSD
14 WS1
13 WS0
12 N/C
11 IREF
10 RF
9 RS
XR-532ACQ
1
2
3
4
5
6
7
8
RS
RG
SDS
PDE
N/C
VCOIN
OUTPD
AGND



NOTES



Hard Disk Pulse Detector

GENERAL DESCRIPTION

The XR-541 is a disk drive Pulse detector designed for use with RLL and MFM coding schemes. Signals from the read/write preamplifier are qualified by an amplitude verifying gating threshold before constant width pulses are output.

The XR-541 is available in 24 Pin Plastic DIP, JEDEC S.O., and 28 Pin PLCC packages. It employs +5V and +12V supplies.

FEATURES

RLL and MFM Decoding
High Performance AGC Preamplifier
Adjustable Detection Threshold
Wide Dynamic Range
Compatible with Embedded Servo
Separate Analog and Digital Grounds
TTL Level Output and Control
Replaces SS1541 Read Data Processor

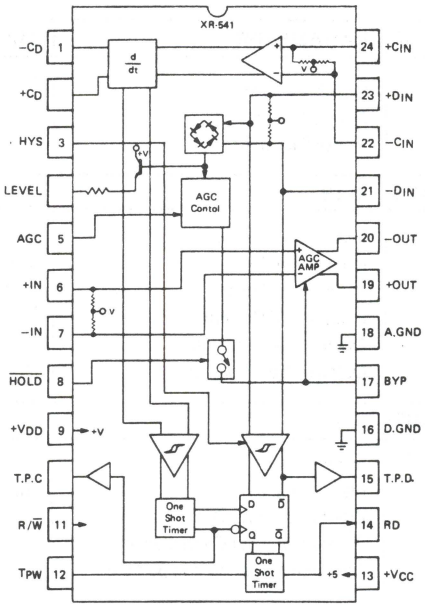
APPLICATIONS

Winchester Disk Drives
Removable Cartridge Disk Drives

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
V_{CC}	6.5V
V_{DD}	14.0V
Storage Temperature	-65°C to l50°C
Operating Junction Temperature	150°C
Power Dissipation	
24 Pin Plastic DIP	1W
Derate Above 25°C	8mW/°C
24 Pin JEDEC SO	1W
Derate Above 25°C	8mW/°C
28 Pin PLCC	1W
Derate Above 25°C	8mW/°C
TTL Input Voltage	-0.3V to 5.5V
Differential Input Signal	+/-3.3V

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-541-1CP	24 Pin DIP/1ns	0°C to 70°C
XR-541-1CJ	28 Pin PLCC/1ns	0°C to 70°C
XR-541-1D	24 Pin S.O./1ns	0°C to 70°C
XR-541-3CP	24 Pin DIP/3ns	0°C to 70°C
XR-541-3CJ	28 Pin PLCC/3ns	0°C to 70°C
XR-541-3D	24 Pin S.O./3ns	0°C to 70°C

SYSTEM DESCRIPTION

Signal from the disk head preamplifier are A.C. coupled into the XR-541. A low pass filter may be employed here to reduce system bandwidth and noise. The input amplifier is AGC controlled, allowing reliable operation with signal levels ranging from 20 mV to 660 mV p-p. A low pass filter removes unwanted components as the signal enters the differentiator and level detection threshold circuitry. Only when the signal rises above this user adjustable threshold is the output one-shot timer enabled.

Detection threshold is set by the voltage on the HYS Pin. Test points are provided for alignment of the delays from the clock input and the gating flip-flop. Dual grounds reduce coupling between the digital sections and the low level signal inputs.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°, V_{CC}= 5V, V_{DD} = 12V, R/$\overline{W}$= High (>2.0V). Unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current		4	14	mA	V_{CC} = 5.5V
I_{DD}	Supply Current		50	70	mA	V_{DD} = 13.2V
P_D	Power Dissipation		600	730	mW	
DIGITAL SIGNALS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input "Low" Current	-0.4			mA	V_{IL}= 0.4V
I_{IH}	Input "High" Current			100	µA	V_{IH}=2.4V
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL}= 4mA $\overline{RD}$ Output
V_{OH}	Output "High" Voltage	2.4			V	I_{OH}=-0.4mA $\overline{RD}$ Output
AGC AMPLIFIER						
$A_V$min	Minimum Gain		0.1	4	V/V	Differential V_{OUT} from 1.0V
A_{Vmax}	Maximum Gain	83	250		V/V	to 2.5Vp-p
R_{IN}	Differential Input Resistance		5		KΩ	
C_{IN}	Differential Input Capacitance			10	pF	
Z_{IN}	Common Mode Input Impedance		1.8		KΩ	R/$\overline{W}$ ≥ 2.4V BothSides
			250	500	Ω	R/$\overline{W}$ ≤ 0.8V Both Sides
e_{ni}	Input Noise Voltage			30	nV/√Hz	Az=maximum:15MHz bandwidth
BW	Preamplifier Bandwidth	30	60		MHz	Av = maximum: -3dB point
CMRR	Common Mode Rejection Ratio	40	60		dB	V_{IN} = 100mVp-p at 5 MHz. Av = Max.
PSRR	Power Supply Rejection Ratio	30	40		dB	ΔV_{CC} or ΔV_{DD} = 100mV Vp-p at 5 MHz. Av = Max
Vout	Output Voltage Swing	3.0	6		Vp-p	R_L≥600Ω Differential. V_{AGC} = 5.5V
Iout	Output Current Swing	13.2	14		mA	
R_O	Output Resistance			32	Ω	
C_O	Output Capacitance			15	pF	
V_{DIN}	V(DIN+) - V(DIN-) Voltage Swing	370	480	560	mVpp/	V_{IN} From 30mVp-p to 550mVp-p
$\overline{V_{AGC}}$	-vs-V_{AGC}				V	V(DIN+) -V(DIN-) From 500Vp-p to 1.5Vp-p
ΔVDIN / $\overline{V_{AGC}}$	V(DIN+) - V(DIN-) Change		1	8	%	VAGC = constant. V_{CC} 110%, V_{DD}±10%. T_AFrom 0°C to 70°C.
I_{AGC}	AGC Fast Charge Current	1.3	1.6	2.0	mA	V(DIN+) - V(DIN-) = 1.6V
I_{AGC}	AGC Slow Charge Current	140	180	220	µA	V(DIN+) - V(DIN-) = 1.6V. VAGC
	Fast to Slow Attack Switching Point		1.25		—	$\frac{V_{DIN}\text{ (initial)}}{V_{DIN}\text{ (Final)}}$
	AGC Capacitor Discharge Current		4.5		µA	Operate (HOLD="High")V_{DIN}=0
		-200	-	200	nA	Hold (HOLD="Low")V_{DIN}=0
t_A	AGC Attack Time		4		µs	Note 1.
t_D	AGC Decay Tvm		50		µs	Note 2.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
WINDOW THRESHOLD COMPARATOR						
R_{IN}	Differential Input Resistance	5		11	KΩ	
C_{IN}	Differential Input Caparitance			6	pF	
Z_{IN}	Common Mode Input Impedance		2		KΩ	V_{HYS} = 0V. R(DIN+ to DIN-)≤1.5KΩ
V_{OS}	Threshold Comparator Offset Voltage	-10		10	Mv	
	Peak Window Threshold Voltage -vs-V_{HYS}	0.16	0.22	0.25	V/V	V_{DIN} Referred. V_{HYS} From 1V to 3V.
I_{HYS}	HYS Pin Input Currernt	-20		0	µA	V_{HYS} From 1V to 3V.
V_{LEVEL}	V_{LEVEL} -vs- V_{DIN}	1.5	2.0	2.5	V/Vp-p	V_{DIN} From0.6V to 1.3Vp-p 10KΩ Load to Ground
I_{LEVEL}	LEVEL Maximum Output Currernt	3.0			mA	
R_O(LEVEL)	LEVEL Output Resistance		180		Ω	I_{LEVEL} = 500mA
V_{OLD}	Test Point D Output Low Voltage	V_{DD} -4		V_{DD} -2.8	V	|IOL|≤500mA
V_{OHD}	Test Point D Output High Voltage	V_{DD} -2.5		V_{DD} -1.8	V	$\|I_{OH}\|$≤ 500mA
DIFFERENTIATOR						
R_{IN}	Differential Input Resistance	5.8		11	KΩ	$\|V_{CIN}\|$ = 100mVp-p at 2.5 MHz
CIN	Differential Input Capacitance			6	pF	$\|V_{CIN}\|$= 100mVp-p at 2.5 MHz
A_{VD}	Differentiator Preamp Gain	1.7	1.8	2.2	V/V	V_{DIF}/V_{CIN}: R_{DIF} = 2kΩ
Z_{IN}	Common Mode Input Impedance		2		KΩ	
V_{OS}	Differentiator Offset Voltage	-10		10	mV	Capacitive Differentiator Network
I_D	Differentiator Drive Current	11.3			mA	
V_{OLc}	Test Point "C" Output Low Voltage		V_{DD}-3.0		V	$\|I_{OL}\|$≤ 500mA
Voc	Test Point "C" Output		400		mVp-p	$\|I_{OL}\|$,$\|I_{OH}\|$≤ 500mA
t_c	Test Point "C" Pulse Width		30		ns	$\|I_{OH}\|$≤ 500mA
CONTROL TIMING						
T_{W-R}	Write to Read Transition Time	1.2	2	3.0	µs	Transition to High R_{IN}.
T_{R-W}	Read to Write Transition Time		0.25	1.0	µs	
T_{R-H}	Read to Hold Transition Time			1.0	µs	
DYNAMIC DATA CHARACTERISTICS						
	Additional Test Conditions: V_{CIN},V_{DIN}=1.0Vp.p2.5MHz Sine Wave,V_{HYS}=1.8V,C_D=65pF, R_D=100Ω,C_{pw}=60pF, $\overline{RD}$ is loaded with 4KΩ to +V_{cc} & 10pF to GND. Refer to Figure 2, Figure 3 and Figure 4					
T_{D1}	D Flip-Flop Set Up Time	0			ns	Delay from V_{DIN} Passing threshold to V_{DIF} Peaking
T_{D3}	Propagation Delay		65	110	ns	Delay from V_{DIN} = V_{CIN} Peaking to $\overline{RD}$ out.
PP	Pulse Pairing			1	ns	XR-541-1 (Note 3)
				3	ns	XR-541-3 (Note 3)

4

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
T_{PW}	Output Data Pulse Width Accuracy	-15		15	%	Error from T_{PW}= 0.67 C_{PW}: C_{PW} from 50pF to 200pF
T_r	Output Rise Time		7	14	ns	To V_{OH} = 2.4V
T_f	Output Fall Time		6	18	ns	To V_{OL} = 0.4V

NOTE 1: Time from Write to Read transition to V_{OUT} reaching 110% of final value using 400mV_{p-p} 2.5 MHz sine wave.
(See Figure 1A, Figure 1B.)

NOTE 2: Time from Vin dropping from 300mV_{p-p} to 150mV_{p-p} to V_{OUT} recovering within 90% of final value using 2.5MHz sine wave.
(See figure 1C, Figure 1D.)

NOTE 3: Pulse Pairing as defined as: $\frac{1}{2}\left[\frac{Tpp1 - Tpp2}{Tpp1 + Tpp2}\right]$
as shown in Figure 3.
Circuit is as shown in Figure 4. $V_{CIN} = V_{DIN}$ = 1Vp-p 2.5 MHz sine wave.

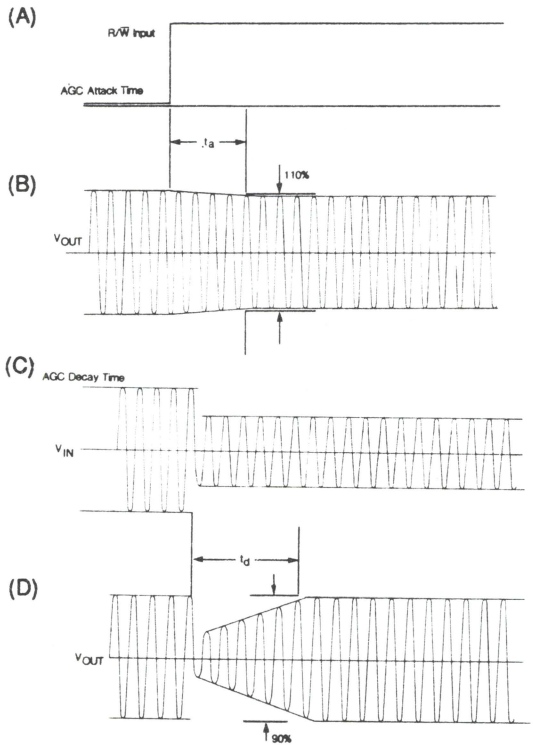


Figure 1. XR-541 AGC Characteristics
(A) R/$\overline{W}$ Control Input
(B) AGC Attack Time
(C) Stepped Input Test Signal
(D) AGC Decay Tim

XR-541 Pin Description (28 Pin PLCC)

Pin	Symbol	Description
1,2	$-C_D$, $+C_D$	**Differentiator Network Terminals.**
3	HYS	**Window Gating Hysteresis.** Window gating comparator level is adjusted by this pin.
5	Level	**AGC Amplifier Level Output.** Rectified Analog signal is output for closing the AGC loop.
6	AGC	**AGC Charge Current Input.** Determins if AGC bypass capacitor is charging at the fast rate, slow rate, or is discharging.
7,8	+IN, -IN	**AGC Preamplifier Input.** Signal input from external read preamplifier.
9	HOLD	**AGC Gain Hold.** When low, AGC Amplifier Gain is held constant.
10	V_{DD}	**+12V Supply.**
11	T.P.C.	**Test Point for monitoring "Clock" path.**
12	R/$\overline{W}$	**Read/Write Control.** A TTL low places the device in standby mode.

13	T_{PW}	**One Shot Timing Select.** Output pulse time is set using a capacitor to +VCC.
15	V_{CC}	**+5V Supply.**
16	$\overline{RD}$	**Read Data Output.** Active low digital output.
18	T.P.D.	**Test Point for monitoring "Data" path.**
19	DGND	**Digital Ground.**
20	BYP	**AGC Control Pin.** A capacitor to ground sets AGC time constants.
21	AGND	**Analog Ground.**
22,23	+OUT,-OUT	**AGC Amplifier Output.**
24,27	$-D_{IN}$, $+D_{IN}$	**"Data" path Input.**
26,28	$-C_{IN}$, $+C_{IN}$	**"Clock" path Input.**

CIRCUIT OPERATION

Standby/Write Mode

During Data Write operations (R/$\overline{W}$ low), the XR-541 AGC input impedance is lowered to reduce the time constant caused by the input coupling capacitors, which limits the speed of Write to Read recovery. The AGC is reset to maximum gain, and the digital circuitry is disabled.

Read Mode

AGC

The analog head signal is A.C. coupled from the head preamplifier to the AGC inputs. The signal is amplified and output through low impedance drivers. Nominal peak output voltage is user-determinable by applying a voltage to the AGC Pin, according to the relationship:

$$V_{AGCOUT}\ (p\text{-}p) = 0.48\ V_{AGC}$$

Where V_{AGCOUT} is the peak to peak pre-amplifier output voltage and V_{AGC} is theDC control voltage on the AGC pin.

For most applications, a peak to peak output voltage of 2 volts is ideal.

AGC gain is held constant between pulses by the capacitor on the BYP Pin. Two rates of current charge this capacitor depending on the relative amplitude. A high level, 1.8mA, provides rapid attack characteristics needed for fast Write to Read recovery time. A low level, 180µA, allows slower gain tracking adjustment and reduces third order harmonic generation.

Preamplifier output is passed through a multiple order Bessel lowpass filter and applied to the Clock and Data inputs. For some applications, different delays are required for the Clock and Data inputs. For this reason, the XR-541 separates these inputs; many applications do not need separate timing and Clock Inputs and Data Inputs are directly connected. Internal path delays are carefully matched.

Hold

In the "Hold" mode, (Hold = low) no current charges C_{BYP} The constant voltage on C_{BYP} keeps the amplifier gain constant at the present valve. This feature is intended to facilitate embedded servo applications, where fixed gain is essential for amplitude comparison used in head positioning.

Data Path

Amplified signal output from the filter is applied to the $+D_{IN}/-D_{IN}$ terminals to allow amplitude qualification of the signal and AGC loop closure. When this input amplitude exceeds the hysteresis threshold, the D flip-flop data inputs are toggled.

These inputs will not change state again until the signal changes direction and crosses the hysteresis threshold on the opposite side of 'zero'. See figures 2a, 2d. Hysteresis comparator output is buffered and appears at T.P.D. for testing or evaluation purposes.

Clock Path

Amplified signal output from the filter is applied to the $+C_{IN}/-C_{IN}$ terminals to determine precise data peak timing. The clock path consists of a differentiator, a zero crossing comparator, and a one-shot timer.

The differentiator phase shifts the incoming waveform, converting data peaks into zero crossings. A capacitor, C_D- typically 20pF to 150pF, determines the amount of

phase shift. Although a phase shift of 90° across all input frequencies would be ideal, this implies an infinte bandwidth. Noise considerations usually dictate adding a resistor, and occasionally an inductor, to limit the differentiator noise bandwidth. With a series RLC network, the differentiator transfer function becomes:

$$A_V = \frac{-2000\ Cs}{LCs^2 + (R + R_1)\ Cs + 1}$$

where s = jw and R_1 = 92Ω (internal impedance of the differentiator).

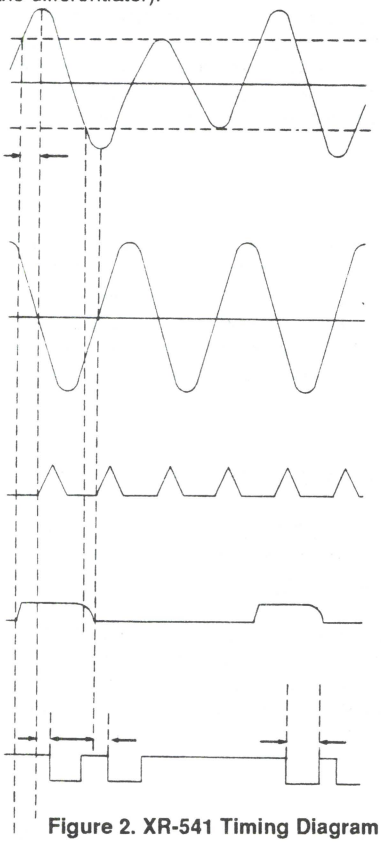


Figure 2. XR-541 Timing Diagram

(A). AGC Amplifier Output (also V_{CIN} & V_{DIN}) showing ±window comparator thresholds.
(B). Differentiator Circuit waveform (V_{CD}).
(C). Test Point "C" Output. Flip-flop clock input.
(D). Test Point "D" Output. Flip-flop D input.
(E). $\overline{RD}$ Output.

Differentiator output is applied to a zero crossing comparator. This comparator fires a bi-directionally triggered one-shot timer whose output is used as the clock of the D flip-flop. Buffered one-shot output appears at T.P.C. for alignment purposes.

Data Output

After the signal is time and amplitude qualified, the D flip-flop toggles. This fires a one shot timer which outputs constant width active low digital data pulse, $\overline{RD}$. The period of this pulse is programmed by a capacitor, Cpw, from pin Tpw to $+V_{CC}$ and is proportioned to this capacitor by the formula:

$$Tpw = 0.67\ Cpw$$

Where Tpw is in ns and Cpw is in pF.
Recommended Cpw values range from 50pF to 200 pf.

The active low $\overline{RD}$ output has a fan out of 1 TTL gate.

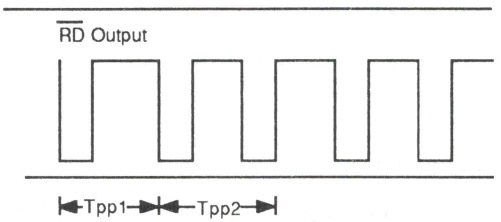


Figure 3. Pulse Pairing Definition

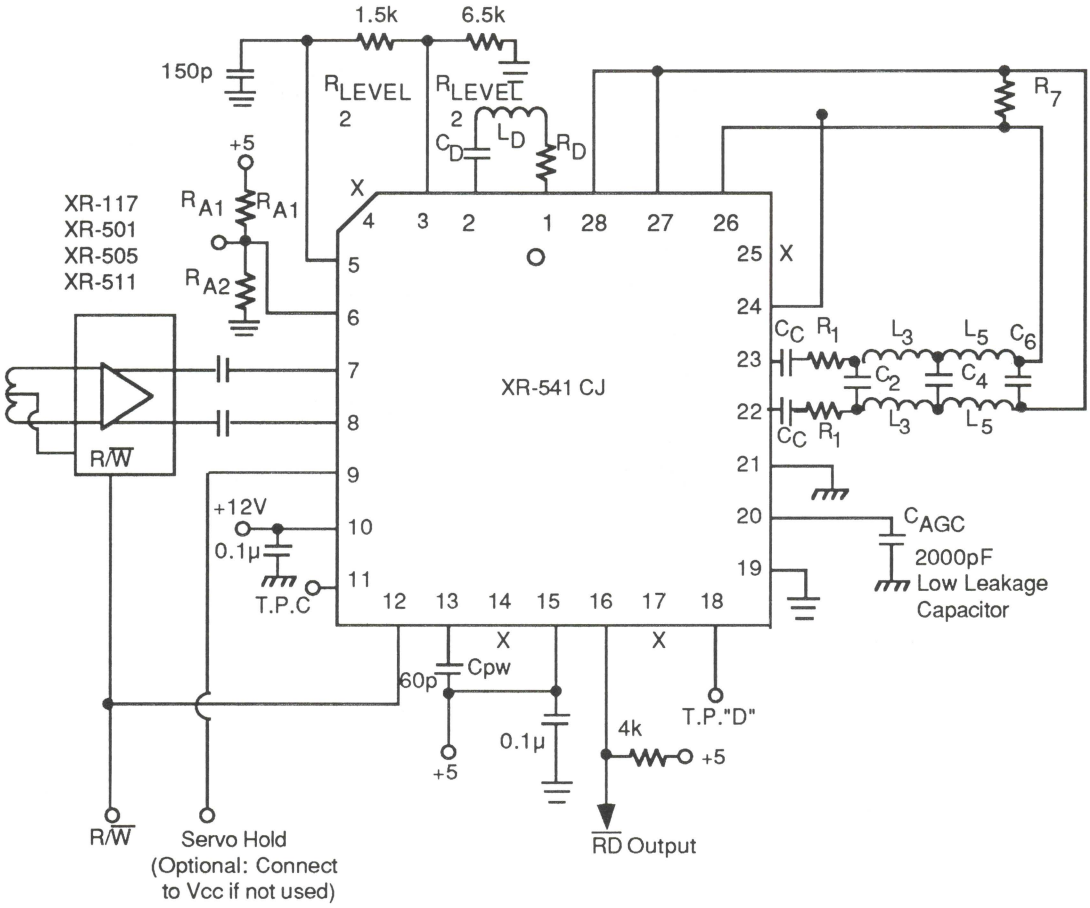
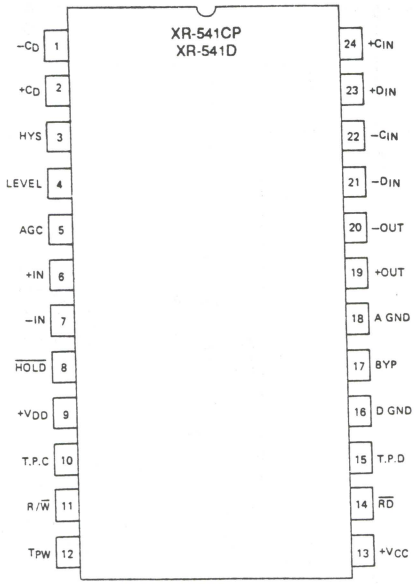
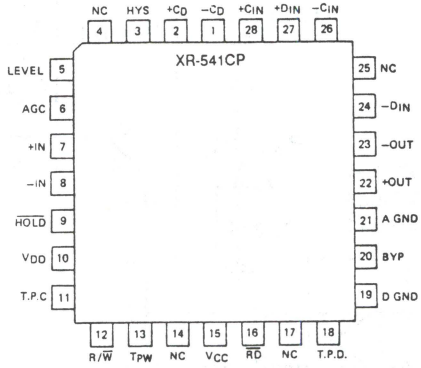


Figure 4. XR-541 Application Circuit





XR−541CJ (PLCC) Pinout

Low Power Programmable Electronic Filter

Preliminary Information

GENERAL DESCRIPTION

The XR-9022 is a programmable electronic BiCMOS filter utilizing only internal capacitors to implement several filtering functions. There is a combination low pass-boost filter function which has a progammable cutoff of 3 to 9 MHz. The boost is programmable from +6 to -6dB at the cutoff frequency of the low pass. There is also an internal differentiator whose inputs are the low pass-boost outputs that has its programmable pole at 2 to 4 times the low pass cutoff. The device frequency programming is done with a serial interface.

APPLICATIONS

Hard Disk Drive Read Channels

FEATURES

+5V operation
Programmable filter
Programmable pulse slimmer -6 to 6dB boost @ fc
Programmable differentiator
Ideal for constant density recording
+- 5% cutoff frequency accuracy
+- 5% group delay variation over complete range fc = 3 to 9 MHz
18 pin DIP and SOIC packages.
Control by a serial uP interface.

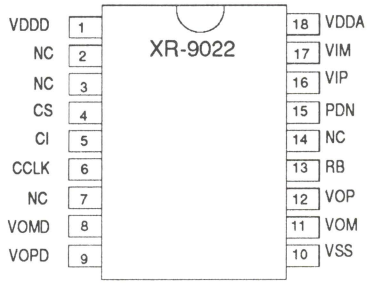
ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Supply Voltage VDDD or VDDA	-0.5 to 7	VDC
Voltage Applied to Inputs	-0.5 to VCC	VDC
Maximum Power Dissipation	200	mW
Storage Temperature, Ambient	-65 to +150	°C
Junction Operating Temperature, Tj	150	°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9022CP	18 Pin Plastic DIP	0 to +70°C
XR-9022CK	18 Pin Japanese SOIC	0 to +70°C
XR-9022CD	18 Pin JEDEC SOIC	0 to +70°C

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-9022 Programmable Continuous Time Filter is a programmable Seventh Order 0.05 degree Equiripple Low-pass Filter with trackable Boost and Differentiator Filters. The Low-pass Bandwidth is programmable via a single resistor to VSS from the RB pin. The cutoff frequency of the Low-pass ranges from 3 to 9MHz.

The Boost Filter is comprised of a variable High-pass Filter with a programmable peak amplitude (boost) at fc that ranges of +/-6dB. This filter is intended for Pulse Slimming in disk drive peak detection applications. The amount of boost is controlled via the serial interface.

The Differentiator Filter is comprised of a variable High-pass Filter such that the High-pass Filter corner frequency can be controlled independent of the Low-pass Filter cutoff frequency. The High-pass corner frequency ranges from 2 to 4 times the Low-pass fc, and will track the Low-pass fc. The corner frequency of the Differentiator is controlled via the serial interface.

There are many power down options for the XR-9022. The Boost and Differentiator functions can be powered down either by the serial interface or by using the external $\overline{\text{HPEN}}$ and $\overline{\text{FBEN}}$ pins of the XR-9021. Either part will completely power down via the PDN pin. When powered down the part draws less than 5 mW.

The XR-9022 is fabricated in BiCMOS, uses only a single +5V supply and is available in 18 pin DIP, and 18 pin Japanese and JEDEC SOIC packages.



NOTES



5V Programmable Pulse Detector and R/W Preamplifier Interface

Preliminary Information

GENERAL DESCRIPTION

The XR-9040 utilizes large scale integration to incorporate several read/write functions into a single integrated circuit.

For the read/write channel the XR-9040 performs the pulse detection function, as well as providing an interface to the preamplifier circuit.

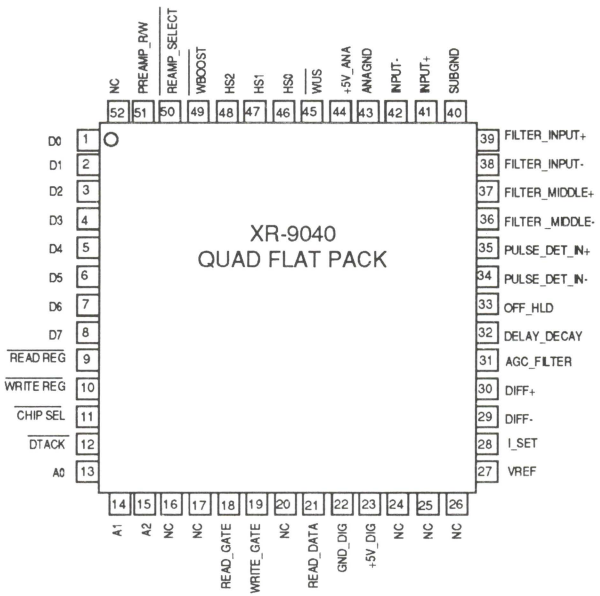
The circuit is designed to connect, through an unmultiplexed eight bit bus, to a microprocessor using a synchronous interface. This interface reduces the need for single point interconnects, as well as allowing features to be incorporated (such as the programmable data qualification threshold) that otherwise would be impractical.

The circuit is designed to operate from a single +5V supply and is fabricated using a BiCMOS process so as to decrease power dissipation and optimize circuit topology. Also incorporated are shutdown modes that allow reduced power dissipation.

FEATURES

+5V Only Operation
BiCMOS Process for Lower Power
High Level u-P Based Interface
Register Based Architecture
Cycled Power Modes to Reduce Power Consumption
Sample and Held, Dual Bandwidth Offset Compensation Circuit to improve Write to Read Recovery
Offset sense on Filter Output.
Variable sense on Filter Output.
Filter Response Registers for Equalization.
Constant Bandwidth, Fast Attack/Decay AGC.
AGC Hold Function.
Dual Bandwidth AGC Loop.
Threshold Qualification.
Programmable Threshold Qualifier Level

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9040ACQ	52 pin QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS:

D.C. Supply Voltage(VCC)	-0.3 to +6 V
Digital Input Voltage Range (VIN)	-0.3 to VCC+0.3V
Junction Temperature	150 °C
Storage Temperature	-65 to 130 °C
Write Disable Operating Range(VCC)	3.0 min
Temperature Range	0°C to 70°C Max
Shock	(TBD)G



NOTES



Data Synchronization / 1,7 RLL ENDEC

Preliminary Information

GENERAL DESCRIPTION

The XR-9050 is a high-speed, single +5V supply, low power fully integrated 1,7 ENDEC and Data Synchronizer. It is a complete system for data encoding and data recovery in magnetic disk drives utilizing the 1,7 RLL recording format, containing a fully integrated, high accuracy PLL with the encode and decode of 1,7 RLL. Combining the XR-9050 with an Exar Read/Write Pre-amplifier and Pulse Detector provides a complete Read/Write channel for a magnetic storage system.

The XR-9050 is implemented in a high performance BiCMOS process, lowering the power dissipation through CMOS logic and providing accurate timing with the bipolar integrated PLL.

FEATURES

Low Noise, Low Jitter Data Synchronizer
High Speed 1,7 RLL ENDEC
Tunable Write Precompensation
Easily Adapted to Zoned Recording Applications
Hard or Soft Sector Capability
Advanced BiCMOS technology
Typical Power Dissipation: 150 mW at 24 Mbits/sec.

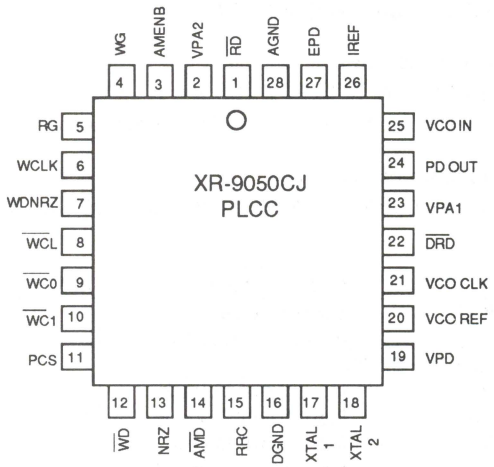
APPLICATIONS

SCSI Bus Hard Disk Drives
IDE Interface (AT) Hard Disk Drives
ESDI Bus Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

VPA1 VPA2 VPD	+7VDC
Digital Inputs	-0.3V to (VPD +0.3V)
Junction Temperature	150 °C
Storage Temperature	-65 °C to 150 °C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9050ACD	28 Pin SOIC	0 °C to 70 °C
XR-9050ACJ	28 Pin PLCC	0 °C to 70 °C

SYSTEM DESCRIPTION

The XR-9050 is a 24 MBit/sec 1,7 RLL Data Synchronizer and ENDEC implemented in a low-power, proprietary BiCMOS process. This allows for independent optimization of the linear VCO and charge pump in high performance bipoloar technology, while using fine geometry and low power CMOS for the ENDEC logic functions. The resultant device is faster than similar bipolar-only versions, while dissipating only about 150 mW during Read operations. The device is fully capable of either hard or soft sector operation. The XR-9050 data rate is adjusted with a single resistor. All necessary internal timings will track each other as this value is changed, easily accommodating zoned recording applications.

ELECTRICAL CHARACTERISTICS

Test Conditions:
T_A = 25 °C to 70°C, 4.75 VDC ≤VPA1 = VPA2 = VPD ≤5.25 VDC, 7.5 MHz≤ 1/ TORC ≤ 20 MHz ,
22.5 MHz < 1/TVCO < 60 MHz, Digital Load Capacitance limited to 15 pF unless otherwise specified.

Typicals measured at:
T_A = 25°C, VPA1 = VPA2 = VPD = 5.0 VDC , 1/ TORC = 10 MHz , 1/ TVCO = 30 MHz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
ICC	Supply Current		30	50	mA	
PD	Power Dissipation		150		mW	
DIGITAL SIGNALS						
VIL	Input "Low" Voltage			0.8	V	
VIH	Input "High" Voltage	2.0			V	
IIL	Input "Low" Current	-0.4			mA	VIL = 0.4 V
IIH	Input "High" Current			10	µA	VIH = 2.4 V
VOL	Output "Low" Voltage			0.4	V	IOL = 4 mA
VOH	Output "High" Voltage	2.8	4.8		V	IOH = -0.4 mA
READ MODE						
	Maximum Data Rate		24.0		Mb/s	
TRD	Read Data Pulse Width	15	TORC - 20		ns	
TFRD	Read Data Fall Time			15	ns	2.0V to 0.8V
TRRC	Read Clock Rise Time			8	ns	0.8V to 2.0V
TFRC	Read Clock Fall Time			5	ns	2.0V to 0.8V
TPNRZ	NRZ Set Up/ Hold Time	.31 TORC			ns	
TAMD	AMD Prop. Delay	10			ns	
	1/3 Bit Cell Delay	.8TD		1.2TD	ns	TD = 1/3 (2/3 Torc) controlled thru I_{REF}
WRITE MODE						
TWD	Write Data Pulse Width	Note #1		Note #2	ns	
TFWD	Write Data Fall Time			8	ns	
TRWC	Write Data Clock Rise Time			10	ns	0.8V to 2.0V
TFWC	Write Data Clock Fall Time			8	ns	2.0V to 0.8V
TSNRZ	WDNRZ Pin Set Up Time	5			ns	
THNRZ	WDNRZ Pin Hold Time	5			ns	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TPC	Precompensation Time Shift Magnitude Accuracy					TPC0 = .053*RC*(CS + CC) RC = 1K to 2K
	$\overline{WC0}$ = 1 $\overline{WC1}$ = 1	0		0	ns	
	$\overline{WC0}$ = 0 $\overline{WC1}$ = 1	0.8* TPC0 -0.2		1.2* TPC0 +0.2	ns	
	$\overline{WC0}$ = 1 $\overline{WC1}$ = 0	1.6* TPC0		2.4* TPC0	ns	
	$\overline{WC0}$ = 0 $\overline{WC1}$ = 0	2.4* TPC0		3.6* TPC0	ns	
DATA SYNCHRONIZER						
TVCO	VCO Center Freq.	0.8*		1.2*	ns	TO = 3.6E-12*(R_{REF} + 2300)
	Period	T0		T0		VCO IN = 2.7 V VCC = 5.0 V 3.5K < R_{REF} < 7.5K
	VCO Dynamic Range	± 25		± 45	%	
KVCO	VCO Control Voltage Gain	0.14 ω_0		0.26 ω_0	rad/ sec V	$\omega 0 = 2\pi/TO$ 1V ≤ VCO IN ≤ VCC - 0.6V
KD	Phase Detector Gain	0.83* KD		1.17* KD	A/rad	KD = 0.19 / (R_{REF} + 530) VCC = 5.0V PLL REF = RD
	KD * KVCO Product Accuracy	-28		+28	%	
	VCO Restarted Phase Error	-10		+10	ns	To RRC
	Decode Window Centering Accuracy			± 2	ns	
	Decode Window	(2/3 TORC) - 2			ns	
CONTROL TIMING CHARACTERISTICS						
TSWS	$\overline{WC0}$ $\overline{WC1}$ Set up time	50			ns	
THWS	WC0 WC1 Hold time	0			ns	

Notes # 1 : (2/3 TOWC) - 5 - (4.76 TPC0) - TPC

Notes # 2 : (2/3 TOWC) + 5 - (4.76 TPC0) - TPC

PIN DESCRIPTION

Pin #	Name	Description
Power Pins		
23	VPA1	+5V for Analog
2	VPA2	+5V for Analog
19	VPD	+5V for Digital
28	AGND	Ground for Analog
16	DGND	Ground for Digital
Control Pins		
3	AMENB	Address Mark Enable. Initiates a Read operation in Soft Sector operation. When asserted, the Address Mark Detection logic searches for 6 "0s" then 9 "0s". When these are found, the pin AMD is asserted and PLL acquisition should begin.
4	WG	Write Gate. Controls the Write operation in either Hard or Soft sector operation. When asserted, encodes the WDNRZ input into 1,7 RLL pulses which are output on pin WD. WG should NOT be deasserted until the last encoded pulse has been output from the IC.
5	RG	Read Gate. RG asserted switches the PLL Phase Detector input from the crystal to the RD pulses, beginning the PLL acquisition. RG must remain asserted through the entire Read cycle. In Soft Sector mode, the controller should assert RG after AMD is asserted. In Hard Sector mode, the controller should assert RG when the head is in the Preamble to initiate PLL acquisition.
8	WCL	Write Compensation Latch. Active low assertion on this pin latches the values on the pins WC0 and WC1. Used for drive microcontroller control of Pre-compensation.
9	WC1	Write Compensation bit 1. Active low, high order bit of Write Pre-compensation multiplier. See electrical characteristics, Write Mode, TPC for values of WC0 and WC1 vs precompensation used.
10	WC0	Write Compensation bit 0. Active low, low order bit of Write Precompensation multiplier.
27	EPD	Enable Phase Detector. When enabled (high) the phase detector and charge pump will drive the Analog pin PD OUT with current pulses.
Data Inputs		
1	RD	Read Data. This active low input is the encoded data pulses recovered from the disk by a Pulse Detector, one digital pulse for every disk pulse. This input is compatible with all Exar Pulse Detectors.
6	WCLK	Write Clock. WCLK is the clock of the WDNRZ input data, and must be synchronous with the data. Can be connected to RRC directly if the serializer utilizing RRC as the shift clock has a small propagation delay.
7	WDNRZ	Write Data Non Return to Zero. This is the serial input of the data to be written onto the disk when WG is asserted. Encoded to 1,7 RLL pulses by the IC, which are output on the pin WD. This pin is Tristated when not in Write mode.

Pin #	Name	Description
	Data Outputs	
12	$\overline{\text{WD}}$	Write Data. $\overline{\text{WD}}$ is the output of active low pulses to the preamp to toggle the write current and place a magnetic transition on the disk. Developed by the internal encoder. Compatible with any Exar Read / Write Preamplifier. The pin WG should not be deasserted before the last desired data pulse has been output from this pin to the Preamplifier.
13	NRZ	Non Return to Zero. This is the decoded data output in a Read operation. It is Tristated in any other mode, so that a bidirectional NRZ line can be made by connecting this pin with the pin WDNRZ.
14	$\overline{\text{AMD}}$	Address Mark Detect. This active low signal is asserted in a Soft Sector Read operation after the detection of the Address Mark (the preamble follows), a pattern of two 7 bit zeros fields followed by two 11 bit zeros fields. It is held low until AMENB is released.
15	RRC	Read/Reference Clock. This is the supplied clock to the controller section of the drive. In Read mode (either Soft or Hard Sector) this is the VCO/3 frequency and is synchronized to the NRZ data output. In all other modes it is XTAL/3. It can be used for serializing the WDNRZ in during Write operations.

Pin #	Name	Description
20	VCO REF	Voltage Controlled Oscillator Reference. This is an open emitter ECL test point to instrument tests of the phase lock accuracy and bit centering in the decode window. A 270Ω resistor connected between this pin and DGND allow observation of the VCO input to the Phase Detector. The negative edge of this output is phase-locked to the leading edge of $\overline{\text{DRD}}$. During all modes except read, the output is the crystal output divided by 2. It is recommended that the resistors be removed during normal operation to reduce power dissipation.
21	VCO CLK	Voltage Controlled Oscillator Clock. This is another open emitter ECL test point, that can be observed with a 270Ω resistor to DGND.
22	$\overline{\text{DRD}}$	Delayed Read Data. This active low, open emitter ECL test point is the Delayed Read Data input to the Phase detector. Its positive edge is phase compared to the negative edge of VCO REF. The jitter on the positive edge is the jitter in the data pulses recovered from the disk. The average position of the positive edge between 2 positive edges of VCO REF indicates the accuracy of the window centering.
	Analog Pins	
11	PCS	Precompensation. This is an analog input for an RC node whose time constant will set the precompensation time used when writing data. The time can be calculated by the formula in the Circuit Operation section. It must have the RC components connected to enable the encoder to function.

Pin #	Name	Description
17	XTAL1	Crystal input # 1. This is the input drive to both the internal divide by 2 and divide by 3 clock dividers. A series resonant crystal can be placed across this pin and XTAL2, or a CMOS compatible clock signal can be input on this pin and XTAL2 left open. Also, a TTL level clock can be capacitively coupled to this pin and XTAL 2 left open. The frequency input on these pins is 3 times the NRZ serial data rate. The crystal or clock should be as close to 50 % duty cycle as possible to make the divide by 3 clock symmetric.
18	XTAL2	Crystal input # 2. This is the response output drive to drive a series resonant crystal. If a CMOS clock is used to drive XTAL1, then this pin must be left open.
24	PD OUT	Phase Detector Output. Output from this analog output pin are current pulses which are proportional to the phase error between the VCO and the input source (either the RD input pulses or the crystal divided by 2). The amplitude of the current is given by the Reference Resistor, and the pulse width is the phase mismatch between the inputs. The loop filter is connected to this pin, as well as the pin VCO IN.
25	VCO IN	Voltage Controlled Oscillator Input. This analog input is a voltage which controls the frequency of the VCO (the higher the voltage, the higher the frequency). Normally connected to the pin PD OUT and the loop filter.
26	IREF	Reference Current. The resistor between this analog input pin and VPA1 sets the window centering and VCO center frequency for a particular data rate. Resistors can be paralleled on this pin through open-collector drivers to easily implement zoned recording applications. The value of resistance to used is in the section Circuit Operation.

CIRCUIT OPERATION

The three basic operational modes of the XR-9050 are Idle, Read and Write. Idle mode is selected by deasserting BOTH pins RG and WG. Both Write Mode and Read Mode have two sub-modes, Hard Sector and Soft Sector. The common operation to both Read and Write modes is the selection of the data rate, and the use of the XTAL inputs to generate internal clocks.

A series resonant crystal at 3 times the data rate should be installed between the pins XTAL1 and XTAL2. As these are both CMOS inputs, no external components should be installed other than the crystal. Alternately, a TTL levels clock can be capacitively coupled to drive the XTAL1 input, and the XTAL2 input should be left floating. This input frequency is divided by 2 for the 1,7 code rate clock and by 3 for the controller NRZ data clock.

The reference current is what sets up the VCO center frequency and 1/3 bit cell delay to center it in the decode window. The resistor value of the external resistor between the pin IREF and VPA1 is given by the formula:

$$RREF = \frac{92.6}{DR} - 2.3 \quad (\text{units kOhms})$$

where DR is the Data Rate in Mbits/sec (controller data rate).

READ MODE

Soft Sector

In the Soft Sector mode of a read operation, the controller should assert AMENB first. Its assertion causes the XR-9050 to enter the Address Mark search phase. The Address Mark on the disk is a pattern of two 7 bit long zeros fields, followed by two 11 bit long zeros fields. When the Address Mark is recognized, the output $\overline{AMD}$ is asserted and will stay true until AMENB is deasserted. At the assertion of $\overline{AMD}$, the controller should assert Read Gate (RG). The XR-9050 will then begin the Preamble Search. This is recognized after 3 consecutive bits are read from the disk. The XR-9050 will switch the Phase Detector input to the data pulses from the disk ($\overline{DRD}$ internally) and begin the PLL Acquisition. The first data pulse after the three bits will start the VCO in zero phase error at the start of the PLL Acquisition. After an additional 16 bits, the decoder is started and the pin RRC will be driven with the PLL clock and the NRZ pin will be driven by the decoded data. The pin RRC will not glitch, but may have a maximum of 2 clock periods with no transitions while this switchover occurs. Data decoding continues until the deassertion of Read Gate, and then the output $\overline{AMD}$ is also deasserted and the Read Operation ends.

Hard Sector

The Hard Sector mode of a Read operation is initiated by having the controller assert Read Gate (RG) before the Preamble. When Read Gate is asserted, the XR-9050 initiates the Preamble Search which is looking for three consecutive bits. After this pattern is found, the Read Operation proceeds the same as a Soft Sector read. The only exception is the deassertion of $\overline{AMD}$, since it was never asserted in a Hard Sector Read operation.

WRITE MODE

Soft Sector

In the Soft Sector mode of a Write operation, first RG must be deasserted, normally following the successful read of a sector header. WG can then be asserted no less than 1 NRZ bit period later. When Write Gate(WG) is initially asserted, WDNRZ should be zero (low). At least 1 NRZ bit period later, AMENB should be asserted by the controller, and the device will encode the Address Mark to the $\overline{WD}$ pin (two 7 bit long zeros fields followed by two 11 bit long zeros fields). Following the Address Mark the 3 "3T" pattern Preamble is written. At this point WDNRZ becomes an active input, and 5 NRZ periods later the 1,7 RLL encoded data starts being output (with Precompensation) from the $\overline{WD}$ output. This encod-ing continues until the end of the Write operation. It is the controller's responsibility to hold WDNRZ low for 5 NRZ periods after the last data bit is serialized to allow the desired data to completely pass through the 1,7 encoder. After these last 5 periods, WG can be deasserted and the Write operation is done.

Hard Sector

To do a Hard Sector Write Operation, RG is deasserted and WG asserted as in Soft Sector, however AMENB is left deasserted. The $\overline{WD}$ output will be "3T" pattern until the WDNRZ pin becomes active. All other sequencing of the Write operation is the same as Soft Sector.

Write Precompensation

Write Precompensation is done on the patterns shown in Table 1. The amount of time shift is determined by the formula:

Shift = WP (0.053)*Rc*(Cc+ Cs)

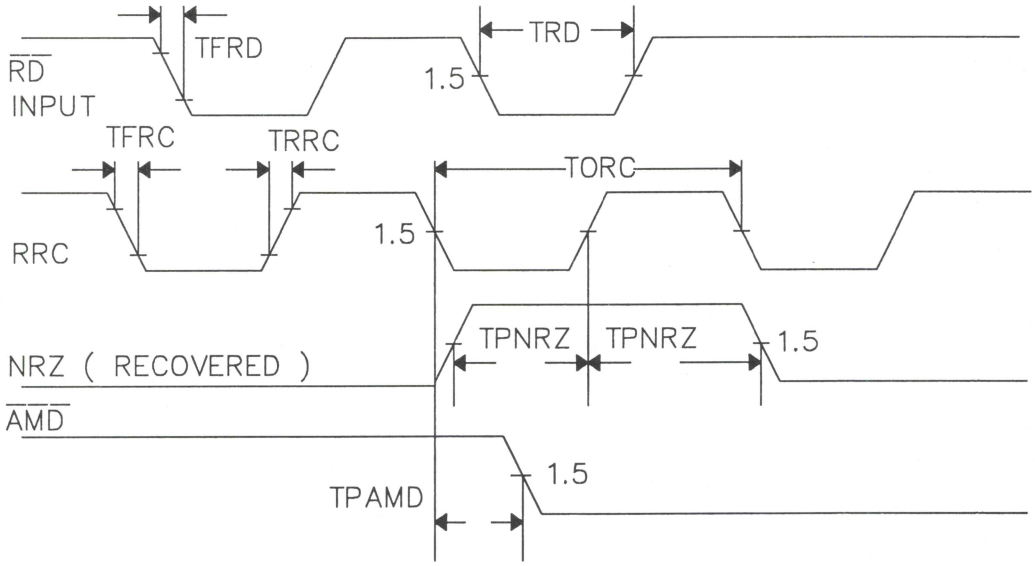
Where: 1) WP is value of $\overline{WCO}$ and $\overline{WC1}$ active low.

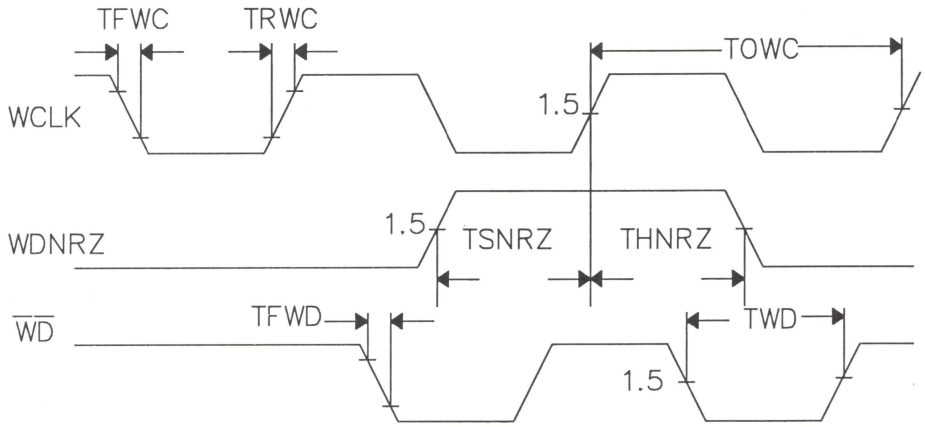
2) Cs is the stray capacitance of the application.

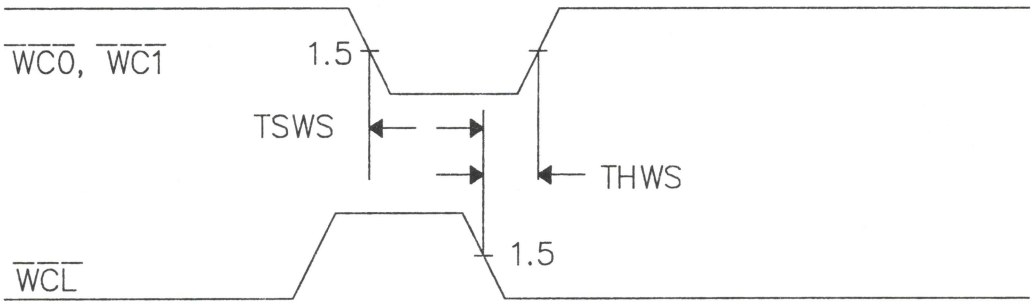
Bit N-2	Bit N-1	Bit N	Bit N+1	Bit N+2	Direction*
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

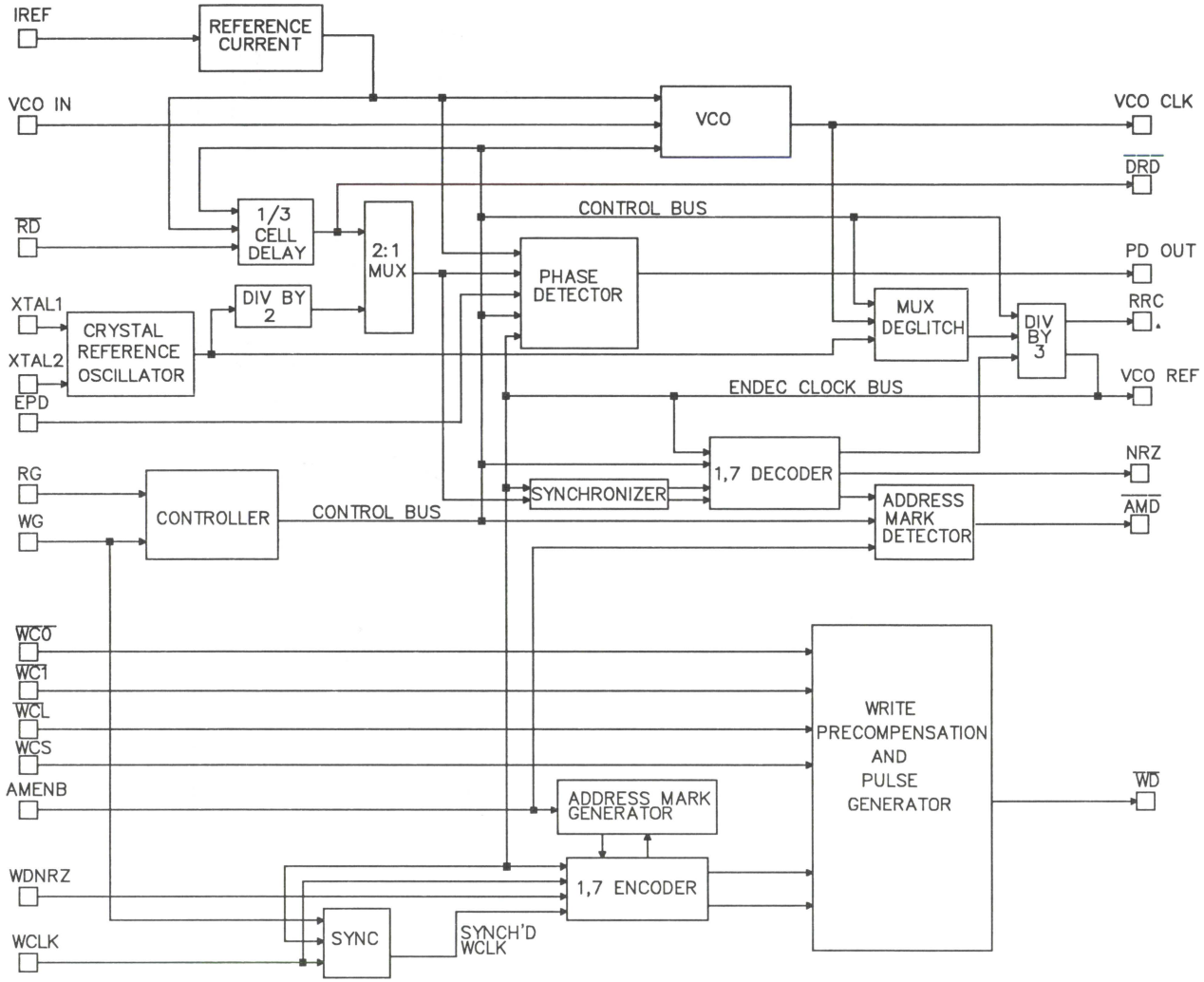
**Bit N is compenstaed. Late means the bit is written toward N+1 bit period (the following period). Early means the bit is written toward the N-1 bit period (the preceding period).*

Table 1. Precompensation Patterns


TFRD
TRD
RD
INPUT
1.5
TFRC
TRRC
TORC
RRC
1.5
TPNRZ
TPNRZ
1.5
NRZ (RECOVERED)
AMD
1.5
TPAMD


TFWC
TRWC
TOWC
WCLK
1.5
1.5
TSNRZ
THNRZ
WDNRZ
TFWD
TWD
WD
1.5


WC0, WC1
1.5
TSWS
THWS
WCL
1.5


IREF
REFERENCE CURRENT
VCO IN
VCO
VCO CLK
DRD
CONTROL BUS
RD
1/3 CELL DELAY
2:1 MUX
PHASE DETECTOR
PD OUT
XTAL1
DIV BY 2
MUX DEGLITCH
DIV BY 3
RRC
XTAL2
CRYSTAL REFERENCE OSCILLATOR
VCO REF
EPD
ENDEC CLOCK BUS
1,7 DECODER
NRZ
RG
SYNCHRONIZER
ADDRESS MARK DETECTOR
AMD
WG
CONTROLLER
CONTROL BUS
WC0
WC1
WCL
WCS
WRITE PRECOMPENSATION AND PULSE GENERATOR
AMENB
ADDRESS MARK GENERATOR
WD
WDNRZ
1,7 ENCODER
SYNC
SYNCH'D WCLK
WCLK

24 Mbit/sec Data Synchronizer, (1,7) ENDEC, Frequency Synthesizer, and Write Precompensation with Register Controls

Preliminary Information

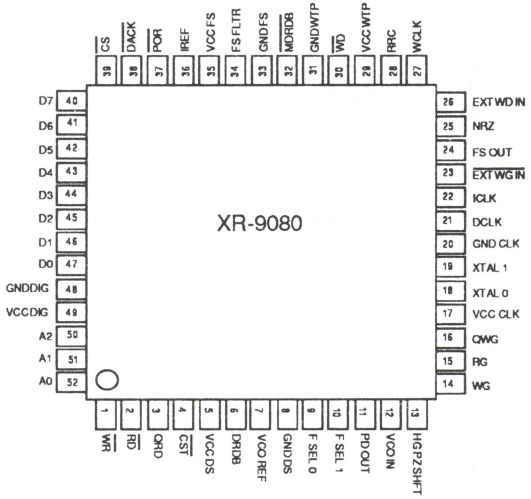
GENERAL DESCRIPTION

The XR-9080 combines the functions necessary for Data R/W in a zoned recording system at multiple data rates. It features high-speed, single +5V supply, low power fully integrated Data Synchronizer, 1,7 RLL ENDEC,PLL Clock Recovery, and a complete M divide by N ratio Frequency Synthesizer. In combination with a disk controller IC, a pulse detector IC, a Read/Write Preamp, and a microcontroller, the electronics of a disk drive system utilizing the 1,7 RLL recording format is realized. All functions can be controlled by the drive control microcontroller via a byte-wide demultiplexed parallel interface. The XR-9080 is implemented in a high performance BiCMOS process, giving low power dissipation through CMOS logic and providing accurate timing with the bipolar integrated PLL.

FEATURES:

Low Noise, Low Jitter Data Separator
Zero Phase VCO Restart to both Data and Crystal
Programmable Lock Detect Field Length
(4 - 31 bits)
Programmable PLL Loop Filter Adjustment:
2 pins for Zones under Register control
1 pin for High Gain adjust during
Lock Detect
Four Levels of Charge Pump Current,
Register Selectable
High Gain Mode during Lock Detect,
Register Selectable
Microprocessor Controlled VCO Center Frequency
and 1/3 Cell Delay Centering
High Speed 1,7 RLL ENDEC
Tunable Write Precompensation
Ratio controlled Frequency Synthesizer
Intended for Any Zoned Recording Application
Advanced BiCMOS technology
Programmable Readback Window Margin Capability
Typical Power Dissipation: 350 mW at 20 Mbits/sec

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9080CQ	52 Pin QFP	0 °C to 70 °C

APPLICATIONS

SCSI Bus Hard Disk Drives
IDE Interface (AT) Hard Disk Drives
ESDI Bus Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

VCC DS, VCC CLK, VCC WTP, VCC FS, VCC DIG	+7VDC
Digital Inputs	-0.3V to VCC DIG + 0.3V
Junction Temperature	150 °C
Storage Temperature	-65 °C to 150 °C

ELECTRICAL CHARACTERISTICS

Test Conditions:

TA = 25 °C

4.75 VDC ≤ VCC DS = VCC CLK = VCC WTP = VCC FS = VCC DIG ≤ 5.25 VDC.

7.5 MHz ≤ 1 / TORC* ≤ 24 MHz, 22.5 MHz ≤ 1/TVCO ≤ 72 MHz

Digital Load Capacitance limited to 15 pF.

*TORC = Time of One Recording Cell

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
ICC	Supply Current		40	60	mA	
PD	Power Dissipation		200		mW	1/TORC =15MHz
DIGITAL SIGNALS						
VIL	Input "Low" Voltage			0.8	V	
VIH	Input "High" Voltage	2.0			V	
IIL	Input "Low" Current	-0.4			mA	VIL = 0.4 V
IIH	Input "High" Current			10	µA	VIH = 2.4 V
VOL	Output "Low" Voltage			0.4	V	IOL = 4 mA
VOH	Output "High" Voltage	2.8	4.8		V	IOH = -0.4 mA
READ MODE						
	Maximum Data Rate		24.0		Mb/s	
TRD	Read Data Pulse Width	15	TORC - 20		ns	
TFRD	Read Data Fall Time		15		ns	2.0V to 0.8V
TRRC	Read Clock Rise Time		8		ns	0.8V to 2.0V
TFRC	Read Clock Fall Time		5		ns	2.0V to 0.8V
TPNRZ	NRZ Set Up/ Hold Time	.31 TORC			ns	
	1/3 Bit Cell Delay	.8TD		1.2TD	ns	TD = .5 TVCO
WRITE MODE						
TWD	Write Data Pulse Width	.94 TVCO		1.06TVCO	ns	
TFWD	Write Data Fall Time			8	ns	
TRWC	Write Data Clock Rise Time			10	ns	0.8V to 2.0V
TFWC	Write Data Clock Fall Time			8	ns	2.0V to 0.8V
TSNRZ	WDNRZ Pin Set Up Time	5			ns	
THNRZ	WDNRZ Pin Hold Time	5			ns	
WRITE PRECOMPENSATION						
TPC	Precompensation Time Shift Magnitude Accuracy					TPC0 = .02TVCO WPC0, WPC1 in register 7
	$\overline{WPC0}$ = 1 $\overline{WPC1}$ = 1					No Shift, This setting
	$\overline{WPC0}$ = 0 $\overline{WPC1}$ = 1	0.8* TPC0 -0.2		1.2* TPC0 +0.2	ns	
	$\overline{WPC0}$ = 1 $\overline{WPC1}$ = 1	1.6* TPC0		2.4* TPC0	ns	
	$\overline{WPC0}$ = 0 $\overline{WPC1}$ = 0	2.4* TPC0		3.6* TPC0	ns	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DATA SEPARATOR						
KVCO	VCO Control Voltage Gain	0.14 ω_0		0.26 ω_0	rad/ sec V	$\omega_0 = 2\pi/TO$ 1V ≤ VCO IN ≤VCC - 0.6V
KD	Phase Detector Gain	0.83 KD		1.17 KD	A/rad	KD = (VCC - VBE)*N / 2π(RREF + 1K) N = 1, 1.5, 2, 2.5, per Register 5 bits 1, 0
	KD * KVCO Product Accuracy	-28		+28	%	
	VCO Restarted Phase Error	-10		+10	ns	To RRC
	Decode Window Centering Accuracy		±2		ns	
	Decode Window	(2/3 * TORC) - 2			ns	
FREQUENCY SYNTHESIZER						
KVCO	VCO Control Voltage Gain	0.14 ω_0		0.26 ω_0	rad/ sec V	$\omega_0 = 2\pi/TO$ 1V ≤ VCO IN ≤VCC - 0.6V
KD	Phase Detector Gain	0.83 KD		1.17 KD	A/rad	KD = (VCC - VBE)*N / 2π(RREF + 1K) VCC = 5.0V PLL REF = RD
	KD * KVCO Product Accuracy	-28		+28	%	
SWITCHING CHARACTERISTICS (see fig. 1 and 2 for waveforms)						
tcsswr	Chip select set up before Write Reg-assertion	10			ns	
tcshwr	Chip select Hold time after Write Reg-deassertion	10			ns	
tdaswr	Data and Address Set up before Write Reg-assertion	10			ns	
tdahwr	Data and Address Hold time after Write Reg-assertion	10			ns	
tpwwr	Pulse width of Write Reg-	50			ns	
tpdawr	Propogation delay from Write Reg- to Acknowledge-assertions			10	ns	
tcssrd	Chip select Set up before Read Reg-assertion	10			ns	
tcshrd	Chip select Hold time after Read Reg-assertion	10			ns	
tasrd	Address Set up time before Read Reg-assertion	10			ns	
tahrd	Address Hold time after Read Reg-deassertion	10			ns	
tpwrd	Pulse width Read Reg-	50			ns	
tpdard	Propogation delay from Read Reg- to acknowledge assertions			10	ns	
tpdvrd	Propogation delay from Read Reg- assertion to Data valid			10	ns	
tdhrd	Data hold time after Read Reg-deassertion	0			ns	

SYSTEM INFORMATION

The XR-9080 is a 24 MBit/sec 1,7 RLL Data Synchronizer, ENDEC, and Frequency Synthesizer implemented in a BiCMOS process. This allows for independent optimization of the linear VCOs and charge pumps in high performance bipolar technology, while using fine geometry and low power CMOS for the ENDEC logic functions, the control DACs, and the microcontroller interface. The resultant device is faster, more compact, and lower power dissipation than any bipolar implementation of the same functions. The XR-9080 data rate is adjusted via register controlled, internal DACs. The register control of the 9080 is covered in the section called "Registers". All necessary internal timings will track the settings of the DACs and allow zoned recording applications.

PIN DESCRIPTION

Power Pins

Pin #	Symbol	Description
5	VCC DS	+5V for Data Separator, Analog 17 VCC CLK+5V for Clock Output Drivers, Digital
29	VCC WTP	+5V for Write Precompensation Circuit, Analog
35	VCC FS	+5V for Frequency Synthesizer, Analog
49	VCC DIG	+5V for ENDEC and Microcontroller Interface, Digital
8	GND DS	Ground for Data Separator, Analog
20	GND CLK	Ground for Clock Output Drivers, Digital
31	GND WTP	Ground for Write Precompensation Circuit, Analog
33	GND FS	Ground for Frequency Synthesizer Section, Analog
48	GND DIG	Ground for ENDEC and Microcontroller Interface, Digital

Control Pins

52	A0	Least significant Register selection address bit
51	A1	Address bit 1
50	A2	Most significant Register selection address bit
47	D0	Least significant Register Data bit read or written
46	D1	Register Data bit read or written
45	D2	Register Data bit read or written
44	D3	Register Data bit read or written
43	D4	Register Data bit read or written
42	D5	Register Data bit read or written
41	D6	Register Data bit read or written
40	D7	Most significant Register Data bit read or written
39	$\overline{CS}$	9080 Chip Select, input, asserts low. Allows writing to or reading from addressed register.
1	$\overline{WR}$	Write Register control, input, asserts low. Latches are state controlled, not edge triggered, therefore address and data inputs should be held valid for full time period that $\overline{WR}$ input is asserted.
2	$\overline{RD}$	Read register control, input, asserts low. Controls the direction switching of the data bus, turning it into outputs. This occurs only when register 3 or 7 is addressed and $\overline{RD}$ is asserted.
38	$\overline{DACK}$	Data Acknowledge,output asserts low. Pulses low after the $\overline{WR}$ or $\overline{RD}$ inputs asserts low and $\overline{CS}$ active. This output is OCL and requires an external pullup.Used for Microcontroller handshake.
37	$\overline{POR}$	Power On Reset, input, asserts low. This input initializes the state of various flip-flops. After initialization, the device register can be properly loaded.

Read Mode Pins

Pin #	Name	Description
3	QRD	Qualified Read Data, input, asserts high. Digital data stream input, 1,7 RLL format.
4	$\overline{CST}$	Coast, input, asserts low. Provides capability to disable the phase detector in the Data Separator. This allows the user to set up applications where the QRD input can have sections of servo and the clock/PLL can "coast over" them without being affected.
6	$\overline{DRD}$	Delayed Read Data, output, asserts low. Provides the delayed version of the QRD signal (after the 1/3 cell delay circuit). DRD runs at ECL levels.
32	$\overline{MDRD}$	Margin Delayed Read Data, output, asserts low. Provides a delayed version of the QRD signal that has also gone through the margin delay circuit. Magnitude of delay available at this output is under control of register 6, bits 5 through 0.The positive edge is the real bit, and is an ECL output which requires a 1 K pull down resistor to ground.
7	VCOREF	VCO Reference Clock. Test point output for Readback Clock
9	F SEL 0	Filter Select Control 0, open collector output to change the PLL loop filter characteristics. Set by register 7 bit 6.
10	F SEL1	Filter Select Control 1, open collector output. Set by register 7 bit 5.
11	PD OUT	Phase Detector Output. Analog output of current pulses of the Data PLL phase detector and charge pump. Normally connected to the loop filter.
12	VCO IN	Voltage Controlled Oscillator Input. Controlling input for the VCO operating point. Also normally connected to the loop filter .
13	HG PZ SHFT	High Gain Phase Shift. Open collector output provides dynamic grounding to change the filter configuration. This occurs while switched into High Gain, during Lock Detect mode.
15	RG	Read Gate, input. Provides overall control of the read operation. When asserted starts the lock detect counter, and switches to the high gain acquisition state of the PLL.
25	NRZ	Non Return to Zero Data. This bi-directional pin is an input in the write mode for the NRZ write data. In all other modes it is an output for the data decoder. The decoder is only active in the readback operation.
28	RRC	Readback Reference Clock. The RRC output is (in all modes except after lock detection) the frequency synthesizer clock divided by three. During a read operation, this output is switched to the PLL clock divided by three.

Write Mode Pins

14	WG	Write Gate, input. Allows control of write operations indirectly by controlling the presence of QWG.
16	QWG	Qualified Write Gate, output. Is asserted immediately after WG goes active,and causes 3T pattern to be output from the $\overline{WD}$ pin. After 6 RRC clock cycles, the $\overline{WD}$ output is switched to the NRZ data encoded to 1,7 RLL.When WG is deasserted, QWG stays asserted 6 clock cycles to allow the1,7 ENDEC to completely encode the NRZ input during the write cycle and output to the $\overline{WD}$ pin.

Pin #	Name	Description
30	$\overline{WD}$	$\overline{Write\ Data}$, output, asserts low. It is a serial data stream of pulses for 1,7 RLL write pattern. This output is intended for a toggling flip-flop in the write circuits of a R/W preamplifier IC. The pulses are encoded from the NRZ input.
27	WCLK	Digital input which clocks the write data input at the NRZ pin. Note that input clocking of the encoder is from the frequency synthesizer output. Therefore WCLK and the NRZ input must be phase /frequency locked to the frequency synthesizer (FS OUT) in order to allow data input flip-flop's timing to be valid.The data latches on the positive edge.
23	$\overline{EXT\ WG\ IN}$	$\overline{External\ Write\ Gate}$, input, asserts low. Register selectable test mode which allows bypassing the WG input.
26	EXT WD IN	External Write Data In. Register selectable test mode which bypasses the NRZ ENDEC for $\overline{WD}$ output.

Frequency Synthesizer

19	XTAL 1	Crystal Input 1. This input is the active node which is either connected to a passive crystal reference or driven actively by direct drive at CMOS levels. TTL input levels should be capacitively coupled.
18	XTAL 2	Crystal Input 2. This is the non-active node. When driving XTAL 1 with a CMOS level clock, this pin should be left floating.
21	DCLK	Digital Clock. TTL level output of the crystal oscillator which can be switched off under internal register control.
22	ICLK	Internal Clock. TTL level output of the crystal oscillator, continuously running.
24	FS OUT	Frequency Synthesizer Output. The output buffer of the Frequency Synthesizer may be turned off under register control.
34	FS FLTR	Frequency Synthesizer Filter. This pin is common to both the frequency synthesizer charge pump output and the VCO control voltage input.Analog Inputs
36	IREF	Reference Current Input. Establishes all modes and delays operating point currents. Requires resistor to VCC DS synthesizer clock divided by three. During a read operation, and after lock detection, this output is switched to the PLL clock which is derived from the RLL data stream.

CIRCUIT OPERATION

The three basic operational modes of the XR-9080 are Idle, Read and Write. Idle mode is selected by deasserting BOTH pins RG and WG. Read is selected by asserting RG and Write is selected by asserting WG. Asserting BOTH pins RG and WG is an illegal state, and the last asserted will be ignored.The common operation to both Read and Write modes is the selection of the data rate, and the use of the XTAL inputs to generate internal clocks. A series resonant crystal should be installed between the pins XTAL 1 and XTAL 2. Optionally, two capacitors to ground can be connected to these inputs when using a crystal. Alternately, a CMOS level clock can be used to drive the XTAL 1 input, and the XTAL 2 input should then be left floating. Also a TTL level clock can be capacitively coupled to XTAL 1 input, and the XTAL 2 input be left floating. The output of the crystal oscillator is fed to the frequency synthesizer which develops the frequency used for both writing data and readback data recovery.

The Frequency Synthesizer output frequency is set by the formula:

$$Fout = \frac{2\ (NUM)\ Fin}{(DEN)}$$

Where:

Fout = Frequency available at FSOUT.
Fin = Frequency applied at XTAL1,2 inputs.
NUM = NUMerator placed in B5-B0 of R0.
DEN = DENominator placed in B6-B0 of R1.

READ MODE

For a read operation, the user asserts RG, when the head is over the 3T Preamble. The PLL immediately begins the Preamble count. This starts the following sequence of operations:

1. Preamble is recognized upon the presence of 3 data bits.

2. Recognition of preamble switches phase detector input from reference clock to delayed readback data (DRD).

3. PLL acquisition, with zero phase restart, begins with the first readback pulse seen after switching of the phase detector input. Lock Detect Counter (register 4) is started. If enabled by register 7, High Gain mode is entered and HIGH GAIN PZ SHIFT becomes a ground, and the Charge Pump currents are quadrupled.

4. The number of pulses specified in register 4 are counted, then decoder functions are started, RRC switches to the readback clock, and decoded data is output from the pin NRZ.

8. Decoded data and readback clock are continually output until RG deasserts.

WRITE MODE

For a write operation, the user should assert WG. This becomes the first step in a sequence of operations:

1. WG input is asserted and NRZ input should begin. WD output outputs 3T pattern immediately.

2. Six cycles of RRC are counted.

3. QWG asserts and encoded RLL output at WD begins.

4. Encoded RLL output continues until deassertion of WG.

5. QWG remains asserted for 6 RRC clocks after the deassertion of WG. $\overline{WD}$ continues encoding until QWG deasserts. This insures that the last data bit is flushed from the encoder in a Write.

This part has a secondary Write mode which is used in a similar manner. First, set the ENAWR (Enable Write) bit placed in register 3. After that, assert $\overline{EXT\ WG\ IN}$ (External Write Gate In) and input data Pulses, (Active low) on the input EXT WD IN. These will bypass the encoder and go directly to the $\overline{WD}$ output and to the preamplifier to be recorded.

SPECIAL FEATURES

$\overline{COAST}$ feature:

When it is asserted, the currents that would flow for a phase error are not output to the loop filter from the PD OUT pin. In effect, the voltage on the loop filter is held constant by this lack of current flow until $\overline{COAST}$-is deasserted. Since Read Gate (RG) is asserted, NRZ decoding continues and is output, and Read Reference Clock is still the PLL VCO divided by 3. There is no "high-gain" mode (High current output from the phase detector,and filter modification signals true) for the device available at $\overline{COAST}$- deassertion. In addition, the zero phase restart logic is not armed by $\overline{COAST}$-. Phase lock is NOT guaranteed after deassertion, no matter the time duration of the $\overline{COAST}$- assertion.

In terms of timing, it should only be asserted after the user data field has been entered, i.e. RG should be asserted and several bytes of data decoding have occurred.

Above Voltage monitor bit (Register 3, B0):

This feature allows the drive microprocessor to set the VCO to the center of its capture range, and to

remove any offset error from the delay one-shots in the Data Separator. By changing the setting of the VCO DAC via register 2, the drive microprocessor can maximize the loop lock range, and minimize margin timing error at power up. The comparator driving this bit allows for setting the VCO DAC (Register 2) to place the Data Separator VFO to its mid-point of operation. It is intended for use as a power-up time calibration, but can be done at any time power is applied to the XR-9080. The microprocessor which loads the register values monitors this bit in the following algorithm:

1. Set the Numerator and Denominator values for the first data rate in Register 0 and 1, respectively.

2. Write the nominal value chosen to the VCO DAC, Register 2.

3. Read the Above Voltage bit: If it is HIGH, decrease the value in Register 2 by 1. If it is LOW, increase the value in Register 2 by 1.

4. Read the bit again; if it has reversed polarity store the value written to Register 2 as the Calibrated VCO DAC Register 2 value for future use when in that zone. If it has not, repeat step 3.

5. Repeat the same procedure (steps 1 to 4) for all zones and store the Calibrated Register 2 values for future use.

REGISTERS

REGISTER ADDRESS (A2-A1-A0)	REGISTER FUNCTION	REGISTER ACCESS
R0 (000)	Frequency Synthesizer: Enable Phase Detector Numerator	Write
R1 (001)	Frequency Synthesizer: Enable Phase Detector Denominator	Write
R2 (010)	Frequency Synthesizer VCO Operating Range DAC	Write
R3 (011)	Assorted Control Bits: Frequency Synthesizer Output Enable Low Power Mode Control Enable External Write Data Mode VCO Correction vs. Reference Voltages	Read & Write
R4 (100)	Lock Detect Field Length	Write
R5 (101)	Charge Pump Current	Write
R6 (110)	Window Margin Controls: DAC for Window Margin Delay Select/Eliminate Window Margin Data	Write
R7 (111)	Assorted Control Bits: Filter Switch Selection Enable High Gain PLL Acquisition Write Precompensation Magnitude D Clock Output Enable	Read & Write

R0, R1, & R2 FREQUENCY SYNTHESIZER & PLL CONTROL REGISTERS

R0 & R1 are totally devoted to control of the frequency synthesizer. R2 controls the operating point of the VCOs in both the frequency synthesizer and the PLL.R3,R7 each contain 1 bit which can affect the output of the frequency synthesizer or one of it's clocks.The frequency synthesizer output is primarily a function of three registers and the reference frequency from the crystal oscillator. Output of the frequency synthesizer is available at the FS OUT pin. This output may be switched on/off under control of R3, B3.ENPD, asserted high, enables the phase detector in the frequency synthesizer.The state of this one bit is controlled by B7 of either R0 or R1. Last register loaded controls the state of the bit.Nominal operating point of the VCO in the synthesizer and the VCO in the PLL are under control of a single DAC, with digital control placed under R2, B7-B0. Setting of VCDAC = 11111111 will achieve max operating frequency capability. Setting to 0 will give the minimum. Monitoring of the AV (Above Voltage) control bit, R3, B0, will aid in the setting of the VCO's to a nominal operating point.

REG#	MSB							LSB
R0:	B7	B6	B5	B4	B3	B2	B1	B0
	+ENPD	DC	NUM5	NUM4	NUM3	NUM2	NUM1	NUM0

REG#	MSB							LSB
R1:	B7	B6	B5	B4	B3	B2	B1	B0
	+ENPD	DEN6	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0

REG#	MSB							LSB
R2:	B7	B6	B5	B4	B3	B2	B1	B0
	VC	VC	VC	VC	VC	VC	VC	VC
	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

(DC = Don't Care, Bit has no internal use.)

R3 CONTROL BITS

EFSOUT - Enable Frequency Synthesizer Output. Bit placed high here enables the output buffer for the frequency synthesizer, bringing FSOUT active. EXDWR - EXternal Data WRite. Before the device can accept the External Write Gate In control and write pulses from the External Write Data in pins, this bit must be set high. To do a normal write, this pin should be reset.

LP - Low Power. Setting this bit high switches the chip into low power mode, shutting down as much circuitry as possible to minimize power consumption. Cycling of POR control after bringing power up on the device will leave this bit set in low power mode. Consequently, the power-up cycling of the device will require: a) turning on of power supplies, b) cycling low of POR briefly to initialize registers, flip-flops, and latches, c) loading of the LP bit with a low state to put the IC into a fully functional mode, d) loading of all registers with proper data necessary for desired operating parameters.

AV - Above Voltage. Readback of a high logic state here indicates that the PLL correction voltage is above that of the reference voltage. Reference voltage equals 2.7 volts, middle of the VCO operating range. Readback of the AV bit while adjusting VCDAC, R2, will allow the user to adjust for a nominal operating point.

REG#	MSB							LSB
R3:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	DC	DC	DC	+EFSOUT	+ENAWR	+LP	+AV

R4 - DEFINITION OF PLL LOCKUP FIELD LENGTH

LDL4 - LDL0: The value placed in this 5 bit register/counter determines the number of data pulses counted before the LOCK DETECT signal is asserted. The number placed here will be counted to, in the form of pulses present at the DRD pin. After this count the mode of the PLL will change from High Gain to Track. This drops the loop into low gain mode, and switches the RRC output from the frequency synthesizer divided by to PLL VCO divided by 3.

REG#	MSB							LSB
R4:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	DC	DC	LDL4	LDL3	LDL2	LDL1	LDL0

R5 - DATA SEPARATOR CHARGE PUMP GAIN

Two bit control of the charge pump provides a gain range of 4:1under register control. Currents available at the charge pump output are:

QP1	QP0	PUMP CURRENT
0	0	I_0
0	1	$1.5 * I_0$
1	0	$2.0 * I_0$
1	1	$2.5 * I_0$

$$I_0 = \frac{1.25 * (VCC - Vbe)}{(RREF + 1\ K)}$$

REG#	MSB							LSB
R5:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	DC	DC	DC	DC	DC	QP1	QP0

R6 - MARGIN DELAY; MAGNITUDE CONTROL AND SELECTION

This register sets the optional margin delay of the Data Separator. It is a separate data path from the normal 1/3 cell delay used in decoding, and is enabled by a write to this register B6. The time relationship is for a capacitor being charged by a current, so the delay is INVERSELY proportional to the setting (+/-) of this DAC.The delay is approximately:

Tdelay =TBD

MDENA: Margin Delay Enable. Controls multiplexing selection of data stream into data detection and synchronization (DD&S) module. When set high, data stream follows path through margin delay circuit into DD&S. Low setting of MDENA takes data stream through 1/3 Cell Delay module.

MD5 - MD0: Margin Delay Control DAC. Controls magnitude of the margin delay time period. Setting all bits high will give maximum delay time period.

REG#	MSB							LSB
R6:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	MDENA	MD5	MD4	MD3	MD2	MD1	MD0

Write Precompensation Pattern

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.
EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

R7 - ASSORTED CONTROL BITS

FS1, FS0: Filter Select 1, Filter Select 0. High assertion states on these control bits bring the corresponding FSEL0 and FSEL1 filter control lines down into a low impedance (< 100 Ohms), ground output state.

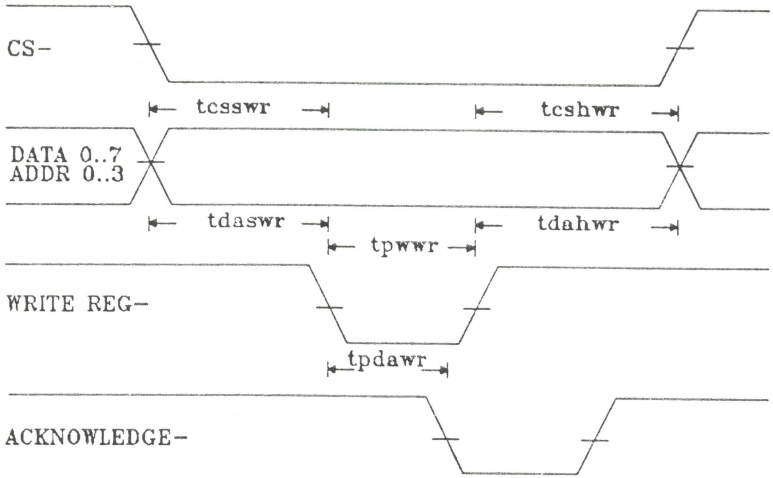
HG: High Gain. High assertion on this control bit allows for a high gain lockup mode during clock acquisition to the data stream. The High Gain is 4 times the normal loop gain, and is changed by quadrupling the Charge Pump current programmed in register 5. The High Gain mode extends between the assertion of READ GATE plus 3 data pulses and LOCK DETECT timeout of the number of bits set in register 4.

WPC1, WPC0: Write Precompensation Magnitude. Controls magnitude of the phase shifts introduced during the write precompensation process. Please note that the assertion is complementary/low for these inputs, i.e. 00gives maximum time shift:

WPC1	WPC0	PRECOMP SHIFT
0	0	3
0	1	2
1	0	1
1	1	0

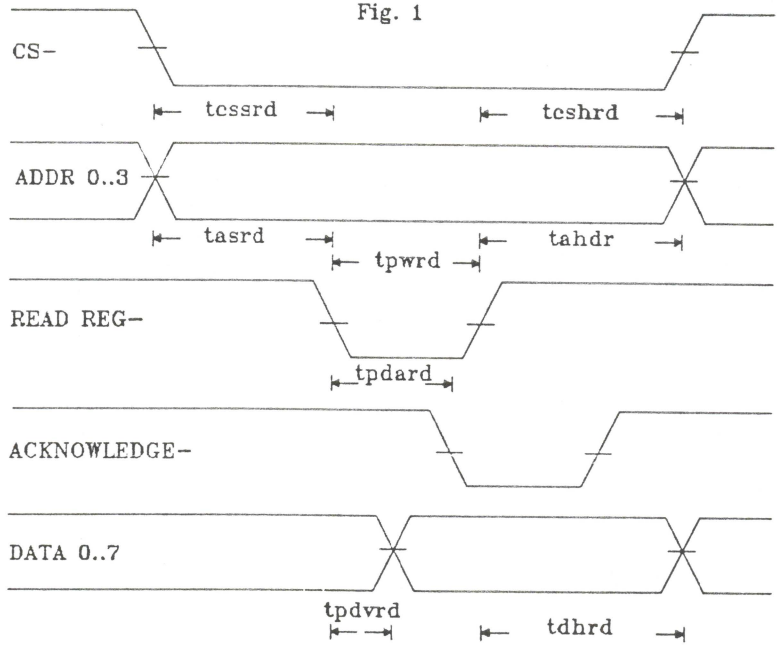
*(3 = Max time shift, 0 = No time precomp.)The actual time shift is Precomp Shift * .02*TVCO*

ENADC: Enable D Clock Output. High assertion state enables the output buffer for the DCLK signal.



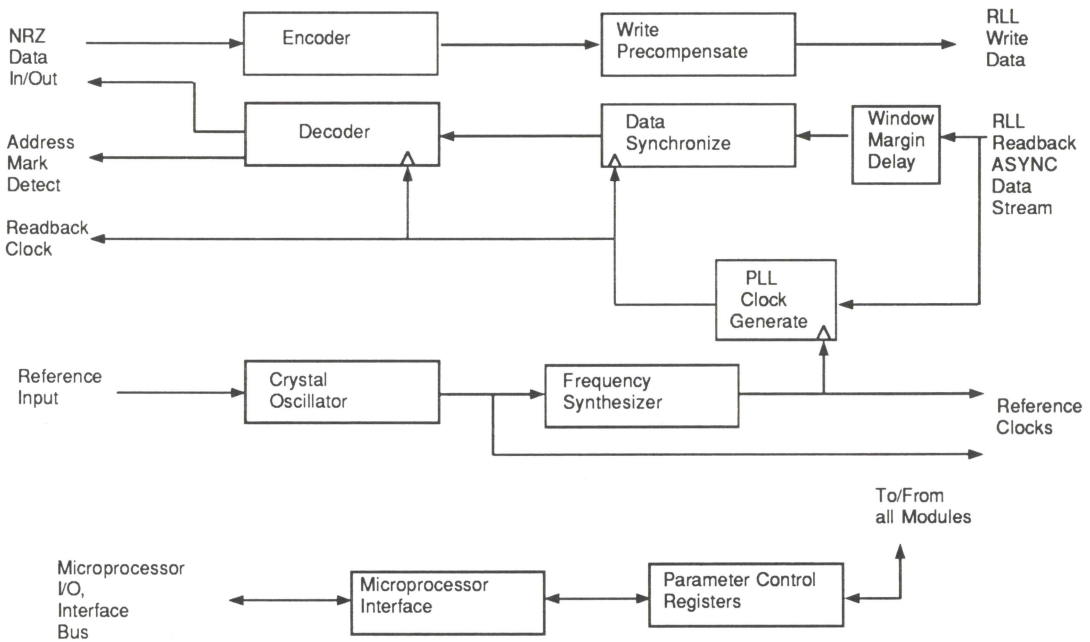
XR-9080 WRITE REGISTER TIMING

Fig. 1



XR-9080 READ REGISTER TIMING

Fig. 2



Note: Above is a simplified overview, not all control, clock, and mode switching signals are shown.

Figure 3. Simplified Functional Overview

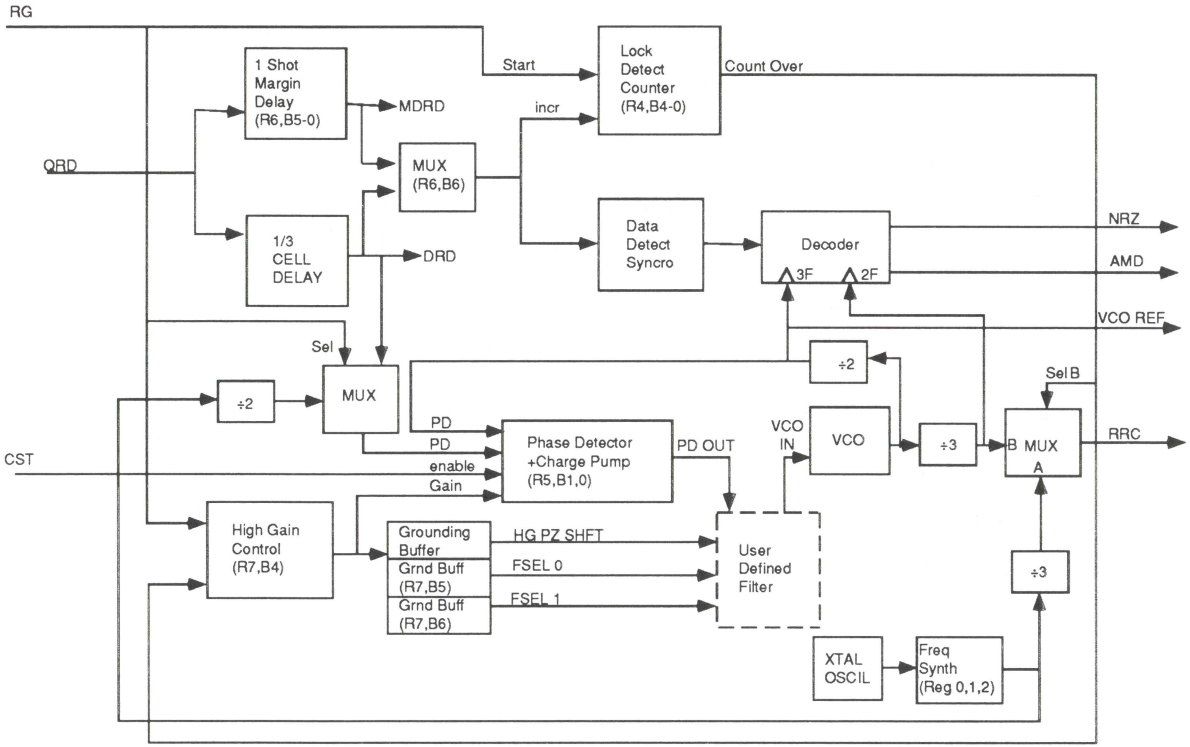
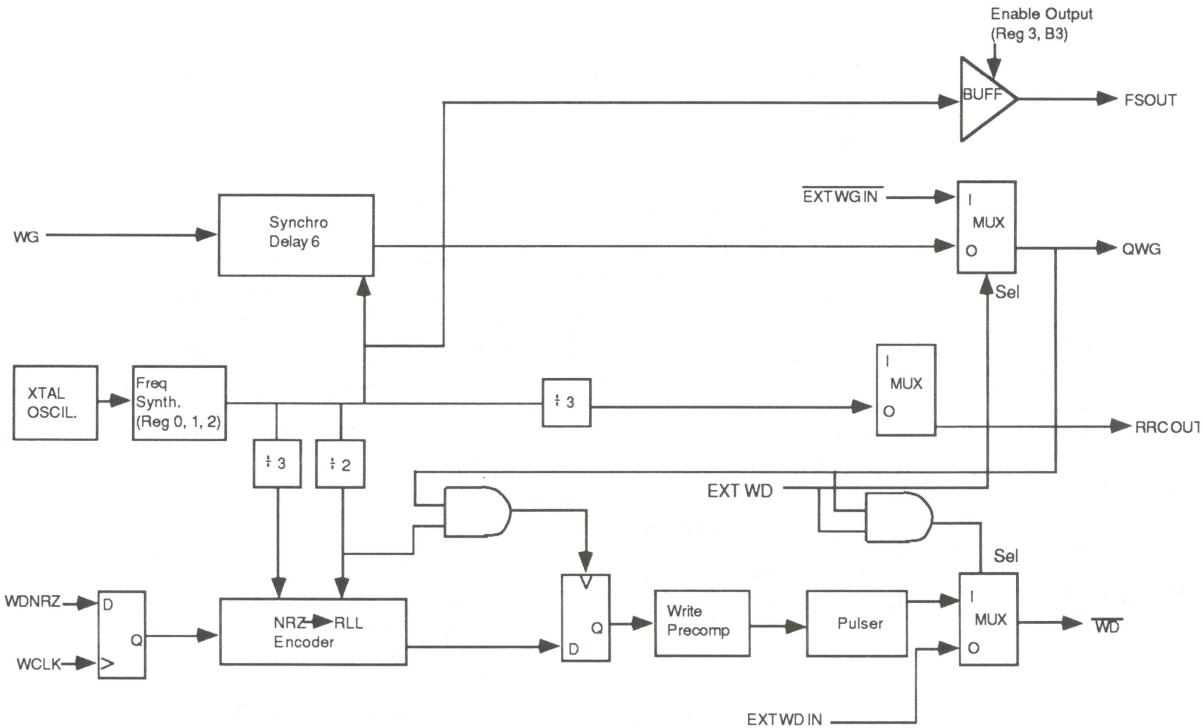


Figure 4. Read Process - 9080



Note: WCLK and the XTAL oscillator must be phase locked for proper Encoder functioning. Generally done by using frequency synthesizer as the WCLK source.

Figure 5. Write Process - 9080

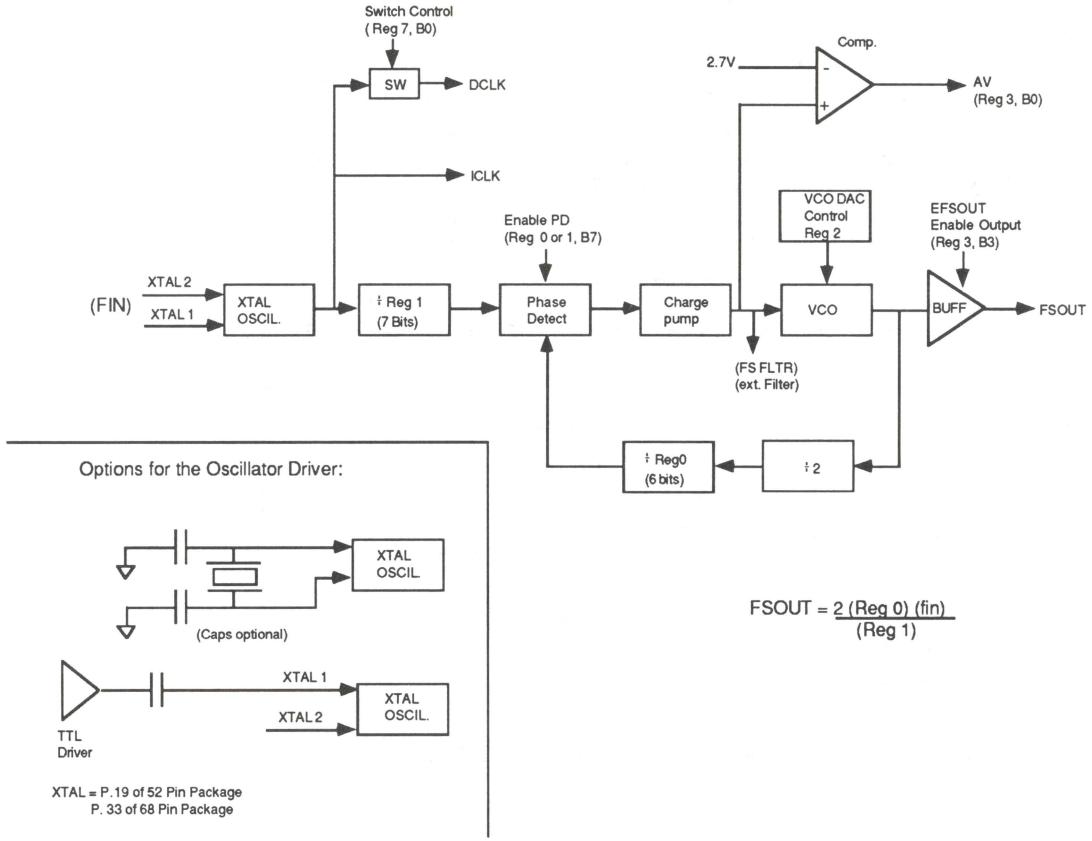


Figure 6. Frequency Synthesizer - 9080

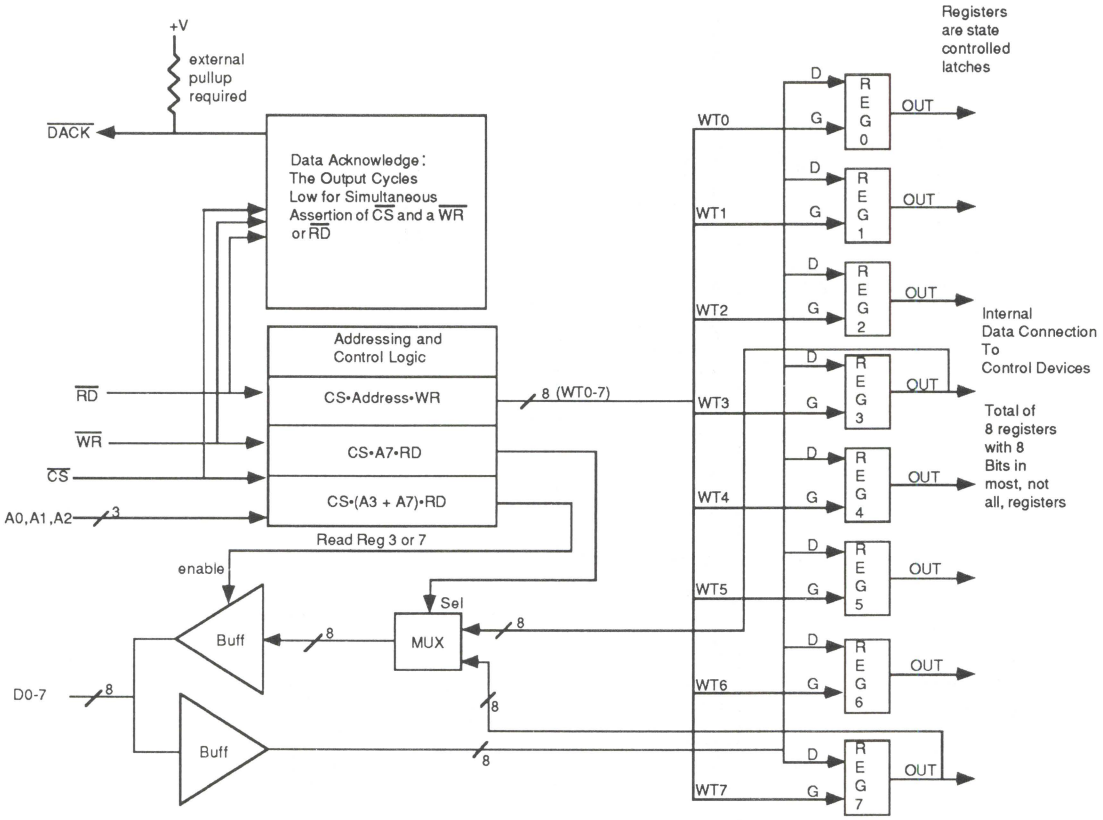


Figure 7. Microprocessor Interface

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ADVANCED CONSUMER PRODUCTS

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Application Notes

AN-35 A Square Wave to Sine Wave Converter Using the XR-1015 5-149

Advanced Consumer Product Selection Guide

Part Number	Description	Product Features	Technology	Supply Voltages	Package
Filters					
XR-1001/8	General Purpose Low Pass Filters	Butterworth, Bessel, & Chebyshev On-board Oscillator	CMOS	4.5 to 11V or ±2.25 to ±5.5V	8 pin DIP
XR-1010	Dual Second Order Switched Capacitor Filter	Shape Programmable	CMOS	+3 to +5.25V	20 pin DIP 20 pin SO
XR-1015/16	Seventh Order Switched Capacitor Filters	Elliptic On-board dual Op-Amp	CMOS	5 to 10.5V or +3/-2 to +5.25V	8 pin DIP 16 pin DIP 16 pin SO
XR-1020	Telecom Instrumentation Filter	10 test filters for IEEE / Bell and CCITT µP Interface	CMOS	9.5 to 10.5V or +4.75 to +5.25V	28 pin DIP
Equalizers					
XR-1091	7-Band Graphic Equalizer Display Filter	Left / Right Sum ESD Protection	CMOS	+4.75 to +6.25V	16 pin DIP
XR-1092	12-Band Graphic Equalizer Display Filter / Multiplexor	Left / Right Sum 3 Aux Inputs Output Mux	CMOS	+4.75 to +6V	20 pin DIP
XR-1093	5-Band Graphic Equalizer Display Filter	Cascadable for 10-Band	CMOS	+4.75 to +6V	14 pin DIP
XR-1094	5-Band Graphic Equalizer Display Filter	40V VFD Driver Peak Hold Driver DIM Control	CMOS	+4.5 to +6V	32 pin DIP
XR-1095	7-Band Graphic Equalizer Display Filter/ Driver w/µP Interface	40V VFD Driver Peak Hold Driver AUX Driver DIM Control µP Interaface Left / Right Sum	CMOS	+4.5 to +6V	42 pin DIP
XR-1096	7-Band Graphic Equalizer Display Filter / Driver	40V VFD Driver Peak Hold Driver DIM Control Left / Right Sum	CMOS	+4.5 to +6V	32 pin DIP

Part Number	Description	Product Features	Technology	Supply Voltages	Package
Equalizer (continued)					
XR-1097	7-Band Graphic Equalizer Display Filter w/ADC	On-board ADC 2 AUX Inputs µP interface Left / Right Sum	CMOS	+4.75 to +6V	14 pin DIP
Audio					
XR-5383	BBE® Sound Enhancement Processor	Monaural	Bipolar	6 to 32V or +3 to +16V	22 pin DIP
XR-5410	BBE® Low Voltage Stereo Sound Enhancement Processor	Stereo Low Voltage	Bipolar	1.6 to 3.0V	32 pin QFP
XR-5451	BBE® Stereo Sound Enhancement Processor	Stereo	Bipolar	6 to 24V or +3 to +12V	32 pin DIP
XR-1071	BBE®II High Definition Audio Processor	Improved Stereo Bass Boost	Bipolar	6 to 24V or +3 to +12V	32 pin DIP
Other Consumer					
XR-1080	8mm VTR ATF	Pilot Generator, Pilot Detector, Video Detector and VGCA, CLOG & SP/LP	CMOS	4.75 to 5.5V	48 pin VQFP
XR-8000/1	Microprocessor Support IC	5V/50mA Reg Reset Control Watchdog Mon	Bipolar	7 to 24V	8 pin DIP
XR-8073	Micropower Step-up Switching Regulator	0.9V min Input, Sleep Mode, Low Batt Detect	Bipolar	0.9 to 20V	8 pin DIP 8 pin SO

General Purpose Low Pass Filter

GENERAL DESCRIPTION

Each of these devices in the series is a fourth order switched capacitor low pass filter providing 24dB/octave (Butterworth) of roll off outside of the pass band, Within this series, Butterworth, Bessel or Chebyshev (0.5 or 0.1dB of ripple) filter responses can be obtained. Also, each filter response is available in either a 50:1 or 100:1 clock-to-corner ratio device for added flexibility. All devices have the same pin out (8 pin dual-in-line), so one can easily be substituted for the other, depending on the application.

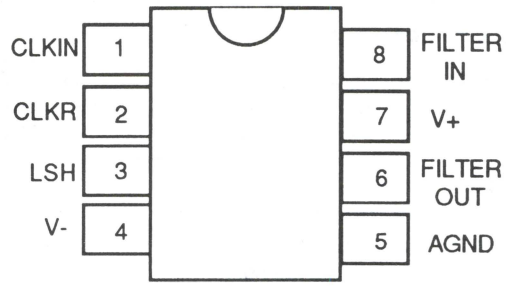
Switched capacitor filters provide the ability to tune the corner frequency of the filter response with the adjustment of the input clock. The XR-1001/1008 can also be used in a stand alone mode, where an external resistor and capacitor will set the input clock frequency. For additional precision, a external crystal can be used to set the corner frequency.

The XR-1001 is pin-for-pin compatible with the MF-4-100 and the XR-1002 in pin-for-pin compatible with the MF- 4-50. The XR-1001/1008 are fabricated in 3 micron dual-polysilicon gate single metal CMOS for additional performance over other processes.

FEATURES

Single 5 Volt Operation
Low Power Consumption
Precise Filter Positioning
Stand Alone Mode with RC or Crystal
Low Noise — Typically –78dBm
Corner Frequency Adjustable to 40kHz

PIN ASSIGNMENT



APPLICATIONS

Mechanical Processes
Telecommunications
Instrumentation
Anti-alias Filters
Reconstruction Filters
Digital Signal Processing
Musical Effects

ABSOLUTE MAXIMUM RATINGS

Power Supply (Single Supply)	14V
Input Signal Level	V^+ –0.7 to V^- +0.7V
Power Dissipation (Package Limitation)	
Ceramic Package	385mW
Derate Above T_A = 25°C	5mW/°C
Plastic Package	300mW
Derate Above T_A = 25°C	6mW/°C
Storage Temperature Range	–65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Response/Ripple	f_{clock}/f_{corner}	Operating Temperature
XR-1001CP/CN/D	Plastic/Ceramic/SO	Butterworth	100:1	0°C to 70°C
XR-1002CP/CN/D	Plastic/Ceramic/SO	Butterworth	50:1	0°C to 70°C
XR-1003CP/CN/D	Plastic/Ceramic/SO	Bessel	100:1	0°C to 70°C
XR-1004CP/CN/D	Plaslic/Ceramic/SO	Bessel	50:1	0°C to 70°C
XR-1005CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.1dB)	100:1	0°C to 70°C
XR-1006CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.1dB)	50:1	0°C to 70°C
XR-1007CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.5dB)	100:1	0°C to 70°C
XR-1008CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.5dB)	50:1	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1001 and XR-1002 with their Butterworth filter responses are suitable for applications where the pass band must be maximally flat, such as instrumentation. The XR-1003 and XR-1004 with Bessel filter response have a maximally flat group delay response. This is ideal for telecommunication and modem applications where phase distortion would affect the performance. The XR-1005 through XR-1008 provide Chebyshev filter response. With Chebyshev filter response, the roll-off outside of the pass band is steeper and attenuates out-of-band signals greater than the Bessel or Butterworth responses. The ripple in the band is larger to obtain the steeper roll-off. The application will determine the amount of ripple which can be accepted within the pass band of the filter response.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 5$ VDC, $V^- = -5$ VDC, $f_{CLOCK} = 1$MHz, $R_{Load} = 1M\Omega$, $C_{Load} = 40$pF, $T_A = 25°C$, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
GENERAL CHARACTERISTICS						
V_{DD}	Supply Voltage					
	Single Supply	4.5		11.0	VDC	Referenced to V_{SS}(Pin 4)
	Split supply	+2.25		5.5	VDC	Refrenced to AGND (PIn 6)
V_{SS}	Supply Voltage					
	Split supply	–5.5		–2.25	VDC	Referenced to AGND (Pin 6)
I_{DD}	Supply Current					
	Single Supply		2.5	3.5	mA	V_{DD} = 10.0 VDC
	Split supply		2.5	3.5	mA	V_{DD} = 5 VDC
	Split Supply		1.50	2.25	mA	V_{DD} = 2.25 VDC
I_{SS}	Supply Current					
	Split supply	–3.5	–2.5		mA	V_{DD} = 5.0 VDC, V_{SS} = –5.0 VDC
	Split Supply	–2.25	–1.5		mA	V_{DD} = +2.25 VDC, V_{SS} = –2.25
FILTER CHARACTERISTICS						
$f_{CLOCKMAX}$	Upper Clocking Freq. Limit	1.0	1.5		MHz	
$f_{CLOCKMIN}$	Lowest Practical Clock		100		Hz	For 1001,1003,1005,1007
			50		Hz	For 1002,1004,1006,1008
	Gain at Corner Frequency	–3.5	–3	–2.5	dB	
A_2f_{corner}	Attenuation at 2 Times	23	24.6	26	dB	For 1001,1002
	The Corner Frequency	11	13	14	dB	For 1003,1004
		30	31	33	dB	For 1005,1006
		33	34	36	dB	For 1007,1008
V_{OUT}	Maximum Output Signal	8			Vpp	Input = ±4.2 VDC
$e_{n\ out}$	Output Noise		0.5		mVrms	From 1Hz to 25kHz
S/N	Signal-to-Noise Ratio		84		dB	
THD	Total Harmonic Distortion		0.1		%	V_{IN} = 2.4Vrms, f_{IN} = 1kHz
V_{OS}	Output Offset Voltage (DC)	–0.4		+0.4	VDC	f_{clock} = 1MHz
	Clock Feedthrough		50		mVpp	
I_{OSS}	Output Short Circuit Current					
	Source	–60	–50		mA	See Note *1
	Sink		30	50	mA	
	Temperature Coefficient of f_{corner}		±35		ppm/°C	From –40°C to +85°C not lested in production
	Passband Gain					
	For 1001,1002	–0.3	0	+0.3	dB	Tested at 3 and 5kHz for
	For 1003,1004	–1.0	–0.1	+0.2	dB	1001,1003,1005,1007
	For 1005,1006	–0.4	–0.1	+0.3	dB	Tested at 6 and 10 kHz for
	For 1007,1008	–0.7	–0.2	+0.3	dB	1002,1004,1006,1008

Note 1: Caution should be used so that the power dissipation does not exceed the package limitation.

ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: $V^+ = 5$ VDC, $V^- = -5$ VDC, $f_{CLOCK} = 1$MHz, $R_{Load} = 1M\Omega$, $C_{Load} = 40$pF, $T_A = 25°C$, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
FILTER CHARACTERISTICS (Continued)						
	Passband Gain					
	For 1001,1002	−0.7	−0.06	−0.0	dB	Tested at 7.5kHz for
	For 1003,1004	−2.0	−1.5	−1.0	dB	1001,1003,1005,1007
	For 1005,1006	−0.3	−0.1	+0.3	dB	Tested at 15kHz for
	For 1007,1008	−0.7	−0.2	+0.3	dB	1002,1004,1006,1008
FILTER CHARACTERISTICS: $V^+ = +2.25$, $V^- = -2.25$ VDC						
$f_{CLOCKMAX}$	Upper Clocking Freq. Limit	0.25	0.5		MHz	
$f_{CLOCKMIN}$	Lower Practical Clock		100		Hz	For 1001,1003,1005,1007
			50		Hz	For 1002,1004,1006,1008
A_2f_{comer}	Attenuation at 2 Times	23	24.6	26	dB	For 1001,1002
	The Corner Frequency	11	13	14	dB	For 1003,1004
		30	31	33	dB	For 1005,1006
		33	34	36	dB	For 1007,1008
	Maximum Output Signal	3	4		Vpp	$V_{IN} = \pm 2.0$ VDC
S/N	Signal-to-Noise Ratio		76		dB	
V_{OS}	DC Offset voltage	−0.4	±0.05	+0.4	VDC	
LOGIC INPUT & LOGIC OUTPUT TESTS: $V = \pm 2.25$ VDC and $V = \pm 5$ VDC, Pin 3 tied to V_{SS}						
	Schmitt Trigger Input					
V_{T+}	Positive Going Threshold Voltage	0.6	1.3	2.0	V	$V = \pm 5.0$ VDC
		0.0	0.55	+1.1	V	$V = \pm 2.25$ VDC
V_{T-}	Negative Going Threshold Voltage	−1.4	−0.7	0.0	V	$V = \pm 5.0$ VDC
		−0.6	−0.2	+0.4	V	$V = \pm 2.25$ VDC
$V_{T+} - V_{T-}$	Hysteresis	0.8	2.1	2.9	V	$V = \pm 5.0$ VDC
		0.2	0.75	1.3	V	$V = \pm 2.25$ VDC
V_{OH}	Output High Voltage	4.5			V	$V = \pm 5.0$ VDC
		2.03			V	$V = \pm 2.25$ VDC, $I_O = 400\mu A$
V_{OL}	Output Low Voltage			1	V	$V = \pm 5.0$ VDC
				0.5	V	$V = \pm 2.25$ VDC, $I_O = -400\mu A$
I_{OS}	Output Sink Current		-5.0	-2.5	mA	$V = \pm 5.0$ VDC
			-1.3	-0.65	mA	$V = \pm 2.25$ VDC
	Output Source Current	3.0	6.0		mA	$V = \pm 5.0$ VDC
		0.75	1.5		mA	$V = \pm 2.25$ VDC
TTL CLOCK INPUT: $V = \pm 5.0$ VDC, Pin 3 tied to 0 VDC						
V_{IL}	Input Low Voltage		0.8		V	
V_{IH}	Input High Voltage		2.8		V	
STAND ALONE OPERATION: $R = 5.0k\Omega$ and $C = 120$pF for $f_O = 985$kHz						
f_O	Frequency Accuracy of Osciltator	−15	±4	+15	%	Measured at Pin 2 Error increases at lower f_O (< 500kHz). See Figure 3.

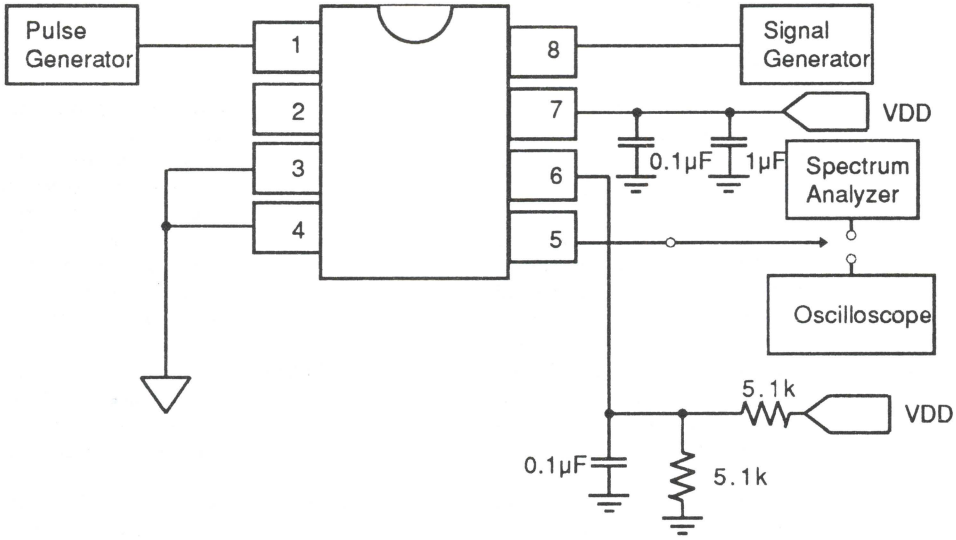


Figure 1. Single Supply Test Circuit

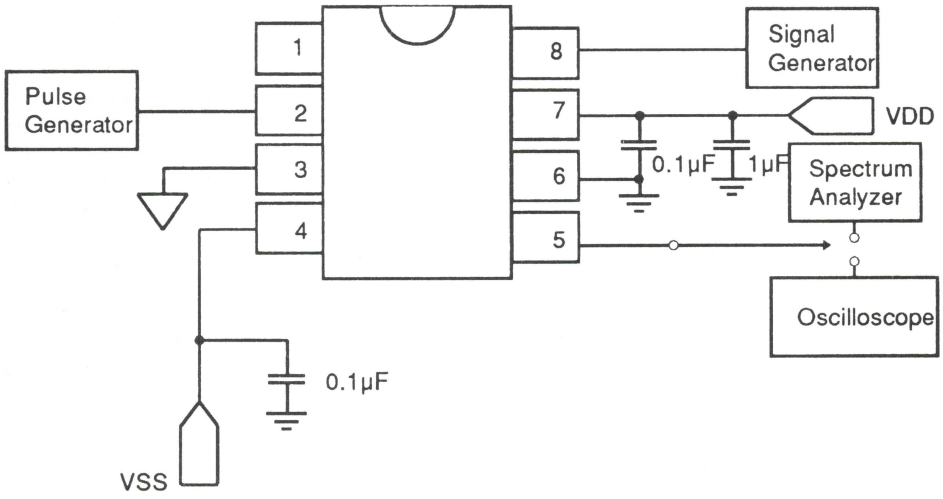


Figure 2. Split Supply Test Circuit

XR-1001/1008 PIN DESCRIPTIONS

Pin#	Symbol	Description
1	CLKIN	*Clock Input:* This input pin is for application of the MOS-level clock used for sampling and switching. For best results, this clock should be approximately 50% duty cycle. A crystal can be used from Pin 1 to Pin 2 to create a self-contained oscillator. A 10MΩ resistor should be hooked up in parallel with the crystal The maximum clock frequency is > 1MHz. For stand alone operation with a resistor and capacitor, the capacitor should be tied from this point to ground.
2	CLKR	*Clock Resistor:* This is an inverted output of signal found on Pin 1. It is used for creating a crystal oscillator or for an RC network. The resistor would be tied back to Pin 1. The frequency of osciillation would be equal to 1/(1.7 x RC). It is also used as the TTL-level clock input. Figure 4 shows the connections for RC mode.
3	LSH	*Level Shift:* This input is used to set the logic zero point of the clock input. For MOS level clocks, it should be tied to V_{SS}. For TTL-level clock. it should be grounded (split supply). For single supply operation, MOS level clock operation is recommended. When a crystal and resistor or a resistor and capacitor are used to create an oscillator, the level shift pin should be tied to V_{SS}.
4	V−	*V_{SS}:* This is the negative supply. It should have substantial decoupling to prevent noise on the output of the filter. A minimum 0.1µF capacitor to ground as close to the device as possible is strongly recommended. The range of operation for dual supplies is from –2.5 VDC to –5 VDC. This device can also be operated from ground positive. In this case, the V_{SS} pin is tied to the analog ground of the circuit. The quality of the ground in this mode of operation is very important. It should have very low series inductance.
5	FILTEROUT	*Filter Ouput:* This is the output of the low pass filter. A 10kΩ load or larger is the smallest load recommended for the output.
6	AGND	*Analog Ground:* This should be tied to the analog ground of the circuit in which the device is being used. The filter output of this device will swing around this potential. For single supply operation, this pin is externally biased at a point one half of the VDD voltage. A 0.1µF capacitor is the minimum capacitance needed for decoupling with single supply operation.
7	V+	*V_{DD}:* The positive supply is tied here. Since this pin is also common with the substrate, a 0.1µF and 1µF capacitor to ground are recommended to decouple any noise on the positive supply. The range of operation is from +5 to +10 VDC for single supply operation. For dual supply operation, +2.5 to +5 VDC can be applied to this pin.
8	FILTERIN	This is the input of the low pass filter. The input signal should be biased to mid-supply before applying to this pin. Also, to prevent alias frequencies from being created, the input frequency should be less than 1/2 of the clock frequency.

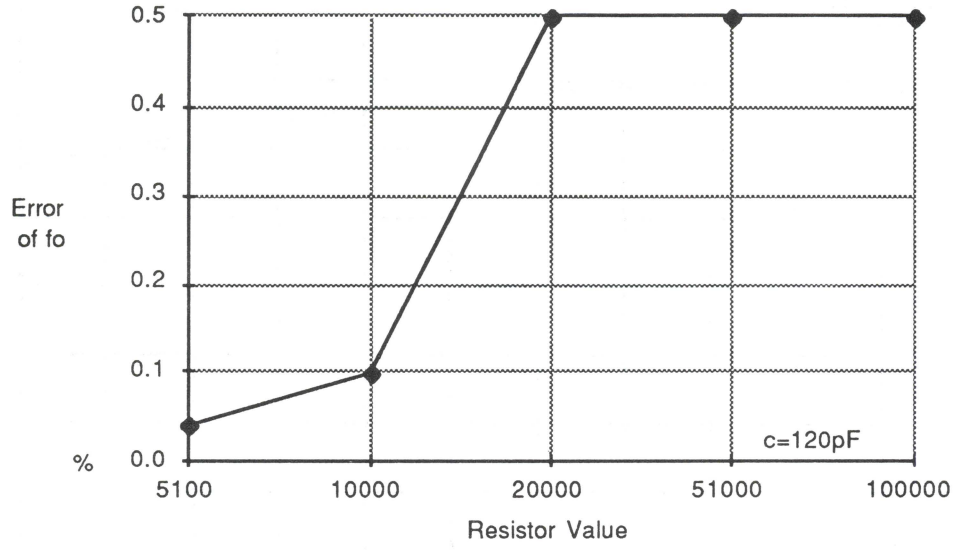


Figure 3. Error vs Timing Resistor

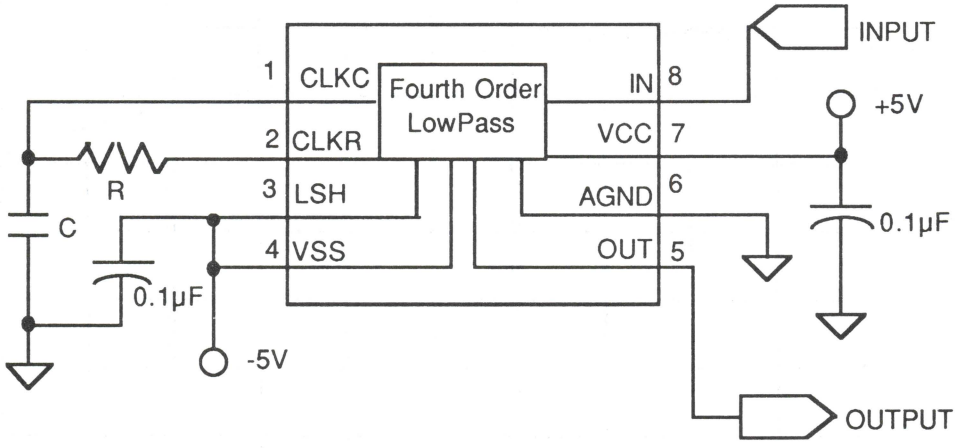
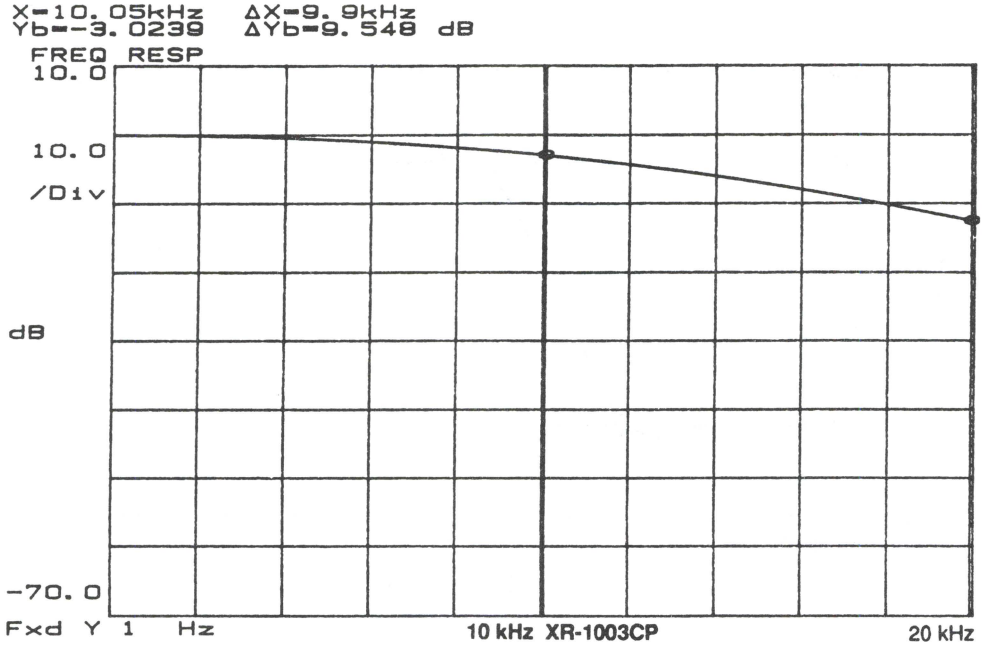
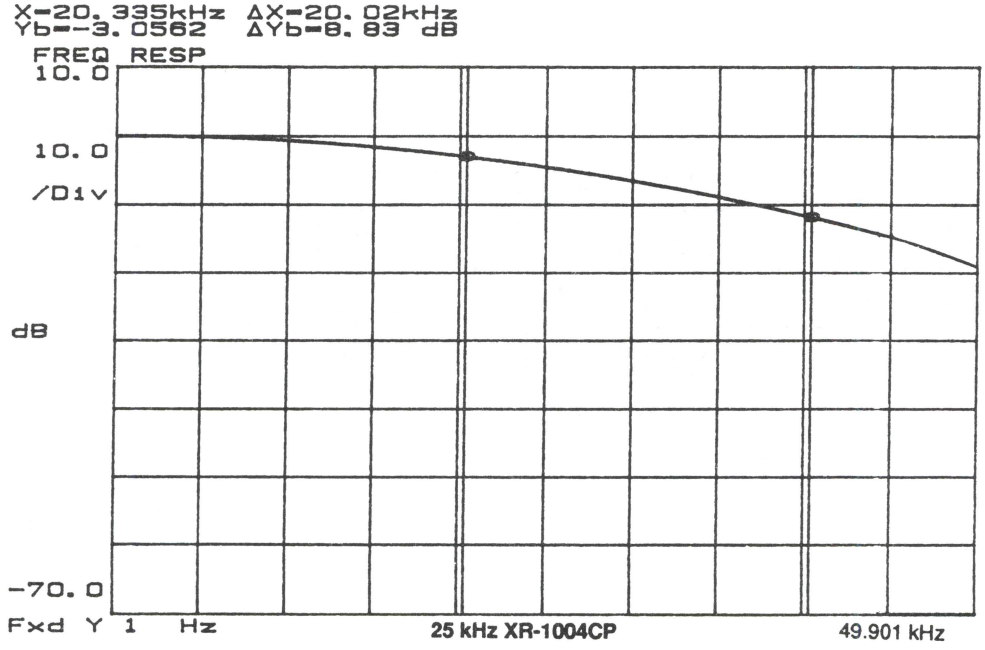
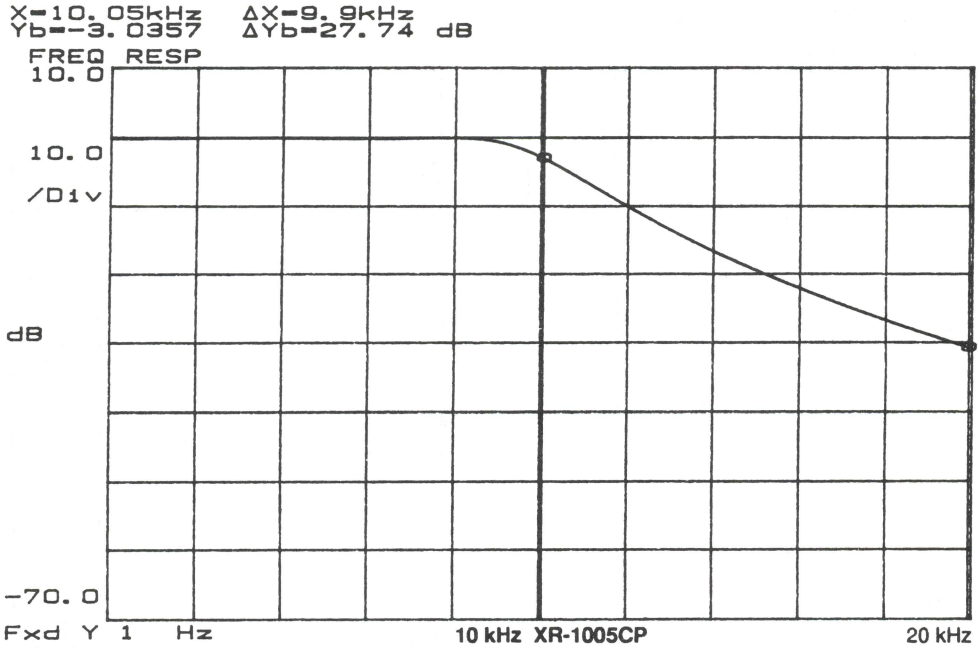
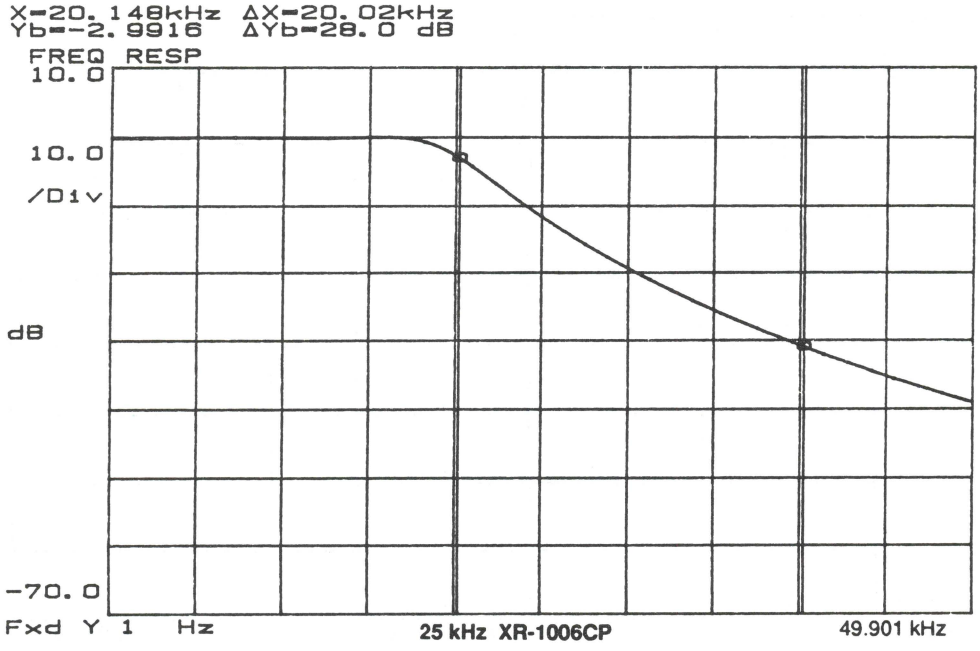


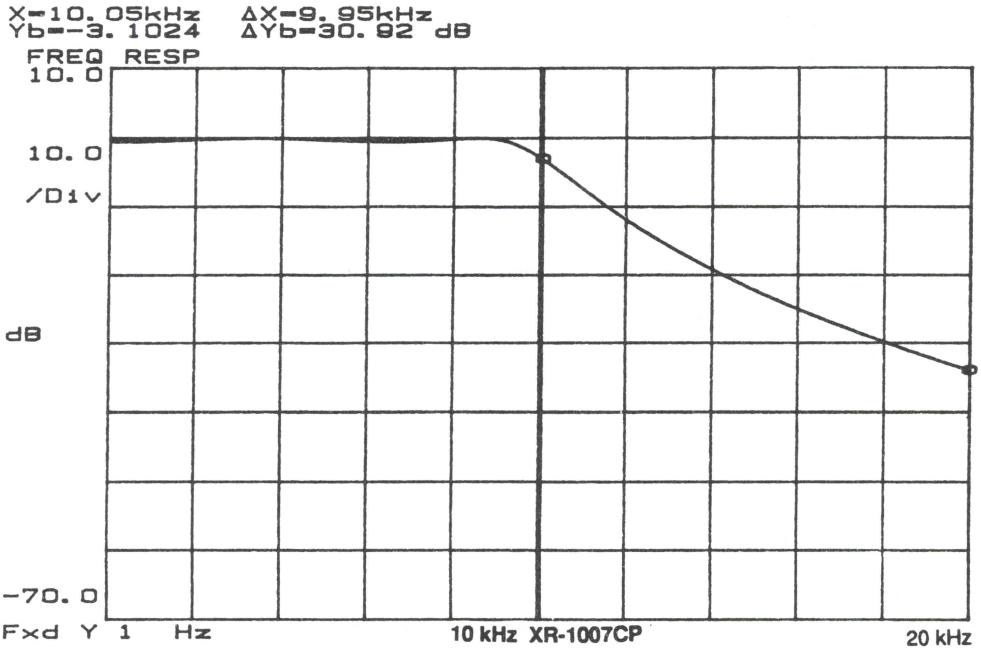
Figure 4. Operation of XR-1001/8 In RC Mode

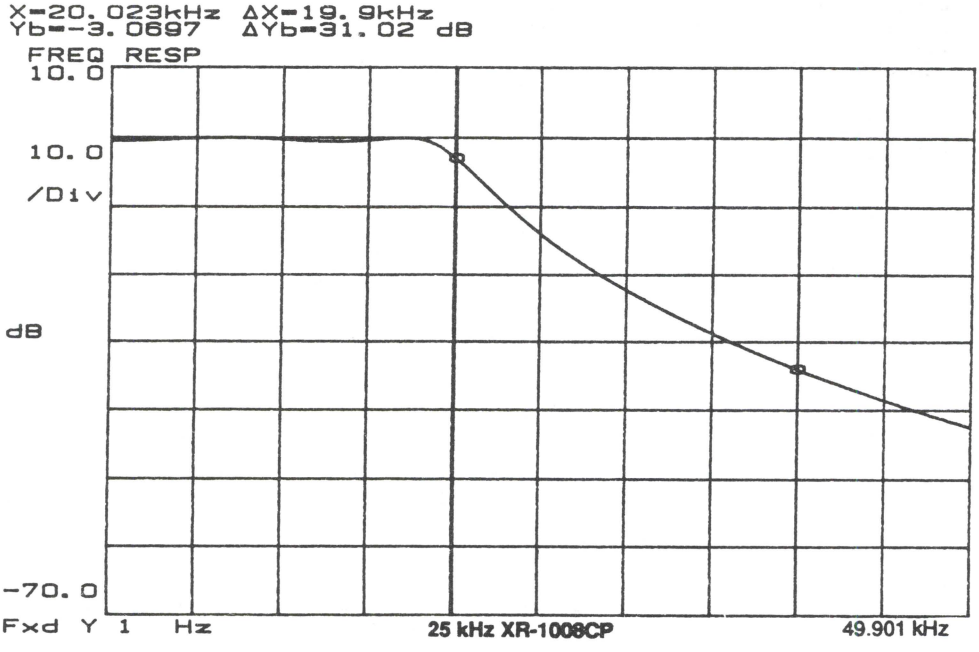

X=10.05kHz ΔX=9.9kHz
Yb=-3.0239 ΔYb=9.548 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1003CP
20 kHz


X=20.335kHz ΔX=20.02kHz
Yb=-3.0562 ΔYb=8.83 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1004CP
49.901 kHz


X=10.05kHz ΔX=9.9kHz
Yb=-3.0357 ΔYb=27.74 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1005CP
20 kHz


X=20.148kHz ΔX=20.02kHz
Yb=-2.9916 ΔYb=28.0 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1006CP
49.901 kHz


X=10.05kHz ΔX=9.95kHz
Yb=-3.1024 ΔYb=30.92 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1007CP
20 kHz


X=20.023kHz ΔX=19.9kHz
Yb=-3.0697 ΔYb=31.02 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1008CP
49.901 kHz

Second Order Switched Capacitor Filter

GENERAL DESCRIPTION

The XR-1010 is a fully adjustable dual second order switched capacitor filter. With the intermediate nodes of the switched capacitor filter brought out, many different filter functions can be obtained. One half of the XR-1010 is composed of an operational amplifier, and two switched capacitor integrators. With the use of external resistors, to adjust the amplitude of the feedback, notch, band pass, all pass, low pass and high pass filter functions can be obtained.

By cascading the two halves of the XR-1010, a fourth order filter can be obtained. With the use of additional XR-1010, higher order filters can be obtained.

The XR-1010 is fabricated in polysilicon gate 3-micron CMOS. With single +6 VDC operation (at 250kHz) low power consumption can be obtained.

FEATURES

Easy to Use: Simple resisitor divider equations for filter Q
No External Capacitors Needed to Set Corner Frequency
Cascadable to Obtain Higher Order Filter Functions
Pin-for-Pin Compatible With the National Semiconductor MF-10

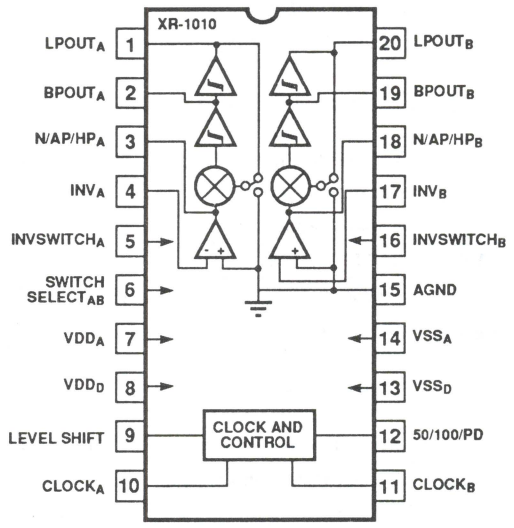
APPLICATIONS

Low Pass, High Pass, Band Pass, Notch & All Pass Filters
Group Delay Compensation Filtering
Modem Filters (CCITT V.21, V.23, V.26)
Band Separation for Analog Front End
Linear Phase Filtering (All Pole Filtering)
Loop Filter for Phase-Lock Loops

ABSOLUTE MAXIMUM RATINGS

Power Supply	14 V_{DC}
Input Signal Level (Logic)	V_{DD} +0.3 to V_{SS} –0.3 V_{DC}
Power Dissipation (Package Limitation)	
Ceramic Package	1.3W
Derate Avove 25°C	5 mW/°C
Plastic Package	1.0W
Derate Above 25°C	8 mW/°C
Storage Temperature	–55°C to +160°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1010N	Ceramic	–40°C to +85°C
XR-1010P	Plastic	–40°C to +85°C
XR-1010CN	Ceramic	0°C to +70°C
XR-1010CP	Plastic	0°C to +70°C
XR-1010CD	JEDEC SO	0°C to +70°C
*XR-1010A	JEDEC SO	–40°C to +85°C

**Consult factory for availability.*

SYSTEM DESCRIPTION

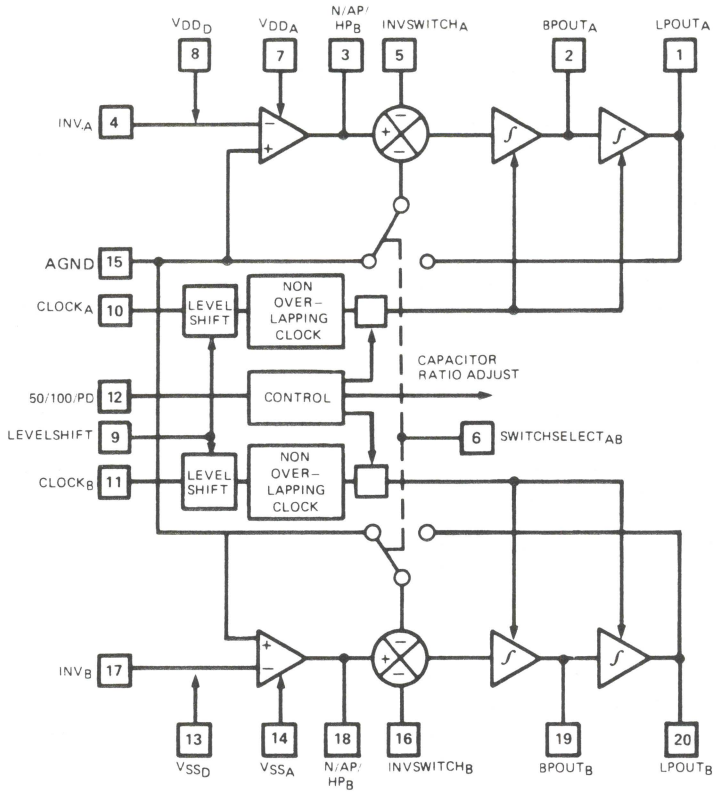
The XR-1010 can be operated with either dual supplies or with a single supply. The center frequency of the filter response is set precisely by the clock frequency. This clock to center ratio can be changed with the use of the 50/100/PD pin on the XR-1010. Either TTL or CMOS clocks can be used.

With the use of external resistors to control the amplitude of the feedback, many different filter functions can be obtained with the XR-1010. Simple algebraic calculations allow for the determination of the values of the resistor to obtain the filter shape needed.

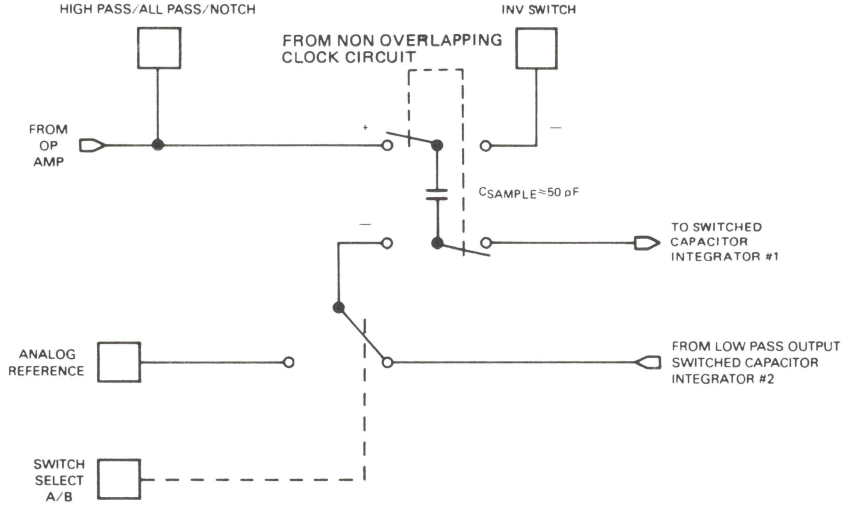
ELECTRICAL CHARACTERISTICS

Test conditons: $V^+ = 5V$, $V^- = -5V$, $f_{clock} = 1MHz$, $R_{load} = 1\ M\Omega$, $C_{load} = 40pF$, $T_A = 25°C$: Mode 1 with R1 = 100kΩ, R2 = 10kΩ, and R3 = 100kΩ, unless specified otherwise.

SYMBOL	PARAMETERS	XR-1010/A MIN	XR-1010/A TYP	XR-1010/A MAX	XR-1010C MIN	XR-1010C TYP	XR-1010C MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS									
V_{DD}	Positive Supply Voltage	3	5.0	5.25	3	5.0	5.25	V V	f_{clock} = 1MHz f_{clock} = 250kHz
V_{SS}	Negative Supply Voltage	−5.25	−5.0	−3	−5.25	−5.0	−3	V V	f_{clock} = 2MHz f_{clock} = 250kHz
I_{DD}	Current on V_{DD}		10	15		10	15	mA	
I_{SS}	Current on V_{SS}	−15	−10		−15	−10		mA	
I_{PDDD}	Power Down Current		300			300		µA	Pin 12 = −5 VDC
FILTER CHARACTERISTICS									
f_o	Frequency Range	20	30		20	30		kHz	Pin 12 High
f_{clock} / f_o	Clock-to-Corner Frequency Ratio		49.94 99.35	±0.6% ±0.6%		49.94 99.35	±1.5% ±1.5%		Pin 12 High Pin 12 at 0V
Q	Accuracy of f_o bandwidth			±3%			±6%		Q = 10 f_o x Q ≤ 200kHz
f_{clock}	Maximum Clock Frequency	1	1.5		1	1.5		MHz	
$H_{lowpass}$	DC Low Pass Gain Accuracy			12%			12%		
	Crosstalk		70			70		dB	
	Clock Feedthrough		30			30		mVpp	f_{clock} = 1MHz
V_{in}	Maximum Input (Unclipped)	8			8			Vpp	$A_V = 1\ \frac{V}{V}$
THD	Total Harmonic Distortion		0.1%			0.1%			Input Level = 1 Vpp
tco_Q	Temperature Coefficient of Q		700			700		ppm/°C	From −40 to +85°C not tested in production
	Temperature Coefficient of f_o		120			120		ppm/°c	From −40 to +85°C not tested in production
OPERATIONAL AMPLIFIER CHARACTERISTICS									
GBW	Gain Bandwidth Product		2.5			2.5		MHz	
I_{OSS}	Output Short Circuit Current Source Sink		 26 -1.5			 26 -1.5		 mA mA	



Equivalent Schematic Diagram



Detail Switched Capacitor Summer

PRINCIPLES OF OPERATION

The XR-1010 is a dual second order switched capacitor state variable filter. Since the state variable filter provides all of the basic filter functions at the same time, it is the most versatile building block to use. With only a few external feedback resistors, band pass, low pass, high pass, notch, and all pass filter functions can be obtained.

With the switched capacitor implementation of the state variable filter, capapcitors, switched at a certain frequency will simulate resistors of a particular value. To allow greater flexibility, the feedback resistors to create the particular filter function are external to the device.

Since switched capacitor filters are sampled data systems, in that they divide a a continuous time signal into samples of charge, some thought must be given to out-of-band signals causing an aliased component to appear in the band of interest. To prevent the appearance of aliased signals, there should be at least two samples per cycle of signal applied to the input of the XR-1010. The sampling frequency of the filter is 1/2 of the clock frequency applied to Pin 10 and 11.

One reference on the subject of sampled data systems is the book "Digital Signal Processing" by Oppenheim and Schaffer, published by Prentice Hall. This book fully covers the concept of aliased signals as well as the Nyquist Criteria.

PIN DESCRIPTIONS

Pin#	Symbol	Desciption
1	$LPOUT_A$	*Low Pass Output A:* The output of the second switched capacitor integrator. The low pass filter function is obtained at this pin. It can typically drive a 10kΩ load.
2	$BPOUT_A$	*Band Pass Output A:* The output of the first switched capacitor integrator. The bandpass filter function would be obtained at this output. This output can typically drive a 10kΩ load.
3	$N/AP/HP_A$	*Notch/All Pass/High Pass Output:* This output provides the notch, all pass or high pass filter functions. The ac-tual filter on the output is dependant upon the connection of external resistors and is described in the section on Modes of Operation.
4	INV_A	*Inverting Input A:* This is the inverting input of op amp A. It is normally used as the input for the filter function. Please note that the input impedance of the filter depends upon the value of the input resistor, R1, when used in some modes of operation. The noninverting input to this operational amplifier is tied internally to the AGND, Pin 15.
5	$INVSWITCH_A$	*Negative Switch Input A:* This input is used for the, filter input in some modes of operation. The input-impedance of this point varies with the clock frequency. For typical operation the source for the signal applied here should be 1kΩ or less.

With a 1 MHz sampling frequency, the input impedance is typically 20kΩ.

6 SWITCHSELECT$_{AB}$ *Signal Switch AB:* This logic input controls the other negative summing input of the filter. When low, the negative input of the summing section of the switched capacitor filter is connected to AGND, Pin 15. If this input is tied high, the other negative summing input is tied internally to the LP output.

With this switch the various filter functions can be implemented.
Please note that this input is not affected by the setting of LEVELSHIFT. A logic low is at V_{SS}; a logic high is at V_{DD}.

7 VDD_A *Analog Positive Supply:* This input provides the positive voltage for the analog portions of the filter. It should be decoupled using a 0.68µF capacitor to ground. If it is known that the noise on the supply is large due to the use of a switching power supply, an additional 10µF capacitor should be used.

8 VDD_D *Digital Positive Supply:* This input provides the positive voltage for the digital portions of the XR-1010. It should be decoupled with a 1.0µF capacitor to digital ground.

9 LEVELSHIFT *Logic Level Select:* This input controls the acceptable clock input swing. With ±5 VDC operation, LEVELSHIFT should be tied to ground. This will allow either TTL or CMOS level clocks to be applied. With single supply operation, this pin should be tied to a voltage that is 1/2 of the algebraic sum of the supply voltages. This will allow input clocks at the V_{SS} level to clock the XR-1010.

10 $CLOCK_A$ *Clock Input A:* This is the clock input for the XR-1010 side A. It must be at the same levels as the clock applied to $CLOCK_B$. The frequency of this clock and the setting of 50/100/PD will determine the center frequency of the filter response.

The sampling frequency is always one half of the clock frequency applied to CLOCK A.

11 $CLOCK_B$ *Clock Input B:* This is the clock input for the XA-1010 side B. The level applied can be either CMOS or TTL depending upon the voltage present on the pin LEVELSHIFT.

12 50/100/PD *Clock to Corner/Power Down:* This input controls the clock to corner ratio as well as providing a power down standby mode. With this pin tied to V_{DD} (digital) the clock to corner ratio is set for 50:1. When this pin is tied to a voltage that is one-half of the sum of the amplitudes of V_{DD} and V_{SS}, the clock to corner ratio is 100:1.

When this pin is tied to V_{SS}, the XR-1010 is in the power down mode and the filter no longer provides an output. If the INVSWITCH input is used, then the input impedance should be infinite. If other modes of operation are used with the op amp the impedance will depend on external resistor values.

13 VSS_D *Negative Digital Supply:* This

5

input provides the negative supply for the digital portions of the XR-1010. It should be decoupled with a 1 μF capacitor to digital ground.

14 VSS_A — *Negative Analog Supply:* This input provides the negative supply for the analog portions of the XR-1010. It should have a 0.68μF ceramic capacitor to decouple any noise to analog ground. If the analog negative supply is known to be noisy such as from a switching power supply, then an additional 1μF capacitor for decoupling of the supply should be used.

15 AGND — *Analog Reference:* This input is used for providing the reference for the analog signals applied to the XR-1010. With equal split supplies, this pin should be tied to the analog ground of the system.

When single supplies or unequal split supplies are used, then this input should be biased to a point that is one half of the algebraic sum of the V_{DD} and V_{SS} voltages. In this application, the AGND pin should be decoupled to the system ground with a 0.68μF capacitor.

16 $INVSWITCH_B$ — *Negative Switch Input B:* This is the negative switch input used for producing the various filter responses. Its input impedance varies with the clocking frequency. When it is being used as an input, the signal source should be 1kΩ or less in output impedance. With a 1MHz sampling clock, the input impedance is typically 20kΩ. As the sampling frequency decreases, the input impedance increases.

17 INV_B — *Inverting Input B:* This is the inverting input of operational amplifier B. It is normally used as the input for the filter function.

18 $N/AP/HP_B$ — *Notch, All Pass, High Pass Output B:* This output provides three of the filter functions as well as a source for feedback for producing other filter functions.

19 $BPOUT_B$ — *Band Pass Filter Output B:* This output provides the band pass filter response as well as a a source for feedback signals for other filter functions.

This output is typically capable of driving a 10kΩ load.

20 $LPOUT_B$ — *Low Pass Filter Output B:* This provides the low pass filter response. It is capable of driving a 10kΩ load.

SELECTION OF MODE

Table 1 shows which mode can provide which filter shape. Also shown in the table is which input is used. This helps to determine the most efficient use of the dual XR-1010 since Pin 6, $SWITCHSELECT_{AB}$ controls both sides of the XR-1010.

If one of the modes selected requires the internal feedback path from the low pass filter output to the switched capacitor summer mode, then the mode for the second half must have the same configuration, although not necessarily the same mode. This is not normally a problem since in most designs, both halves are used to obtain the final filter function needed.

OFFSET VOLTAGES

With any operational amplifier or integrator circuit, some offset voltage is seen on the output. The XR-1010 output offset voltages typically are less than 100mV. This in most applications is neglible.

If the output offset voltage is not acceptable, then typical offset compensation circuits can be employed, as used with any operational amplifier.

TABLE 1
Filter Shapes Available with a Particular Mode

	Mode1	Mode 1a	Mode 2	Mode 3	Mode 3a	Mode 4	Mode 5	Mode 6a	Mode 6b
Low Pass	yes	yes	yes	yes	yes	yes	yes	yes	inv. non-inv.
High Pass	no	no	no	yes	yes	no	*	yes	no
Band Pass	yes	inv. non-inv.	yes	yes	yes	yes	yes	no	no
Notch	yes	no	yes	no	yes	no	yes	no	no
All Pass	no	no	no	no	no	yes	yes	no	no
Input Used	Op Amp	Inv. Switch	OP Amp	OP Amp	OP Amp	OP Amp & Inv. Switch	OP Amp & Inv. Switch	OP Amp	Inv. Switch

* Depends on Band Pass location

GLOSSARY

f_{CLOCK} — The frequency of the clock applied to the switched capacitor filter. It is this clock that will determine the position of the corner or center of the filter (along with 50/100/PD).

f_o — The center frequency of the filter. This also sets the complex pole pair of the filter. Figure 1A shows a normalized complex pole pair on the jω vs. ω axis. Figure 1B shows the response seen on the band pass filter output with this pole pair position. f_{center} corresponds to the peak of the band pass filter.

Q — The quality of the filter. With a band pass filter it is defined as the center frequency of the band pass response divided by the –3dB bandwidth of the band pass filter.

The Q of the filter also indicates the position of the complex conjugate pole positions. Figure 2a shows the position of the complex pole positions and Figure 2b shows its affect on the band pass filter's –3dB bandwidth.

$H_{bandpass}$ — The gain of the band pass filter at $f_o = f_{center}$. This parameter is unit-less.

$H_{lowpass}$ — The gain of the low pass filter as f approaches 0Hz. This is shown in Figure 3.

$H_{highpass}$ — The gain of the high pass filter output as f_o approaches $f_{clock}/2$. This is shown in Figure 4.

Q_{zero} — The quality of the complex zero pair. This specification has no units. It is difficult to measure this specification externally from the band pass output. Figure 5a shows the effect of a particular complex zero position on a output frequency response.

Figure 5b also shows an all pass filter response. This synthesized filter response has no amplitude ripple which would be the ideal response. Figure 5c shows the phase response of the all pass filter.

f_{zero} — The center frequency of the notch as see at the N/AP/HP output. In situations of high Q_{zero}, the f_{notch} will match f_{zero}.

f_{notch} — The center frequency of the notch as seen at the N/AP/HP output. In situations of high Q_{zero}, the f_{notch} will match f_{zero}.

$H_{notch@0}$ — The gain of the notch output as f_{notch} approaches 0Hz.

$H_{notch@f_{clock}/2}$ — The gain of the notch output as f_{notch} approaches $f_{clock}/2$.

5

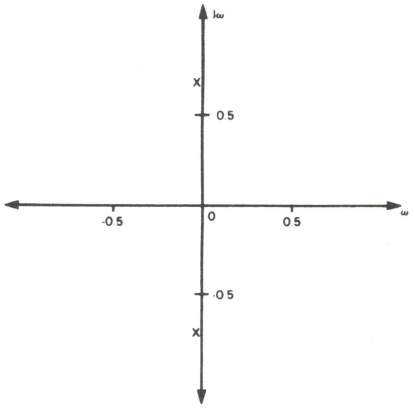


Figure 1A. Band Pass Complex Pole Position

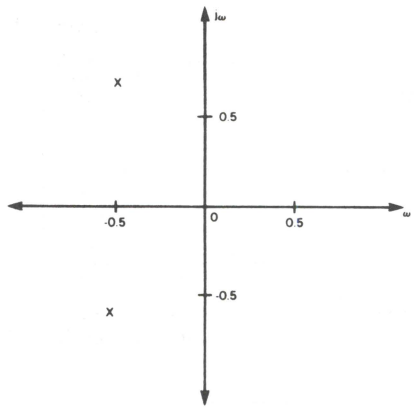


Figure 2A. Low Pass Complex Pole Position

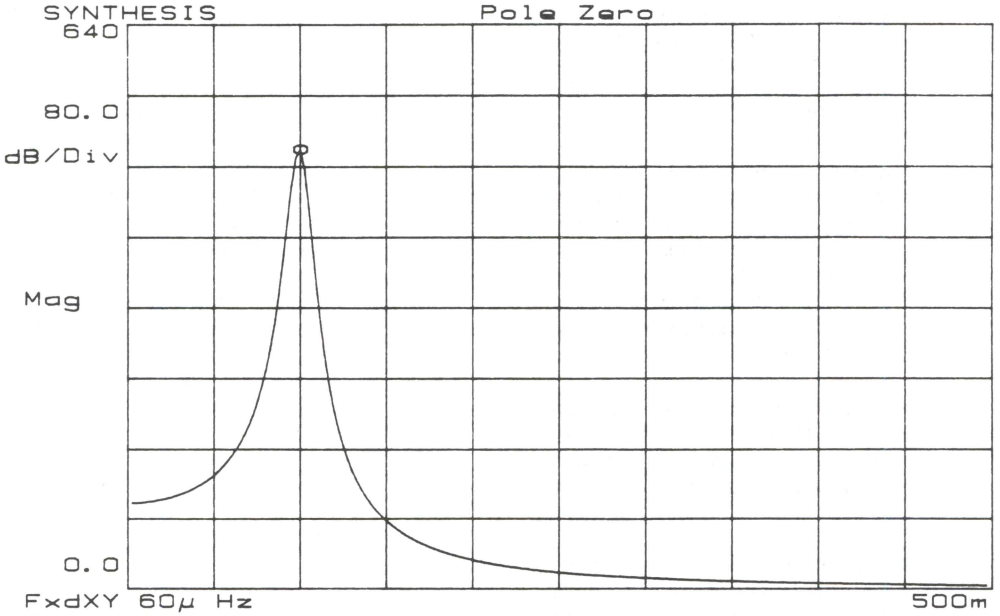


Figure 1B. Band Pass Filter

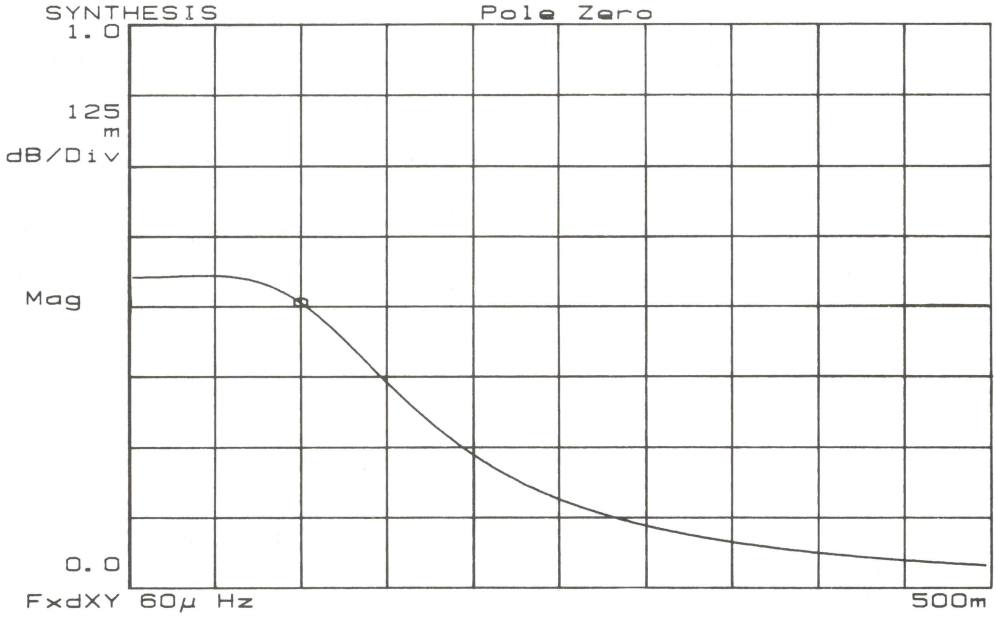


Figure 2B. Low Pass Filter

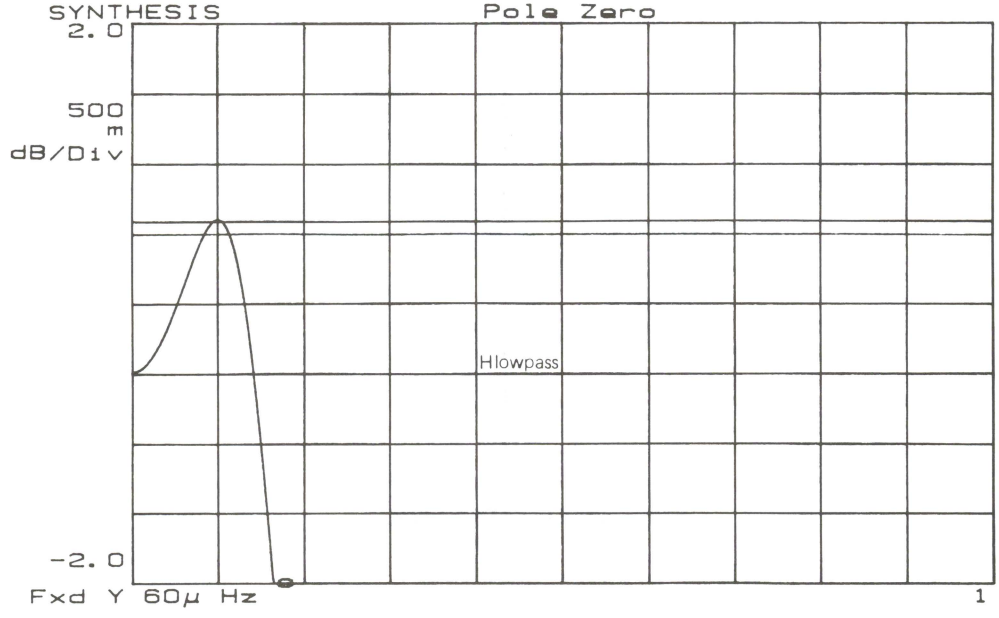


Figure 3. Definition of $H_{LOWPASS}$

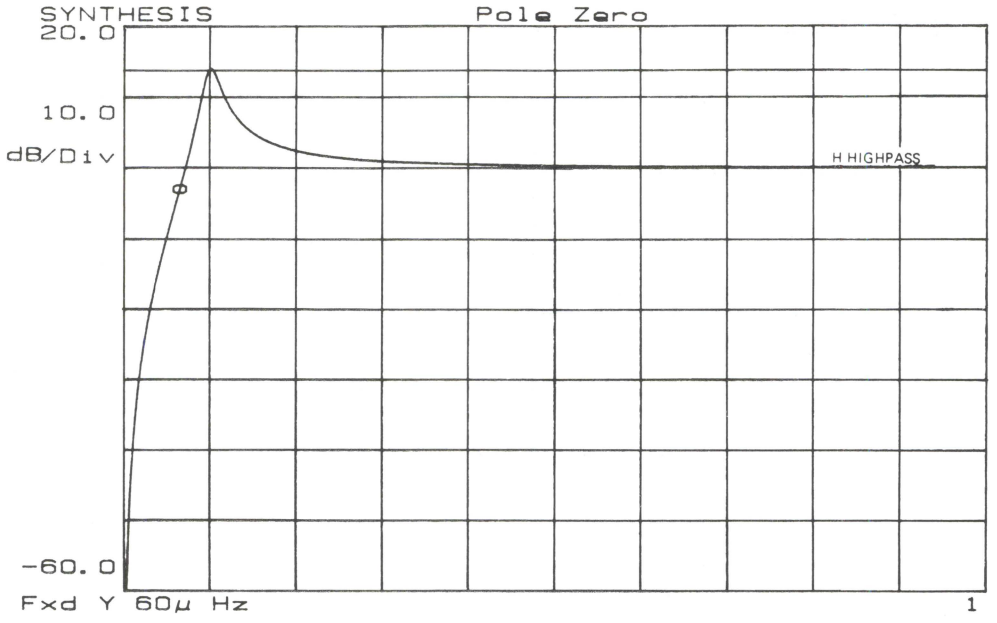


Figure 4. Definition Of $H_{HIGHPASS}$

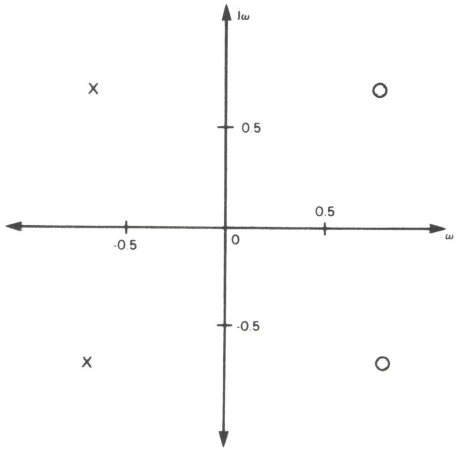


Figure 5A. All Pass Filter

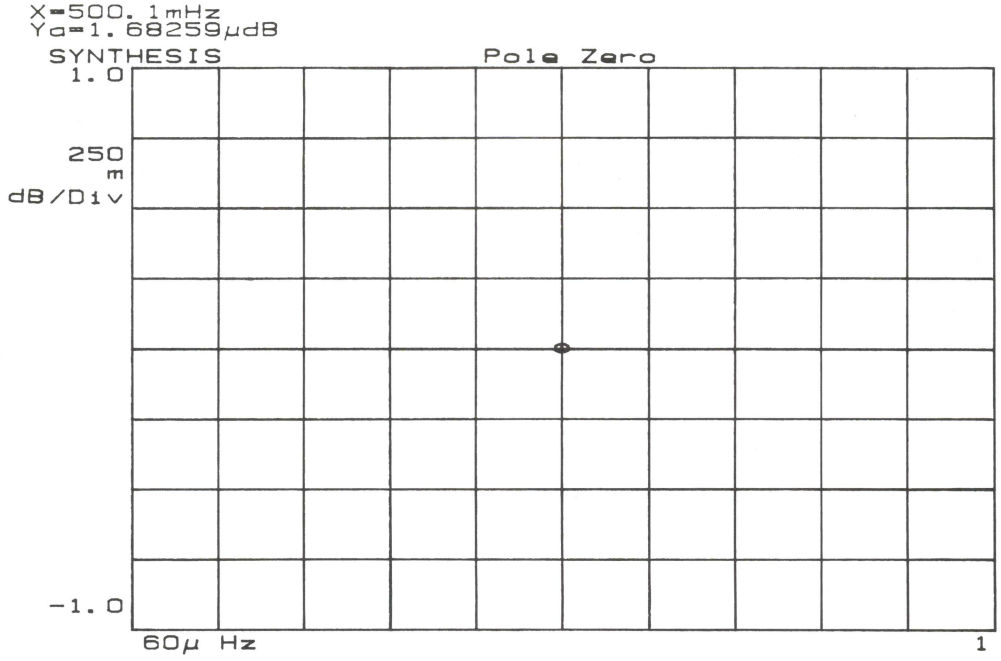


Figure 5B. Amplitude Response of a Perfect All Pass Filter

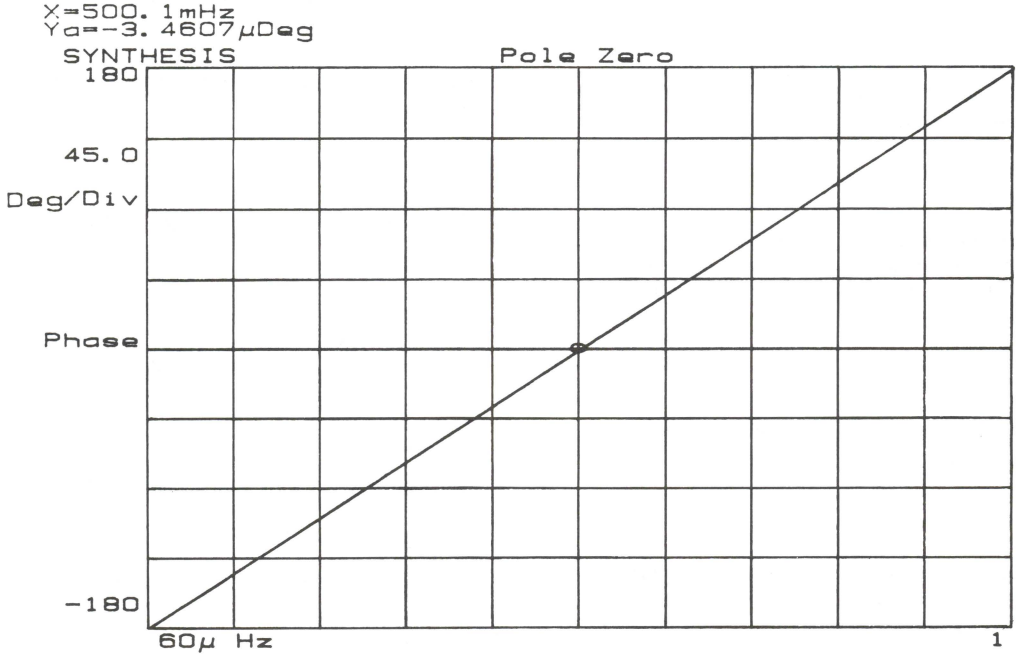


Figure 5C. Phase Response of a Perfect All Pass Filter

MODES OF OPERATION

The XR-1010 is a switched capacitor filter using switched capacitors to simulate resistors and controlled feedback to simulate inductors. This is a sampled data device which is most easily studied in the frequency domain.

The value of the resistors control the amount of feedback, and consequently, the gain of the filter responses and the Q of the filters. The following are the formulas used to calculate the resistor values needed to obtain the various filter responses.

Mode 1: Inverting Notch, Bandpass or Lowpass Filter Reponse

This mode involves a small number of external resistors. High Q band pass filters can be constructed with this circuit, however at the same time, the gain of the low pass filter response. The gain of all outputs are controlled by a separate feedback resistor. Figure 6 shows the connections to be made to side A of the XR-1010.

- $f_o = \frac{f_{clock}}{100}$ or $\frac{f_{clock}}{50}$

  depending on the level at 50/100/PD.

- $H_{lowpass} = -\frac{R2}{R1}$

  Please note that in this configuration R1 is the input impedance of the filter. In this fashion, the formula becomes an equation with only one unknown, R2, the amount of feedback.

- $f_{zero} = f_o$

  The center frequency of the complex zero pair is equal to the center frequency of the real pole pair. In this mode, the uncertainty of the position of the zero is reduced.

- $H_{bandpass} = -\frac{R3}{R1}$

  The gain of the band pass filter at the center frequency is set by this resistor ratio.

- $H_{notch} = -\frac{R2}{R1}$

  The gain of the notch filter output as f_o approaches 0Hz or as f_o approaches $f_{clock}/2$. Please note that the depth of the notch is a factor band pass filter's Q.

- $Q = \frac{R3}{R2}$

  The quality factor of the second order pole pair is control led by the ratio of R3/R2. This quality is also defined by f_0/bandwidth where the bandwidth is the –3dB points of the band pass filter.

Dynamic Gain Calculations

- $H_{bandpass} = H_{lowpass} \times Q$
  $H_{bandpass} = H_{notch} \times Q$

  This can be seen through the algebraic manipulations of the formula for notch low pass and Q from above. It can be seen from this that the device gain of the bandpass filter is independant of the Q of the filter.

- $H_{lowpass(peak)} = Q \times H_{lowpass}$

  The gain of the low pass filter is affected by the Q of the filter at the center frequency of the band pass filter. If clipping of the low pass filter output occurs, the feedback of this clipping used to create the band pass response will cause distortion.

Mode 1a: Inverting Band Pass, Non-inverting Band Pass, and Low Pass Filter Responses

This is the simplest configuration of the XR-1010, requiring only two external resistors. Please refer to Figure 7 for details.

- $f_o = \frac{f_{clock}}{100}$ or $f_o = \frac{f_{clock}}{50}$

  Depending on the level at Pin 12, 50/100/PD.

- $Q = \frac{R3}{R2}$

  The Q and the gain of the band pass are related. In the situation of large Q values, clipping may occur at certain signal levels.

- $H_{lowpass} = 1$

  This is due to the unity gain configuration.

- $H_{lowpass@f_o} = Q \times H_{lowpass}$

  This is true for applications with high Q values.

- $H_{bandpass(inverting)} = -\frac{R3}{R2}$

Dynamic Calculations

- $H_{bandpass(inverting)} = Q$

  If the input signal is too large, the output at this pin will be clipped causing an increase of noise. Clipping at this output will affect the device operation at other outputs.

- $H_{lowpass(peak)} = Q \times H_{lowpass}$

  This is true in the case of high Q filter. This again shows the importance of preventing clipping from occurring in the filter. Such clipping would not be normally visible on the low pass filter output, but, this would affect the performance.

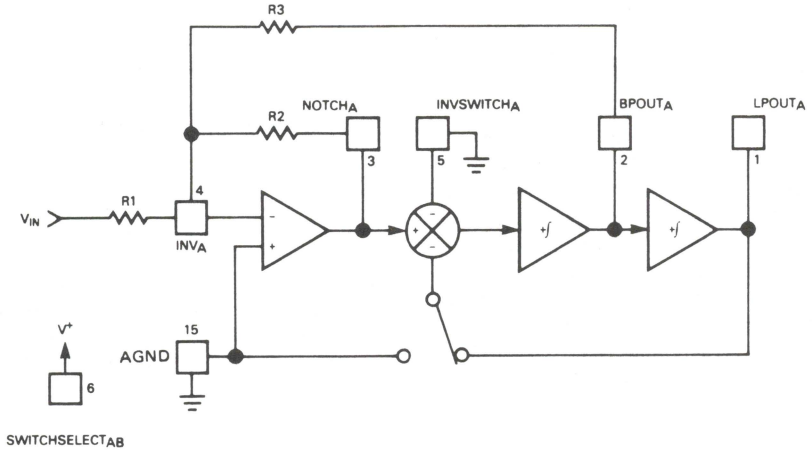


Figure 6. Mode 1 Shown for Side A of XR-1010

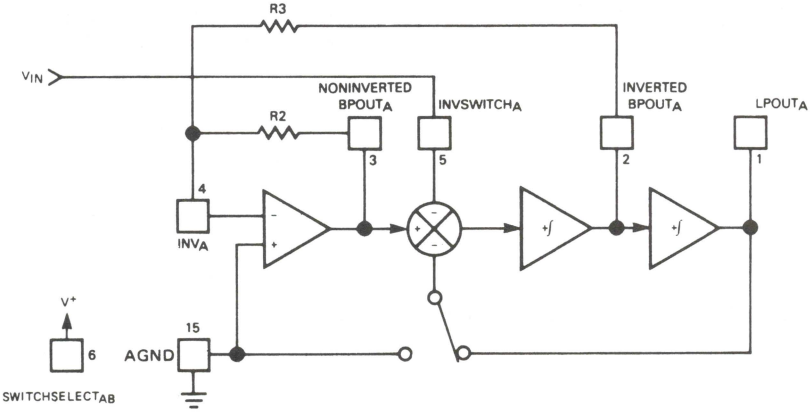


Figure 7. Mode 1A

This mode can provide a very large gain band pass filter due to the effect of the Q on the filter gain. It is not normally recommended for high Q filters due to the danger of clipping the inverting band pass output. The clock-to-corner ratio is fixed in this mode of operation due to the simplicity of the feedback of the filter.

The signal input impedance, Pin 5 or Pin 16, will vary with the clock frequency. With a clock frequency of 1 MHz, the input impedance is 20kΩ typically.

Mode 2: Notch$_{mode2}$ (f_{notch} less than f_o) Band Pass, Low Pass Filters

Mode 2 provides adjustment of the center frequency of the band pass and low pass filters. This is done through the use of the feedback resistor R4. Please note that in Mode 2, the feedback path of the low pass filter output is through R4 to the inverting input of the operational amplifier, Pin 4 (17) as well as to the inverting input of the switched summing circuit. Figure 8 provides the detail for connection of the external resistors for side A of the XR-1010. Mode 2 is best suited for notch filter applications since the clock-to-corner ratio is reduced for the other shape.

Design Equations

- $f_o = \frac{f_{clock}}{100}\left(\frac{R2}{R4}+1\right)^{1/2}$ or $f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}+1\right)^{1/2}$

  depending on the level at Pin 12, 50/100/PD. It should be noted that the f_o frequency must be greater than 100 times (50 times – Pin 12 high) the clock frequency or negative resistance will result when these equations are used.

- $f_{notch} = \frac{f_{clock}}{50}$ or $f_{notch} = \frac{f_{clock}}{100}$

  depending on the level set on Pin 12, 50/100/PD.

- $Q = \left(1+\frac{R2}{R4}\right)^{1/2}\frac{R2}{R3}$

  The Q of the filter is related to the gain of the low pass and notch filter as well as the band pass gain.

- $H_{lowpass} = \frac{-\frac{R2}{R1}}{\frac{R2}{R4}+1}$

  $H_{notch} = \frac{-\frac{R2}{R1}}{\frac{R2}{R4}+1}$

  The low pass filter gain is the same as the gain for the notch filter as f_o approaches 0Hz.

Mode 3: Inverting High Pass, Band Pass, and Low Pass Filters

This circuit allows high Q band pass filters with the ability to adjust the band pass filter gain without significantly affecting the Q of the filter. It is also possible to obtain a shift in the f_{corner} or the f_o of the filter with the adjustment of the values of the resistors R2 and R4, as shown in the equations below. This allows, with a single clock frequency, multiple-pole filters. Figure 9 shows the external resistor interconnections.

Design Equations

- $f_o = \frac{f_{clock}}{100} \times \left(\frac{R2}{R4}\right)^{1/2}$

  This formula calculates the center frequency of the band pass filter, or the corner frequency of the low pass filter. When 50/100/PD is tied to ground. It is with the adjustment of the value of R2 and R4 that the variation of the center frequency or the corner frequency is obtained.

- $f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}\right)^{1/2}$

  This formula is used if Pin 12, 50/100/PD is tied to V+.

- $Q = \frac{R3}{R2}\left(\frac{R2}{R4}\right)^{1/2}$

  The Q of the filter is affected by the value of the feedback resistors R2 and R4 as well.

- $H_{highpass} = -\frac{R2}{R1}$

  It can be seen that the adjustment of the gain of the high pass filter output will have some effect on the Q of the filter as well as on the f_o of the filter outputs.

- $H_{bandpass} = -\frac{R3}{R1}$

  The gain of the band pass filter output will affect the Q of the filter.

- $H_{lowpass} = -\frac{R4}{R1}$

  The gain of the low pass filter output will have some effect on the fo of the filter as well as on the Q of the filter.

Equations for Dynamic Circuit Operation

- $H_{highpass} = H_{lowpass}$

  This equation shows that the band pass filter will be affected by the Q of the filter as well as by the amount of shift created by the ratio R2 of the corner frequency.

- $H_{lowpass\ @\ f_o} = Q \times H_{lowpass}$

  The Q of the filter will have an effect on the amount of gain at the corner frequency of the low pass response. In situations of extremely large values of Q, this can cause clipping and should be considered.

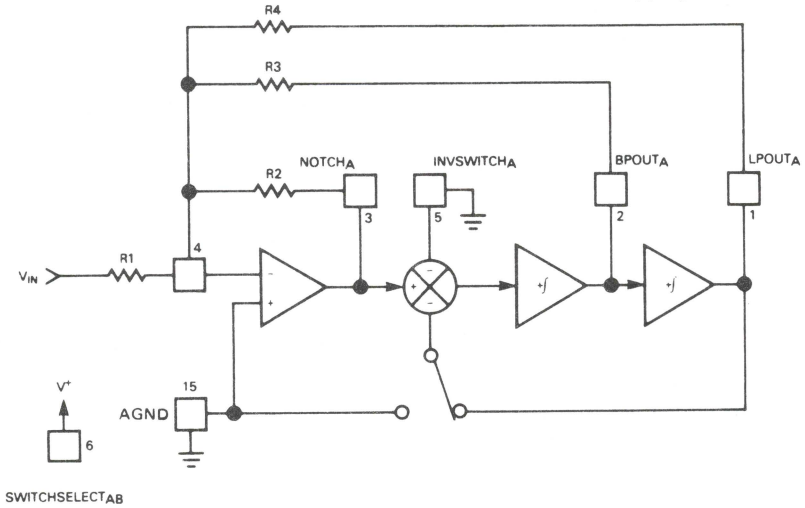


Figure 8. Mode 2

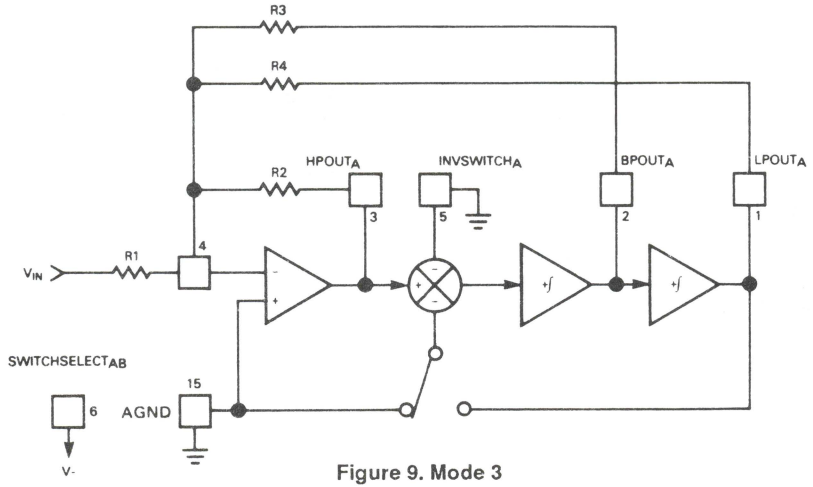


Figure 9. Mode 3

- $H_{bandpass} = (Q \times H_{highpass} \times H_{lowpass})^{1/2}$

  The Q of the filter will have an effect on the gain of band pass filter output. The gain of the high pass and low pass filters will also have some effect on the band pass filter gain.

Mode 3A: High Pass, Band Pass, Low Pass and Notch Filters

With the addition of an external operational amplifier such as the XR-4560, XR-082 or the XR-5532A a notch filter can be obtained from the same circuit as Mode 3. The output of the high pass and the low pass filter are summed to obtain a notch filter response. The limitation of the notch depth will be the slope of the rolloff of the high pass and low pass filter responses. An operational amplifier with a large gain bandwidth product is recommended to minimize its effect on the filter response.

Figure 10 gives the details as to the filter configuration.

Design Equations

- $f_o = \frac{f_{clock}}{100} \left(\frac{R2}{R4}\right)^{1/2}$

  The center frequency of the notch or band pass filter or the corner frequency of the low pass can be adjusted to some degree by the ratio of the low pass and high pass filter gain resistors. This formula is used if Pin 12, 50/100/PD is tied to analog ground.

- $f_o = \frac{f_{clock}}{50} \times \left(\frac{R2}{R4}\right)^{1/2}$

  This formula is used if 50/100/PD is tied to V_{DD}.

- $f_{notch} = \frac{f_{clock}}{50} \times \left(\frac{R2}{R4}\right)^{1/2}$ or $f_{notch} = \frac{f_{clock}}{100} \times \left(\frac{R2}{R4}\right)^{1/2}$

  The notch filter center frequency at the output of the external operational amplifier.

- $H_{bandpass} = -\frac{R3}{R1}$

  The gain of the band pass filter output is controlled by the ratio between the feedback resistor (R2) and the input resistance (R1).

- $H_{highpass} = -\frac{R2}{R1}$

  The gain of the high pass filter output is controlled by the ratio between the feedback resistor R2 (operational amplifier output to inverting input) and the input resistor R1.

- $H_{lowpass} = -\frac{R4}{R1}$

  The gain of the low pass filter output is adjusted by the ratio between the feedback resistor R4 (integrator 2 output to inverting input of operational amplifier) and resistor R1.

- $H_{notch@0} = \frac{R_{gain}}{R_{lowpass}} \times \frac{R4}{R1}$

  The gain of the notch filter as the input frequency approaches 0Hz can be calculated using the formula at left. From Figure 10, it can be seen that the gain of the external operational amplifier will affect the gain seen at the notch output. Also, this does allow some adjustment to the gain of the pass band of the notch filter without affecting the gain of the low pass filter output.

  The outputs of the XR-1010 can typically drive a 10kΩ load. The parallel combination of R4 and $R_{lowpass}$ should be 10 kΩ or greater.

- $H_{notch@f_{clock}} = \frac{R_{gain}}{R_{lowpass}} \times \frac{R2}{R1}$

  The gain of the notch filter output as the input frequency approaches fclock is calculated using the equation at left. Figure 10 shows how the gain of the high pass filter output can be adjusted independently of the notch filter gain. Care should be taken to ensure that clipping of the signal does not occur, due to excessive gain set at the notch filter output.

  It should be considered that the output of the XR-1010 can drive 10 kilohms typically. Care should be taken so that the parallel combination of the feedback resistor R2 and the input resistor $R_{lowpass}$ is not less than 20kΩ.

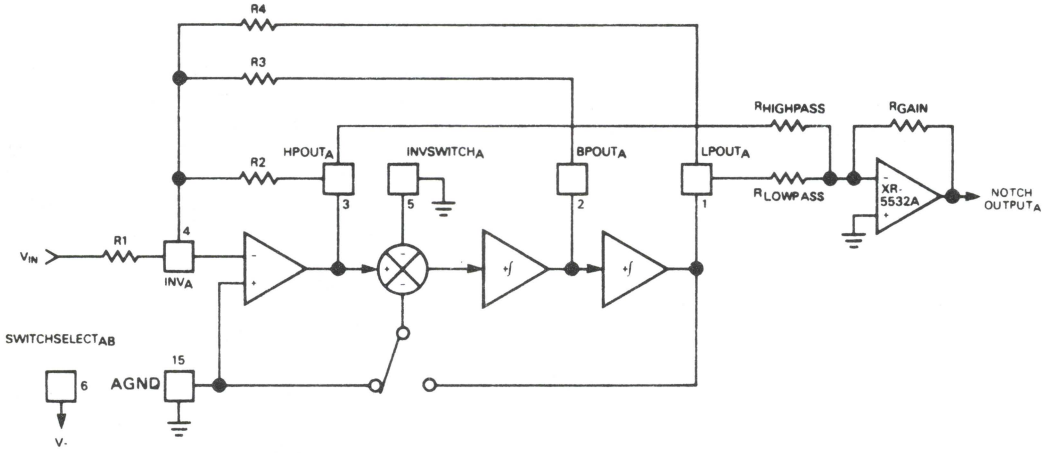


Figure 10. Mode 3A

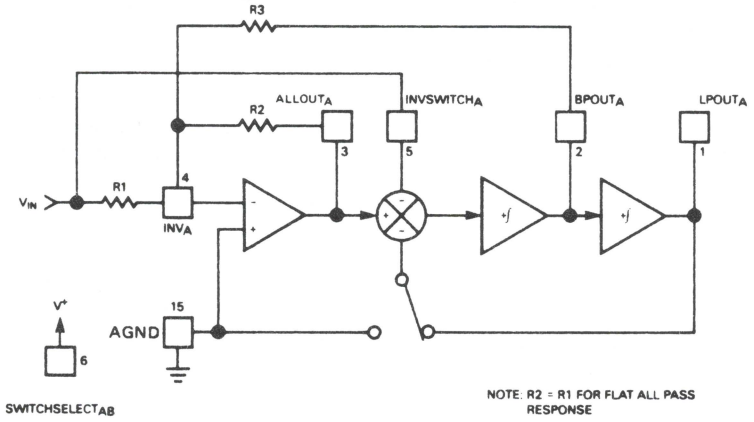


Figure 11. Mode 4

Mode 4: All Pass, Band Pass, and Low Pass Filtering

This mode provides an inverted all pass, band pass, and low pass filter output. Through variation of the f_{clock}, the amount of delay through the all pass filter can be varied. The output gain of the all pass filter is fixed at –1 to reduce the amount of ripple. Unlike other all pass filters, the XR-1010 has typically less than 1dB of ripple in the response of the all pass filter output. This allows the use of Mode 4 in any all pass system. The f_o in this mode is fixed to either 100:1 or 50:1.

Figure 11 shows the external connections for Mode 4. As with the other circuits, it is important that the connections to the inverting input of the operational amplifier should be kept short to prevent noise pickup. Figure 12 (a/b) shows the change in delay for f_{clock} = 500kHz and f_{clock} = 1MHz. From this, it can be determined that for maximum delay, the frequency of the clock should be decreased within the limits of the maximum input frequency.

Design Equations

- $f_o = \frac{f_{clock}}{100}$

  The center or corner frequency of the filter responses does not vary with the adjustment of the resistor values. The formula at left is used when Pin 12, 50/100/PD is tied to 0 VDC.

- $f_o = \frac{f_{clock}}{100}$

  The formula at left is used when the 50/100/PD pin is tied to V+.

  The f_o of the complex zero pair is approximately equal to the f_o of the complex pole.

- $Q = \frac{R3}{R2}$

  The Q of the band pass filter output can be calculated using the equation above. In the case of the large Q, this will have some effect on the gain of the low pass filter outputs at f_{corner}.

- $Q_{zero} = \frac{R3}{R1}$

  The Q of the complex zero pair which cannot be measured externally.

- $H_{allpass} = -\frac{R2}{R1}$

  The gain of the all pass filter output should be set to –1 (R2 = R1). When R2 is larger than R1, a slope will appear on the all pass output.

- $H_{bandpass} = -2 \times \frac{R3}{R1}$

  The gain of the band pass filter output is controlled by the ratio of R3 to R1.

- $H_{lowpass} = -2 \times \frac{V}{V}$

  The gain of the low pass filter output is fixed at –2 where f_o approaches 0Hz. This can be seen by the two inputs used in this mode (Mode 4). One input is applied directly to the INVSWITCH input. The second is applied through R1 to the inverting input of the operational amplifier. At the switched capacitor summer, the amplitude of the two signals would be equal in amplitude (@ 180°) providing twice the amplitude to be applied to the low pass integrator.

Mode 5: Complex Zero, Band Pass and Low Pass Filter Outputs

This mode provides additional flexibility over Mode 4, in that the complex zero location can be moved separately from the complex pole position. This can reduce the amount of ripple in the all pass response, as well as provide additional control over the position of the corner frequency of the low pass filter and the center frequency of the band pass filter output. Please see Figure 13.

Design Equations

- $f_0 = \left(1 + \frac{R2}{R4}\right)^{1/2} \times \frac{f_{clock}}{100}$

  The formula above calculates the corner or center frequency of the XR-1010 filter outputs when Pin 12, 50/100/PD is tied to analog ground.

- $f_0 = \left(1 + \frac{R2}{R4}\right)^{1/2} \times \frac{f_{clock}}{50}$

  When 50/100/PD is tied to V_{DD}, the formula above should be used. This formula shows the advantage that Mode 5 has over Mode 4 in that the corner or center frequency of the filter can be moved relative to the fixed clock-to-corner ratio.

  If only a small change to the clock-to-corner (center) ratio is desired, then R4 can be made larger. However, this will have a direct effect on the gain of the low pass filter output. Clipping on the output of the low pass filter could occur, which would affect the other filter outputs.

- $f_{zero} = \left(1 - \frac{R1}{R4}\right)^{1/2} \times \frac{f_{clock}}{100}$

  The equation above is used for caluclating the location of the complex zero pair, when Pin 12, 50/100/PD is tied to ground. With the ability of moving the complex zero to a location of the pole, many different filter shapes can be obtained.

  In the case of a large value for R1 and a small value of R4, the location of the zero would be close to 0Hz. The equation is not defined for values of R1/R4 which are greater than or equal to 1.

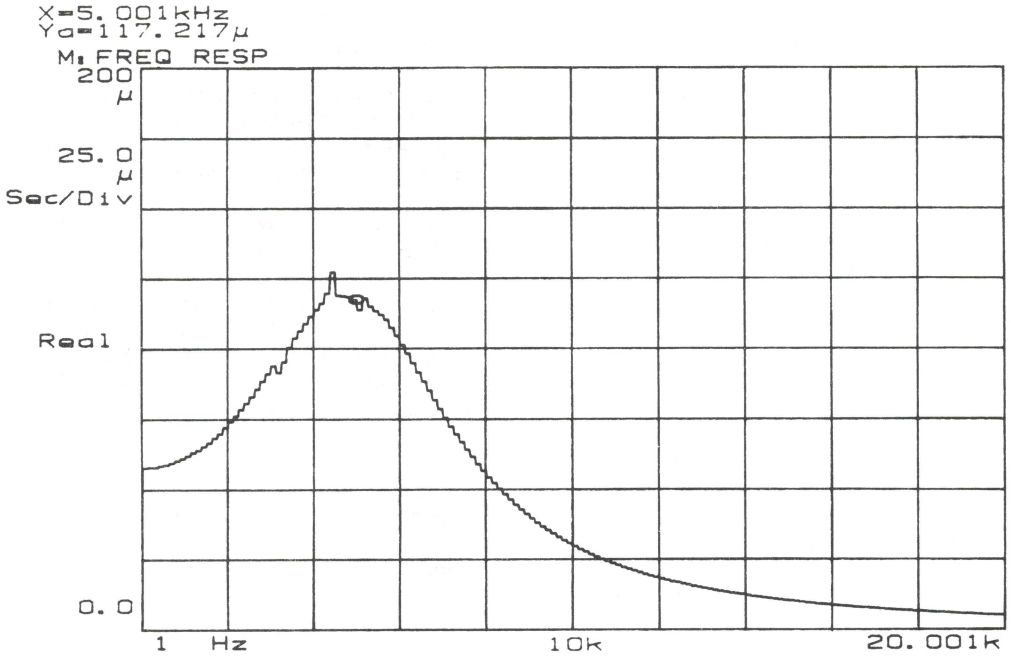


Figure 12A. Delay of Mode 4 All Pass Output f_{clock} = 500kHz

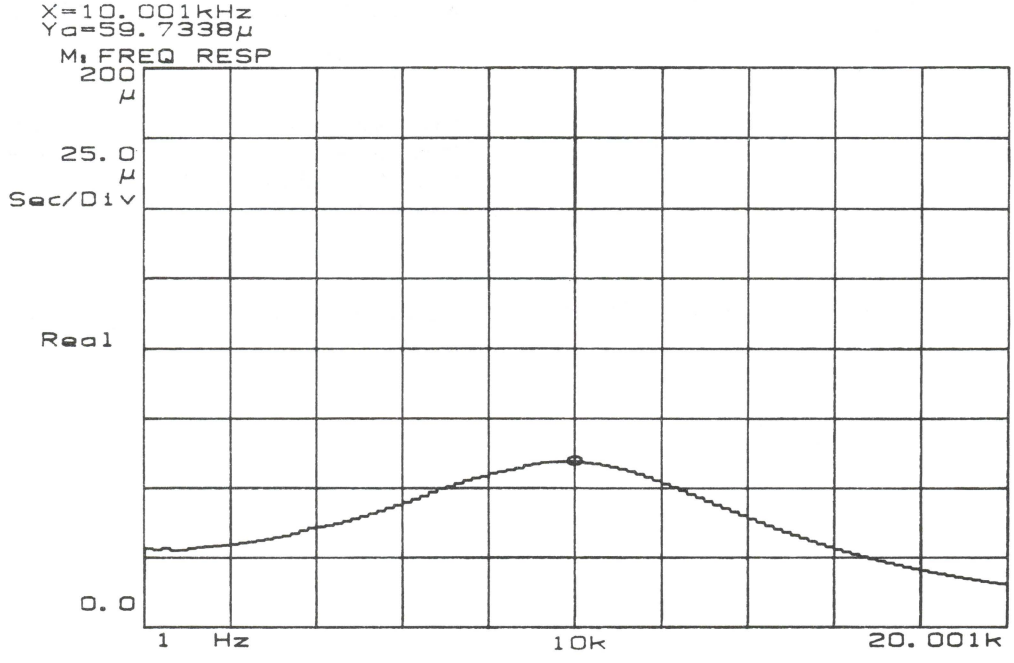


Figure 12B. Delay of Mode 4 All Pass Output f_{clock} = 1MHz

- $f_{zero} = \left(1 - \frac{R1}{R4}\right)^{1/2} x \frac{f_{clock}}{50}$

  This equation is used when Pin 12, 50/100/PD is tied to V_{DD}.

- $Q_{pole} = \left(1 + \frac{R2}{R4}\right)^{1/2} x \left(\frac{R3}{R2}\right)$

  The equation above calculates the quality of the filter relative to the complex pole pair. With the variation of R3 (band pass feedback) and R4 (inverting low pass filter feedback), the magnitude of the real component can be varied.

- $Q_{zero} = \left(1 - \frac{R2}{R4}\right)^{1/2} x \left(\frac{R3}{R1}\right)$

  This equation is used to calulate the quality of the complex zero pair. The magnitude of R4 (inverting low pass filter feedback) and R3 (band pass filter feedback) control the location of the zero on the jω, ω axis.

  This formula works well with large values (relative to R2) of resistance of R4. When R4 becomes equal to, or smaller than R2, the formula becomes meaningless.

  The Q_{zero} in such a case is much less than 1 and does not have any practical use.

- $H_{zero\ @\ 0} = \frac{R2(R4-R1)}{R1(R2+R4)}$

  The gain on the output of the complex zero filter as the input frequency approaches 0Hz is calculated by this formula.

- $H_{zero\ @\ f_{clock}/2} = -\frac{R2}{R1}$

  As the input frequency approaches $f_{clock}/2$, the gain of the output is limited by the gain of the operational amplifier.

- $H_{bandpass} = \left(\frac{R2}{R1} + 1\right) x \frac{R3}{R2}$

  The gain of the bandpass filter at f_o is calculated using the formula above.

- $H_{lowpass} = \left(\frac{R2 + R1}{R2 + R4}\right) x \frac{R4}{R1}$

  The formula above is used to caluculate the gain of the low pass filler as f_o approaches 0Hz. The response of the filter near the corner frequency is affected by the gain of the band pass filter.

Mode 6a: First Order Clock Controlled High Pass and Low Pass Filter (Inverted)

This mode allows the construction of first order high pass and low pass filters with the f_{corner} adjustable from the clock frequency or by adjusting the resistor ratios. This is far more useful than the continuous time RC version, since the XR-1010 will track any other stage in the system.

The output of the second integrator is not normally used. The output is typically near V_{DD} or V_{SS}.

Design Equations

- $f_o = \frac{f_{clock}}{50} x \left(\frac{R2}{R3}\right)$

  This equation is used for calculation of the position of the corner frequency of the low pass filter or the high pass filter when Pin 12, 50/100/PD is tied to V_{DD}.

- $f_o = \frac{f_{clock}}{100} x \left(\frac{R2}{R3}\right)$

  This equation is used when Pin 12, 50/100/PD is tied to analog reference. Please note that if the gain of the low pass and high pass filter outputs is not the same, the clock-to-corner ratio will be affected.

- $H_{highpass} = -\frac{R2}{R1}$

  This formula is used to calculate the gain of the high pass filter output.

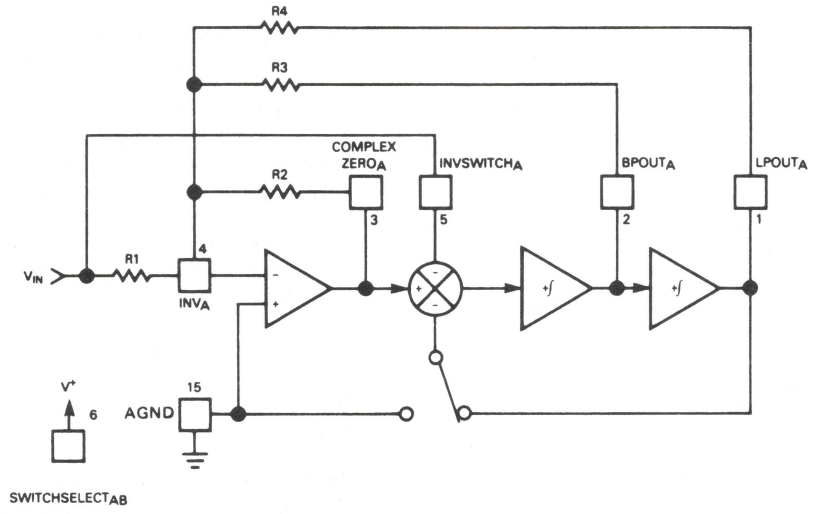


Figure 13. Mode 5

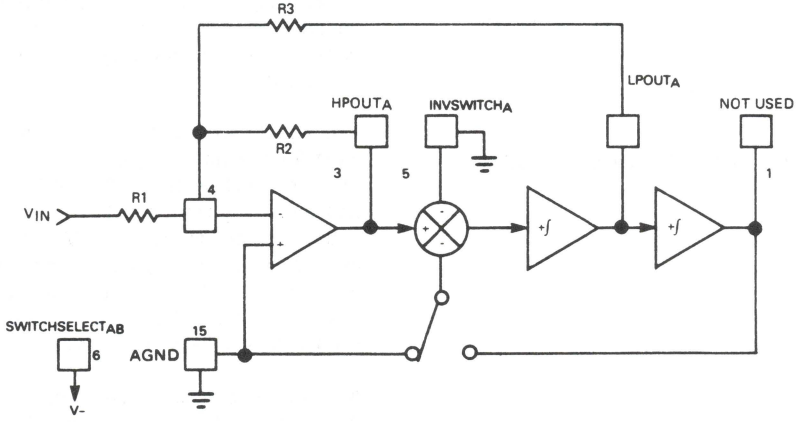


Figure 14. Mode 6A

Mode 6b: Single Pole Low Pass Filter — Inverting and Non-Inverting Output

This mode is used for circuits which only need a single pole, but need the flexibility of clock control for the corner frequency. As with Mode 6, the output at Pin 1 is not used and is normally either near V_{DD} or V_{SS}.

Design Equations

- $f_{corner} = \frac{f_{clock}}{100} \times \left(\frac{R2}{R3}\right)$

  This equation is used when Pin 12, 50/100/PD is tied to mid-supplies, usually 0 VDC.

- $f_{corner} = \frac{f_{clock}}{50} \times \left(\frac{R2}{R3}\right)$

  When Pin 12, 50/100/PD is tied to V_{DD}, this formula is used to calculate the position of the corner of the low pass filter.

- $H_{lowpass\ (inverting)} = -\frac{R3}{R2}$

  The gain of the inverting low pass filter output is controlled by the ratio of the feedback resistor R3 to the resistor R2.

- $H_{lowpass\ (noninverting)} = +1\ \frac{V}{V}$

  The gain of the non-inverting low pass filter output is fixed at +1.

GENERAL APPLICATION CRITERIA

The following aspects of the use of any filter should be considered when the design is started:

1. Prevention of saturation of the first stage or any subsequent stages. If a design is composed of two stages, consideration to the output amplitude of the first stage must be given. The Q of the filter could cause clipping on the first stage, which would be filtered by the second stage back to a sinusoidal signal. This would cause an increase in noise and error in the phase response of the filter.

   Any DC offset of the signal can cause clipping or even rectification of the signal. The offset of the signal should be determined for the first stage and any other stages.

2. The order of the filters may be important to the design. Once again this would be due to the gain or Q of the filters. For example, a low pass filter may be desired before a band pass filter to reduce the chance that out-of-band signals will affect the band passfilter. Also, any clipping at the output of the band pass filter would be apparent. This would not be the case if the band pass filter was the first stage and the low pass filter was second.

3. The signal-to-noise ratio should be maximized. In most designs the limiting factor for the signal to noise ratio is not the filter itself, rather the layout of the board and decoupling of the supplies. Proper use of analog and digital grounds should be observed in any system using a filter. Proper grounds imply that no differential voltage will occur from the INV SWITCH when grounded and AGND. A separate analog V_{DD} and V_{SS} should be provided when possible.

   Also, shielding of the low amplitude signals from large digital signals should be considered.

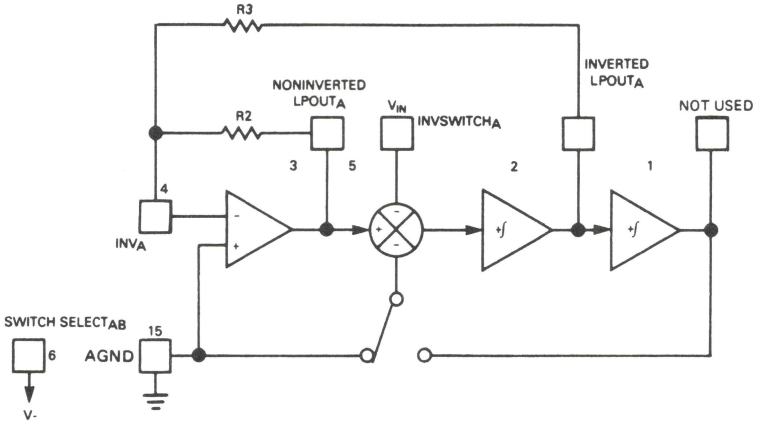


Figure 15. Mode 6B

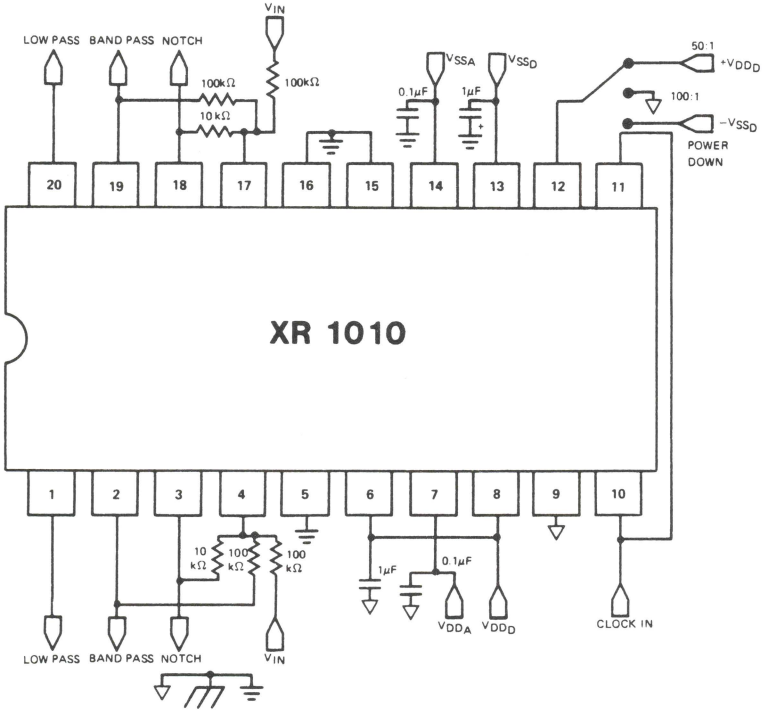


Figure 16. Spilt Supply Operation Mode 1



NOTES



Seventh Order Elliptic Low Pass Filters

GENERAL DESCRIPTION

The XR-1015 and XR-1016 are seven pole and six zero elliptic low pass switched capacitor filters. The position of the passband of the filter is set by the frequency of the clock which allows for easy adjustment. The use of switched capacitor filters reduces the amount of variation in the filter response that occurs with discrete use of capacitors, inductors and resistors. The XR-1015 and XR-1016 also provide synchronized sampled inputs and outputs that allows the device to be cascaded without the need of an additional sample-and-hold. The XR-1015 and XR-1016 are produced with a 3 µm polysilicon gate dual metal CMOS process for low power consumption.

The XR-1015 is an eight pin device that can operate from +3, –2.0 VDC to ±5VDC. The device can also be biased so that it can be operated with a single +5 to +10 VDC supply. It is pin-for-pin compatible with the Reticon R5609 with the added advantage of operating to +5 VDC single supply. The clock to corner ratio of the XR-1015 is fixed at 100:1.

The XR-1016 is a 14 pin device which provides two uncommitted operational amplifiers for use as a reconstruction filter, anti-aliasing filters or for additional prefilter gain. The XR-1016, as does the XR-1015, provides a clock output with the voltage output from rail to rail. The XR-1016 has the ability to change the clock to corner ratio from 100:1 to 50:1. The output clock can be used to strobe an analog to digital converter or to synchronize any additional circuits in the system.

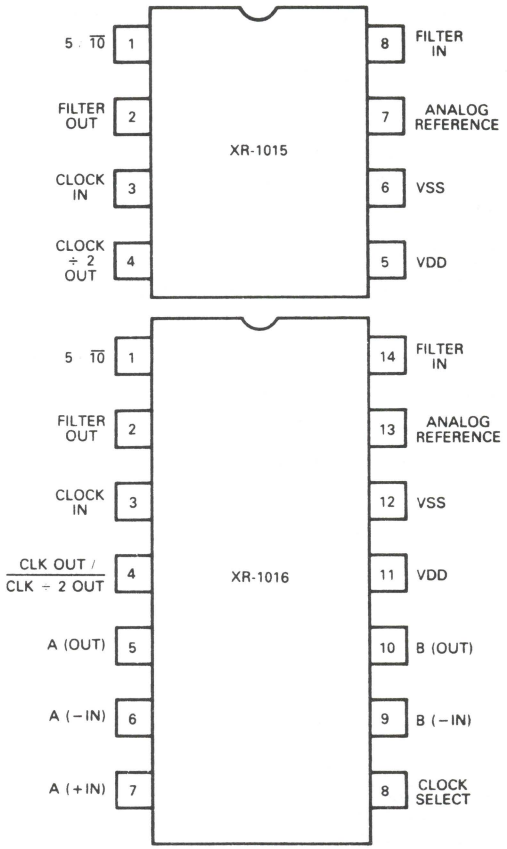
FEATURES

Greater than 70 dB Stopband Rejection
Operation at +5 VDC
Precise Filter Positioning
Low Power Consumption
No External Components Required for Filter

APPLICATIONS

General Purpose Filtering
Anti-alias Filters (for analog-to-digital converters)
Reconstruction Filters (for digital-to-analog converters)
Band Limiting of Voice
Digital Signal Processing Front End
Filtering of Voice for Music for Special Effects
(echo, phasing, etc.)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Power Supply	14V
Input Signal Level	V^+ +0.3 to V^- ±0.3V
Power Dissipation — XR-1016 (Package Limitation)	
Ceramic Package	1000mW
Derate Above T_A = +25°C	6mW/°C
Plastic Package	800mW
Derate Above T_A = +25°C	7mW/°C
Power Dissipation — XR-1015	
Ceramic Package	385mW
Derate Above T_A = +25°C	8.3mW/°C
Plastic Package	300mW
Derate Above T_A = +25°C	8.3mW/°C
Storage Temperature	–55°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1015CN	Ceramic	0°C to 70°C
XR-1015CP	Plastic	0°C to 70°C
XR-1016CN	Ceramic	0°C to 70°C
XR-1016CP	Plastic	0°C to 70°C
XR-1016CD	JEDEC SOL-16	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1015 and XR-1016 General Purpose Seventh Order Elliptic Switched Capacitor Low Pass Filters are usually used as the first or last stage in any sampled signal system.

Any signal from the –3dB point of the low pass response to 1/2 of the sampling frequency (1/4 of the clock frequency) will be attenuated by typically 75dB, referenced to the pass-band. This allows its use with analog-to-digital converters to prevent the A-to-D from aliasing signals that are above 1/2 of the sampling frequency of the analog-to-digital converter. A simple second order active filter can be used in front of the XR-1015 or XR-1016 if it is known that some input signals will be above the Nyquist frequency of the XR-1015 or XR-1016.

The reverse of the above circuit can be used for digital-to-analog converters, to prevent the sampling frequency from causing difficulties with other stages in the system.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 5$ VDC, $V^- = -5$ VDC, $f_{CLOCK} = 2$MHz, $R_L = 1$ MΩ, $C_L = 40$pF, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	XR-1015 MIN	XR-1015 TYP	XR-1015 MAX	XR-1016 MIN	XR-1016 TYP	XR-1016 MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS									
	Supply Voltage								
	Single Supply	5		10.5				V	See Figure 1
					5		10.5	V	See Figure 3
	Split Supply	+3, –2		15.25				V	See Figure 2
					+3, –2		±5.25	V	See Figure 4
	Supply Current								
	Single Supply		10	11				mA	See Figure 1
						10	11	mA	See Figure 3
	Split Supply								
	Positive		10	12				mA	See Figure 2
	Negative		10	12				mA	
	Positive					10	12	mA	See Figure 4
	Negative					10	12	mA	
FILTER SECTION									
f_{CLOCK}	Upper Frequency Limit	2	2.5					MHz	See Figure 2
					2	2.5		MHz	See Figure 4
$f_{CLOCKMIN}$	Lowest Practical		1					kHz	See Figure 2
						1		kHz	See Figure 4
	Input Impedance								
	Pin 8		1					MΩ	See Figure 2, $f_{CLOCK} = 1$MHz
	Pin 14					1		MΩ	See Figure 4. $f_{CLOCK} = 1$MHz
tpw	Minimum f_{CLOCK} Pulse Width	200						ns	See Figure 2
					200			ns	See Figure 4
THD	Total Harmonic Distortion								Vin = 2 Vpp
			0.02%			0.02%			$f_{CLOCK} = 500$kHz
			0.1%			0.1%			$f_{CLOCK} = 2$MHz

ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: $V^+ = 5$ VDC, $V^- = -5$ VDC, $f_{CLOCK} = 2$MHz, $R_L = 1$ MΩ, $C_L = 40$pF, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	XR-1015 MIN	XR-1015 TYP	XR-1015 MAX	XR-1016 MIN	XR-1016 TYP	XR-1016 MAX	UNITS	CONDITIONS
FILTER SECTION (Continued)									
	Clock Feed through		30			30		mVpp	
V_{INMAX}	Maximum Input Voltage			8			8	Vpp	Above which distortion increases.
	Corner Freq. Accuracy		±0.5%	±1%		±0.5%	±1%		$f_{CLOCK} = 2$MHz
A_V	Passband Gain	–0.5	0	+0.5	–0.5	0	+0.5	dB	Tested at $f_{in} = 293$Hz, 3.9kHz, 8.6kHz, 12.1kHz
		–1	0	+1	–1	0	+1	dB	Tested at $f_{in} = 15.3$kHz, 17.1kHz
	Ripple Passband		±0.1			±0.1		dB	$f_{CLOCK} = 500$kHz
			±0.5	1		±0.5	1	dB	$f_{CLOCK} = 2$MHz
V_{OS}	Voltage Offset	–0.5	–0.2	+0.5	–0.5	–0.2	+0.5	VDC	
	Output Noise		0.6			0.6		mVrms	1Hz–20Hz, See Figure 8
OPERATIONAL AMPLIFIER									
	Unity Gain Bandwidth		1.2			1.2		MHz	
CMRR	Common Mode Rejection Ratio (2 Vpp Input)		50			50		dB	
V_{IO}	Input Offset Voltage	–30		30	–30		30	mV	

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Application Information

The XR-1015 and XR-1016 are fabricated in P-well CMOS. This uses a N-substrate and requires the V_{DD} to be applied first before V_{SS} in order to prevent latchup of the device.

In addition to the above caution, the input signals should not be applied above the power supply levels, to prevent latchup. The same is true of the input clock.

The input signal should not have any traces or wires near the clock or other system clocks. The same is true of the output. This will help to reduce the clock feedthrough and provide measurements equal to the datasheet values, or better.

PRINCIPLES OF OPERATION

The XR-1015 and XR-1016 are switched capacitor filters with seven poles and six zeros with an elliptic response. With the elliptic response of the filter, the stop band rejection is greater than 75dB. The elliptic filter response is called an equal-ripple response, where the ripple in the stop band is an approximation of the ripple in the pass band. In this way the rolloff of the filter response is very fast as shown in Figure 5.

The use of zeros to obtain the stop band attenuation does cause some change in the linearity of the group delay of the elliptic filter. The rapid change in group delay occurs near the corner frequency as shown in Figure 6. This would only be a factor in situations where the output signal must not be delayed by different times for different input frequencies. For applications where the distortion of the phase information is important, the corner frequency of the filter can be placed higher in frequency so that the linear portion of the group delay response of the filter can be located within the information band.

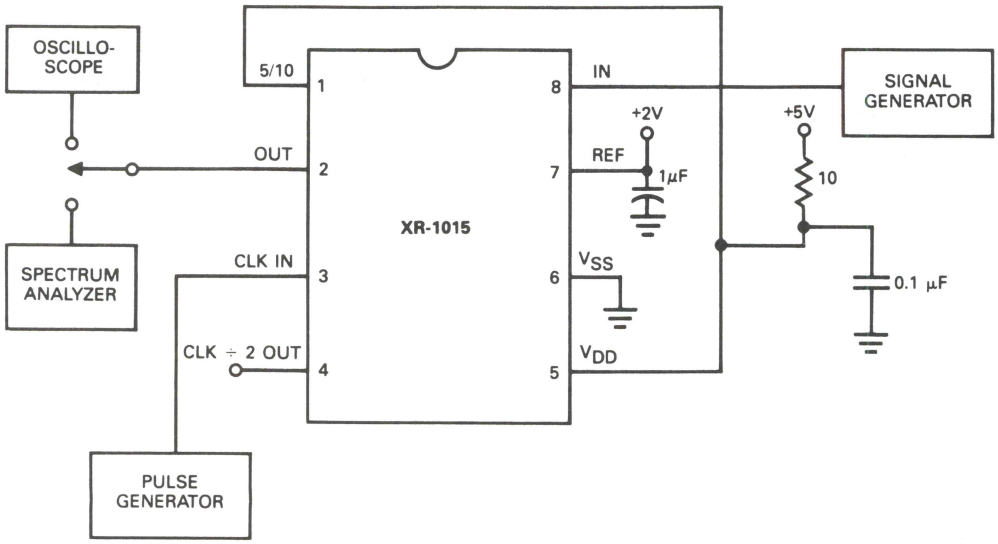


Figure 1. XR-1015 Test Circuit: 5V Operation (V_{DD} = +5V, V_{SS} = 0V, Ref = +2V)

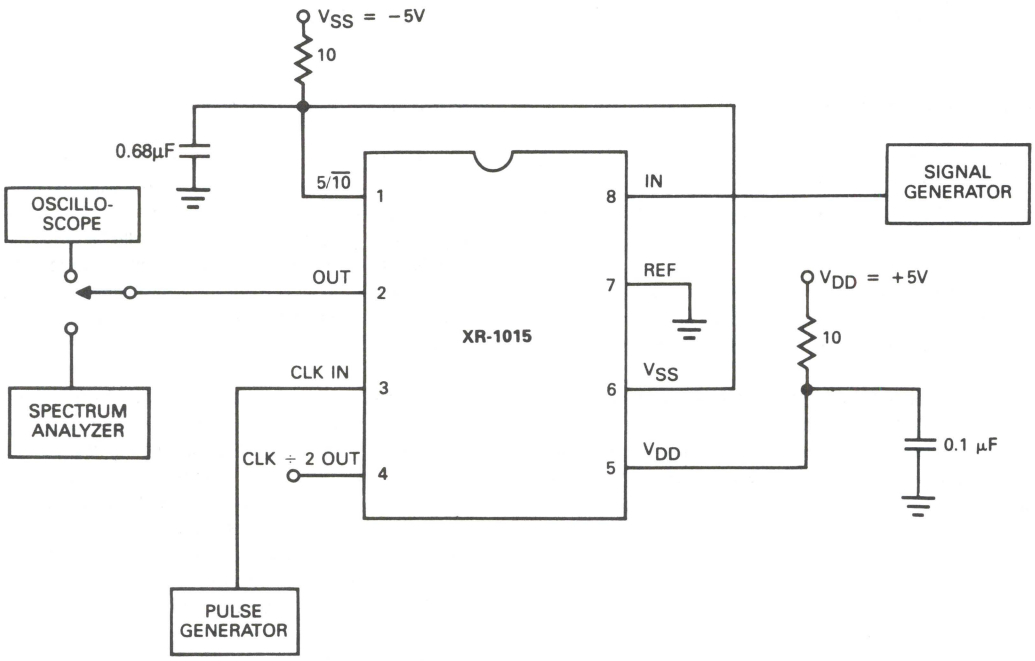


Figure 2. XR-1015 Test Circuit: 10V Operation (V_{DD} = +5V, V_{SS} = –5V)

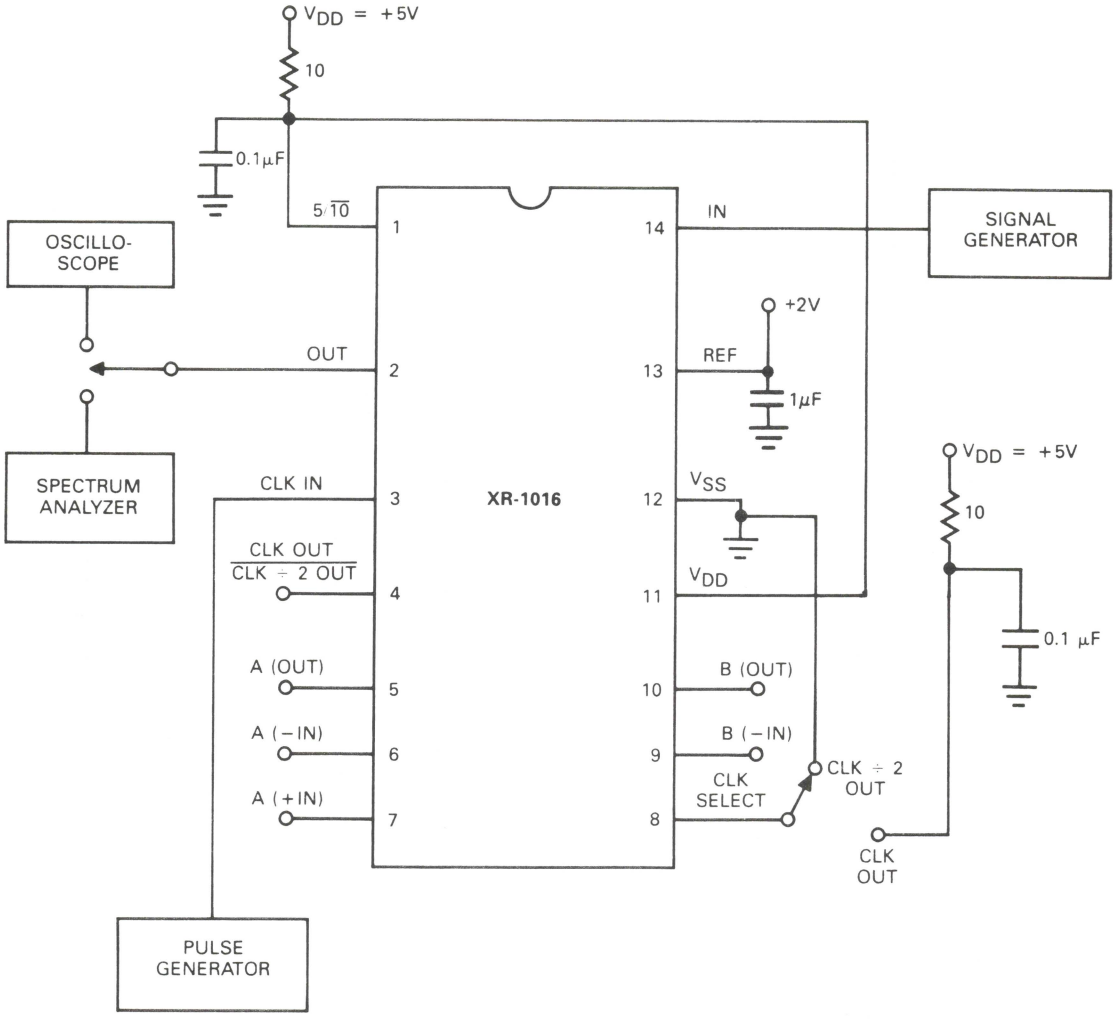


Figure 3. XR-1016 Test Circuit: 5V Operation (V_{DD} = +5V, V_{SS} = 0V, Ref = +2V)

Since the XR-1015 and XR-1016 are sample data filters in that they divide the continuous time signal into an amount of charge at a given time, certain limitations must be made on the signals placed on the input of the filters. The frequency of the signal applied to this input must have a period so that at least two samples of the signal are made during the period of the signal. This is true even if the signal is in the stop band response of the filter. The reason for this is that it would take a minimum of two samples of the frequency being applied to establish the period of the signal as well as an approximation of the amplitude. If this sampling criteria is not followed, then the output of the filter will be an aliased signal of the input since the period of the signal would be not accurately known and the frequency would not be known.

If this situation may occur, a simple second order filter can be added to the input. With the XR-1016, operational amplifier A could be used to create this filter. The precision of the location of the corner frequency of the filter is not critical in this situation so that precision resistors and capacitors would not be needed.

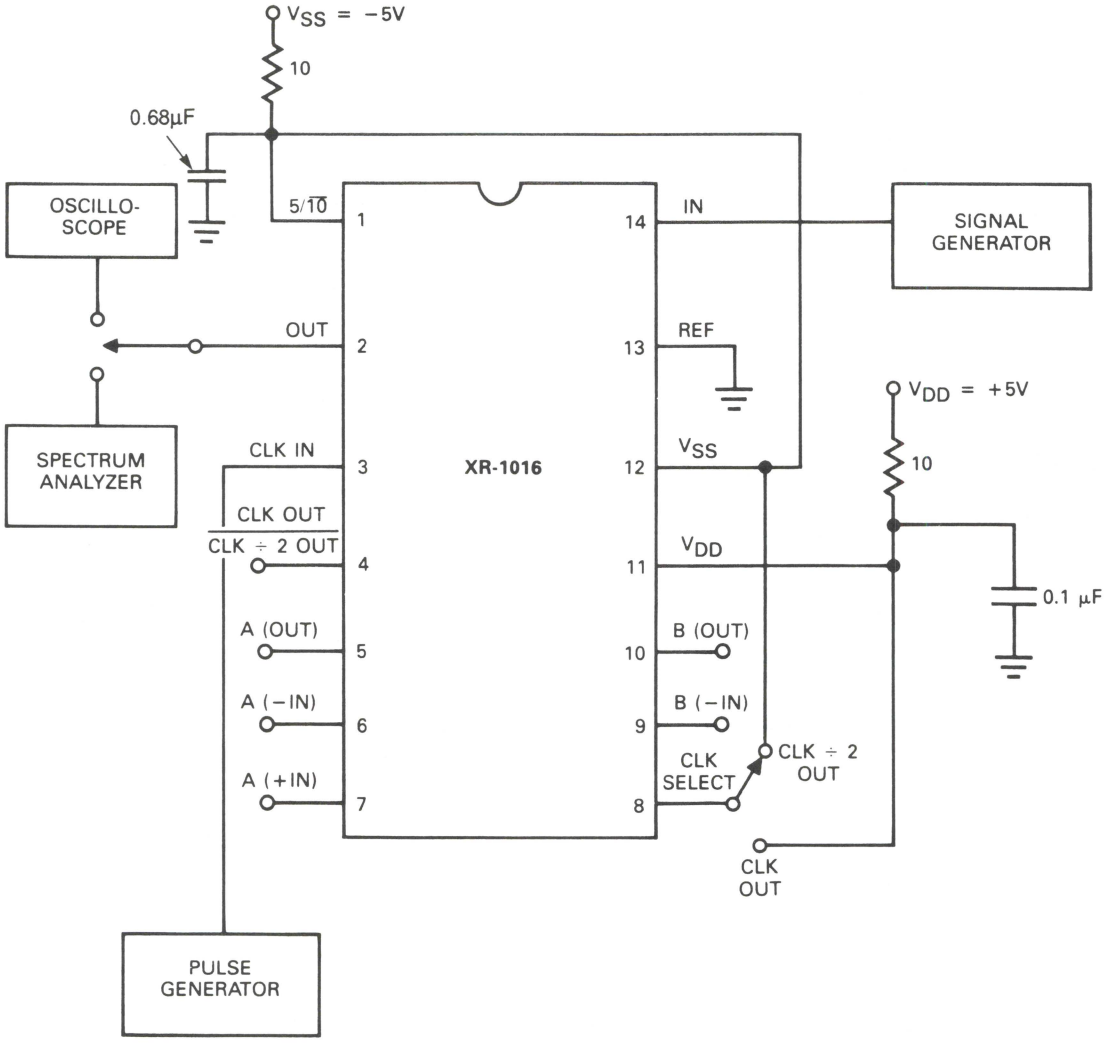


Figure 4. XR-1016 Test Circuit: 10V Operation (V_{DD} = 5V, V_{SS} = −5VDC)



Figure 5. Amplitude Response

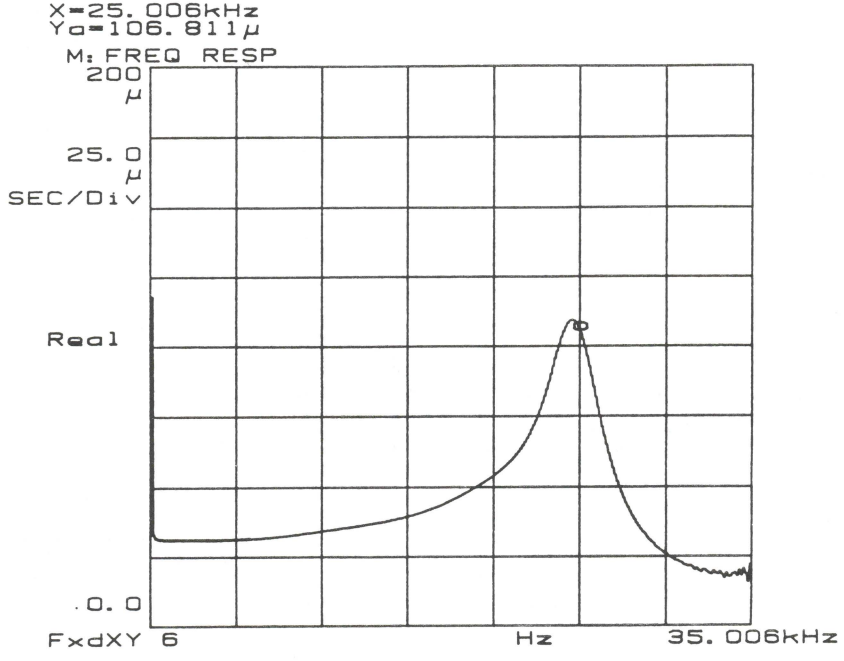


Figure 6. Group Delay Response

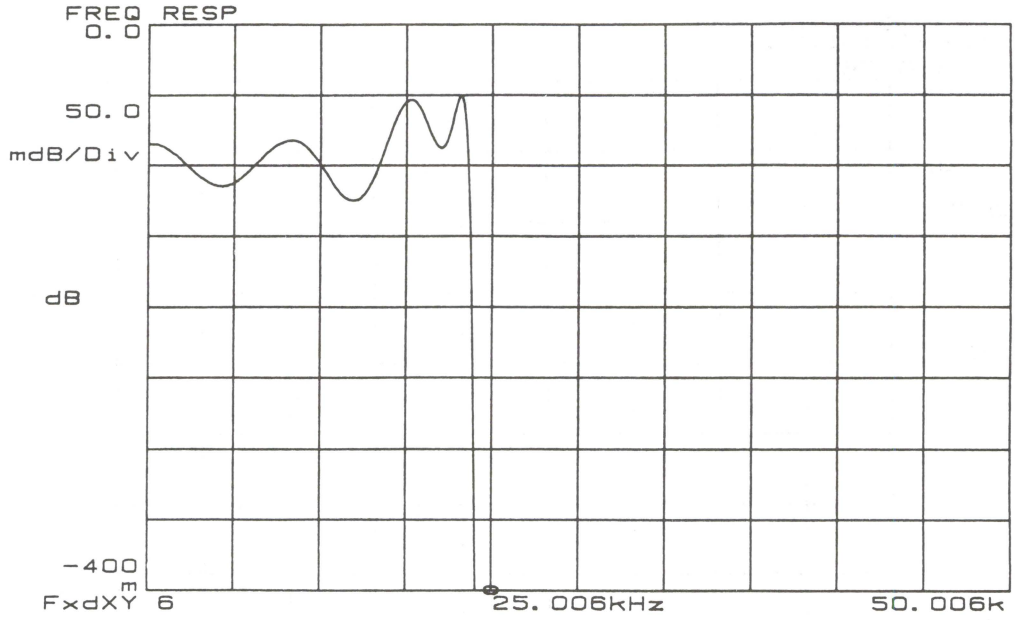


Figure 7. Typical Passband Ripple

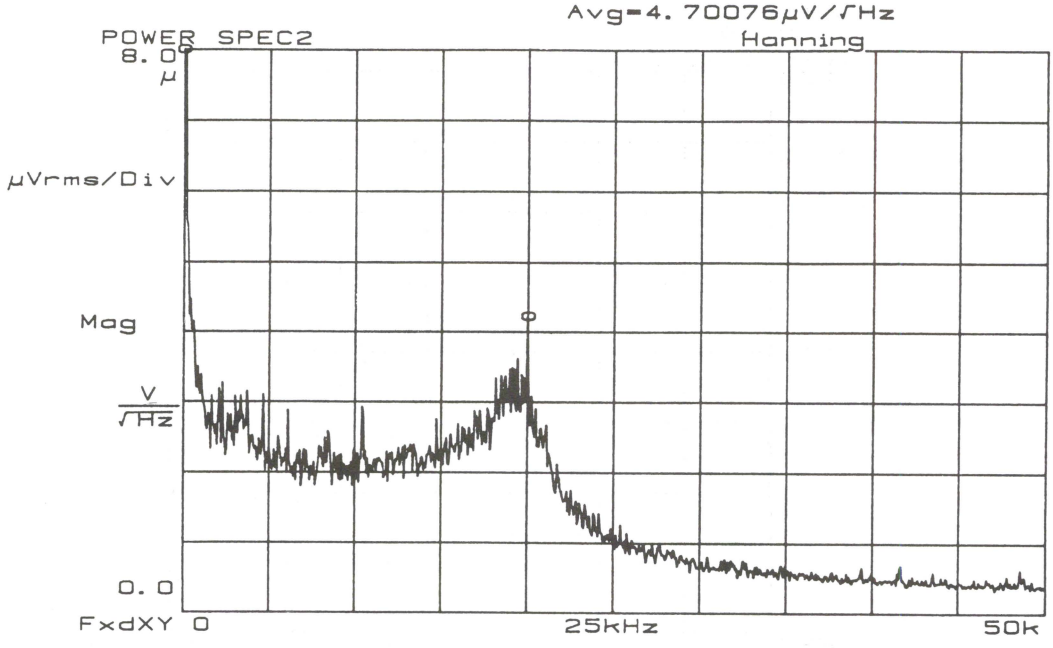


Figure 8. Typical Output Noise

PIN DESCRIPTIONS

1015 Pin	1016 Pin	Name	Description
1	1	5/10	This controls the reference level of the internal level shifters of the XR-1015 or XR-1016 in order to determine the point at which the device considers the digital inputs to be a logic 1 or a logic 0. When this input is at V_{SS}, the decision level is at 2/3 of the sum of the magnitudes of the V_{DD} and V_{SS} levels relative to V_{SS}. When the 5/10 pin is tied high, then the decision level is set for 2/3 of the sum of the magnitudes of the V_{DD} and V_{SS} in voltage relative to V_{DD}. Table 1 shows some of the possibilities of the input logic thresholds. The level at pin 1 does not affect the clock output amplitude. This output is always from near V_{DD} to near V_{SS} in amplitude.

Table 1

V_{DD}/V_{SS}	Level at Pin 1	Logic Decision Level
+5/–5 VDC	–5 VDC	1.8 VDC
	+5	–1.8 VDC
+5/0 VDC	0	3.7 VDC
	+5	1.8 VDC
+2.5/–2.5 VDC	–2.5	1.2 VDC
	+2.5	–0.7 VDC
+10/0 VDC	0	6.8 VDC
	+10	3.2 VDC

2	2	OUTPUT	The filter output. This output will drive a 10kΩ load. The signal will be centered around the voltage set by ANALOG REFERENCE.
3	–	CLOCKIN	The input clock is applied at this point. The input clock controls the position of the corner frequency of the filter using the ratio: $\frac{f_{clock}}{f_{corner}} = 100:1$ The logic threshold level needed at this point is controlled by pin 1, 5/10. Please see the pin description of 5/10 for details.
–	3	CLOCKIN	The input clock is applied to this point. The XR-1016 has an internal divider which provides either a clock to corner ratio of 100:1 or 50:1. This is controlled by pin 8 (CLOCK SELECT). If CLOCKIN is low, $f_{clock}/f_{corner} = 100:1$.
4	4	CLOCK/2	This output is the same frequency as the sampling frequency of the XR-1015 or XR-1016. It can be used to synchronize an analog-to-digital converter to the filter's output. The failing edge of the CLOCK/2 output is the edge which the output (pin 2) should be sampled in order to ensure that the output has settled.
–	5	A(OUT)	Operational amplifier A output. This is provided for creating additional filtering if desired. This output can drive a load of typically 10kΩ.
–	6	A(–INPUT)	Operational amplifier A negative input. This is a CMOS gate input with virtually infinite input impedance.
–	7	A(+INPUT)	Operational amplifier A positive input. This is a CMOS gate input with virtually infinite input impedance.

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–	8	CLOCK SELECT	This pin on the XR-1016 will select the clock to corner ratio of the filter. When this pin is at logic 0, the filter will have a clock to corner of 100:1. When this pin is tied to a logic 1, the clock to corner ratio will be 50:1. The CLOCK/CLOCK÷2 will always represent the sampling frequency of the XR-1016. The logic level control of this digital input is controlled by pin 15/10 as described under that pin description.
–	9	B(–INPUT)	Operational amplifier B negative input. Notice that the positive input of this operational amplifier 8 is tied internally to the ANALOG REFERENCE.
–	10	B(OUT)	Operational amplifier B output.
5	11	V_{DD}	Positive supply input. The range of voltages of this point is from +2.5 VDC to +5 VDC when used with dual supplies of equal magnitude. If a single supply is used the range is from +5 VDC to +10 VDC. It is recommended that a 0.47µF capacitor be tied from this pin to ground to decouple the noise on the supply line which can degrade the performance of the filter. If very low clock frequencies are used, then the size of the capacitor should be increased to keep the noise on the supply at a minimum. This capacitor should be located as close to the V_{DD} pin as possible. It is suggested that a 10Ω resistor from the positive supply to V_{DD} be used to filter system supply noise from the filter.
6	12	V_{SS}	Negative supply input. The range of the input is from –5 VDC to 0 VDC depending on the voltage present at V_{DD}. It is recommended that the pin be decoupled with a 0.47µF capacitor located as physically close as possible to the V_{SS} pin and tied from V_{SS} to ground. It is recommended that a 10Ω resistor from the negative supply to V_{SS} be used to filter system supply noise from the filter.
7	13	ANALOG REFERENCE	This pin provides the level at which the analog signals will be referenced. If equal split supplies are used, then this point is tied to ground. If unequal supplies or a single supply is used, then this point should be tied to a resistor divider circuit to provide a voltage at the analog reference pin that is 1/2 of the algebraic sum of the two supplies. Since this point is used as analog ground inside the device, it is recommended that a 0.47µF capacitor be tied from this pin to ground. As with the V_{DD} and V_{SS} decoupling, the size of this capacitor should be made larger if the clock frequency is decreased.
8	14	FILTER IN	*Fitter input:* The signal that needs to be filtered is applied to this point. It has an input impedance of 4MΩ at 1MHz clock frequency. It should be noted that any signal applied to this input greater than 1/2 of the sampling frequency will be aliased into the band of interest.

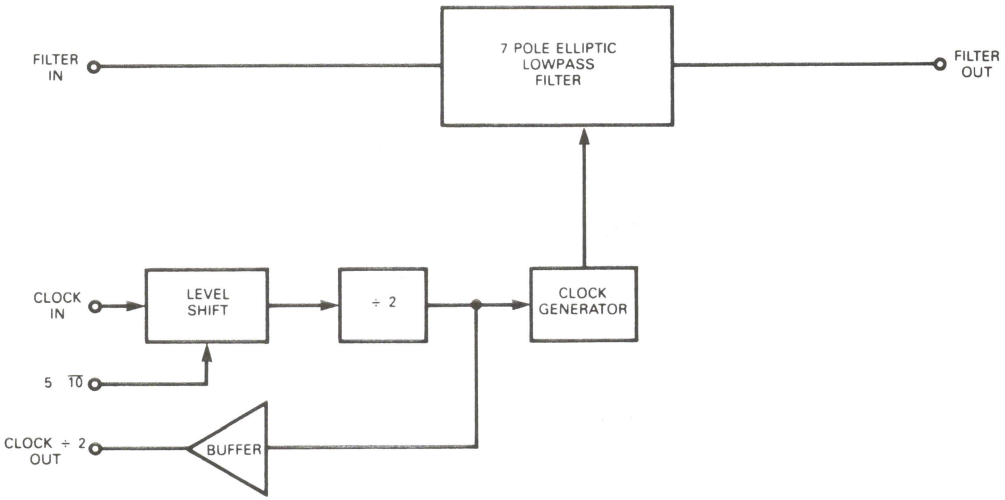


Figure 9. XR-1015 Block Diagram

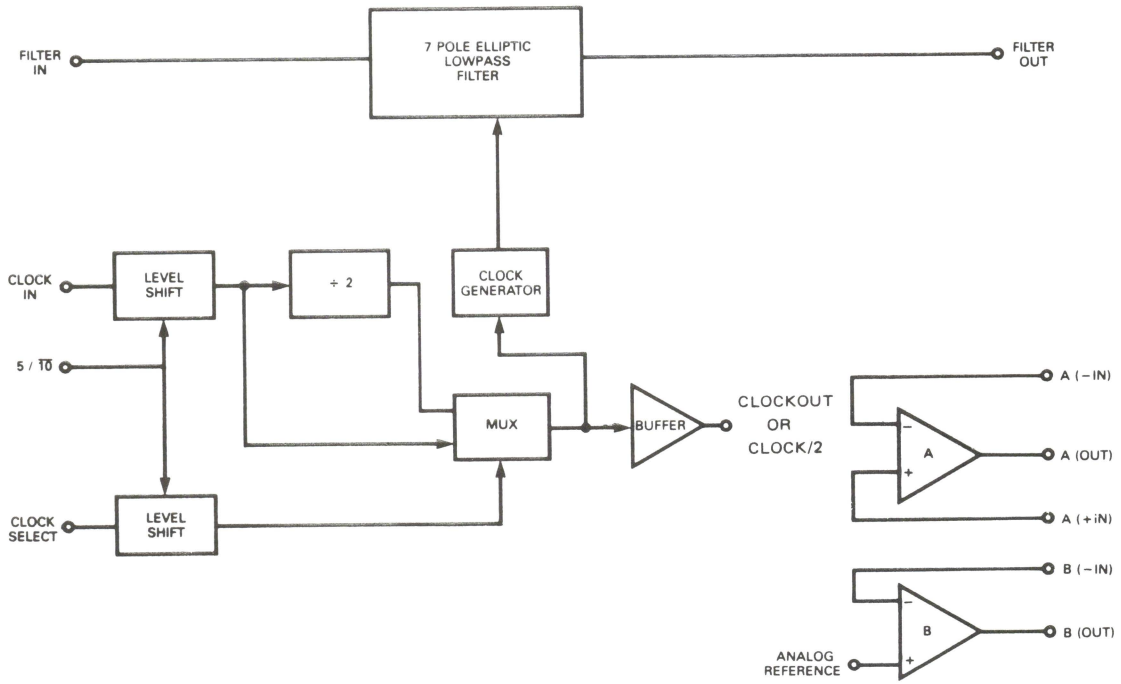
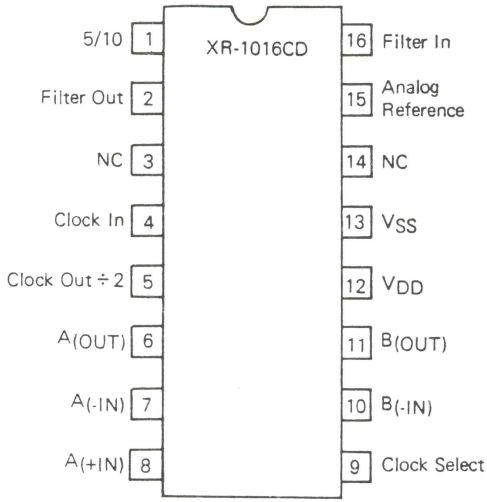


Figure 10. XR-1016 Block Diagram


XR-1016CD
5/10 1
Filter Out 2
NC 3
Clock In 4
Clock Out ÷ 2 5
A(OUT) 6
A(-IN) 7
A(+IN) 8
16 Filter In
15 Analog Reference
14 NC
13 VSS
12 VDD
11 B(OUT)
10 B(-IN)
9 Clock Select

Telecom Instrumentation Filter

GENERAL DESCRIPTION

The XR-1020A is a data communication/telecommunication instrumentation filter. This device provides ten of the filters used to characterize communication links for both IEEE/Bell and CCITT standards. The filters are:

1. C-message weighting filter
2. C-notch filter (1010Hz)
3. Psophometric filter (CCITT equivalent of C-message weighting filter)
4. CCITT psophometric notch filter (825Hz)
5. Program weighting filter
6. 3kHz flat filter
7. 15kHz flat filter
8. 1kHz band-pass filter (phase jitter measurements)
9. 50 kilobit filter (low-pass filter partion only)
10. Peak-to-average ratio band-pass filter (P/AR)

The control and selection of the ten filters is achieved with an eight bit microprocessor bus structure, complete with a strobe line ($\overline{S}$) and chip select ($\overline{CS}$). This simplifies the control of the filter functions. On-chip reconstruction filters provide the smoothing of the signals needed for precise measurements. The XR-1020A provides lower output noise then the original XR-1020.

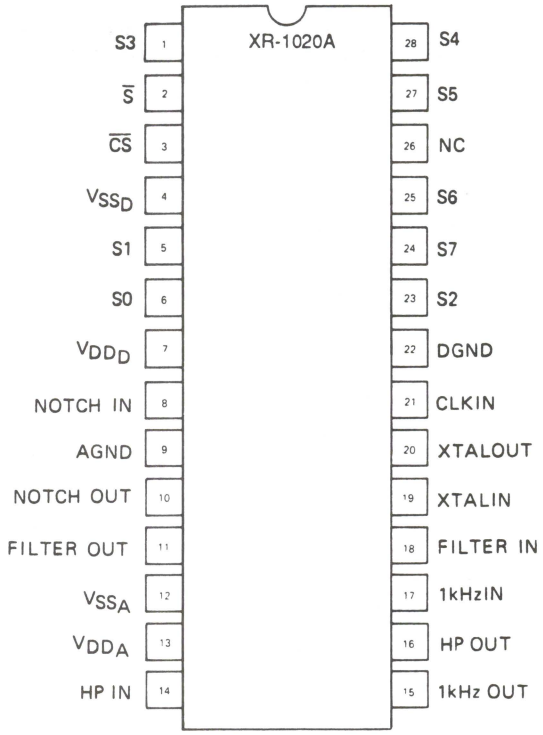
The XR-1020A uses a single 3.579545MHz crystal to provide the clock needed for the switched capacitor filters. This creates a nearly self-contained unit, requiring only digital controls for the filter selection. Additional external clock input is provided if a crystal controlled clock cannot be obtained. Also included is a power down mode allowing the device to be used in battery operated applications.

The XR-1020A uses switched capacitor techniques to implement the filter functions. The XR-1020A is fabricated in 3 micron polysilicon gate CMOS process for low noise.

FEATURES

Ten Filters Provided in One 28 Pin Dual In-Line (DIP) Package
Microprocessor Bus Interface
Low Noise
Power Down Mode for Battery Operation
3.579MHz Clock Operation with On-chip Oscillator
Separate Notch Filter Output
Separate 1 kHz Band-Pass (Phase Jitter Measurements) Filter Output
TTL/CMOS Compatible Digital Inputs
On-chip Output Smoothing Filters

PIN ASSIGNMENT



APPLICATIONS

Telephone Impairment Measurement Sets (TIMS)
C-message Weighted Meters
Telecommunication Test Instruments
Audio Test Systems
General Instrumentation Purposes
Network Management Systems

ABSOLUTE MAXIMUM RATINGS

Power Supply (Relative to V_{SS})	14 VDC
Power Dissipation (Package Limitation)	
Ceramic Package	1.4W
Derate Above 25°C	5mW/°C
Plastic Package	1 W
Derate Above 25°C	6 mW/°C
Operating Temperature	0°C to +70°C
Storage Temperature	65°C to + 150°C
Voltage at any Input	V_{SS} – 0.3 to V_{DD} + 0.3 VDC

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1020ACN	Ceramic	0°C to 70°C
XR-1020ACP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1020A provides most of the filters used to characterize telephone line quality as well as other telecommunication lines. It can be used with a microprocessor, allowing easy selection of a particular filter function.

The XR-1020A supplies the filters for the Bell Systems Technical Reference 41009, the IEEE Standard 743-1984 and the CCITT Series 0 Recommendations. The XR-1020 is used either with an external clock or with a 3,579545MHz Colorburst crystal.

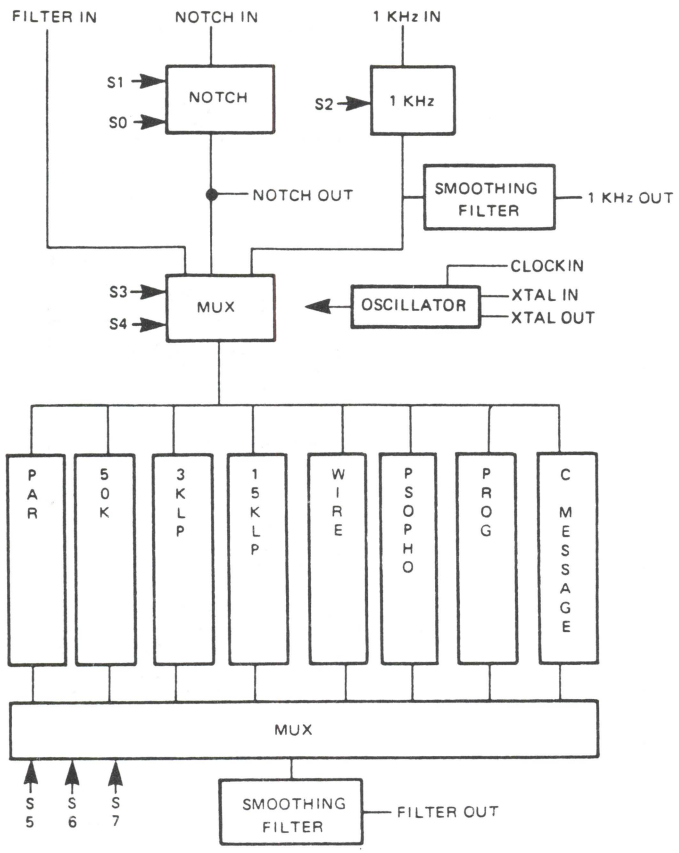
The XR-1020A provides an on-chip latch which allows the device to be memory mapped, that is, considered 8 memory location rather than a special access port. This simplifies the software writing and increases the versatility of the device.

The functional block diagram of the device is illustrated in Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5 VDC, V_{SS} = –5 VDC, R_{load} = 1MΩ, C_{load} = 40pF, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{DD}	Positive Supply Voltage					
	Single Supply	9.5	10	10.50	VDC	V_{SS} = 0 VDC
	Split Supply	4.75	5	5.25	VDC	
V_{SS}	Negative Supply Voltage					
	Split Supply	–5.25	–5	–4.75	VDC	
I_{DD}	Positive Supply Current					
	Single Supply		10	14	mA	V_{SS} = 0 VDC
	Split Supply		10	14	mA	
I_{SS}	Negative Supply Current		–10	–14		
BUS INPUT CHARACTERISTICS						
V_{IL}	Input Voltage, Logic Low			0.8	V	
V_{IH}	Input Voltage, Logic High	2.8			V	
I_{IL}	Input Current, Logic Low	–1.0		+1.0	µA	
I_{IH}	Input Current, Logic High	–1.0		+1.0	µA	
t_{CS}	Time for Chip, Select to Latch	100			nS	See Figure 5
t_{SB}	Time for Strobe to Latch	100			nS	See Figure 5
t_{data}	Time for Data to be Stable	150			nS	See Figure 5
t_{delay}	Delay Time from Strobe or Chip Select to Data Change	50			nS	



S1	S0	FUNCTION
X	0	Notch Off (Powered Down)
0	1	1010Hz Notch
1	1	825Hz Notch

S2	FUNCTION
0	1K Off (Powered Down)
1	1K

S4	S3	FUNCTION
0	X	FILTER IN PIN
1	0	NOTCH OUTPUT
1	1	1K OUTPUT

* S4-S3 determine what is selected by the input mux as input to the mode selected by S7-S5.

S7	S6	S5	FUNCTION
0	0	0	PAR
0	0	1	50K
0	1	0	3K LP
0	1	1	15K LP
1	0	0	WIRE
1	0	1	PSOPHOMETRIC
1	1	0	PROG-WEIGH
1	1	1	C MESSAGE

— The 1KHz and NOTCH (825Hz & 1010Hz) filters have separate outputs. The 1KHz output is possed through a smoothing filter. The WIRE mode can be used for smoothing the NOTCH filter output, if desired.

— The highpass portion of the 50K filter (external) is connected in between the HPIN and HPOUT terminals: HPIN is connected to the output of the highpass? HPOUT is connected to the input of the highpass.

— 3.579545MHz colorburst crystal is connected in between the XTALIN and XTALOUT pins. In this case, the CLKIN pin should be connected HI or LO. 20pF capacitors on both sides of the crystal to ground, as well as a 10MΩ resistor across the crystal are needed.

If the above clock frequecy is already available in the system then the CLKIN Pin can be used. In this case, the XTALIN pin should be connected to V_{DD} or to V_{SS}.

— The microcompatibility is controlled by the S (strobe) and CS (chip select) pins. Both inputs must be LO for input to latch.

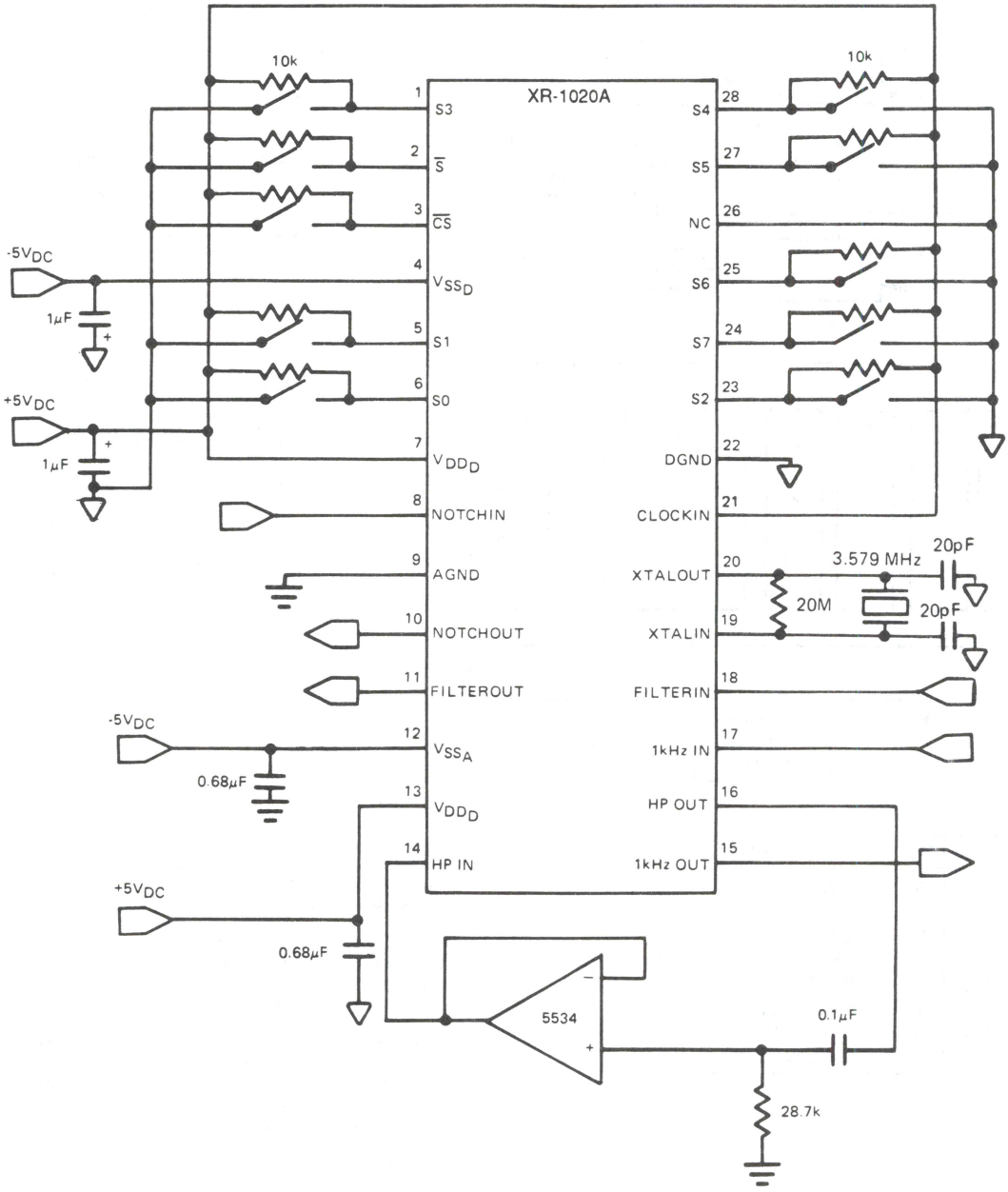


Figure 2. Typical Test Circuit

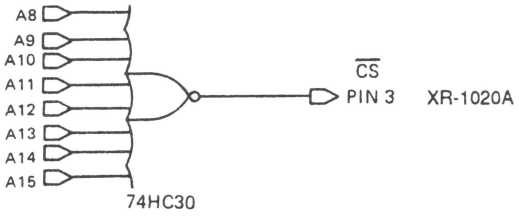


Figure 3. Typical Method for High Order Byte Decoding

SYSTEM DESIGN USING THE XR-1020A

The XR-1020A has been optimized for use with a standard 16 bit wide address bus. A decoder circuit will be needed for using the CS pin of the XR-1020, The lower 8 bits should be tied directly to the S0 through S7 digital inputs of the XR-1020A

The higher order bits, A8 through A15, need a decoder depending upon the system and the present use of the microprocessor. In one application, where location OXFFXX is to be used for the XR-1020A, the 74HC30 can be used for decoding the location. Figure 3 shows the use of the XR-1020A with the 74HC30. When the high order byte is high, the output of the 74HC30 will go low, which would select the XR-1020A for use. With the use of inverters, other locations can be decoded and used.

Figure 1 gives information as to which function is selected. The pin description provides information as to which bit controls which filter function.

The strobe pin, used to latch in the information present on the address bus, can be used when the data lines and lower byte address are multiplexed on the same eight lines.

In applications where a microprocessor will not be used (analog meters or other manual select systems), a decoder can be used such as the 74HC148 to convert the switch information to a binary format. Figure 5 shows the use of the XR-1020A with the 74HC148 for a push button system. The pin descriptions can be used in this application to determine the decoding of the button function of the system.

The use of the 50 kilobit filter requires a 50Hz high-pass filter to be added to the HPOUT and HPIN pins of the XR-1020A. Figure 13 shows the filter shape used for this: The schematic for this first order, continuous time high-pass filter is shown in Figure 1. To prevent degradation of the performance of the XR-1020A, it is recommended that a low noise operational amplifier such as the XR-5532 be used for the filter shaping. Also, the components should be 1% precision in order to prevent the filter shape from changing with production variations. Such a situation may cause peaking in the pass-band response and affect the measurements obtained with the 50 KBPS filter.

If no consideration is given to the layout of the external operational amplifier circuit, additional noise may be added to the signal present on the output of the low-pass reducing the dynamic range of the 50 KBPS amplitude and distortion tests. The feedback trace from the operational amplifier output to the inverting input should be kept as short as possible. This will reduce the chance of any stray noise from being amplified by the filter.

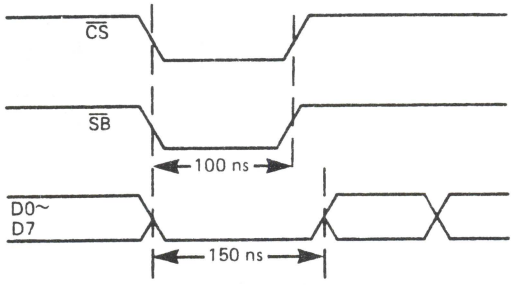


Figure 4. Typical Timing for CS and S Data Bus

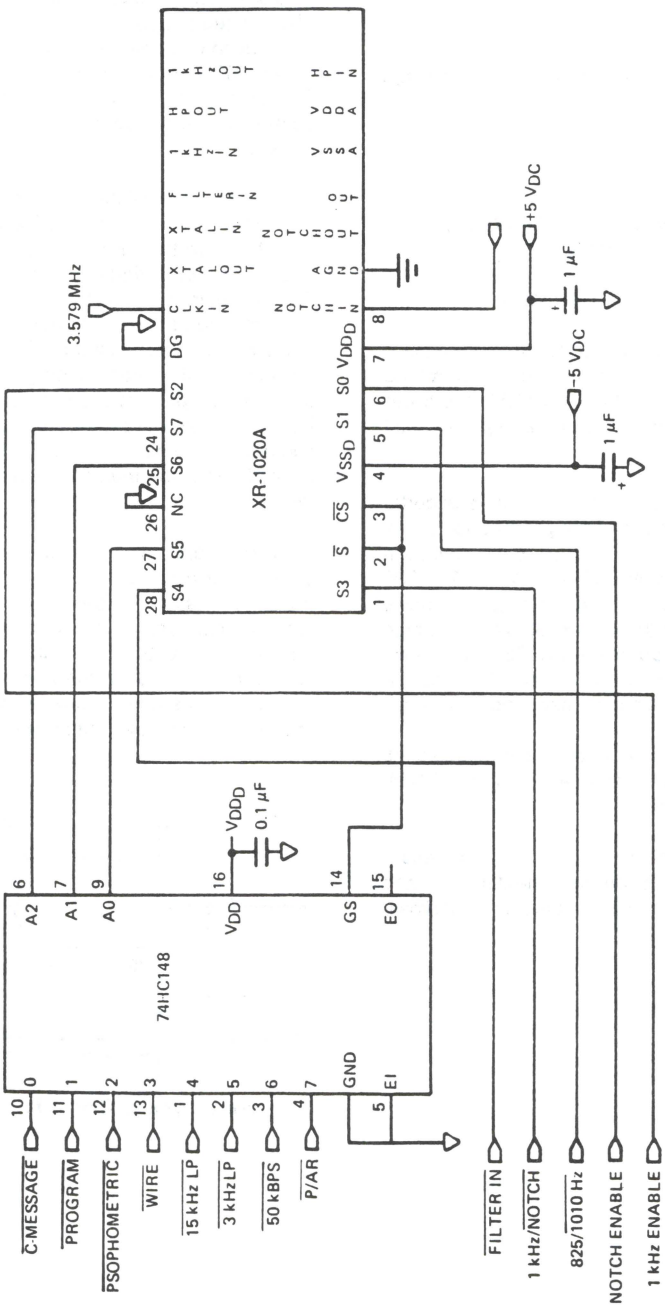


Figure 5. Push Button Interface with the XR-1020 (without microprocessor)

PIN DESCRIPTIONS

Pin#	Symbol	Desciption
1	S3	*Digital Input S3:* This with S4, Pin 28 selects which input is applied to the filter bank as shown in the block diagram.
2	S	*Strobe:* This input, when high, latches in the data present on the lines S0 through S7. When S is high, changes on the address bus will not affect the state of XR-1020A.
3	CS	*Chip Select:* This input, when low, selects the XR-1020A for addressing. The delay between chip select going high and strobing in the new address is 50ns.
4	V_{SS_D}	*Digital V_{SS}:* This input is the negative supply for the digital portion of the XR-1020A. In order to obtain the low noise operation that is needed in an instrumentation filter, this input must be decoupled with a 10µF tantalum, in parallel with a 0.68µF ceramic capacitor.
5	S1	*Digital Input S1:* Selection of the 825Hz or 1010Hz filter is done with this input. When this input is latched high, the 825Hz notch for CCITT standard measurements is selected. When this input is latched low, the 1010Hz notch filter for Bell standard measurements is selected. This assumes that S0 is latched high.
6	S0	When high, the notch filter is selected. When a logic low is latched on this pin, the notch filter is in the power down mode. S1 input is in a "don't care" situation when S0 is latched low.
7	V_{DD_D}	*Digital V_{DD}:* This input is the positive supply for the digital portion of the XR-1020A. Proper decoupling of this pin is required for low noise operation of this instrumentation filter. Decoupling with a 10µF tantalum capacitor, in parallel with a 0.68µF ceramic capacitor is required.
8	NOTCH IN	*Notch filter input:* This is the input to the notch filter. The location of the notch (1010Hz or 825Hz) is set with the address bus as outlined in Figure 1. Since this is an analog input, it is best to keep this signal as far as possible from any digital inputs. Shielding is recommended in most applications to prevent any clock coupling from occurring. The input impedance at this pin is 1MΩ.
9	AGND	*Analog ground:* This pin is the analog reference for the XR-1020A. In order to obtain the low noise operation possible with the XR-1020A, it is very important to have a very low noise ground available. For split supply operation, the AGND pin should have its own separate trace from the supply connector on the edge of the system board-to here. To prevent any inductive components, this trace should be as wide as possible, or as short as possible. An ideal case would be to have the analog ground also act as ground plane or shield for pins 8 through 18. The shield should be kept away from the digital inputs and clocks.
10	NOTCHOUT	*Notch filter output:* This is the output of the 1010 or 825Hz notch filter. It is designed to drive a typical 10kΩ load. For distortion analysis, it is necessary to keep this signal from any clocks or other signals that may couple to this trace and cause an error in measurements. Note that the notch filter input (Pin 8) is separated from the output by analog ground for this reason. To combine the notch output with other portions of the system, the SD5000 quad NMOS field-effect transistors or the 74HC4053 is recommended, due to the low on resistance and the small cross coupling.

5

11 FILTEROUT *Filter output:* This is the output of the output multiplexer and continous-time smoothing filter. The filter shape available at this point is controlled by the address lines S0 through S7. The C-message weighting, Program weighting, psophometric, 3 or 15kHz low pass, 50 KBPS low pass, and peak-to-average filters can be obtained at this pin.

This output should be kept away from other clocks in the system to avoid coupling of this signal to the signal present at this pin.

As with the notch filter output, this output is designed to typically drive a 10kΩ load.

12 V_{SS_A} *Analog V_{SS}:* This is the negative supply for the analog portions of the XR-1020A. It must be a low noise, low impedance supply to obtain satisfactory performance from the XR-1020A and avoid any degradation in the operation of the filters.

With split supply operation, this pin is tied to –5 VDC ± 5%. It must be decoupled with a 0.68µF ceramic capacitor to analog ground. In parallel with the ceramic capacitor, a 10µF tantalum capacitor must be used. This will prevent any noise on the supply lines from being coupled to the signals to be filtered. These two caps must be located as close as possible to Pin 12 of the device. If possible, the best arrangement is obtained when a separate V_{SS} regulator is used. The LM79L05AC could be used in such a case. The output of the regulator should be tied only to V_{SS_A}, Pin 12 of the XR-1020A.

13 V_{DD_A} *Analog V_{DD}:* This is the positive analog supply and must be decoupled to analog ground with a 10µF tantalum capacitor as well as a 0.68µF ceramic capacitor. These capacitors should be as physically close to Pin 13 of the package as possible.

This analog V_{DD} should be separated from the digital V_{DD} throughout the system connecting only at the supply connector of the system This pin is set to +5 VDC (±5%).

Note that in both single and split supply operation, decoupling is needed. In single supply operation, this pin should be tied to +10 VDC (±5%).

For optimum performance, a regulator such as the XR-4194 with the above decoupling should be used. This regulated should only be used with the XR-1020 V_{DD_A}. An LM78L-05AC could be used as well. This prevents any noise present on the system V_{DD} from affecting the measurements made with the XR-1020A.

14 HP IN *50 KBPS input:* This, in most applications, is tied to the output of the external 50Hz high-pass filter. Note that this input is tied internally to the output multiplexer so that no external selector needs to be used in most applications.

The entire 50 Hz continuous time high-pass filter as well as the input and output of the 50 KBPS filter should be kept away from the rest of the system's clocks, to prevent degradation of the measurements made.

15 1kHz OUT *1kHz band-pass filter output:* This output is provided separate from the other filters for tests requiring phase jitter measurements at the same time as other measurements.

A continuous time smoothing filter is provided to eliminate the need of an external filter.

Note that there are some address selections that can keep the 1kHz (phase jitter) filter in the power down mode and provide no output. Refer to Figure 1 for details.

As with other outputs, this pin can typically drive a 10kΩ load.

16 HP OUT

50 KBPS filter output: This output is used to add the external 50Hz high-pass filter to the 50 KBPS low-pass filter shape.

Note that no output will appear at this pin if the 50 KBPS is not selected using the address bus. Refer to Figure 1 for more information.

The output is designed to drive a 10kΩ load. This should be considered when the external circuit is designed.

17 1kHz IN

1kHz band-pass filter input: This input provides access to the phase jitter band-pass filter input. It is separated from the other filter functions in order to allow for flexibility in measurements.

As with the other filter inputs, this input should be kept away from any system clocks that may add noise to the inputs. A ground plane or trace surrounding this and other filter input pins will be helpful.

The input impedance at this pin is 1MΩ.

18 FILTER IN

Filter multiplexer input: This input provides access to the eight filter functions, as described in Figure 1.

The input impedance at this pin is 1MΩ.

19 XTAL IN

Crystal input: This is used with the XTAL OUT to create a 3.579545MHz oscillator. A parallel ressonant crystal should be used to obtain the ±0.01% accuracy to prevent clock inaccuracy from affecting the position of the filter shape. If not used, it must be tied to either $V_{DD_D} - V_{SS_D}$.

20 XTAL OUT

Crystal output: This input is used with the Pin 19 crystal input to obtain the clock. Note that external capacitors are used to accurately get the crystal oscillating frequency as shown in the Typical Application Circuit diagram.

A parallel resonant crystal must be used to obtain the proper oscillatory frequency. If this pin is not used, it should be disconnected.

21 CLK IN

Clock input: At this pin is applied the 3.579545MHz clock from the system if it is desired not to use the on-chip oscillator. If this pin is not used, it should be tied to either V_{DD_D} or V_{SS_D}.

22 DGND

Digital ground: This input provides the reference for the digital portions of the XR-1020A. It should be tied to the digital ground of the system, separate from the analog ground of Pin 9, AGND. The two grounds may connect at the supply.

As with the analog ground, a wide trace is needed to reduce any inductive components in the system.

23 S2

Digital input S2: This is address line 2 and controls the use of the 1kHz band-pass (phase jitter) filter. When latched high, the 1kHz band-pass filter is selected. When this input is latched low, the 1kHz band-pass filter is in the power down mode. Details on its operation are given in Figure 1. With split supply operation, all digital inputs are TTL compatible.

24 S7

Digital input S7: This input, along with the address lines S6 and S5, controls the selection of the eight filters obtained with the on-chip multiplexers. Details are given with the pin description for digital input S5.

25 S6 — *Digital Input S6:* This input, with address lines S7 and S5, controls the input and output multiplexers. This is detailed with the pin description for S5, digital input S5 (Pin 27).

26 NC — *No internal connection:* Due to the closeness to the other digital inputs, it is recommended that this pin be tied to digital ground (DGND), Pin 22.

27 S5 — *Digitai input S5:* This digital input, along with S7 and S6, controls which of eight filter functions will be selected using the on-chip multiplexers.

S7	S6	S5	Function
0	0	0	Peak-to-average filter is selected.
0	0	1	50 KBPS filter is selected.
0	1	0	3kHz low-pass filter is selected.
0	1	1	15kHz low-pass filter is selected.
1	0	0	Wire (direct from input multiplexer to output multiplexer).
1	0	1	Psophometric weighting filter (for CCITT noise measurements).
1	1	0	Program-weighting filter.
1	1	1	C-message weighting filter (for Bell noise measurements).

28 S4 — *Digital input S4:* This digital input, along with S3 (Pin 1), selects which of the three inputs will be applied to the input multiplexer.

S4	S3	Function
0	X	Filter input. Note that when S4 is latched low, S3 is in the "don't care" mode.
1	0	1010 Hz (825 Hz) notch filter is the input selected, Note that if SO is latched low, then no usable signal would be applied to the filter bank since the notch filter would be in the power down mode.
1	1	When this combination is latched into the XR-1020A, the 1kHz band-pass (phase jitter) filter is selected. Note that S2, the 1kHZ band-pass filter enable, must be latched high, or no usable output will appear at the filter output.

Board Layout

The device is divided approximately in half with Pins 1 through 7, and Pins 19 through 28 having digital functions, and the rest having an analog function. It is best to use the XR-1020A at the dividing point between the analog and digital portions of the systems as would be done with an analog-to-digital converter.

An analog ground plane for the filter inputs and outputs is recommended, as long as the trace from the ground plane to the supply ground can be made wide enough to prevent the ground plane from acting as a capacitor or an antenna.

FILTER CHARACTERISTICS

1KHz Band-pass Filter (Phase Jitter), see Figure 6

Parameter	Min.	Typ.	Max.	Unit	Conditions
Output Offset					
Voltage–0.5	0	+0.5		V	V_{IN} = 0V
Input Frequency					
Less than 100Hz		–35		dB	V_{IN} = 1Vrms
150Hz			–28	dB	
250Hz			–20	dB	
300Hz	–15		–18	dB	
500Hz	–10		–8	dB	
600Hz	–5	–5		dB	
700Hz	–3	–3		dB	
1000Hz	–1	0	+1	dB	
2000Hz		–12		dB	
3000Hz		–20	–18	dB	
Greater than					
3500Hz			–25	dB	

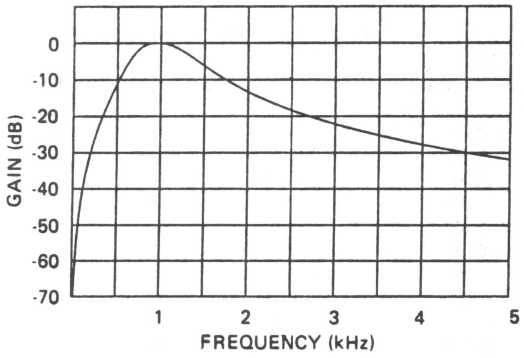


Figure 6. Amplitude Response: 1kHz Band-pass

FILTER CHARACTERISTICS

C-Message Weighting Filter, see Figure 7

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
100Hz		–42.5		dB	V_{IN} = Vrms
200Hz	–27.0	–25.1	–23.0	dB	
300Hz		–16.3		dB	
400Hz	–12.2	–11.2	–10.2	dB	
500Hz		–7.7		dB	
600Hz		–5.0		dB	
700Hz		–2.8		dB	
800Hz		–1.3		dB	
900Hz		–0.3		dB	
1000Hz	–1.0	0.0	+1.0	dB	
1200Hz		–0.4		dB	
1300Hz		–0.7		dB	
1500Hz		–1.2		dB	
1800Hz		–1.3		dB	
2000Hz		–1.1		dB	
2500Hz		–1.1		dB	
2800Hz		–2.0		dB	
3000Hz	–4.0	–3.0	–2.0	dB	
3300Hz		–5.1		dB	
3500Hz	–9.1	–7.1	–5.1	dB	
4000Hz		–14.6		dB	
4500Hz		–22.3		dB	
5000Hz	–31.7	–28.7	–25.7	dB	

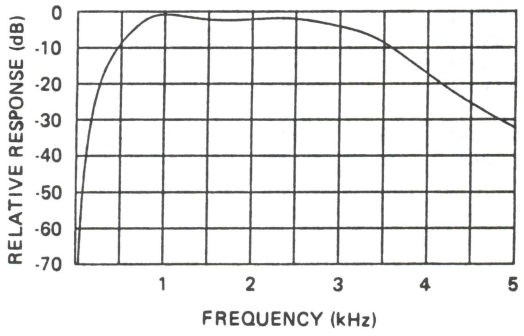


Figure 7. Amplitude Response: C-Message

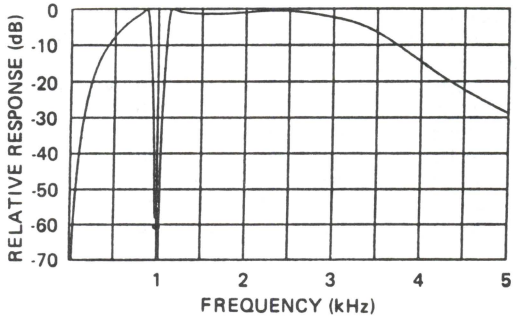


Figure 8. Amplitude Response: C-Notch (1010 Notch with C-Message Weighting Filter)

FILTER CHARACTERISTICS

Psophometric Weighting Filter, see Figure 9.

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
16.66Hz		–85		dB	V_{IN} = Vrms
50Hz		–63.0		dB	
100Hz		–41.0		dB	
200Hz	–23.0	–21.0	–19.0	dB	
300Hz		–10.6		dB	
400Hz	–7.3	–6.3	–5.3	dB	
500Hz		–3.6		dB	
600Hz		–2.0		dB	
700Hz		–0.9		dB	
800Hz	–1.0		+1.0	dB	
900Hz		+0.6		dB	
1000Hz		+1.0		dB	
1200Hz	–1.0	0.0	+1.0	dB	
1400Hz		–0.9		dB	
1600Hz		–1.7		dB	
1800Hz		–2.4		dB	
2000Hz		–3.0		dB	
2500Hz		–4.2		dB	
3000Hz	–6.6	–5.6	-4.6	dB	
3500Hz		–8.5		dB	
4000Hz		–15.0		dB	
4500Hz		–25.0		dB	
5000Hz		–36.0		dB	
6000Hz	–47	–43	–39	dB	

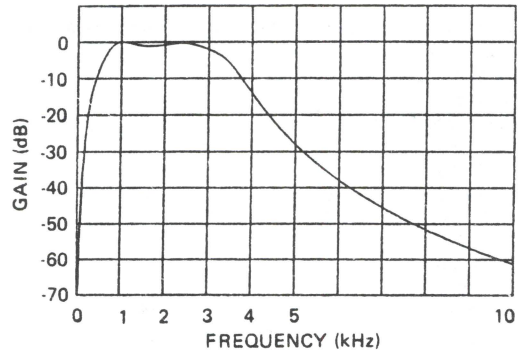


Figure 9. Amplitude Response: Psophometric Filter

FILTER CHARACTERISTICS

3kHz Low-Pass Filter, see Figure 10

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
30Hz		0		dB	V_{IN} = Vrms
60Hz		0		dB	
400Hz	–1	0	+1	dB	
1000Hz	–1	0	+1	dB	
2010Hz	–1.8	–0.2	+0.2	dB	
3000Hz	–4.8	–3.0	–1.2	dB	
6000Hz	–15.3	–12.3	–9.3	dB	

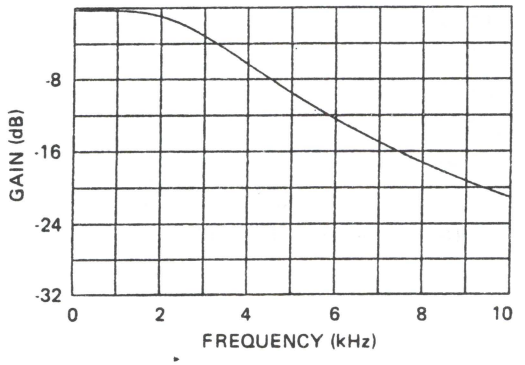


Figure 10. Amplitude Response: 3kHz Low-Pass Filter

FILTER CHARACTERISTICS

825Hz Notch, see Figure 11

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
325Hz	–1.5	0		dB	V_{IN} = Vrms
570Hz	–2.0	0		dB	
690Hz	–4	0		dB	
827Hz		–70	–50	dB	
855Hz		–70	–50	dB	
1000Hz	–4	0		dB	
1105Hz	–2	0		dB	
1360Hz	–1.5	5	0	dB	

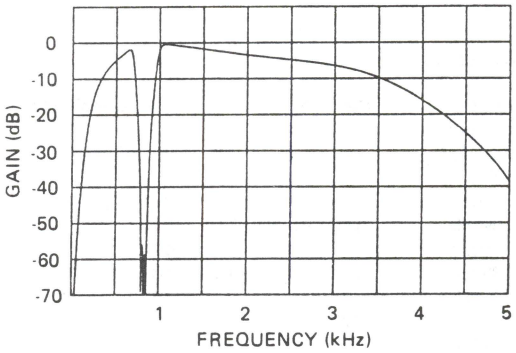


Figure 11. 825Hz Notch and Psophmetric Filter

FILTER CHARACTERISTICS

1010Hz Notch Filter, see Figure 12

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0.1	0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
400Hz	–1.5	0		dB	V_{IN} = Vrms
529Hz		0		dB	
700Hz	–2.0	0		dB	
860Hz	–4	–1		dB	
995Hz		–70	–50	dB	
1010Hz		–70	–50	dB	
1025Hz		–70	–50	dB	
1180Hz	–4.0	0		dB	
1330Hz	–2.0	0		dB	
1700Hz	–1.5	0		dB	

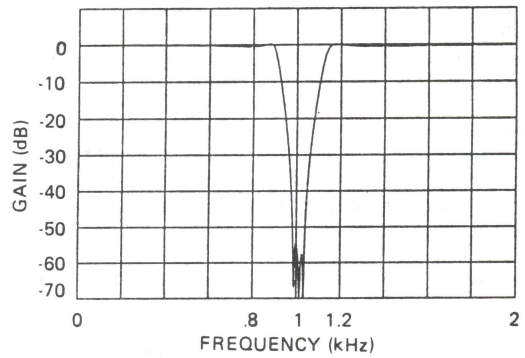


Figure 12. 1010Hz Notch Amplitude Response

FILTER CHARACTERISTICS

50 KBPS Weighting Filter Low-Pass Filter Section, see Figure 13

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5		+0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
50Hz		0		dB	V_{IN} = Vrms
200Hz		0		dB	
400Hz	–1	0	+1	dB	
1000Hz	–0.2	0.0	+0.2	dB	
5000Hz		0		dB	
10000Hz	–1.8	–0.1	+0.2	dB	
15000Hz	–4.8	–0.4	–0.2	dB	
20000Hz		–1.0		dB	
25000Hz	–3.1	–1.9	–1.1	dB	
30000Hz	–4.6	–3.1	–1.6	dB	
35000Hz		–4.7		dB	
40000Hz		–7.9		dB	
45000Hz		–14.0		dB	
55000Hz			–29.0	dB	
Greater than 550000Hz			–30.0	dB	

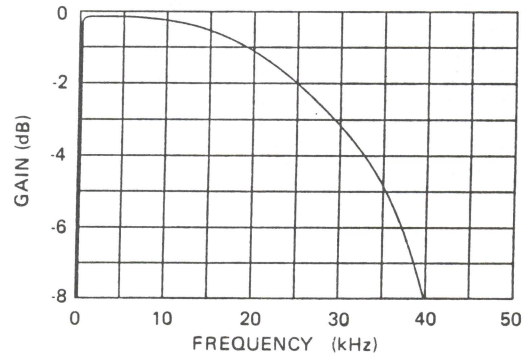


Figure 13. Amplitude Response: 50 kBPS Filter with 50Hz High-pass Filter

FILTER CHARACTERISTICS

Peak-to-Average Ratio (P/AR) Band-pass Filter, see Figure 14

Receiver Response

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency: f_o					
140Hz		–50.5		db	V_{IN} = Vrms
390Hz	–34.5	–31.5	–28.5	dB	
640Hz	–22.4	–20.4	–18.4	dB	
890Hz	–12.63	–10.6	–8.63	dB	
1140Hz		–2.1		dB	
1390Hz	–1.6	–0.6	+0.4	dB	
1640Hz		–5.5		dB	
1890Hz	–12.5	–10.5	–8.5	dB	
2140Hz		–14.5		dB	
2390Hz		–17.7		dB	
2640Hz	–22.4	–20.4	–18.4	dB	
2890Hz		–22.7		dB	
3140Hz		–24.6		dB	
3390Hz		–26.4		dB	
3640Hz		–27.9		dB	
3890Hz	–33.3	–29.3	–26.3	dB	

Receiver Phase

Includes removal of an approximate = cycle (at 56kHz) linear phase error (inherent in sample data devices) which can be subtracted out by normal system linear phase compensation networks.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input Frequency: f_o					
140Hz		173.77		degree	
390Hz		161.2		degree	
640Hz		143.6		degree	
890Hz		114.0		degree	
1140Hz		55.2		degree	
1390Hz		–31.2		degree	
1640Hz		–87.2		degree	
1890Hz		–114.5		degree	
2140Hz		–129.6		degree	
2390Hz		–138.8		degree	
2640Hz		–145.1		degree	
2890Hz		–149.8		degree	
3140Hz		–153.3		degree	
3390Hz		–156.1		degree	

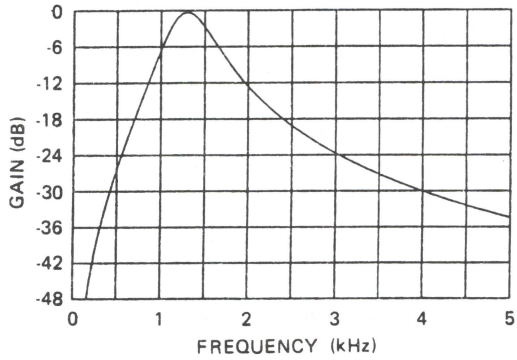


Figure 14. Amplitude Response: Peak-to-Average Ratio Band-pass Filter

FILTER CHARACTERISTICS

Program Weighting Filter, see Figure 15

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0.1	+0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
100 Hz		–26.3		dB	V_{IN} = Vrms
200 Hz	–19.3	–17.3	–15.3	dB	
300 Hz		–12.2		dB	
400 Hz		–9.0		dB	
500 Hz	–8.6	–6.6	–4.6	dB	
600 Hz		–4.7		dB	
700 Hz		–3.2		dB	
800 Hz		–2.0		dB	
900 Hz		–0.8		dB	
1000 Hz	–1.0		+1.0	dB	
1500 Hz	+2.2	+3.2	+4.2	dB	
2000 Hz	+3.5	+4.8	+5.5	dB	
2500 Hz		+5.6		dB	
3000 Hz		+6.0		dB	
4000 Hz		+6.5		dB	
5000 Hz	+3.5	+6.5	+9.5	dB	
6000 Hz		+6.4		dB	
7000 Hz		+5.8		dB	
8000 Hz	0.0	+4.0	+8.0	dB	
9000 Hz		+1.5		dB	
10000 Hz	–12.5	–8.5	–4.5	dB	

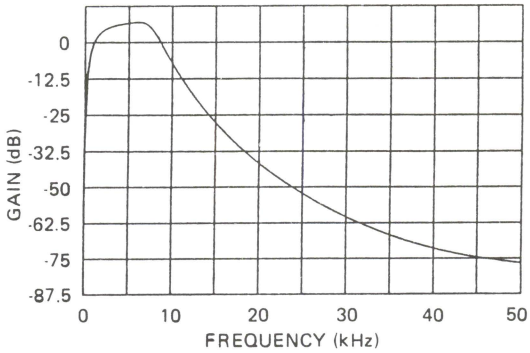


Figure 15. Amplitude Response: Program Weighting Filter

5

FILTER CHARACTERISTICS

15kHz Low-Pass Filter, see Figure 16

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency: f_o					
30 Hz		0		dB	V_{IN} = Vrms
60 Hz		0		dB	
400 Hz	–1	0	+1	dB	
1000 Hz	–1	0	+1	dB	
10000 Hz	–1.8	-0.8	+0.2	dB	
15000 Hz	–4.8	–3.0	–1.2	dB	
30000 Hz	–15.3	–12.3	–9.3	dB	

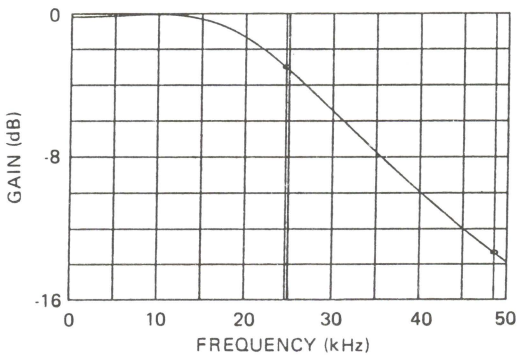


Figure 16. Amplitude Response: 15 kHz Low-pass Filter



NOTES



Graphic Equalizer Display Filter

GENERAL INFORMATION

The XR-1091 is an eight output switched-capacitor band pass filter dedicated for use in audio applications. Seven of the outputs are from bandpass filters spaced 1 1/2 octaves apart starting at 63 Hz. The eighth output is the peak of the seven outputs. All of the outputs provide a peak hold for use with most display circuits. The two inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant audio information from being displayed.

The XR-1091 is available in a 16 pin plastic DIP. The XR-1091 is fabricated in 2 μm double polysilicon CMOS for low noise and low clock feedthrough. The nominal operating voltages are ±5 VDC to ±6 VDC. The self contained oscillator is designed to operate at 400 KHz with an external resistor and capacitor.

FEATURES

Internal R/C Oscillator
Provides seven filters in one 16 pin package
Dual Inputs for summing Left and Right Channels
Provides 30 dB of Gain
Low Noise CMOS
Electro-Static Discharge (ESD) Protection

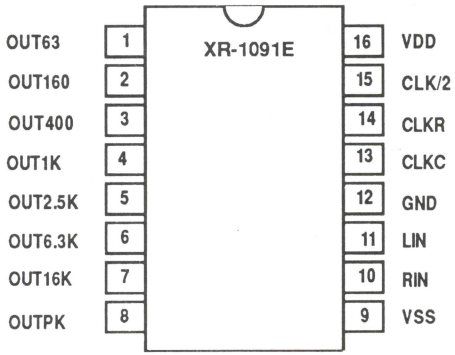
APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems

ABSOLUTE MAXIMUM RATINGS

V_{DD}	+7 VDC
V_{SS}	-7 VDC
Power Dissipation	
16 Pin Plastic Dip	650 mW
derate above 25°C	5 mW/°C
Storage Temperature	-60°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1091E	CP16 Pin Plastic DIP	-30°C to +75°C

SYSTEM DESCRIPTION

The XR-1091 unlike most switched-capacitor filters does not require an external clock source in order to provide the sampling clocks. This allows the designer to place the XR-1091 in any application where an active filter design is in place. The XR-1091 provides bandpass filters with center frequencies at 63 Hz, 160 Hz, 400 Hz, 1 KHz, 2.5 KHz, 6.3 KHz, and 16 KHz. These frequencies are standards in the consumer audio market. The peak detector outputs referenced to 0V can be used to drive a variety of display decoders.

The XR-1091 contains a continuous time anti-aliasing filter with a corner frequency of 80 KHz. This prevents most signals from affecting the performance of the filters. If two separate displays are desired, then two XR-1091's could be used with the unused inputs grounded.

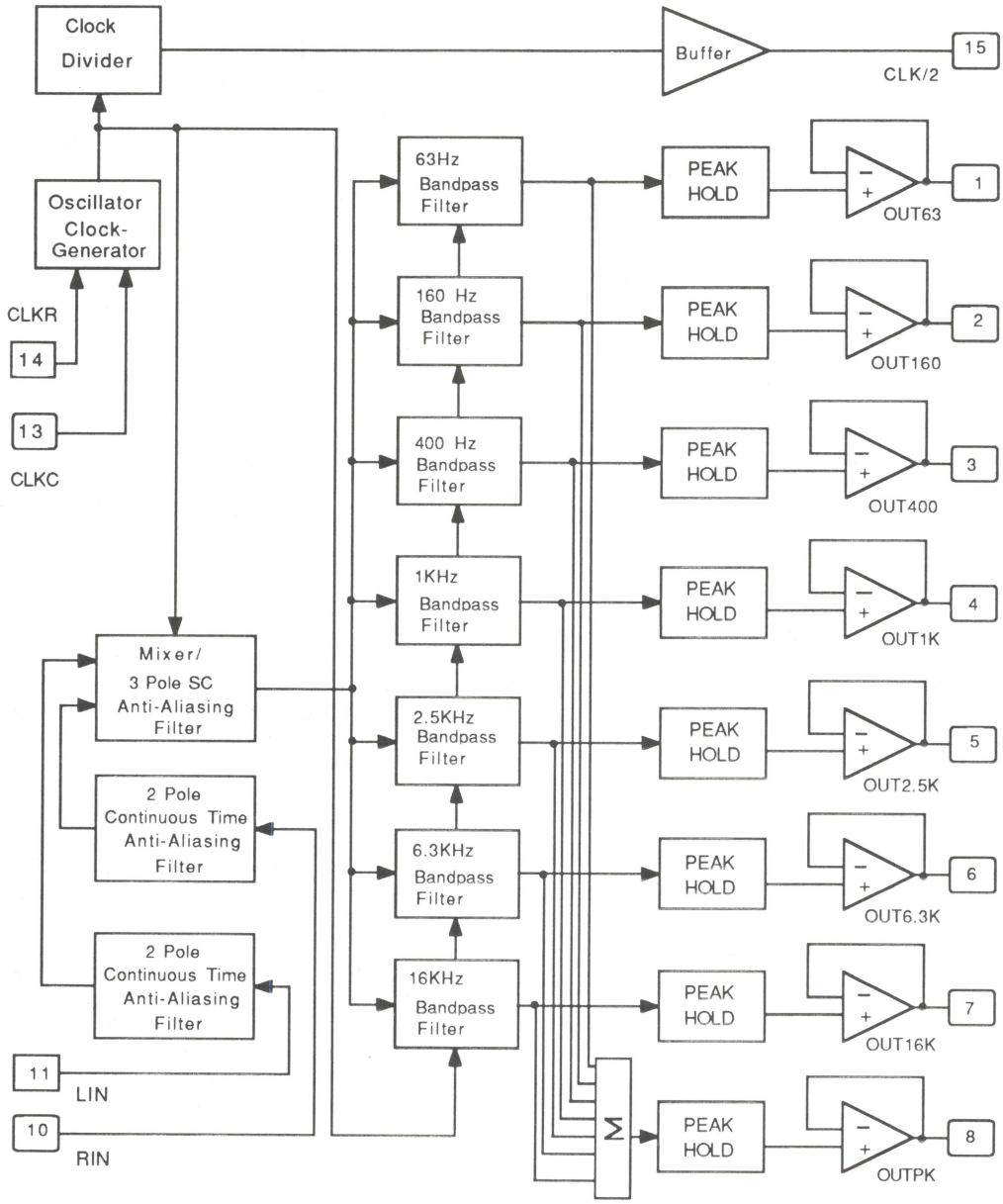


Figure 1. Functional Block Diagram XR-1091
7-Point Graphic Equalizer Display Filter

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +6 VDC, V_{SS} = -6 VDC, T_A = 25°C, S1 open, S2, S3 to ground, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
IDD5	Supply Current		10.0		mA	V_{DD} = 5 VDC, V_{SS} = -5 VDC
IDD6	Supply Current		10.7	18.0	mA	V_{DD} = +6 VDC, V_{SS} = -6 VDC
IIL	Input Leakage	-10		+10	µA	
TCLKRP (R-C)	Clock Freq	385	400	415	KHz	R = 1.46 KΩ, C = 1 nF
TCLK2P (R-C)	Clock/2 Freq	185	200	215	KHz	R_L = 100 KΩ, CL = 100 pF
ECLKR	External Clock Voltage	5			Vpp	$V_{CLK\ IN}$ = ± 2.5 Vpk
ECLK2	Clock/2 External Source	190	200	210	KHz	R_L = 100 KΩ, CL = 100 pF
VOS	Output Offset	0	125	200	mV	S1 to Pins 1 thru 8 sequentially
VOUT6.3KR	6.3 KHz Output, RIN	3.33	3.95	4.7	V	S3 to signal source = 125 mVpk f_{IN}=6.3 KHz, S1 to Pin 6
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 6.3 KHz
VOUT63	63 Hz Output, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 63 Hz, S1 to Pin 1
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 63 Hz
VOUT160	160 Hz Output, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 160 Hz, S1 to Pin 2
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 160 Hz
VOUT400	400 Hz Output, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 400 Hz, S1 to Pin 3
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 400 Hz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
VOUT1K	1 KHz Output, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 1 KHz, S1 to Pin 4
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 1 KHz
VOUT2.5K	2.5 KHz Output, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 2.5 KHz, S1 to Pin 5
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 2.5 KHz
VOUT6.3K	6.3 KHz Output, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 6.3 KHz, S1 to Pin 6
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 6.3 KHz
VOUT16K	16 KHz Output,LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 16 KHz, S1 to Pin 7
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 16 KHz
VOUT PEAK	PEAK OUT, LIN	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk f_{IN} = 1 KHz, S1 to Pin 8
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 1 KHz

Recommended power on sequence: VSS first, followed by VDD. When only 1 channel input is used, then the other input has to be grounded.

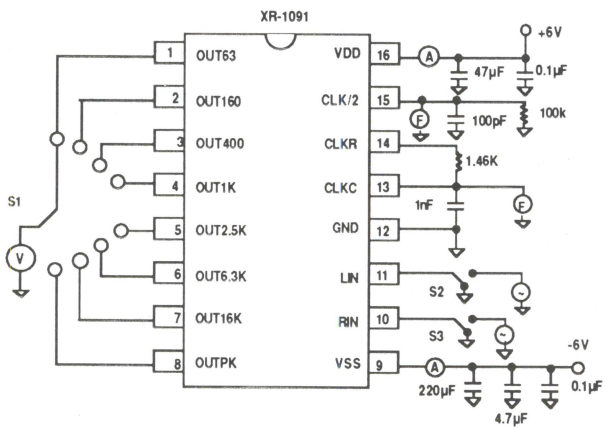


Figure 2. Test Circuit

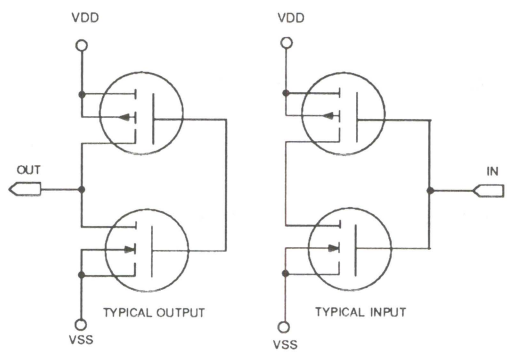


Figure 3. Input / Output Structure

PIN DESCRIPTION

PIN#	SYMBOL	DESCRIPTION
1	OUT63	Peak held output of the 63 Hz filter. This output can drive a 10 KΩ load.
2	OUT160	Peak held output of the 160Hz bandpass filter.
3	OUT400	Peak held output of the 400Hz bandpass filter.
4	OUT1 K	Peak held output of the 1KHz bandpass filter.
5	OUT2.5 K	Peak held output of the 2.5KHz bandpass filter.
6	OUT6.3 K	Peak held output of the 6.3KHz bandpass filter.
7	OUT16 K	Peak held output of the 16KHz bandpass filter.
8	OUT	Peak output of the above also peak held.
9	VSS	Nominally -6 VDC. This should be decoupled with at least a 0.47μF capacitor to ground located as close as possible to this pin.
10	RIN	Right Channel Input. The input impedance of this pin is greater than 1 x 10^{12}Ohms.
11	LIN	Left Channel Input. The input impedance of this pin is greater than 1 x10^{12}Ohms.
12	GND	Ground for both digital and analog.
13	CLKC	Clock Capacitor: The timing capacitor should be tied to this pin to ground.
14	CLKR	Clock resistor: The timing resistor would be tied from this pin to pin 13 CLKC.
15	CLK/2	This output is at 200 KHz in normal operation. the clock swings from VSS to VDD.
16	VDD	Nominally tied to +6 VDC. This pin should be decoupled with a 0.47 μF capacitor to ground located as close as possible to this pin.

To Display IC or Microprocessors
Analog Inputs.

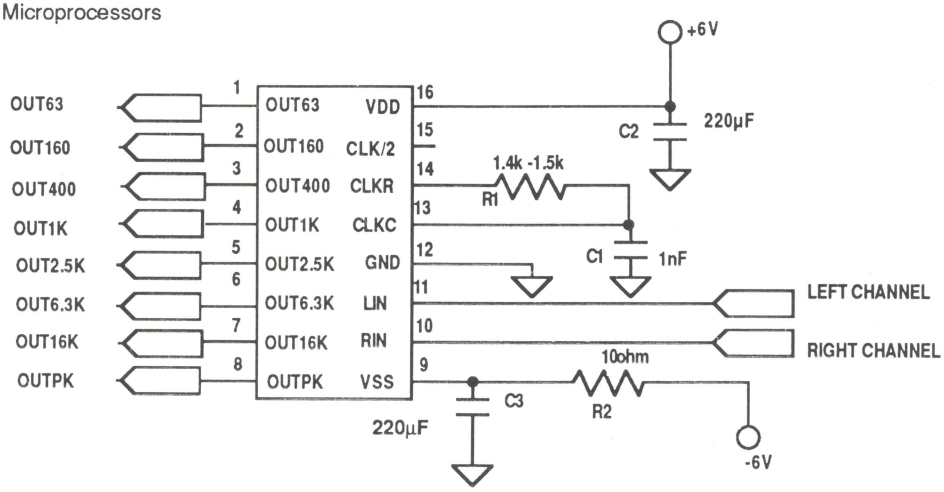


Figure 4. Typical Applications Circuit

12-Channel Graphic Equalizer Filter

GENERAL DESCRIPTION

The XR-1092 is a 12 point switched capacitor bandpass filter with peak hold outputs for use in audio applications. The 12 filters have one octave spacing from 16Hz to 16kHz with the last filter at 20kHz. An additional output has the peak value of the 12 filters. The peak hold outputs have a slow decay time constant (330mS) for use with display circuits. There are 3 auxiliary inputs which, along with the 13 filter outputs, can be multiplexed to one of four chip outputs. An additional output pin can select from any one of the 4 output multiplexers, and thus all 16 signals. There are two inputs, one for the left channel and one for the right. These are used to sum the left and right channels if only one display is desired.

The XR-1092 is fabricated in a low noise 2µm double poly-silicon CMOS process and comes in a 20 pin plastic package. The device may be operated off of either +/- 5V (4V peak output) or +/- 6V (5V peak output) supplies. The chip oscillator operates at 400kHz and requires only an external resistor and capacitor.

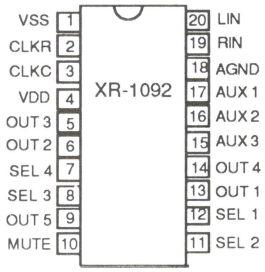
FEATURES

Twelve Filters in one 20 Pin Package
Dual Inputs for Summing Left and Right Channels
On Chip R/C Oscillator
Three Auxiliary Inputs
Output Multiplexor
Mute Mode
Provides 30dB of Gain

APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems
Spectrum Analyzers

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1092CP	20 Pin DIP	-30°C to +75°C

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+/- 7V
Input Current	+/- 10 mA
Storage Temperature	-60°C to +150°C
Power Dissipation (package limitation)	
20 pin plastic package	650mW
derate above 25°C	5.0mW/°C
Maximum Input Voltage	V_{DD} +0.4V
Minimum Input Voltage	V_{SS} -0.4V

SYSTEM DESCRIPTION

The XR-1092 generates its clocks with an internal oscillator and does not require an external clock source, so it can be used in any application where active filters are now being used. The chip has octave spaced filters at 15.625Hz, 31.25Hz, 62.5Hz, 125Hz, 250Hz, 500Hz, 1kHz, 2kHz, 4kHz, 8kHz, 16kHz and 20kHz, the standard octave frequencies in the consumer audio market. The peak detector outputs are referenced to 0V and drive positive to be compatible with a variety of display decoders.

The chip has on board anti-alias filters that provide 30 dB of rejection above 50kHz, preventing most external signals from affecting filter performance. If separate left and right displays are desired, two chips are used and the unused inputs grounded.

PIN DESCRIPTIONS

PIN #	SYMBOL	DESCRIPTION
1	V_{SS}	Negative Supply Voltage
2	CLKR	Clock Resistor from this Pin to CLKC (R_{nom} = 6.97K)
3	CLKC	Clock Capacitor from this Pin to VSS (C_{nom} = 200 pf)
4	V_{DD}	Positive Supply Voltage
5	Out3	Multiplexed output from 4kHz, 8kHz, 16kHz, 20kHz Filters
6	Out2	Multiplexed output from 250Hz, 500Hz, 1kHz, 2kHz Filters
7	Sel4	Mux Select line for Out 5
8	Sel3	Mux select line for Out 5
9	Out5	Multiplexed output Mux for Out1 to Out4
10	Mute	Connects all Outputs to Ground Reference
11	Sel2	Mux select line for Out1 through Out4
12	Sel1	Mux select line for Out1 through Out4
13	Out1	Multiplexed output from 15.625Hz, 31.25Hz, 62.5Hz, 125Hz Filters
14	Out4	Multiplexed output from Peak Sum and Aux Inputs
15	Aux3	Auxiliary Input 3
16	Aux2	Auxiliary Input 2
17	Aux1	Auxiliary Input 1
18	AGND	Analog and digital Ground
19	R_{IN}	Right Channel Input
20	L_{IN}	Left Channel Input

S2	S1	OUT1	OUT2	OUT3	OUT4
0	0	15.625 Hz	250 Hz	4 kHz	Peak Sum
0	1	31.25 Hz	500 Hz	8 kHz	Aux1
1	0	62.5 Hz	1 kHz	16 kHz	Aux2
1	1	125 Hz	2 kHz	20 kHz	Aux3

Table 1. Select 1 and Select 2 Setup Table

S4	S3	OUT 5
0	0	OUT 1
0	1	OUT 2
1	0	OUT 3
1	1	OUT 4

Table 2. Select 3 and Select 4 Setup Table

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5V, V_{SS} = -5V, T_A = 25°C, R = 6.97 kOhms, C = 200 pF

GENERAL CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{DD}	Positive Supply	4.75	5.0	6.0	V	
V_{SS}	Negative Supply	-6.0	-5.0	-4.75	V	
I_{DD}	Positive Current		15	25	mA	V_{SS} = -5V
I_{SS}	Negative Current	-25	-15		mA	V_{DD} = +5V
INPUT CHARACTERISTICS						
I_{IL}	Input Leakage		±10		µA	
Rin	Input Impedance		10		MΩ	
OSCILLATOR CHARACTERISTICS						
F_{CLK}		384	400	416	kHz	
OUTPUT CHARACTERISTICS						
V_{OO}	Output Offset		50	200	mV	Vin = 0V
R_O	Output Impedance		100		Ω	
I_O	Output Current		1		mA	
C_L	Capacitive Load	15	30	50	pF	
T_D	Output Decay Time		330		ms	
FILTER CHARACTERISTICS						
fo	Filter Center Frequency	-5	0	+5	%	Measured at 15.625 Hz, 31.25 Hz, 62.5 Hz, 125 Hz, 250 Hz, 500 Hz, 1 kHz, 2 kHz, 4 kHz, 8 kHz, 16 kHz, 20 kHz
Av	Channel Gain	28.5	30	31.5	dB	Vin = 125 mVpk, Measured at filter center frequency

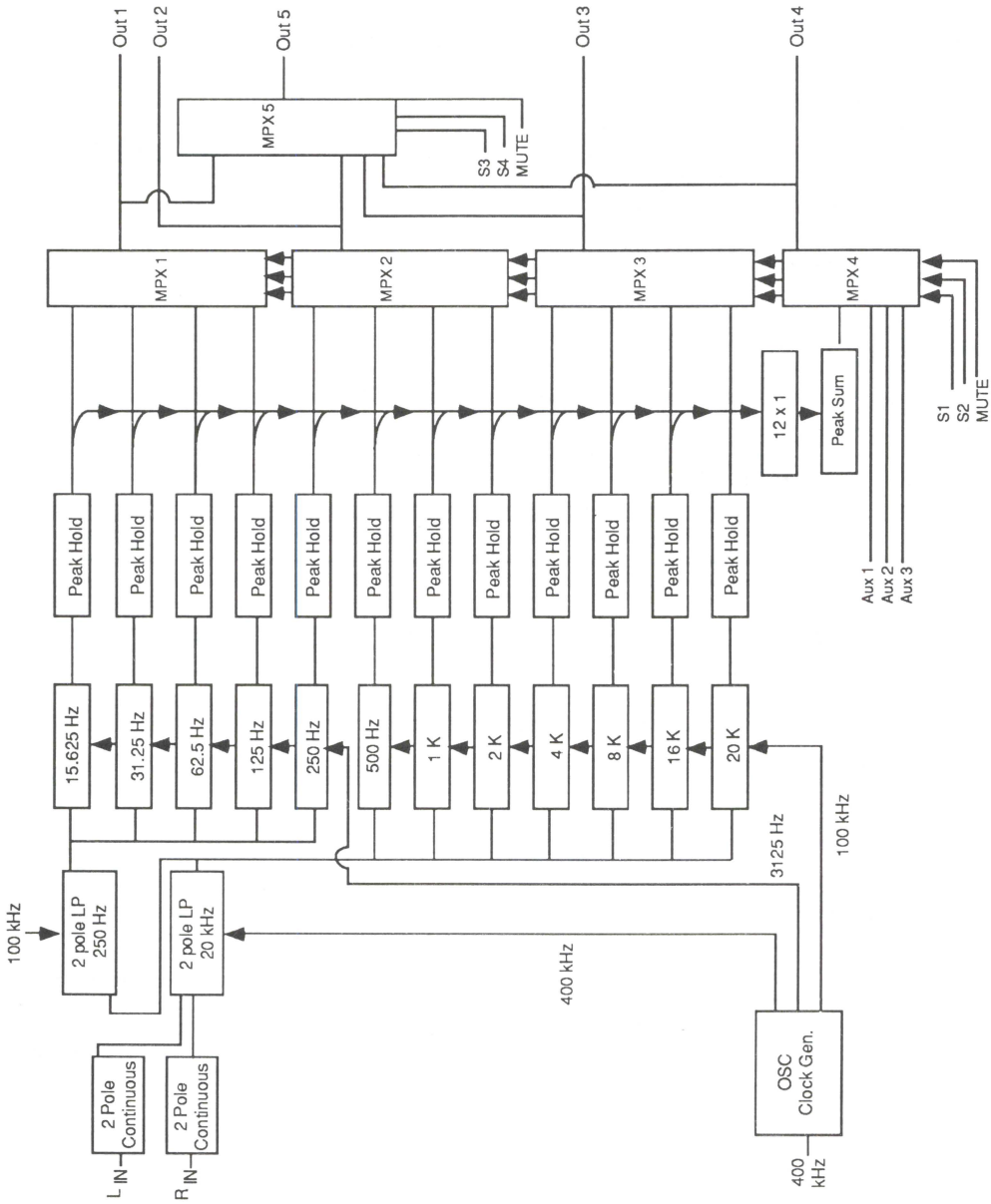


Figure 1. XR-1092 12 - Point Graphic Equalizer Display Filter

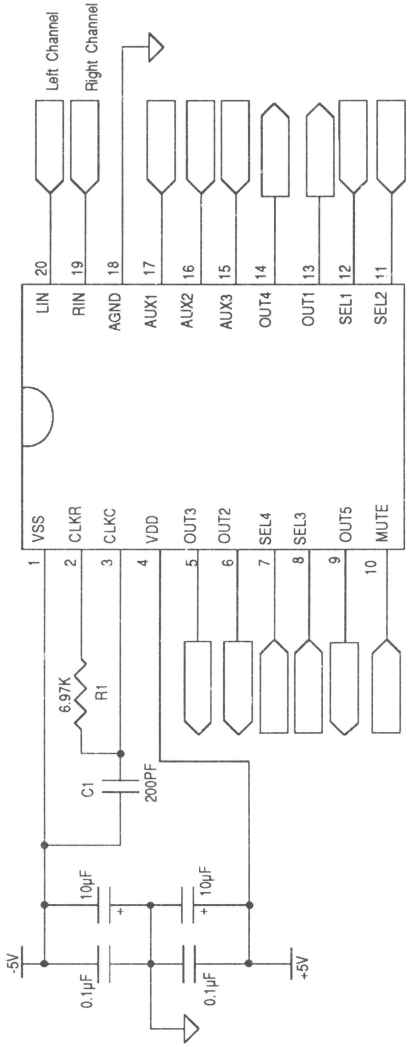


Figure 2. Typical Application Circuit



NOTES



5-Band Graphic Equalizer Filter

GENERAL DESCRIPTION

The XR-1093 is a 5-band switched capacitor bandpass filter with peak hold outputs for use in audio applications. The 5-filters have two octaves spacing from 63Hz to 16kHz. The 16kHz filter is a selectable filter with the option of selecting either 10kHz or 16kHz depending on the user's requirements. Selection of either frequency is done with an external select pin. An additional output has the peak value of the 5-filters. All of the outputs provide a peak hold with slow decay time constant (330 msec) for use with most display circuits.

The XR-1093 is fabricated in a low noise 3 micron double poly-silicon CMOS process and comes in a 14 pin plastic DIP package. The nominal operating voltages are +/- 5Vdc (4V peak output) or +/- 6Vdc (5V peak output). The chip oscillator operates at 400kHz and requires only an external resistor and capacitor. Also provided on chip is a CLK/2 or 200kHz output clock to be used to drive a second XR-1093 device if a 10-point equalizer is desired.

FEATURES

6 Filters in one 14 Pin Package
On Chip R/C Oscillator
Provides 30dB of Gain

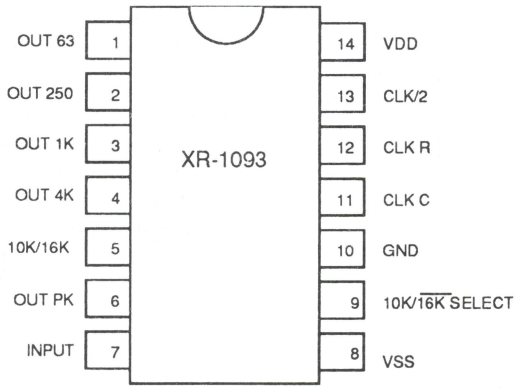
APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems
Spectrum Analyzers

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+/- 7V
Input Current	+/- 10mA
Storage Temperature	-60°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1093CP	14 Pin Plastic DIP	-30°C to 75°C

SYSTEM DESCRIPTION

The XR-1093 generates its clocks with an internal oscillator and does not require an external clock source, so it can be used in any application where active filters are now being used. The chip has two octave spaced filters at 63Hz, 250Hz, 1kHz, 4kHz and 16kHz, the standard octave frequencies in the consumer audio market. The 16kHz filter can be switched to provide a 10kHz filter via an external select pin. The peak detector outputs are referenced to 0V and drive positive to be compatible with a variety of display decoders.

The chip has on board anti-alias filters that provide 30dB of rejection above 50kHz, preventing most external signals from affecting filter performance.

PIN DESCRIPTION

PIN #	SYMBOL	DESCRIPTION
1	OUT 63	Peakhold output of the 63Hz filter
2	OUT 250	Peakhold output of the 250Hz filter
3	OUT 1K	Peakhold output of the 1kHz filter
4	OUT 4K	Peakhold output of the 4kHz filter
5	10K/16K	Peakhold output of the 10kHz/16kHz filter
6	OUT PK	Peak output of the above. This output is also peakhold.
7	INPUT	Device Input
8	VSS	Negative Supply Voltage
9	10K/16K SELECT	10kHz/16kHz filter select input. Logic "O" (low) on this pin will select the 16kHz and logic "1" (high) will select the 10kHz filter
10	GND	Ground
11	CLK C	Clock capacitor from this pin to GND (Cnom = 1nf)
12	CLK R	Clock resistor from this pin to CLK C (Rnom = 1.46kOhm)
13	CLK/2	This output is at 200kHz in normal operation. This buffered output pin can be used to drive a second device if a 10-point equalizer is needed.
14	VDD	Positive Supply Voltage

ELECTRICAL CHARACTERISTICS

Test Conditions: VDD = 5V, VSS = -5V, TA = 25°C, R =1.46kOhm, C = 1nF

GENERAL CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{DD}	Positive Supply	4.75	5.0	6	V	
V_{SS}	Negative Supply	-6.0	-5.0	-4.75	V	
I_{DD}	Positive Current		8	12	mA	
I_{SS}	Negative Current		-8	-12	mA	
OSCILLATOR CHARACTERISTICS						
f_{VCO}		375	400	425	kHz	R =1.46kOhm C = 1nF
OUTPUT CHARACTERISTICS						
V_{OS}	Output Offset		150	200	mV	Vin = 0V
R_O	Output Impedance		100		Ω	
C_L	Capacitive Load		30		pF	
T_D	Output Decay Time		330		mS	
FILTER CHARACTERISTICS						
fo	Filter Center Frequency	-5	0	+5	%	Measured at 63Hz, 250Hz, 1kHz, 4kHz, 10/16kHz
AV	Channel Gain	28.5	30	31.5	dB	Vin = 125mVpk

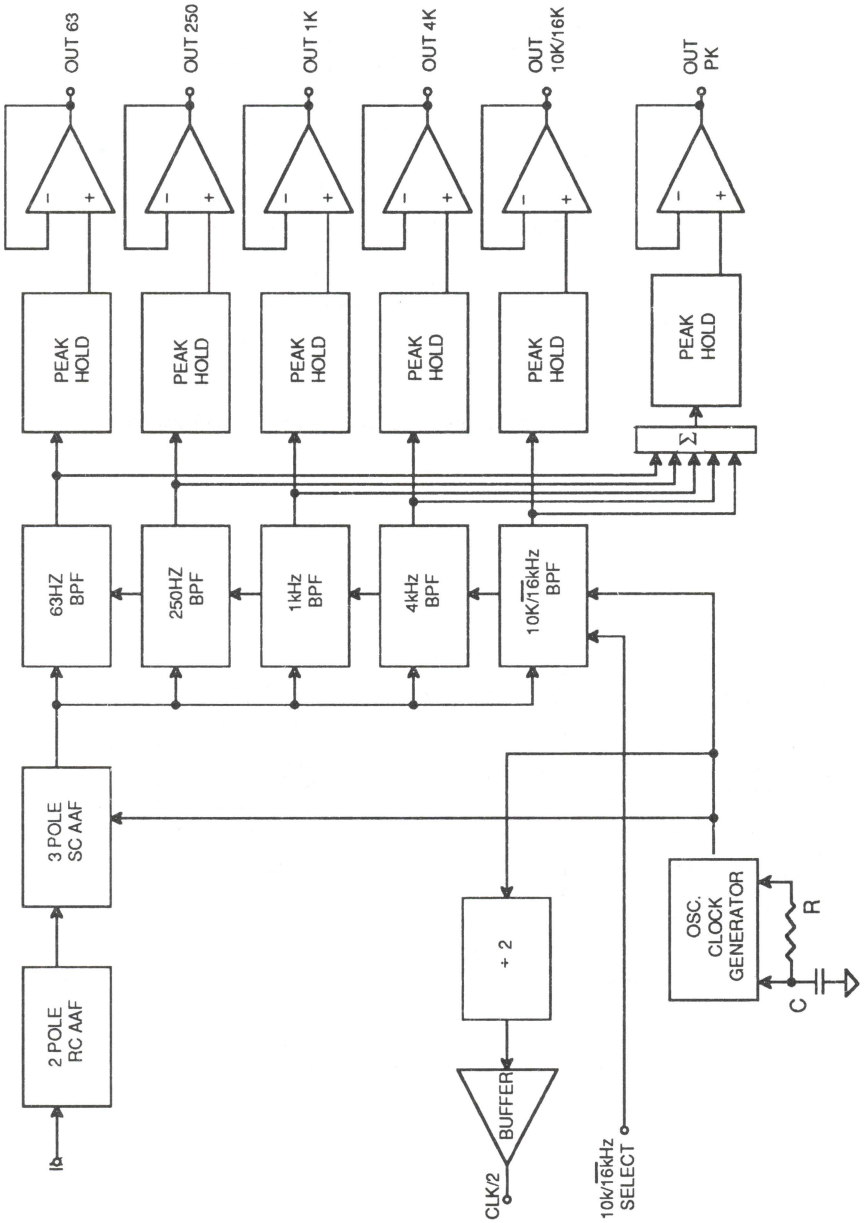


Figure 1. 5-Band Graphic Equalizer Display Filter

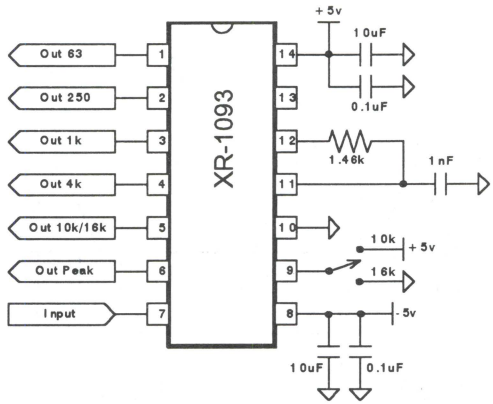


Figure 2. Typical 5-Band Application Schematic

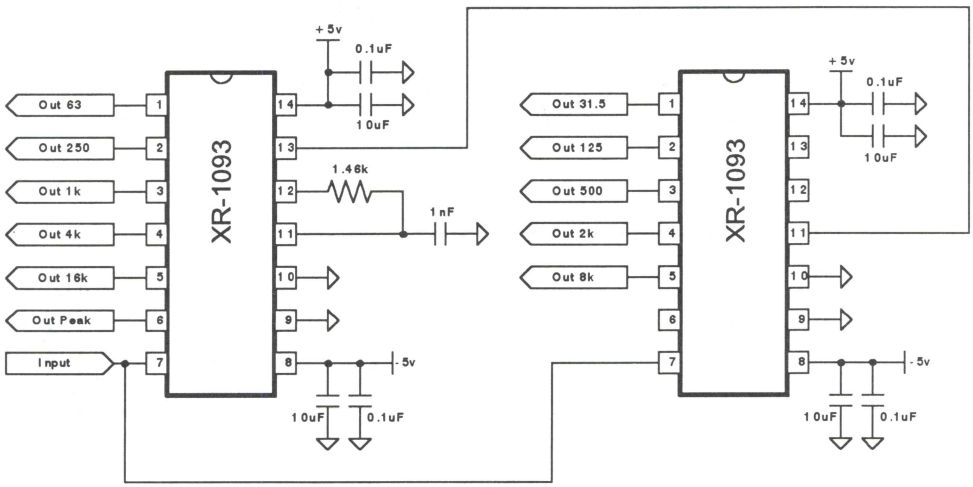


Figure 3. Typical 10-Band Application Schematic

Advanced Information

Five Band Graphic Equalizer Filter and Display Driver

GENERAL INFORMATION

The XR-1094 is a single chip graphic equalizer and display driver containing switched-capacitor band-pass filters, filter multiplexer, data latches and high voltage vacuum fluorescent display driver. The five band-pass filters have two octave spacing from 63Hz up to 16kHz. The high filter can be selected for either 10kHz or 16kHz center frequency. They are followed by five peak detectors, a filter multiplexer, and high voltage driver. A digital peak detector is provided for he maximum signal level (total output) in the band-pass filter frequency range. An on-chip power on reset circuit blanks the display outputs for one second after power up to eliminate power up noise on the display.

The output multiplexer is designed to interface with most vacuum florescent display drivers. The display can have up to 13 levels and 5 frequency bands, as well as peak sum. The high voltage P-channel drive transistors can drive up to 45 volts.

The XR-1094 is fabricated in a 3um double polysilicon CMOS process, resulting in accurate filters, tight gain tolerances and low noise. The nominal operating voltage is +/-5VDC. The chip includes a self contained RC oscillator with a nominal frequency of 400kHz. Only an external resistor and capacitor are needed.

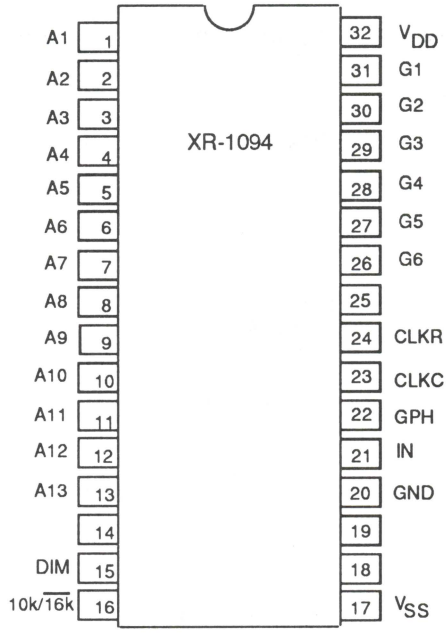
FEATURES

Single Chip Equalizer and Display Driver
Accurate Switched-Capacitor Filters
30dB of Gain
Peak Hold Display Drive
Simple Resistor and Capacitor Oscillator
DIM Control for Display Brightness
Low Noise, Low Power CMOS
Selectable 10kHz/16kHz Filter

APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems
Spectrum Analyzers

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1094 CP	32 Pin Plastic SDIP	-30°C to 75°C

ABSOLUTE MAXIMUM RATINGS

V_{DD}	7VDC
V_{SS}	-7VDC
VDS of High Voltage P-Channel Driving Transistors Relative to V_{DD}	- 45 V
Power Dissipations (package limitation)	
32 Pin Plastic Package	1W
Derate above 25°C	9 mW/°C
Storage Temperature	-60 to +150°C

5

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VDD	+Supply	4.5	5.0	6.0	VDC	
VSS	-Supply	-4.5	-5.0	-6.0	VDC	
IDD	Supply current		10		mA	VDD=5; VSS=-5
Iil	Input leakage	-2		2	µA	Digital Inputs Analog Inputs
Ioff	Output off leakage A & G Outputs			10	µA	Vin=0V; VD=-38V
Vih	Digital input high voltage threshold		1.6	2.4	VDC	
Vil	Digital input low voltage threshold	0.8	1.6		VDC	
Fclk	Clock frequency accuracy	375	400	425	kHz	
f_o	Filter Center Frequency	-7	0	7	%	
VOUTG	All G outputs	-1.0	2.5	5	V	VDD=5V IGL=14mA
VOUTA	All A outputs	2.5	3.75	5	V	VDD=5V IAL=2.5mA
T_D	Output Decay Time		330		ms	
t_d	Duty cycle		1/11.4 1/39.5			Dim = 0 Dim = V+
GPH	Display peak hold time		0.5		S	R=100KΩ, C=1µf

ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
A1(Note1)	-12dB	7.5	8.4	9.5	mvpk	
A2	-10dB	9.5	11	12	mvpk	
A3	-8dB	12	13	15	mvpk	
A4	-6dB	15	17	19	mvpk	
A5	-4dB	19	21	24	mvpk	
A6	-2dB	24	26.7	29	mvpk	
A7	-0dB	29	34	38	mvpk	
A8	+2dB	38	42	47.5	mvpk	
A9	+4dB	47.5	53	59.8	mvpk	
A10	+6dB	59.8	67	75.3	mvpk	
A11	+8dB	75.3	84	95	mvpk	
A12	+10dB	95	106	119	mvpk	
A13	+12dB	119	134	150	mvpk	

Note 1: Amplified levels are relative to VSS at -5 volts nominal. Levels will vary linearly with voltage on VSS.

PIN DESCRIPTION

PIN#	SYMBOL	DESCRIPTION
1-13	**A1-A13**	Display levels 1-13, indicating signal strength on G1-G6
26-31	**G6-G1**	Time allocation for display function G1 63Hz G2 250Hz G3 1kHz G4 4kHz G5 10kHz/16kHz G6 Total Output
15	**DIM**	DIM Display: This pin, when high, reduces the brightness of the display by adjusting the on-time of the segments
16	**10k/$\overline{16k}$**	10kHz/$\overline{16kHz}$ filter select input. Logic "0" (low) will select the 16kHz filter and logic "1" (high) will select the 10kHz filter
17	**VSS**	Minus supply, nominally -5VDC
20	**GND**	Analog input reference
21	**IN**	Audio input
22	**GPH**	Filter amplitude display duration control resistor and a timing capacitor from this pin to VSS will control the duration of peak hold for all six outputs
23	**CLKC**	Oscillator timing capacitor between this pin and VSS
24	**CLKR**	Oscillator timing resistor between this pin and CLKC pin
32	**VDD**	Plus supply, nominally 5VDC

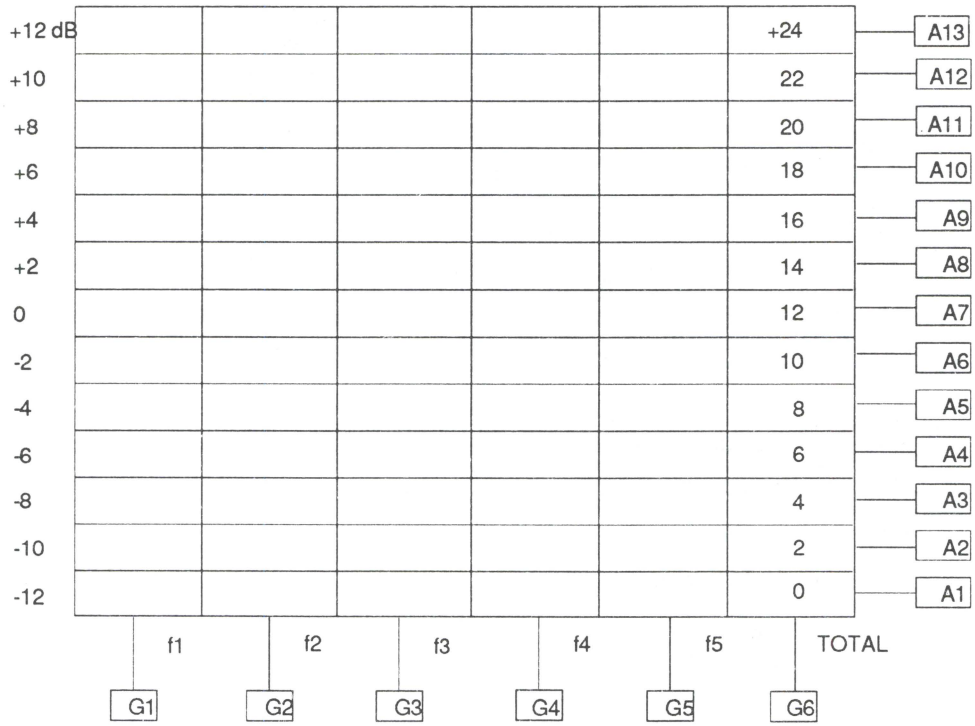


Figure 1. Typical Display

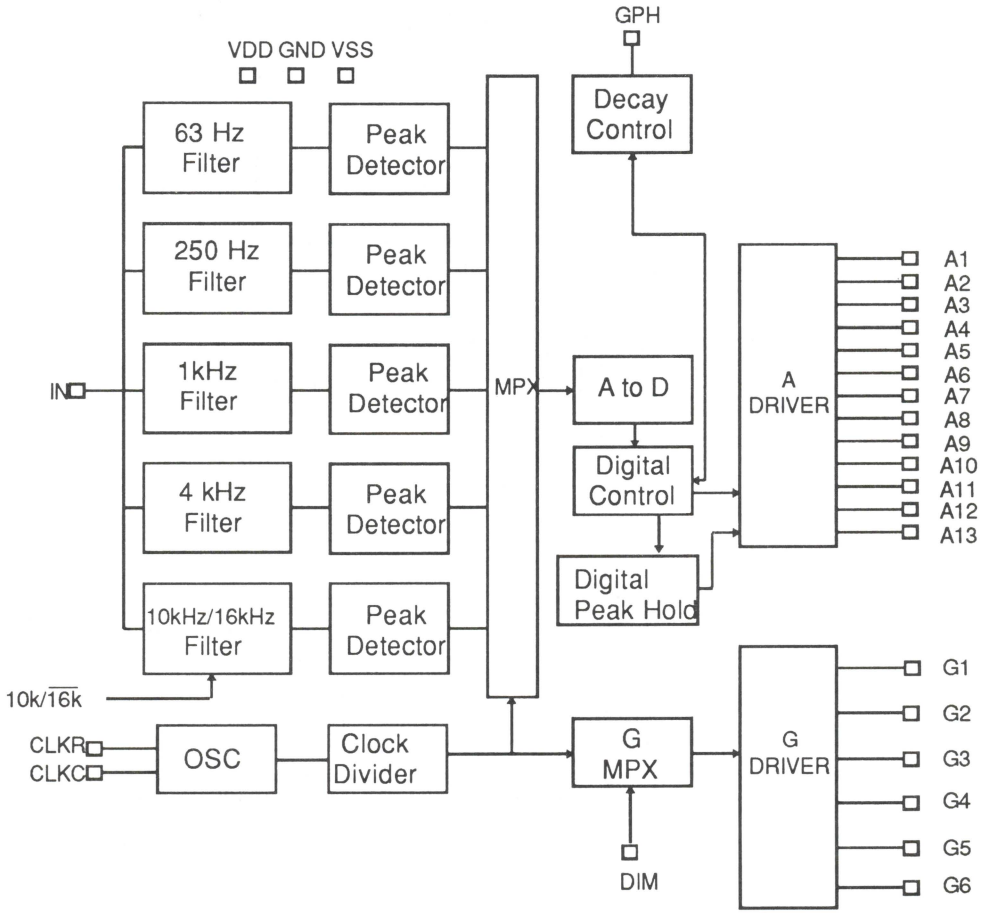


Figure 2. Block Diagram

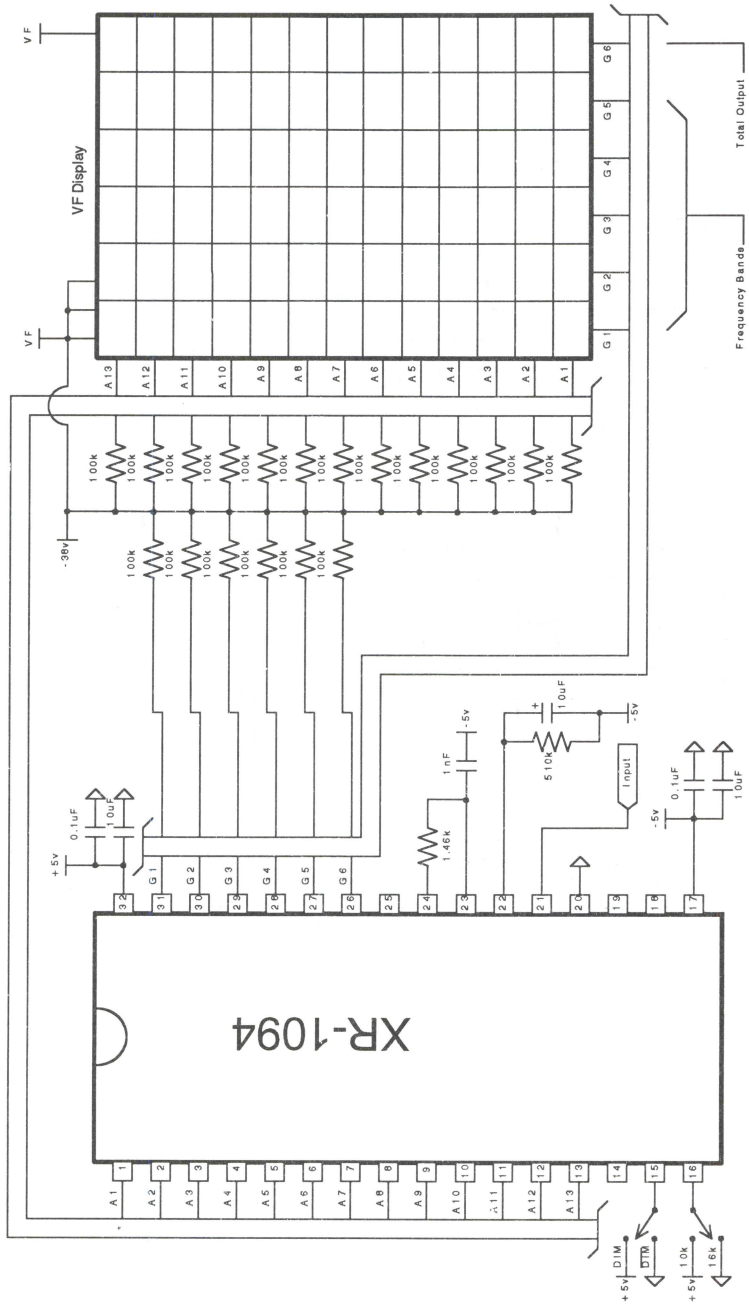


Figure 3. Typical Application Schematic

Advanced Information

Seven Band Graphic Equalizer Filter and Display Driver with Micro-Controller Interface

GENERAL DESCRIPTION

The XR-1095 is a single chip graphic equalizer and display driver containing switched-capacitor band-pass filters, filter multiplexer, micro-controller interface, data latches and high voltage vacuum fluorescent display driver. The seven band-pass filters have 1.32 octave spacing from 63Hz up to 16kHz. They are followed by seven peak detectors, a filter multiplexer, and high voltage driver. A digital peak detector is provided for the maximum signal level (Total Output) in the band-pass filter frequency range. The chip also contains an accessory display driver. An internal micro-controller serial interface port facilitates the loading of control data for the display, accessory display data, and filter display data when the device is in set data mode.

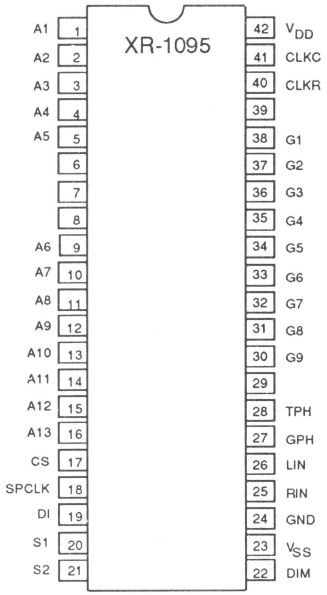
Two separate inputs are included for summing the left and right channel inputs. If a separate display is desired for each channel, the unused input should be grounded and a separate device used for each input. The output multiplexer is designed to interface with most vacuum florescent display drivers. The display can have up to 13 levels and 7 frequency bands, as well as peak sum and accessory display. The high voltage P-channel drive transistors can drive up to 45 volts. An on-chip power on reset circuit blanks the display outputs for 1/2 second after power up to eliminate power up noise on the display.

The XR-1095 is fabricated in a 3 micron double polysilicon CMOS process, resulting in accurate filters, tight gain tolerances and low noise. The nominal operating voltage is +/-5VDC. The chip includes a self contained RC oscillator with a nominal frequency of 400kHz. Only an external resistor and capacitor are needed.

FEATURES

Single Chip Equalizer and Display Driver
Accurate Switched-Capacitor Filters
30dB of Gain
Peak Hold Display Driver
Accessory Display Driver
Micro-Controller Interface
Simple Resistor and Capacitor Oscillator
DIM Control for Display Brightness
Inputs to Sum Left and Right Channels
Low Noise, Low Power CMOS
Set Data Mode with Flash Option

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1095CP	42 Pin Plastic SDIP	-30°C to 75°C

APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems
Spectrum Analyzers

ABSOLUTE MAXIMUM RATINGS

V_{DD}	7VDC
V_{SS}	-7VDC
VDS of High Voltage P-Channel Driving Transistors: Relative to V_{DD}	- 45 V
Power Dissipations (package limitation)	
42 Pin Plastic Package	1W
Derate above 25°C	9 mW/°C
Storage Temperature	-60°C to +150°C

5

ELECTRICAL CHARACTERISTCS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VDD	+Supply	4.5	5.0	6.0	VDC	
VSS	-Supply	-4.5	-5.0	-6.0	VDC	
IDD	Supply current		10		mA	VDD=5; VSS=-5
Iil	Input leakage	-2		2	µA	Digital Inputs Analog Inputs
Ioff	Output off leakage A & G Outputs			10	µA	Vin=0V; VD=-38V
Vih	Digital input high voltage threshold		1.6	2.4	VDC	
Vil	Digital input low voltage threshold	.8	1.6		VDC	
Fclk	Clock frequency accuracy	375	400	425	kHz	
f_o	Filter center frequency accuracy	-7		+7	%	
Fspc	Maximum serial port clock frequency	1.0			MHz	
tstrp	Data valid before Serial Port clock	100			nS	
thold	Data valid after Serial Port clock	0			nS	
tspc	Serial Port Clock pulse width	200			nS	
VOUTG	All G outputs	-1.0	2.5	5	V	VDD=5V IGL=14mA
VOUTA	All A outputs	2.5	3.75	5	V	VDD=5V IAL=2.5mA
FSS	Flash frequency		2		Hz	
t_f	Duty Factor		833 240		us us	Dim = 0 Dim = V+

ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_d	Duty cycle		1/11.4 1/39.5			Dim = 0 Dim = V+
TPH	Total hold time		0.5		S	R=100KΩ, C=1μf
GPH	Individual fc hold time		0.5		S	R=100KΩ, C=1μf
A1(Note1)	-12dB	7.5	8.4	9.5	mvpk	
A2	-10dB	9.5	11	12	mvpk	
A3	-8dB	12	13	15	mvpk	
A4	-6dB	15	17	19	mvpk	
A5	-4dB	19	21	24	mvpk	
A6	-2dB	24	26.7	29	mvpk	
A7	-0dB	29	34	38	mvpk	
A8	+2dB	38	42	47.5	mvpk	
A9	+4dB	47.5	53	59.8	mvpk	
A10	+6dB	59.8	67	75.3	mvpk	
A11	+8dB	75.3	84	95	mvpk	
A12	+10dB	95	106	119	mvpk	
A13	+12dB	119	134	150	mvpk	

Note 1: Amplified levels are relative to VSS at -5 volts nominal. Levels will vary linearly with voltage on VSS.

PIN DESCRIPTION

PIN#	SYMBOL	DESCRIPTION
1-5, 9-16	A1-A5 A6-A13	Display levels 1-13, indicating signal strength on G1-G8 and accessory display on G9.
		Time allocation for display function
38	G1	63Hz
37	G2	160Hz
36	G3	400Hz
35	G4	1kHz
34	G5	2.5kHz
33	G6	6.3 kHz
32	G7	16kHz
31	G8	Total Output
30	G9	Accessory Display
25	RIN	Right channel input
26	LIN	Left channel input
22	DIM	Brightness control varies width of G outputs. Also accessible via microcontroller interface
27	GPH	Filter amplitude display duration control. A resistor and timing capacitor from this pin to VSS adjust Peak Hold Decay Time.
28	TPH	Filter amplitude display duration control. A resistor and timing capacitor from this pin to VSS adjust Peak Hold Decay Time.
40	CLKR	Oscillator timing resistor between this pin and CLKC pin
41	CLKC	Oscillator timing capacitor between this pin and VSS
20	S1	Chip select 1 pin
21	S2	Chip select 2 pin
19	DI	Serial port data
18	SPCLK	Serial port clock
17	CS	Chip Select
42	V_{DD}	Plus supply, nominally 5VDC
23	V_{SS}	Minus supply, nominally -5VDC
24	GND	Analog input reference

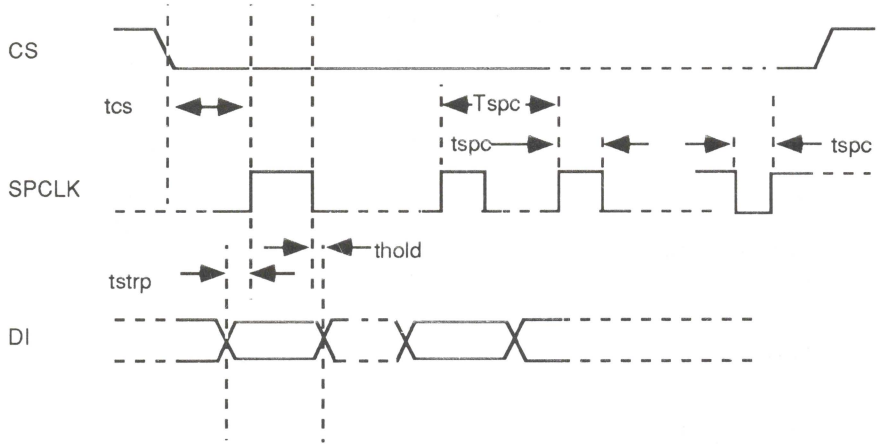


Figure 1. Timing Chart Serial Interface Port

tcs: Chip Select valid before Serial Port Clock (200 ns min)

tstrp: Data valid before Serial Port Clock (100 ns min)

thold: Data valid after Serial Port Clock (0 ns min)

tspc: Serial Port Clock Pulse Width (200 ns min high or low)

Fspc: Serial Port Clock Frequency (1 MHz max)

Tspc: Serial Port Clock Period (1 us min)

Note: tspc-high or tspc-low can be 200 ns min, but not both. Tspc must be 1 us min.

SERIAL PORT BIT MAP

b0	not used *

b4	b5	Accessory memo
0	0	off
1	0	on

*b9	Total peak hold
0	off
1	on

b10	Peak hold
0	off
1	on

b11	Accessory A1 control
0	on
1	off

b12	Set data/level display
0	Set data display GEQ
1	Set level display SPEANA

b13	Dimmer on/off
0	off
1	on

b1	b2	b3	Flash command data
0	0	0	No flash
1	0	0	f1 flash
0	1	0	f2 flash
1	1	0	f3 flash
0	0	1	f4 flash
1	0	1	f5 flash
0	1	1	f6 flash
1	1	1	f7 flash

b6	b7	b8	Accessory Mn control
0	0	0	off
1	0	0	M1
0	1	0	M2
1	1	0	M3
0	0	1	M4
1	0	1	M5
0	1	1	M6

b14	b15	Accessory display
0	0	off
1	0	Right
0	1	Left
1	1	MIX

b16 to b50 are set data for each filter

LSB		MSB	Filter
b16	-	b20	f1
b21	-	b25	f2
b26	-	b30	f3
b31	-	b35	f4
b36	-	b40	f5
b41	-	b45	f6
b46	-	b50	f7

**b9 low turns the Total peak hold display off*

LSB				MSB	Display
0	0	1	1	1	+12dB
0	1	0	1	1	+10dB
0	0	0	1	1	+8db
0	1	1	0	1	+6dB
0	0	1	0	1	+4dB
0	1	0	0	1	+2dB
0	0	0	0	1	+0dB
0	1	1	1	0	-2dB
0	0	1	1	0	-4dB
0	1	0	1	0	-6dB
0	0	0	1	0	-8dB
0	1	1	0	0	-10dB
0	0	1	0	0	-12dB

SERIAL PORT BIT MAP (cont.)

b51 - b61 Key code (S1/S2 select)

S1	S2	b51	b52	b53	b54	b55	b56	b57	b58	b59	b60	b61	
0	0	0	0	0	1	0	0	1	1	1	1	1	Chip select 0
1	0	1	0	0	1	0	0	1	1	1	1	1	Chip select 1
0	1	0	1	0	1	0	0	1	1	1	1	1	Chip select 2
1	1	1	1	0	1	0	0	1	1	1	1	1	Chip select 3

** First bit loaded into the Serial port is bit b61, last bit loaded in is bit bø*

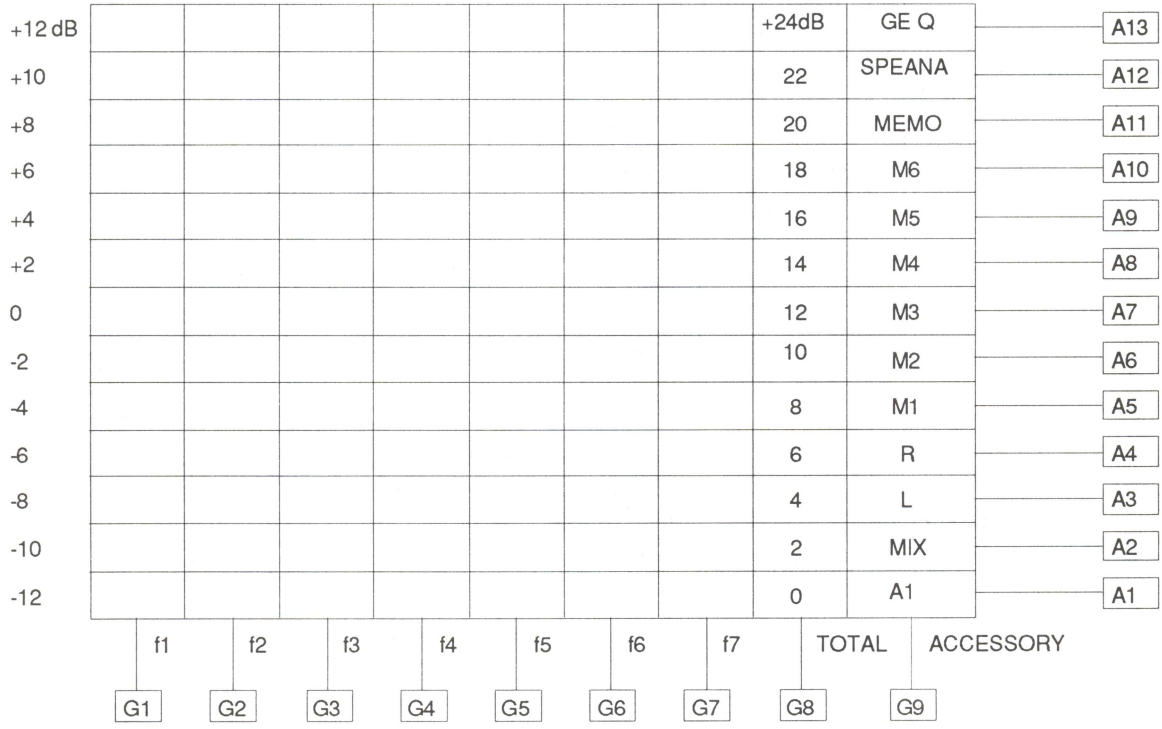


Figure 2. Typical Display

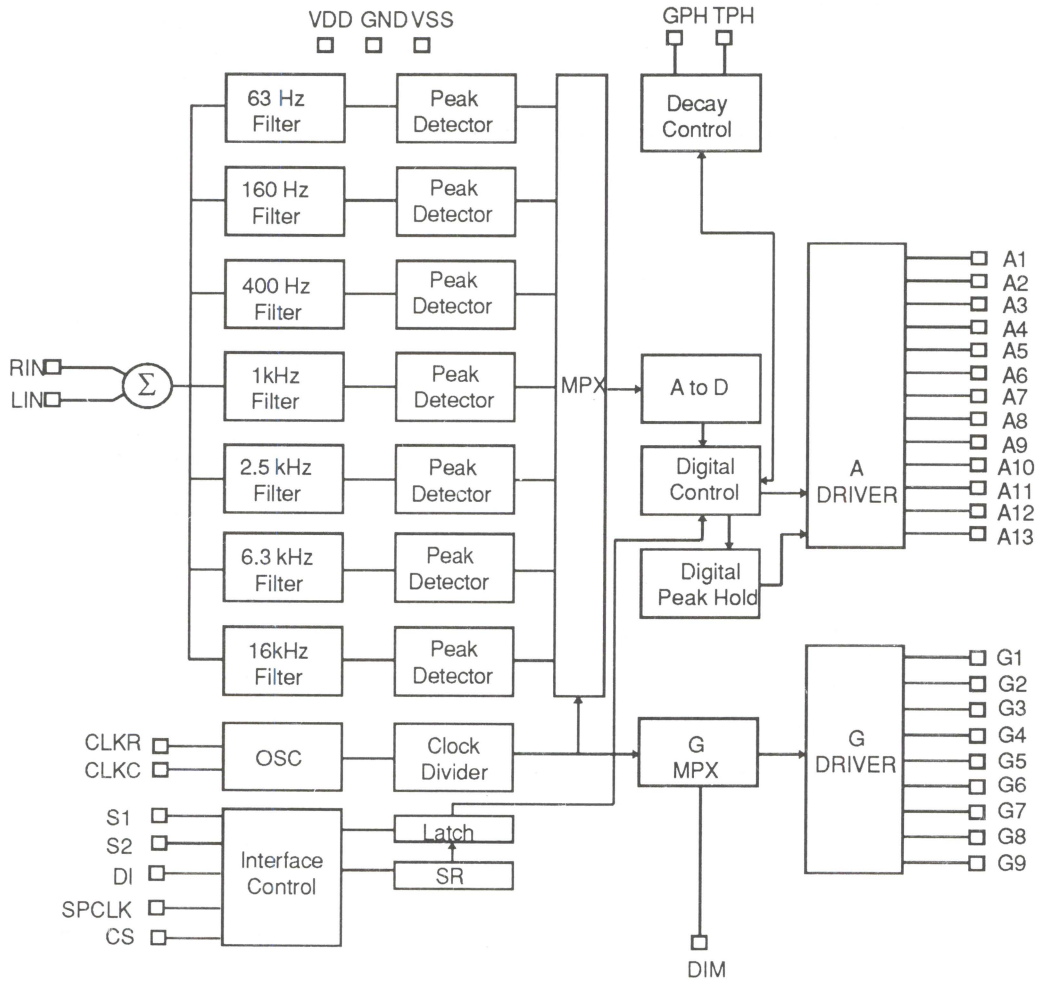


Figure 3. Block Diagram

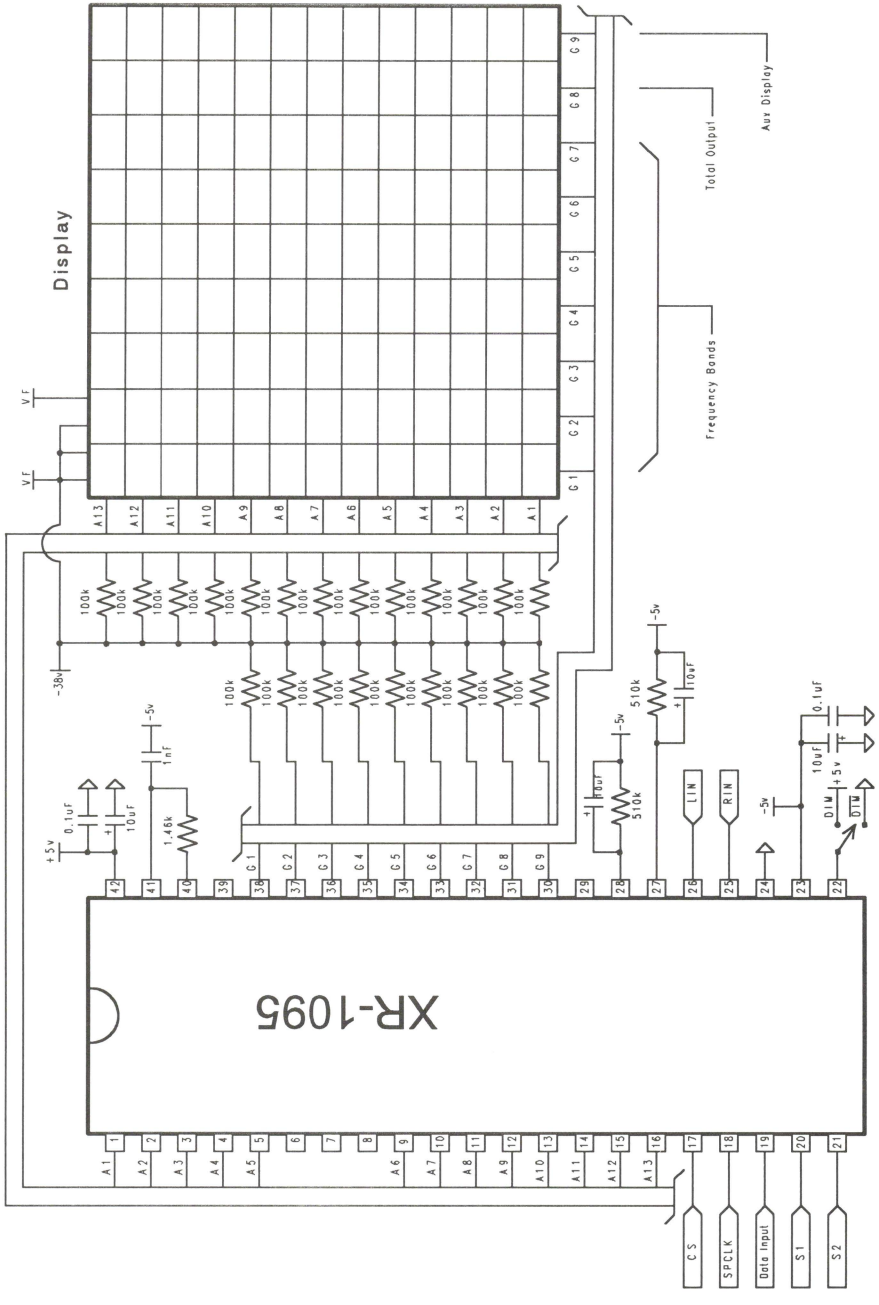


Figure 4. Typical Application Schematic



NOTES



Graphic Equalizer Filter and Display Driver

GENERAL DESCRIPTION

The XR-1096 is a switched-capacitor filter, multiplexer and high voltage driver dedicated for use in audio applications to perform the band splitting function and Vacuum Florescent display driver. The XR-1096 contains seven band-pass filters spaced 1.32 octaves apart from 63 Hz to 16kHz followed by seven analog peak detectors. A digital peak detect is also provided for the total output which is an indication of the maximum signal level within the range of the band-pass filters. Two separate inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant information in the audio from being displayed.

The internal band-pass filters and peak detect circuits of the XR-1096 have low output offset voltage to prevent false displays from occurring during the playback of low volume music or music with wide dynamic range. The nominal operating voltages are ±5VDC. The self contained oscillator is designed to operate at 400 kHz with an external resistor and capacitor.

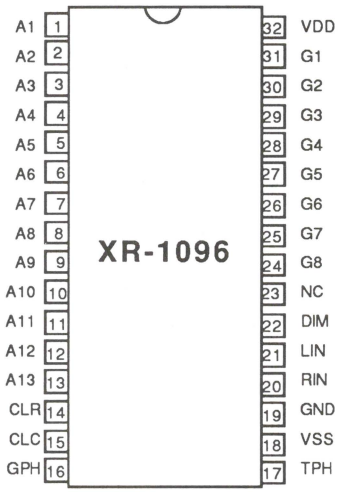
The output multiplexer is designed to interface with most vacuum florescent display drivers having up to 13 steps for level and seven frequency bands. The total output is also provided for displays with this band as well. The high voltage P-channel driving transistors in the XR-1096 have a maximum drain to source voltage of -40V.

The XR-1096 is fabricated in 3 μm double polysilicon CMOS for lower noise and less clock feedthrough in the internal stages and is available in a 32 pin shrink DIP plastic package.

FEATURES

Simple Resistor and Capacitor oscillator
Provides seven filters and display Multiplexer in one
DIM pin for controlling display brightness
Peak Holding delay Control with a resistor and a capacitor
Dual Inputs for summing Left and Right Channels
Provides 30 dB of Gain
Low Noise CMOS

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1096CP	32 Pin Plastic SDIP	-30°C to 75°C

APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems
Spectrum Analysis

ABSOLUTE MAXIMUM RATINGS

VDD	7VDC
VSS	-7VDC
VDS of High Voltage P-Channel Driving Transistors:	
Relative to VDD	- 45 V
Power Dissipations (package limitation)	
32 Pin Plastic Package	1 W
Derate above 25°C	9 mW/°C
Storage Temperature	-60°C to +150°C

5

ELECTRICAL CHARACTERISTICS: Preliminary

Test Conditions: VDD = +5V, VSS = -5V, VD = -33 V TA = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
IDD5	Supply Current		15	20	mA	V_{DD} = 5VDC, V_{SS} = 5VDC
IIL	Input Leakage	-2		2	µA	LIN, RIN, DIM, CLC
TCLKRP (R-C)	Clock Freq Accuracy	375	400	425	kHz	R = 1.46kΩ, C = 1n
f_o	Filter Freq Accuracy	-7	0	7	%	
I OFF	All A outputs off			10	µA	V_{IN} = 0V, V_D = -35 V
VOUT G	All G outputs	-1.0	2.5	5	V	V_{DD} = 5V I_{GL} = 14mA
VOUT A	All A outputs	2.5	3.75	5	V	V_{DD} = 5V I_{AL} = 2.5mA
T_D	Output Decay Time		330		ms	
t_d	Duty Cycle		1/11.4			
t_f	Duty Factor		833 240		µs µs	With DIM at V_{SS} With DIM at V_{DD}
TPH	Total Hold Time		0.5		s	R = 100KΩ, C = 1µf
GPH	Individual f_c hold time		0.5		s	R = 100KΩ, C = 1µf
A1 (Note 1)	Amplitude Test Limit-30dB	5.8	7.7	8.5	mVpk	
A2	-28dB	8.5	9.5	10.7	mVpk	
A3	-26dB	10.7	12.0	13.5	mVpk	
A4	-24dB	13.5	16.0	18.0	mVpk	
A5	-22dB	18.0	20.0	22.5	mVpk	
A6	-20dB	22.5	25.5	28.5	mVpk	
A7	-18dB	28.5	32.5	35.5	mVpk	
A8	-16dB	35.5	41.0	45.5	mVpk	
A9	-14dB	45.5	50.5	57.0	mVpk	
A10	-12dB	57.0	64.0	70.0	mVpk	
A11	-10dB	70.0	77.0	89.0	mVpk	
A12	-8dB	89.0	102.0	116	mVpk	
A13	-4dB	116	127	150	mVpk	

Note 1: Amplified levels are relative to V_{DD} at 5 volts nominal. Levels will vary linearly with voltage on V_{DD}.

SYSTEM DESCRIPTION

The XR-1096, unlike most switched-capacitor filters, does not require an external clock source in order to provide the sampling clock. This frees the designer to place the XR-1096 in any application where an active filter design was in place. The XR-1096 provides filters at 63 Hz, 160 Hz, 400 Hz, 1kHz, 2.5 kHz, 6.3 kHz, and 16 kHz. These frequencies are relative standards in the consumer audio market. The display decoder is designed for use with vacuum florescent displays and provides the control expected in such a multiplexer. These include dimming of the display's brightness and delay for peak hold of all 8 bands (7 frequency bands and 1 total output).

The XR-1096 contains a continuous-time anti-aliasing filter. This prevents out of band signals from affecting the filters performance. If two separate displays are desired, then two XR-1096 could be used, and the unused input should be grounded.

PIN DESCRIPTION

Pin #	Symbol	Description
1-13	A1-A13	Amplitude levels 1-13: This indicates the signal strength.
14	CLKR	Clock resistor: The timing resistor would be tied from this pin to pin 15, CLKC.
15	CLKC	Clock Capacitor: The timing capacitor should be tied from this pin to V_{SS}.
16	GPH	A resistor and a timing capacitor from this pin to V_{SS} will control the duration the display bands are peak held.
17	TPH	A resistor and a timing capacitor from this pin to V_{SS} will control the duration the total output is peak held.
18	VSS	Nominally -5VDC.
19	GND	Ground: Should be tied to a low impedance ground line.
20	RIN	Right Channel Input
21	LIN	Left Channel Input
22	DIM	Dim Display: This pin, when high, reduces the brightness of the display by adjusting the on time of the segments.
23	NC	No internal connection.
24-31	G8-G1	Time allocation for different frequency bands. See table below: G1 63 Hz G2 160 Hz G3 400 Hz G4 1 k Hz G5 2.5 kHz G6 6.3 kHz G7 16 kHz G8 Total Output e.g. when G1 is high (VDD),data at A1-A13 is for 63Hz signals.
32	VDD	Nominally tied to +5VDC.

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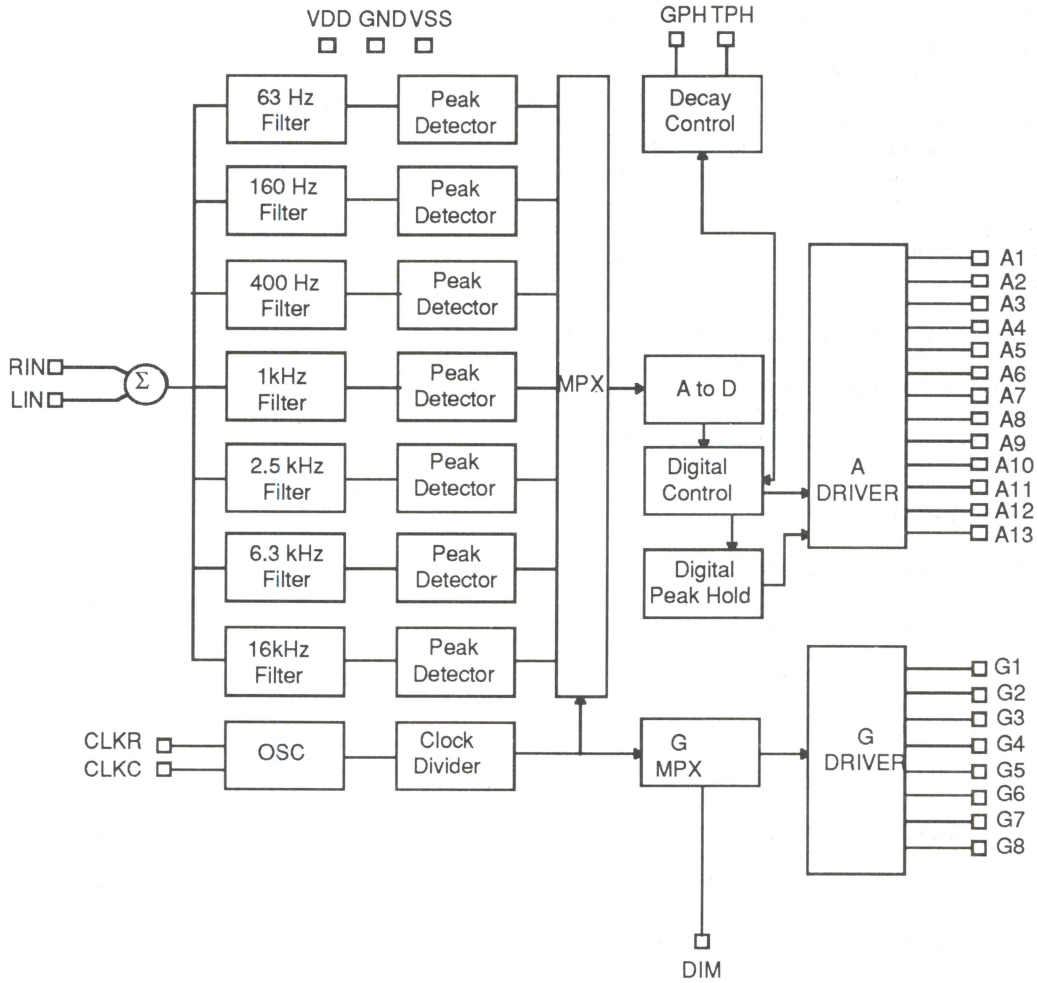


Figure 1. Block Diagram

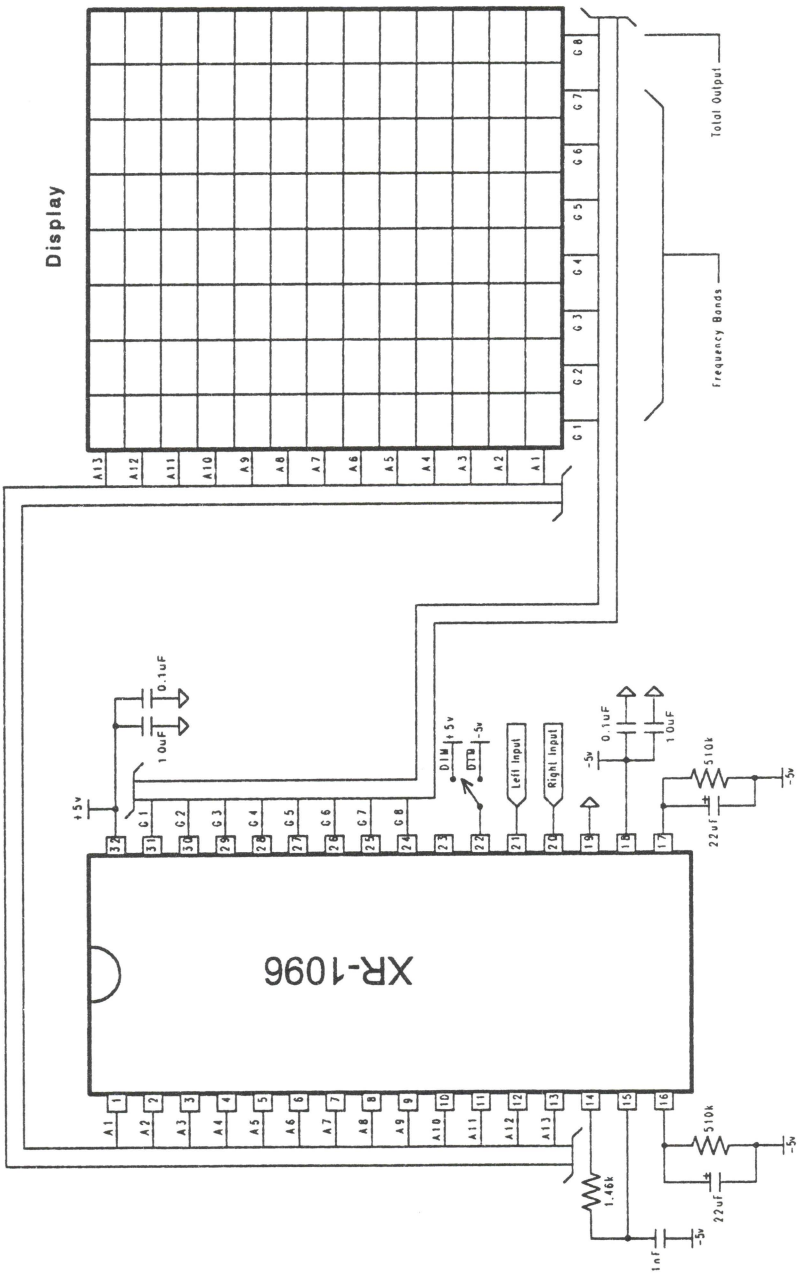


Figure 2. Typical Application Scematic



NOTES



Preliminary Information

7-Channel Graphic Equalizer Filter with A/D Converter

GENERAL INFORMATION

The XR-1097 is a 7-point switched capacitor filter dedicated for use in audio applications. The 7 filters are spaced 1 1/2 octaves apart starting at 63Hz. The two filter inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant audio information from being displayed. The 7 filter outputs, along with the peak value of all filters each go into a peak hold circuit with a slow decay time constant (330ms). The eight filter outputs and 2 auxiliary inputs are multiplexed into an A/D converter which produces the digital output that is used by the system microprocessor.

The XR-1097 is fabricated in a low noise 2 micron double poly-silicon CMOS process and comes in a 14-pin plastic package. The device may be operated off of either +/- 5V or +/- 6V supplies. The chip oscillator operates at 400kHz and requires only an external resistor and capacitor.

FEATURES

Internal R/C Oscillator
Provides seven filters in one 14-pin package
Dual inputs for summing Left and Right Channels
Provides 30dB of Gain
Two auxiliary inputs
Microprocessor Bus Interface
On Chip A/D Converter

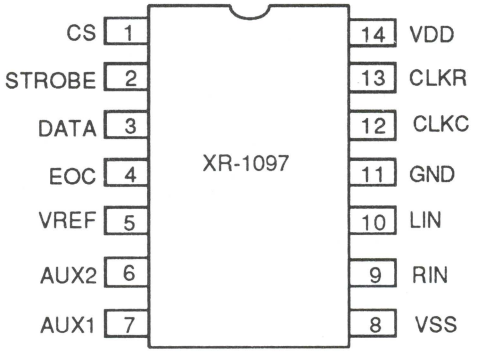
APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+/- 7V
Storage Temperature	-60 to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1097CP	14 Pin Plastic Dip	-30°C to 75°C

SYSTEM DESCRIPTION

The XR-1097 generates its clocks with an internal oscillator and does not require an external clock source. This allows the designer to place the XR-1097 on any application where an active filter design is in place. The XR-1097 provides bandpass filters with center frequencies at 63Hz, 160Hz, 400Hz, 1kHz, 2.5kHz, 6.3kHz, and 16kHz. These frequencies are standards in the consumer audio market. The peak detector outputs referenced to 0V are multiplexed into an A/D converter. The digital interface allows the system microprocessor to control the multiplexer and the A/D externally. All digital I/O (including A/D output) goes through a serial port. All digital inputs are TTL compatible, and all digital outputs swing from GND to VDD.

The XR-1097 contains a continuous time anti-aliasing filter with a corner frequency of 80kHz. This prevents most signals from affecting the performance of the filters.

ELECTRICAL CHARACTERISTICS

Test Conditions: VDD = +5V, VSS = -5V, TA = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS						
VDD	Positive Supply	4.75		6	V	
VSS	Negative Supply -6		-4.75	V		
IDD5	Supply Current		8	15	mA	
OSCILLATOR CHARACTERISTICS						
TCLKRPClock	Frequency 380 400	420	kHz		R =1.46 kOhm	C = 1nF
A/D CHARACTERISTICS						
	Accuracy			8	bit	
	Error			±1	LSB	
VREF	Reference Voltage		2.5		V	
TCONV	Conversion Time 400	80	440	µS		

PIN DESCRIPTION

PIN #	SYMBOL	DESCRIPTION
1	CSB	Chip Select Pin
2	STROBE	Clock pin to shift in/out data through the serial port
3	DATA	Serial port for digital signals to and from microprocessor
4	EOC	(A/D) End of Conversion pin
5	VREF	A/D Converter Reference voltage input
6	AUX2	Auxiliary Input 2
7	AUX1	Auxiliary Input 1
8	VSS	Negative Supply Voltage
9	RIN	Right Channel Input
10	LIN	Left Channel Input
11	GND	Ground
12	CLKC	Clock Capacitor from this pin to GND (Cnom = 1nF)
13	CLKR	Clock Resistor from this pint to CLCC (Rnom = 14.6 kOhm)
14	VDD	Positive Supply Voltage

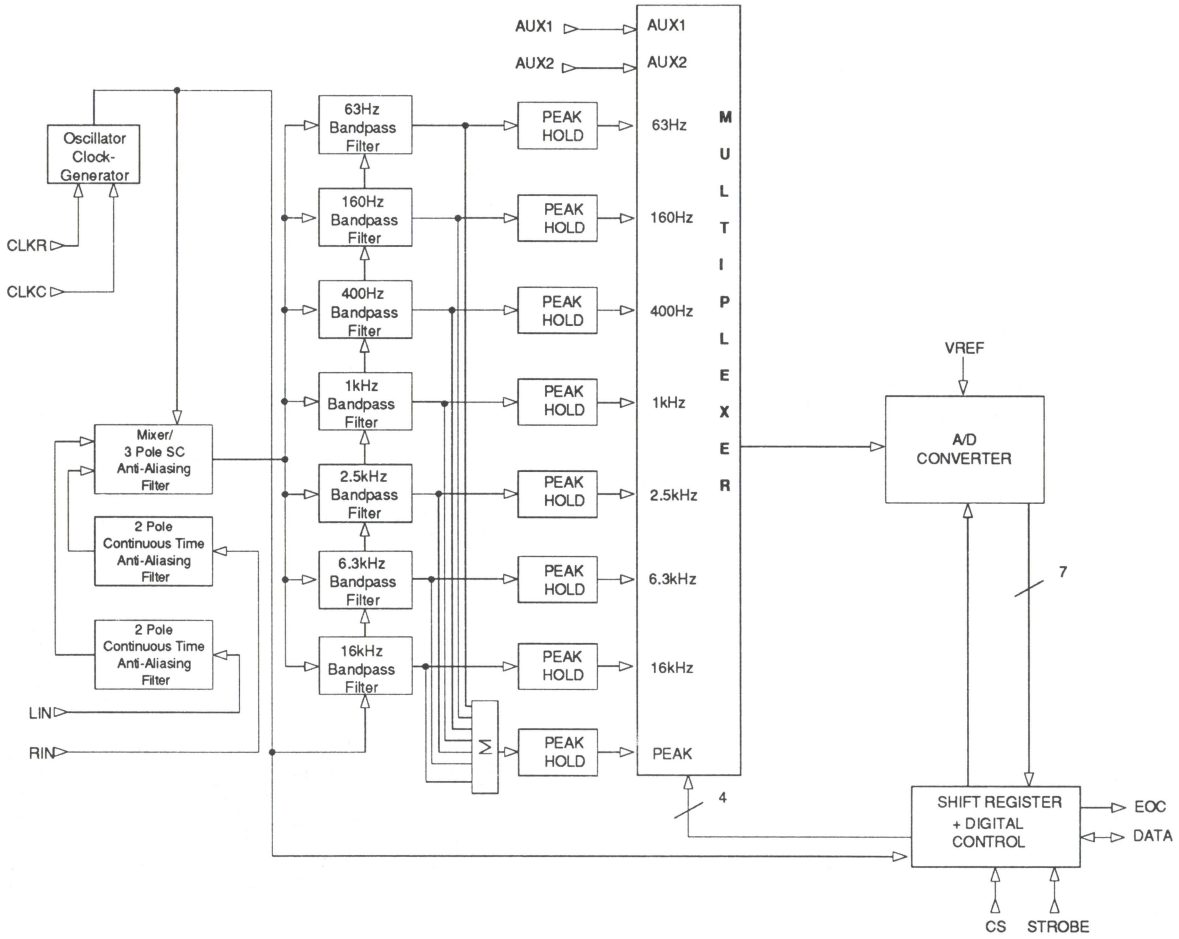


Figure 1. 7-Band Graphic Equalizer Display Filter with A/D Converter

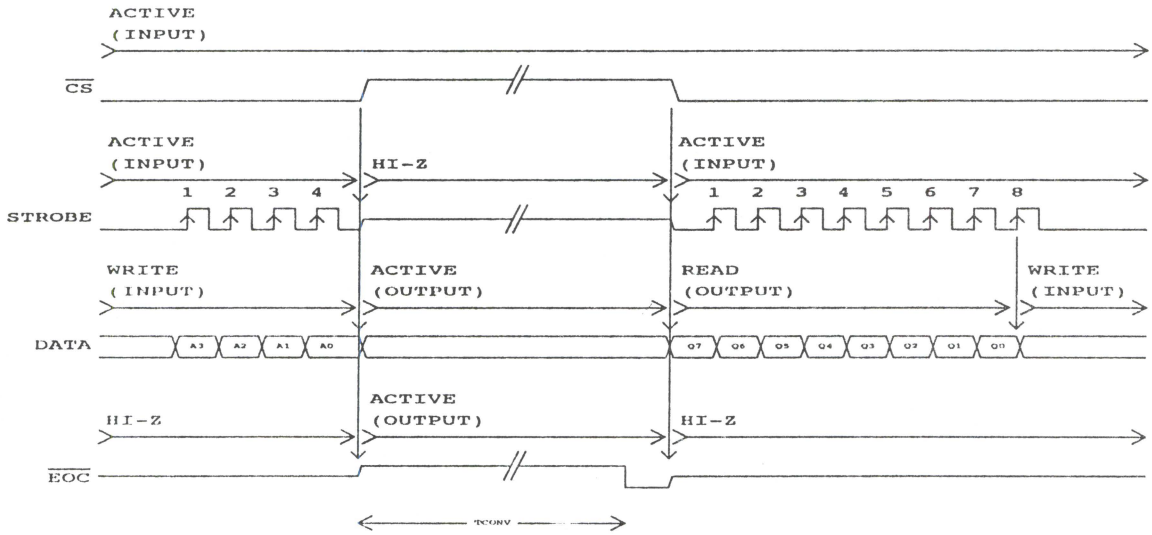


Figure 2. Microprocessor Interface Timing Diagram

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
FCLK	STROBE Frequency		2.5	MHz	#1
TH	STROBE High Pulse Width	160		ns	
TL	STROBE Low Pulse Width	160		ns	
TS	DATA Set-up Time	100		ns	
TD	DATA Hold Time	100		ns	
TO	STROBE Hold Time	100		ns	#2
TE	EOC Delay Time	100		ns	#3
TCONV	A/D Conversion Time	400	440	µs	#4
TR	STROBE Set-up Time	100		ns	#5
TK	EOC to CSB	100		ns	
TC	CSB to Q7	150		ns	
TV	STROBE to Q6-Q0	150		ns	
TI	STROBE to DATA Write Mode	150		ns	#6

Table 1. Timing Characteristics

Notes:

#1: TCLK=400ns. minimum.

#2: STROBE needs to be held low for TO after CSB goes high. After TO, STROBE becomes hi-z and DATA becomes an output port.

#3: After TE, EOC becomes a logical high.

#4: After TCNOV, EOC goes low, signalling the end of conversion.

#5: STROBE needs to be held low for TR before CSB goes low.

#6: After TI, DATA goes back to an input port.

A3	A2	A1	A0	SELECTION
0	0	0	0	63Hz
0	0	0	1	160Hz
0	0	1	0	400Hz
0	0	1	1	1KHz
0	1	0	0	2.5KHz
0	1	0	1	6.3KHz
0	1	1	0	16KHz
0	1	1	1	PEAK
1	0	0	0	AUX1
1	0	0	1	AUX2
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 2. Multiplexer Selection

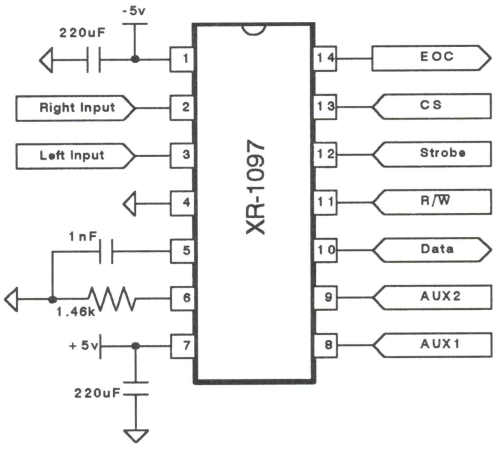


Figure 3. Typical Application Schematic



NOTES



Preliminary Information

BBE® II High Definition Audio Processor

GENERAL INFORMATION

The XR-1071 is an improved version of the high definition audio matched-pair sound enhancement processor using the patented BBE® II Sound Enhancement technique. It is designed for use with stereo sound systems to enhance the music to provide more realism to the sound regardless of its source. No initial encoding of the source signal is needed to achieve the sound enhancement. The XR-1071 provides this enhancement without additional speakers and is compatible with full-sized and headphone transducers for use with a variety of systems.

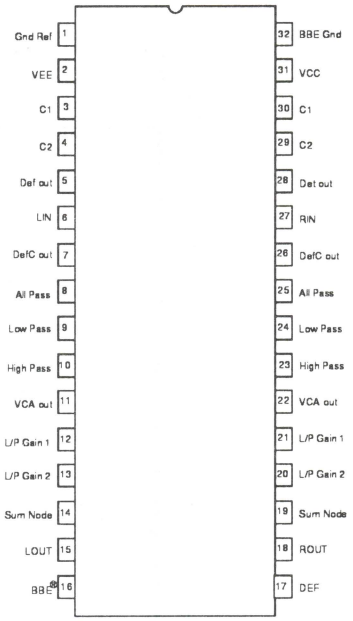
With the use of the DEFINITION control, the amount of enhancement can be adjusted to the preference of the listener. This single control affects both channels equally, reducing the complexity of the system adjustment. In addition, bass boost control is also provided to balance the dynamically changing high-band. Several fixed-level or variable-level configurations with minimal external components are possible. Furthermore, a single control disables the sound enhancement with internal analog switches.

The XR-1071 is fabricated using bipolar technology to provide extremely low noise (-95dBA typ), low total harmonic distortion, and acceptable current consumption (15mA typ) for battery operated applications and is available in 32 lead shrink-DIP for use over the -30°C to +75°C temperature range.

FEATURES

Recreate Concert Sound without Initial Encoding
Single Definition Control for Ease of Adjustment
Fixed and Variable Bass Boost Control
Super Low Noise: -95dBA typ IEC-A weighted
No Undesirable "Pumping" or "Breathing" Effects
Matched Circuits for Stereo Applications
Buffered Outputs
Transducer Independent
No Extra Speakers Needed

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1071CP	32 Pin SDIP	-30°C to +75°C

APPLICATIONS

Home Stereo Systems
Television Sound Systems (stereo ready)
Portable Battery Powered Systems
Automobile Stereo Systems

ABSOLUTE MAXIMUM RATING

Power Supply Voltage: V_{CC} - V_{EE}	26 VDC
Power Dissipation (package limitation)	
32 Pin SDIP package	1W
Derate above 25°C	9mW/°C
Storage Temperature	-65°C to +150°C
Maximum Input Voltage	V_{CC}+0.3V
Minimum Input Voltage	V_{EE}-0.3V

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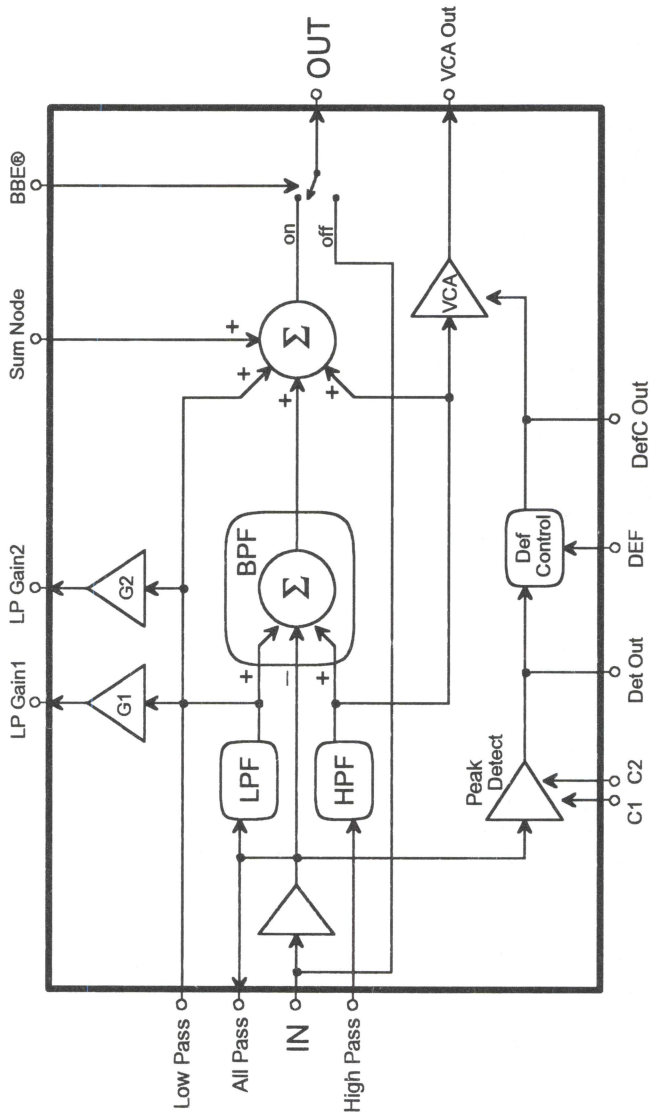


Figure 1. Block Diagram - one channel of XR-1071

PIN DESCRIPTION

PIN#	SYMBOL	TYPE	Description
1	Gnd Ref	I	**Ground Reference Input.** This is the reference input to the BBE Analog Ground generating circuit. Since the circuit is self biased, only a capacitor need be connected.
2	VEE	P	**Negative Power Supply.**
3,30	C1		**Capacitor One.** Connection point for peak detector capacitor.
4,29	C2		**Capacitor Two.** Connection point for peak detector capacitor.
5,28	Det out	O	**Detector Output.** Connection point for capacitor on output of peak detector.
6	LIN	I	**Left Channel Input.**
7,26	DefC out	O	**Definition Control Output**. Connection point for capacitor on output of definition control circuit.
8,25	All Pass	O	**All Pass Input**. Buffered output of signal to be fed thru capacitor to High Pass Input.
9,24	Low Pass		**Low Pass.** Connection point for low pass filter capacitor.
10,23	High Pass	I	**High Pass Input.** The high pass filter capacitor is connected between this point and the All Pass Output.
11,22	VCA out	O	**Voltage Controlled Amplifier Output.** The VCA output is capacitively coupled from this point to the Sum Node.
12,21	L/P Gain1	O	**Low Pass Gain One Output.** See text for explanation.
13,20	L/P Gain2	O	**Low Pass Gain Two Output.** See text for explanation.
14,19	Sum Node	I	**Summing Node Input.** Additional high and low signals generated elsewhere are added to the signal at this pin.
15	LOUT	O	**Left Channel Output.**
16	BBE	I	**BBE Bypass Control Input.** Control point for internal by pass switches. Controls both channels.
17	DEF	I	**Definition Control Input.** Control point for amount of amplitude compensation in the high band. Controls both channels.
18	ROUT	O	**Right Channel Output.**
27	RIN	I	**Right Channel Input.**
31	VCC	P	**Positive Power Supply.**
32	BBE Gnd	O	**BBE Ground Output.** This is the output to the BBE analog ground generating circuit. This very clean ground is used for several peripheral component connections.

SYSTEM DESCRIPTION

The XR-1071 is designed to provide even more life-like audio to reproduced sound than previous versions of the BBE® Sound Processors. The XR-1071 would normally be located in the preamplifier section of a sound system after the tuner or input section and before the amplifier stages that drive the transducers (speakers or headphones). Since no initial encoding of the signal source is needed, virtually any audio signal, including both monaural and stereo broadcasts and recordings, can benefit from the use of the XR-1071 BBE®II sound enhancement process. The XR-1071 provides a means to compensate for the transient distortion caused by the non-ideal interface between amplifier and transducer. BBE® sound enhancement compensates for this distortion by making corrections to the amplitude and phase.

ELECTRICAL CHARACTERISTICS: V_{CC} = +5VDC, V_{EE} = -5VDC, T_A = +25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS						
V_{CC} - V_{EE}	Total Supply Voltage	6		24	V	
I_{CC}	Positive Supply Current		15.0	22.0	mA	
I_{EE}	Negative Supply Current		15.0	22.0	mA	
V_{REG}	Regulator Output	-0.32	-0.22	-0.12	V	no load
$\Delta V_O/\Delta I_O$	Load Regulation	-10	+5	+20	mV	+1mA load
FILTER						
A_{MB}	Midband Signal Path Gain	1.1	1.6	2.1	dB	
$A_{LB}1$	Loband Signal Path 1 Gain	0.0	0.5	1.0	dB	
$A_{LB}2$	Loband Signal Path 2 Gain	4.5	5.0	5.5	dB	
$A_{LB}3$	Loband Signal Path 3 Gain	7.0	7.5	8.0	dB	
$A_{LB}4$	Loband Signal Path 4 Gain	9.2	9.7	10.7	dB	
A_{HB}	Unboosted Hiband Signal Path Gain	0.4	1.4	2.4	dB	
A_{HB}max	Max Boost Hiband Signal Path Gain	8.7	9.7	10.7	dB	
A_{OFF}	Gain of BBE® OFF Signal Path	-0.5	0.0	0.5	dB	
RECTIFIER						
N_{ON}	Noise in BBE® ON Mode					(IEC-A weighted)
			-95		dBA	Bass Boost = min
			-93		dBA	Bass Boost = max
N_{OFF}	Noise in BBE®OFF (Bypass) Mode		-113		dBA	(IEC-A)
PSRR	Power Supply Ripple Rejection		30		dB	10Hz
			45		dB	60Hz
			50		dB	100Hz

PHASE COMPENSATION

Phase compensation is utilized to change the time sequence of the frequency spectrum so that the transducer may reproduce the sound envelope more faithfully. The time shift introduced by the phase compensation is fixed internally and is not controlled by the user.

The block diagram of Fig.1 shows one channel of the stereo XR-1071 device. Signal entering the device at IN is buffered and filtered into three bands (Lo, Mid, and Hi) by the LPF, BPF, and HPF. Note that the HPF is fed via the All Pass output. Also note that the BPF is generated by subtracting the signal from the LPF and HPF outputs. In this way, the BPF output is at -180° phase, and the HPF is at -360° phase. All signal paths are recombined at the final summing node. The total system phase response is approximately linear and remains virtually unchanged regardless of all system adjustments (see Fig.2). In this way, the appropriate phase compensation for proper sound enhancement is quaranteed.

AMPLITUDE COMPENSATION

With the DEFINITION control, adjustments can be made for different types and sizes of transducers and environments, and for the personal preference of the listener. The DEFINITION control indicates the degree of amplitude compensation for the high frequencies of the incoming signal. This circuit has been improved to eliminate undesirable "pumping" and "breathing" effects while improving musical quality and voice intelligibility.

Referring again to the block diagram of Fig.1, buffered input signal is monitored by a single, wide-band peak detector. Both the detector's output and a voltage at DEF are fed to the DEF Control circuit. The voltage at DEF is listener adjusted via a 5K linear-taper potentiometer. In this way, the DEF Control circuit generates a control voltage for the VCA that is based on the amount of music present and input from the listener. Hiband signal fed to the VCA is then amplified according to this control voltage. The additional Hiband from the VCA output is recombined with the signal via the Sum Node input. The result is a dynamically changing Hiband with the listener adjusting the maximum boost. The resulting gain curves can be seen on the right half of Fig. 3.

It should be noted that a single DEF input controls both channels of the dual channel device

BASS BOOST

Bass boost control is implemented to give a fuller sound complementing the dynamically changing high frequency band. The bass boost control can be configured as fixed or left variable for adjustment by the listener.

Bass boost is accomplished by G1 and G2 from Fig.1, which independently amplify the Loband signal. Outputs L/P Gain1 and/or L/P Gain2 may be used to add additional Loband signal via the Sum Node input. Resulting gain curves can be seen in the left half of Fig. 3.

The level of bass boost can be fixed to any of four levels shown in the table of Fig.4 without the use of any external components (see Fig.6a). If variation is desired, switches can be used for listener selection from these four levels (see Fig.6b). Fixed resistors can be used to set a customizable fixed boost level (see Fig.6c). Boost versus resistance can be seen in Fig.5. Even more elegant, the use of two ganged audio-taper 100kOhm potentiometers will allow finely adjustable bass boost ranges (see Fig. 6d).

BBE® BYPASS FUNCTION

The XR-1071 has on-board bypass capability. Noise in the bypass mode is extremely low (-113dBA). The BBE® bypass function is performed by two internal analog switches (one for each channel). These switches can be controlled with one external SPST switch, as seen in Fig.7. Pin 16 has an internal pulldown current such that the external switch needs only a single throw. The external resistor Rs can be calculated as follows:

$$R_S = \frac{V_{CC} - V_{ee}}{72\mu A} \quad \Omega$$

If Rs is too large, the internal switch circuit may not function properly. If Rs is too small, "popping" sounds may occur when switching to and from bypass mode.

POWER CONNECTION

The XR-1071 has internal biasing for analog reference, eliminating the need for an external bias source in single-supply applications. However, the XR-1071 can also be used in split-supply applications. Pin 32, BBE Gnd output, is approximately 1/2 way between the supply voltages and is provided for several key connections to minimize noise feed-through. Appropriate connections can be seen in Fig 7.

LICENSE AGREEMENT

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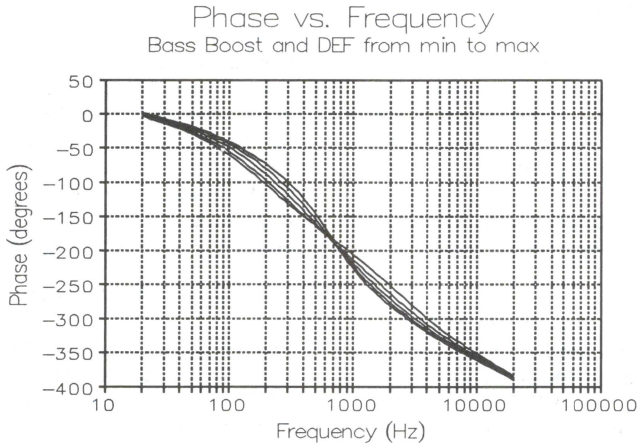


Figure 2. Phase Response

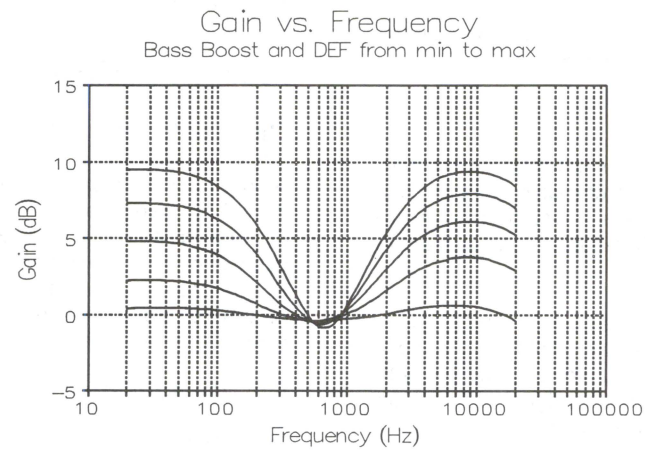


Figure 3. Gain Response

Path #	Connections		Fixed Path Gain	Gain with 100K Pot
	L/P Gain2	L/P Gain1		
1	no	no	0.5dB	n/a
2	no	yes	5.0dB	1.1 to 5.0dB
3	yes	no	7.5dB	1.1 to 7.5dB
4	yes	yes	9.7dB	1.1 to 9.7dB

Figure 4. Bass Boost - Connection & Control

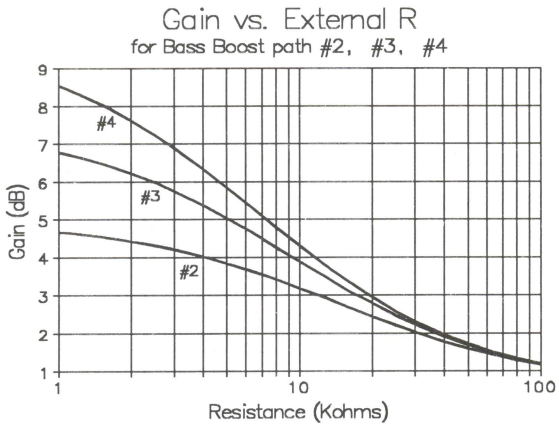
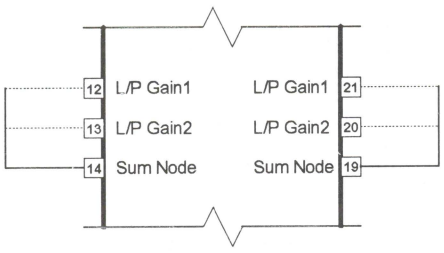
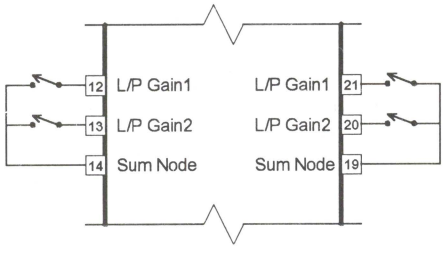


Figure 5. Bass Boost - Variable Control

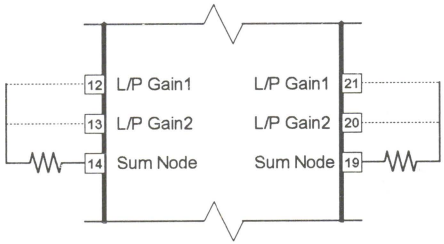
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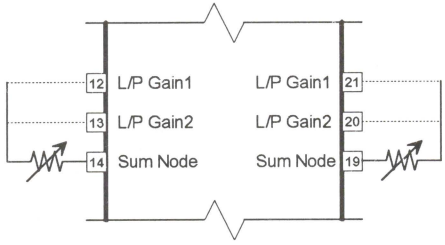
a) Fixed - Connection Controlled



b) Variable - Switch Controlled



c) Fixed - Resistor Controlled



d) Variable - Potentiometer Controlled (audio taper)

Figure 4. Fixed and Variable Control Configurations for Bass Boost

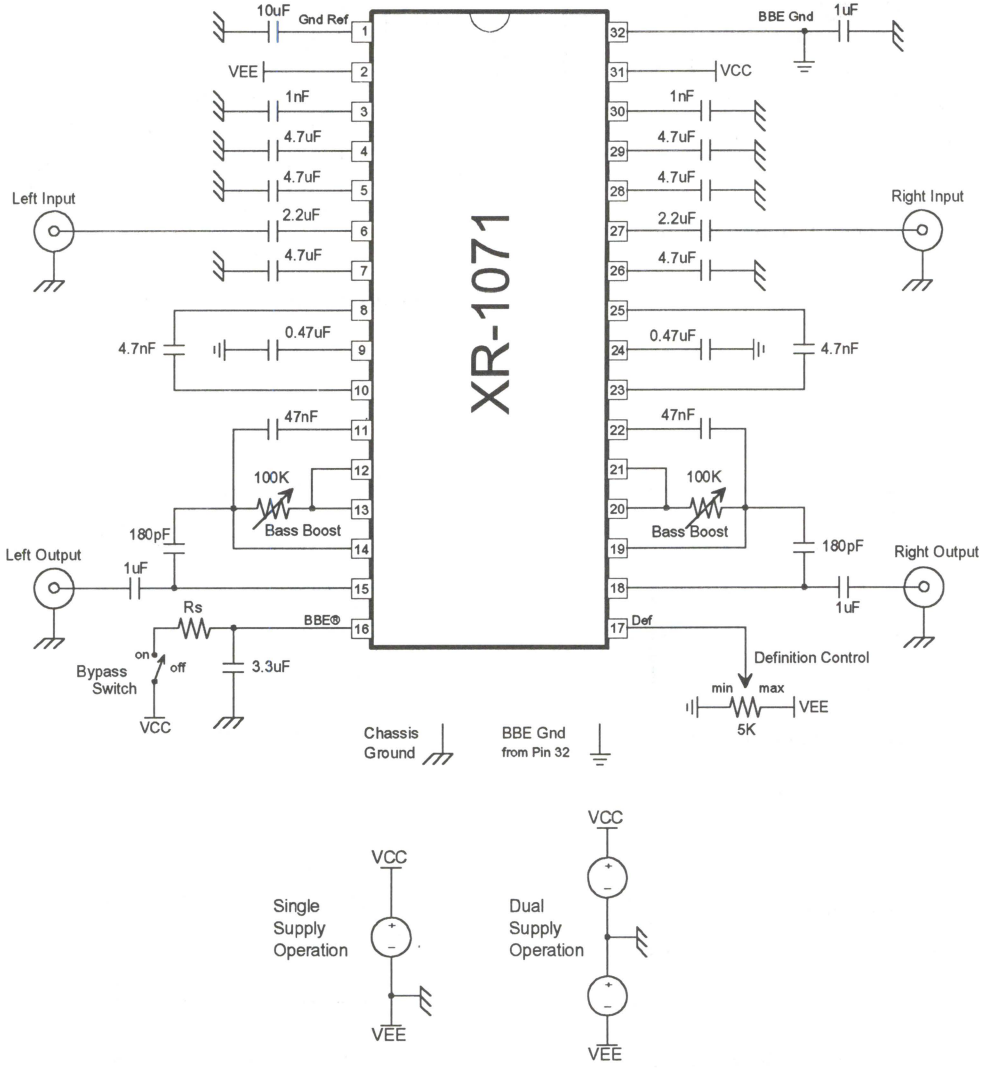


Figure 5. Typical Application Schematic

XR-5383 BBE®Sound Enhancement Processor

Preliminary Information

GENERAL DESCRIPTION

The XR-5383 is a single channel sound enhancement processor using the patented BBE technique to provide more lifelike audio to reproduced sound regardless of its source. No initial encoding of the source signal is needed to achieve the sound enhancement. The XR-5383 provides this enhancement without additional speakers and is compatible with headphone transducers for use with walkabout or portable stereo systems.

With the use of the definition control the amount of enhancement can be controlled to the listeners liking. Each channel has its own control allowing for greater adjustment of the effect in case of non-matched speakers.

The XR-5383CP is a available in a 22 pin plastic DIP, 0.3 inches wide.

The XR-5383 is fabricated using bipolar technology to provide extremely low noise, low total harmonic distortion and low current consumption (4 mA typical) for battery operated applications.

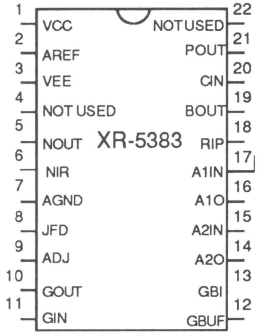
FEATURES

Recreate Concert Sound without Initial Encoding
Single Control for Ease of Adjustment
Extremely Low Noise: -85 dBV typically
  using IEC Weighting
More Flexibility with the Single Channel
Transducer Independent: Functions with
  headphones or large speakers
No extra speakers needed to achieve the effect.

APPLICATIONS

Walkabout Stereo or Monaural Systems
Portable Sound Systems
Sound Enhancement for Home Stereo (Hi-Fi)
  Systems
Television Sound Systems (Stereo Ready)

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5383CP	22 Pin Plastic DIP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Power Supply VCC	36V
Power Dissipation (Package Limitation)	
Plastic DIP	1Watt
Derate above 25°C	6 mW/°C
Storage Temperature Range	-65°C to +150°C
Voltage Applied to any Input	VEE- 0.3 to VCC +0.3

SYSTEM DESCRIPTION

The XR-5383 is designed for use with both monaural and stereo sound systems to enhance the music to provide more realism to the sound. The XR-5383 would normally be located in the preamplifier section of a sound system after the tuner or input selection and before the amplifier stages to drive the transducers (speakers or headphones). The definition control is adjusted until satisfactory to the listener. Any low noise switch can be used to provide a bypass of the BBE sound processor.

5



NOTES



BBE® Low Voltages Stereo Sound Enhancement Processor

GENERAL INFORMATION

The XR-5410 is a low voltage version of the high definition audio matched-pair sound enhancement processor using the patented BBE® Sound Enhancement technique. It is designed for use with stereo sound system to enhance the music to provide more realism to the sond regardless of its source. No initial encoding of the source signal is needed to achieve the sound enhancement without additional speakers and is compatible with large and headphone transducers for use with walkabout or portable stereo and telephone systems.

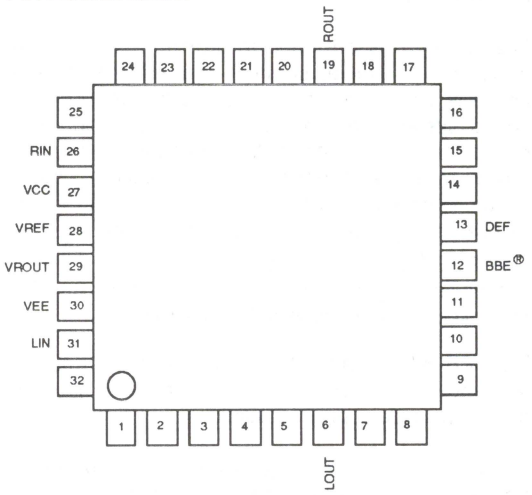
With the use of the definition control, the amount of enhancement can be controlled to the listener's liking. This single control affects both channels equally, reducing the complexity of the systems adjustment. In addition, fixed bass boost is provided to balance the dynamically chanding high band. Furthermore, a single control disables the sound enhancement with internal analog switches.

The XR-5410 is fabricated using bipolar technology to provide extremely low noise, low total harmonic distortion and low current consumption (4mA typical) for battery operated applications and is available in 32 lead QFP packaging for use over the -30°C to +75°C temperature range.

FEATURES

Recrate Concert Sound without Initial Encoding
Low Power Supply Voltage: 1.6v to 3.0v
Single Definition Control for Ease of Adjustment
Extremely Low Noise: -85dBV max using IEC-A Weighting
Matched Circuits for Stereo And Other Two Channel Applications
Transducer Independent: Functions with headphones or large speakers
No extra speakers needed to achieve the effect

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5410CQ	32 Pin QFP	-30°C to +75°C

APPLICATIONS

Walkabout Stereo Systems
Portable Sound Systems
Telephones and Speakerphones

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	4.5V
Power Dissipation (package limitation)	
32 pin QFP package	400mW
derate above 25°C	TBDmW/°C
Storage Temperature	-60°C to +150°C
Maximum Input Voltage	V_{CC} +0.3V
Minimum Input Voltage	V_{EE} -0.3V

5

SYSTEM DESCRIPTION

The XR-5410 is designed to provide more life-like audio to reproduced sound. The XR-5410 would normally be located in the preamplifier section of a sound system after the tuner or input section and before the amplifier stages that drive the transducers (speakers or headphones). The definition control, which affects both channels of the dual channel device, is adjusted until satisfactory to the listener.

The BBE® bypass function is performed by two internal analog switches. These switches can be controlled with one external SPDT switch.

The XR-5410 has internal biasing for analog reference, eliminating the need for an external bias source in single supply applications.

Since no initial encoding of the signal source is needed, virtually any audio signal, including both monaural and stereo broadcasts and recordings, can benefit from th euse of the XR-5410 BBE® Sound Enhancement Processor.

PRINCIPLES OF OPERATION

The XR-5410 provides a means to compensate for the delay and amplitude distortion caused by loudspeakers, headphones and other transducers of electrical signals to mechanical motion. With the DEFINITION control, adjustments for different types and sizes of transducers and environments, as well as the listener's taste, can be performed. The degree of amplitude compensation to the incoming signal's high frequencies is controlled by the DEFINITION control.

A fixed bass boost of +3.25dB is implemented to give a fuller sound complementing the dynamically changing high frequency band.

Phase compensation is utilized to change the time sequence of the frequency spectrum so that the transducer may reproduce the sound envelope more faithfully. The time shift introduced by the phase compensation is fixed internally and is not controlled by the user.

LICENSE AGREEMENT

The XR-5410 is manufactured by EXAR under license from BBE® Sound Inc. BBE® is a registered trademark of BBE® Sound Inc. A license from BBE® Sound Inc. (714-897-6766) is required for sales of the XR-5410.

ELECTRICAL CHARACTERISTICS: VCC=+2.0VDC, VEE=0VDC, T_A=+25°C unless otherwise specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS						
V_{CC}	Supply Voltage	1.6		3.0	V	
I_{CC}	Supply Current	2.0		4.6	mA	
V_{ROUT}	Reference Output Voltage	1.324		1.464	V	
	Load Regulation	-3		3	mV	±100µA load
INPUT AND OUTPUT						
V_{IN}	Nominal Input Signal Level		70		mVrms	
V_{IN}	Maximum Input Signal Level		400		mVrms	Def=min
V_{OS}	Output Offset Voltage	-120		120	mV	Def=max
AMPLITUDE						
A_{LB}	Loband Signal Path Gain	2.5		4.0	dB	
A_{MB}	Midband Signal Path Gain	1.4		2.8	dB	
A_{HB}	Unboosted Hiband Signal Path Gain	-0.5		1.3	dB	
ΔA_{HB}	Hiband Signal Path Gain Channel Match	-6		6	%	
A_{HB}min	Minimum Hiband Path GAin (Cut)	-9.2		-8.0	dB	Def=max
A_{HB}max	Maximum Hiband Path Gain (Boost)	8,0		9.2	dB	Def=max
A_{OFF}	BBE® Off Signal Path Gain	-0.82		0.26	dB	
SYSTEM						
D_{LB}	Loband Signal Path Distortion			1.0	%	
D_{MB}	Midband Signal Path Distortion			1.0	%	
D_{HB}	Hiband Signal Path Distortion			1.0	%	Def=min
D_{HB}	Hiband Signal Path Distortion			1.0	%	Def=max
D_{OFF}	BBE® Off Path Distortion			1.0	%	
N_{ON}	Noise in BBE® On Mode		-87		dBV	IEC-A Weighted
N_{OFF}	Noise in BBE® Off (bypass) Mode		-104		dBV	IEC-A Weighted

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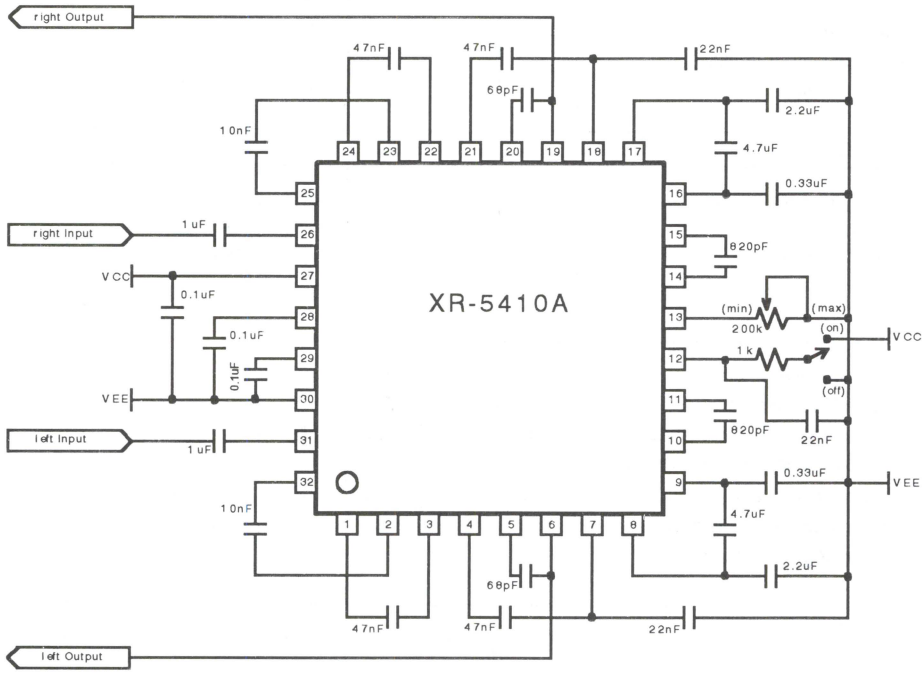


Figure 1. Typical Application Circuit

BBE® Stereo Sound Enhancement Processor

GENERAL DESCRIPTION

The XR-5451 is a matched pair of sound enhancement processors using the patented BBE® Sound Enhancement technique to provide more lifelike audio to reproduced sound regardless of its source. No initial encoding of the source signal is needed to achieve the sound enhancement. The XR-5451 provides this enhancement without additional speakers and is compatible with headphone transducers for use with walkabout or portable stereo systems.

With the use of the definition control the amount of enhancement can be controlled to the listener's liking. This single control affects both channels equally, reducing the complexity of the system adjustment. In addition, a single control disables the sound enhancement with internal analog switches.

The XR-5451 is fabricated using bipolar technology to provide extremely low noise low total harmonic distortion and acceptable current consumption (15 mA typical) for battery operation applications and is available in 32 lead shrink DIP packaging for use over the -30 to +75°C temperature range.

FEATURES

Recreate Concert Sound without Initial Encoding
Single Definition Control for Ease of Adjustment
Extremely low noise: -92 dBV typically using IEC-A Weighting
Matched Circuits for Stereo Applications
Transducer Independent: Functions with head phones or large speakers
No extra speakers needed to achieve the effect

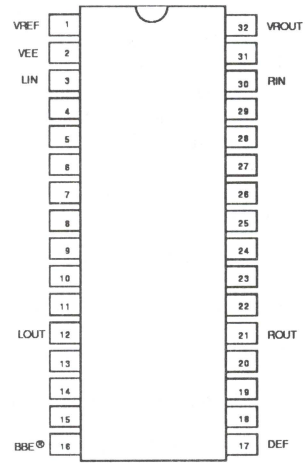
APPLICATIONS

Walkabout stereo systems
Portable Sound Systems
Sound Enhancement for Home Stereo Systems
Television Sound Systems (Stereo Ready)

ABSOLUTE MAXIMUM RATINGS

Power Supply: V_{CC}	26 VDC
32 Pin DIP Package	TBD mW
Derate above 25°C	TBD mW/°C
Storage Temperature	-65°C to +150°C
Voltage Applied to any input	V_{EE}- 0.3 to V_{CC} +0.3

PIN ASSIGNMENT



SYSTEM DESCRIPTION

The XR-5451 is designed for use with stereo sound systems to enhance the music to provide more realism to the sound. The XR-5451 would normally be located in the preamplifier section of a sound system after the tuner or input section and before the amplifier stages to drive the transducers (speakers or headphones). The definition control, which affects both channels of the dual channel device, is adjusted until satisfactory to the listener. An external SPST switch can be used to provide the BBE bypass function for the sound processor.

The XR-5451 has internal biasing for analog reference, eliminating the need for an external bias source in single supply applications. However the XR-5451 can also be used in split supply applications.

Since no initial encoding of the signal source is needed, virtually any audio signal, including both monaural and stereo broadcasts and recordings, can benefit from the use of the XR-5451 BBE® sound enhancement processor.

ELECTRICAL CHARACTERISTICS: VCC = +5 VDC VEE = -5VDC T_A = +25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
ICC	Positive Supply Current		15.0	22	mA	
IEE	Negative Suppy Current		15.0	22	mA	
VREG	Regulator Output	-0.32	-0.22	-0.12	V	no load
	Load Regulation	-10	+5	+20	mV	+ 1 mA load
FILTER SECTIONS						
MBGAIN	Midband Signal Path Gain	0.65	1.15	1.65	dB	
LBGAIN	Loband Signal Path Gain	3.6	4.1	4.6	dB	
HBGAIN	Hiband Signal Path Gain	0.4	1.4	2.4	dB	
GMIN	Minimum Hiband Signal Path Gain	-9.6	-8.6	-7.6	dB	
GMAX	Maximum Hiband Signal Path Gain	8.6	9.6	10.6	dB	
OFFG	Gain of BBE OFF Signal Path	-0.5	0.0	0.5	dB	
RECTIFIER SECTIONS						
MBDOFF	Offset of Midband Detector	-20	0	+20	mV	
HBDOFF	Offset of Hiband Detector	-20	0	+20	mV	
MBDGN	Gain of Midband Detector	-11.2	-9.8	-8.4	VDC/VPP	
HBDGN	Gain of Hiband Detector	-5.9	-5.2	-4.4	VDC/VPP	
OMNSE	Noise in BBE ON Mode		-92		dBV	IEC-A Weighted
OFFNSE	Noise in BBE OFF (BYPASS) Mode		-112		dBV	
PSRR	Power Suuply Ripple Rejection		30		dB	10 Hz
			45		dB	60 Hz
			50		dB	100Hz

PRINCIPLES OF OPERATION

The XR-5451 provides a means to compensate for the delay and amplitude distortion caused by loudspeakers, headphones and other transducers of electrical signals to mechanical motion. With the DEFINITION control adjustments for different types and sizes of transducers and environments, as well as the listener's taste, can be performed

The amplitude compensation is controlled by the energy content of the signal. If a signal has a deficiency of energy in the upper frequency region, the signal energy level of the upper frequencies will be amplified to compensate for the transducers' limitations. The degree of compensation to the incoming signal is controlled by the DEFINITION control.

The phase compensation changes the time sequence of the frequency spectrum so that the transducer may reproduce the sound envelope more faithfully. The time shift introduced by the phase compensation is fixed internally and is not controlled by the user.

APPLICATION INFORMATION

The XR-5451 requires some caution as to the layout in order to obtain the low noise low Total Harmonic Distortion and good channel separation that is possible with the device. Figure 2 provides the typical application circuit. The XR-5451 requires 27 capacitors, 1 resistor and 1 potentiometer to be used to obtain the signal processing functions needed for the sound enhancement of the BBE sound system. These components must have certain characteristics to obtain good performance from the XR-5451.

The potentiometer and capacitor can be of any type since it is controlling a slowly changing DC level. The resistors can be either carbon film, carbon composition or metal film. 10% tolerance is adequate for their value.

The decoupling capacitors on V_{CC}, V_{EE} and V_{REF} can be aluminum electrolytic capacitors. The recommended value is 1.0 µF. In a single supply application, the VCC/2 output would have a 1.0 µF capacitor from pin 32 to the signal ground of the system. V_{EE} would be tied to ground and no capacitor would be needed for this pin.

The filter capacitors are recommended to have a tolerance of ± 20% maximum in order to obtain correct filtering of the audio input. Ceramic dielectric capacitors can be used for the filter capacitors as long as no strong electric fields will be near them. If this cannot be prevented, a foil type capacitor (MYLAR® or Polyester) is recommended so that the outer foil layer can be used as a shield by grounding the outer layer. Non-polarized capacitors are recommended for all locations except where polarity is indicated on the typical application schematic (figure 2). This will allow the same circuit to be used for split supply or single supply operation.

The ground traces should be the widest traces on the printed circuit board. Since the entire circuit contained in the XR-5451 is analog, there is no need to separate any of the grounds associated with the device. However, if any switched-capacitor filter technology shares the power supply with the XR-5451, it is recommended to use separate ground traces to prevent clock coupling.

The XR-5451 is designed to work in both single supply and split supply applications.

The IC has an internal mid supply voltage reference circuit which has been tuned to optimize signal headroom for low supply voltage applications. Internal to the BBE IC, all signals are referenced to this voltage. The reference voltage is available externally on Pin 32.

In order to maintain high power supply ripple rejection, the capacitors from Pin 8 and Pin 25 must be connected to IC Pin 32. It is recommended that other capacitors be connected to chassis ground. Chassis ground is VEE (Pin 2). The decoupling needed for VEE and VCC will depend upon the noise present on the supplies. The XR-5451 will not generate any noise on VDD or VEE.

The control pin for the analog switch has an internal pulldown current so that externally only a single throw switch is required. The external switch resistor (Rs on the application schematic) should be made as large as possible in order to minimize the "popping" sound which can occur when switching from BBE_ON to BBE OFF mode. If Vmin is the lowest possible voltage between Pin 31 and Pin 2 in your application, then the switch resistor should be chosen so that $Rs \leq Vmin / 72\mu A$. If Rs is larger than that value, the switch circuit may not function properly over all device variations.

LICENSING AGREEMENT

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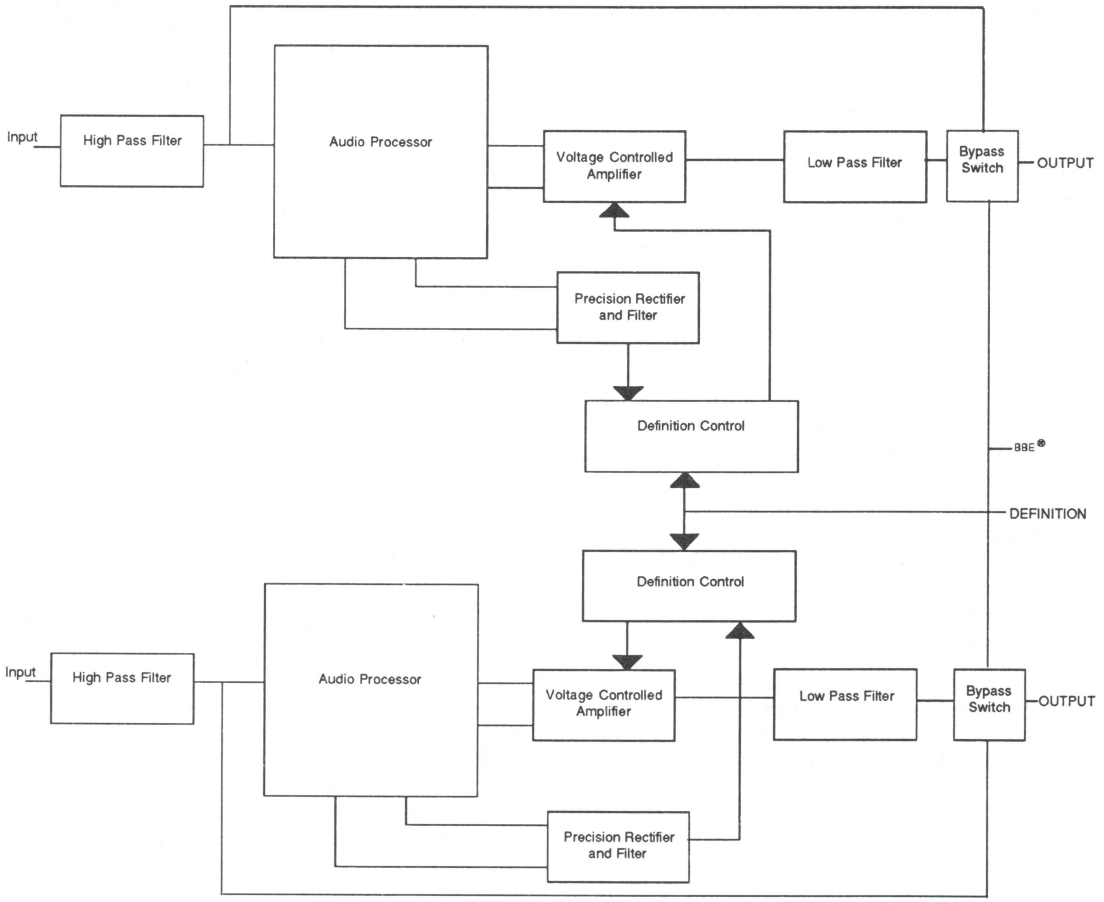


Figure 1. XR-5451 Simplified Block Diagram

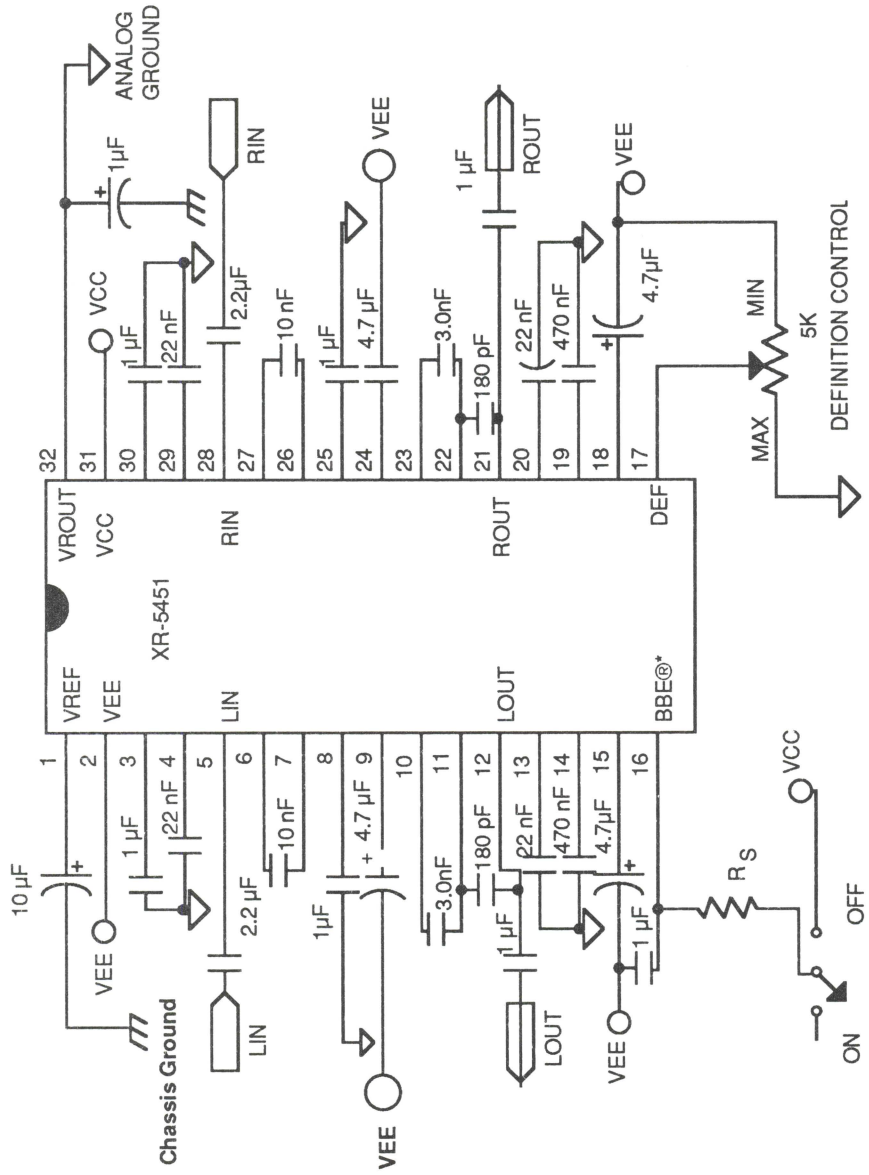


Figure 2. XR-5451 Typical Applications Schematic



NOTES



8mm VTR ATF

Preliminary Information

GENERAL DESCRIPTION

The XR-1080 is a mixed analog/digital IC dedicated for use in Automatic Track Finding (ATF) for 8mm Video Tape Recorder applications. The XR-1080 contains three major functional modules: the ATF record pilot signal generator, the ATF pilot signal detector, and the video signal detector. The device is fabricated using EXAR's CMOS process providing low noise, high speed, and low power, and is available in 48 pin VQFP versions for use over the -30°C to 75°C temperature range.

FEATURES

Mixed analog/digital integration to reduce discrete components
Pilot signal generator and detector on the same chip
On chip video signal GCA amplifier and detectors
Accurate switched-capacitor filters
Low noise, low power dissipation CMOS

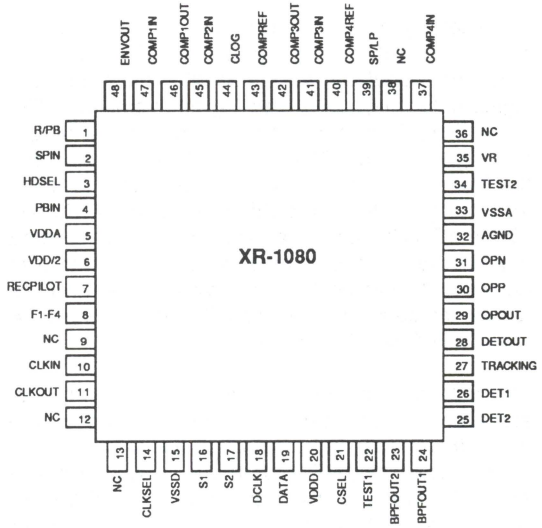
ABSOLUTE MAXIMUM RATINGS

VDD	-0.4 to 7V
Input Voltage	-0.4 to 7V
Output Voltage	-0.4 to 7V
Storage Temperature	-40 to +125°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1080CV	48 Pin VQFP	-30°C to +75°C

PIN ASSIGNMENT



48VQFP

SYSTEM DESCRIPTION

The XR-1080 is designed to reduce the part count for implementing ATF functions in 8mm VTR's. The XR-1080 contains an ATF record pilot signal generator, an ATF pilot signal detector, and a video signal detector.

The record pilot signal generator consists of an oscillator, a programmable frequency divider and a sine wave generator circuit. The oscillator generates the master clock signal for the entire chip. The clock frequency of either 5.95 MHZ or 11.9 MHZ (NTSC) is controlled by an external control signal. Two digital control lines (S1,S2) program the internal frequency divider chain to produce one of the four possible pilot signals (4f control). The selected pilot frequency is filtered by a band-pass filter to produce the sine wave output pilot signal.

SYSTEM DESCRIPTION (cont.)

The pilot signal detector consists of a pre-amplifier, band-pass filter, gain control amplifier (GCA), balanced modulator, reference pilot filters, tracking signal detectors, and a tracking error amplifier. The input signal is amplified by the pre-amplifier first, it has a gain of 20dB. Then the band-pass filter passes the four different pilot frequencies and adds an extra 10dB of gain. It rejects video and chroma signals above 170kHz. After the larger video and chroma signals have been removed, the pilot signal is amplified by the GCA for improved signal to noise ratio in the balanced modulator. The gain of the GCA is controlled by a 4-bit digital word.

The balanced modulator mixes the incoming pilot signals with the reference clock selected by the digital inputs (S1, S2) to produce two tones, one at approximately 16 kHZ, and another at approximately 46 kHZ. These signals are then filtered by the reference pilot filters to remove the unwanted balanced modulator output products. The reference pilot signals are then converted into a DC level through the peak detectors. The detector outputs are compared and the error signal is amplified before being brought off the chip. The DC reference is determined by the tracking input. The error signal is used to determine the tracking errors in the system.

The video signal detector consists of a video gain control amplifier (VGCA), a video signal peak detector, CLOG detector and SP/LP detector.The input video signal is amplified by the VGCA, and its gain is selected by a 4-bit digital word. Then the envelope of the video signal is detected by a video detector, which is followed by the detection of CLOG and SP/LP status.

ATF PIN DESCRIPTION (48 pin VQFP)

Pin#	Name	Description
1	R/PB	Record/Playback cont.
2	SPIN	Auxiliary video input
3	HDSEL	Video input signal sel.
4	PBIN	Playback signal input
5	VDDA	Analog power supply
6	VDD/2	AC ground input
7	RECPILOT	Analog Pilot signal output
8	F1F4	Digital pilot signal output
9	NC	Not Connected
10	CLKIN	Clock input
11	CLKOUT	Clock output
12	NC	Not connected
13	NC	Not connected
14	CLKSEL	11.9/5.95 Clock sel.
15	VSSD	Digital ground
16	S1	Pilot frequency cont.
17	S2	Pilot frequency cont.
18	DCLK	Serial port clock input
19	DATA	Serial port data input
20	VDDD	Digital power supply
21	CSEL	Chip select input
22	TEST1	Test pin #1
23	BPFOUT2	16K bandpass output
24	BPFOUT1	47K bandpass output
25	DET2	detector input
26	DET1	detector input
27	TRACKING	Detector reference
28	DETOUT	Detector output
29	OPOUT	Opamp output
30	OPP	Opamp positive input
31	OPN	Opamp negative input
32	AGND	AC ground output
33	VSSA	Analog VSS
34	NC	Not connected
35	VR	Reference Voltage
36	NC	Not connected
37	COMP4IN	SP/LP reference
38	NC	Not connected
39	SP/LP	SP/LP status output
40	COMP4REF	SP/LP comp input
41	COMP3IN	SP/LP input
42	COMP3OUT	Compared output
43	COMPREF	Video DC reference
44	CLOG	CLOG status output
45	COMP2IN	CLOG comparator input
46	COMP1OUT	Compared output
47	COMP1IN	CLOG reference
48	ENVOUT	Video detected output

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5.0, Xtal = 12.0MHz

SYMBOL	PARAMETER	MIN	TYP	MAX	Unit	CONDITION / TBD
PBF1	Passband Response	29	31.5	34	dB	PBIN = 10m V_{PP}, f = 103.5kHZ
PBF2		29	31.5	34	dB	PBIN =10m V_{PP}, f = 120.1kHZ
PBF3		29	31.5	34	dB	PBIN = 10m V_{PP}, f = 166.8kHZ
PBF4		29	31.5	34	dB	PBIN = 10m V_{PP}, f = 150.1kHZ
RIPPLE	Passband Ripple		0.5	2	dB	
SB10K	Stopband Response	5	3		dB	PBIN = 100m V_{PP}, f = 10kHZ
SB500K		-30	-35.5		dB	PBIN = 100 m V_{PP}, f = 500kHZ
BPF16K	LBPF2 Output (16K)	350	450	550	mV_{PP}	PBIN = 10m V_{PP}, 165kHZ, GCA = 0dB, Carrier = 149 kHZ
BPF47K	LBPF1 Output (47K)	350	450	550	mV_{PP}	PBIN = 10m V_{PP}, 165kHz GCA = 0dB, Carrier = 118kHz
BPDIFF	LBPF	-80	0	80	mV	
BPR16K	LBPF2 Rejection at 12kHz		80	100	mV	PBIN = 10m V_{PP}, 137kHz GCA = 0dB, Carrier = 149kHz
BPR47K	LBPF1 Rejection at 19kHz		80	100	mV	PBIN = 10m V_{PP}, 137kHz, GCA = 0dB, Carrier = 118kHz
GCA1	GCA Gain	0.86	1.07	1.28	dB	PBIN = 10m V_{PP}, 149kHz, 1dB
GCA2		1.8	2.13	2.5	dB	PBIN = 10m V_{PP}, 149kHz, 2dB
GCA4		3.8	4.27	4.7	dB	PBIN = 10m V_{PP}, 149kHz, 4dB
GCA8		7.7	8.53	9.4	dB	PBIN = 10m V_{PP}, 149kHz, 8dB

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{DD} = 5.0V

SYMBOL	PARAMETER	MIN	TYP	MAX	Unit	CONDITION / TBD
DETOS1	Detector Offset	-30	0	30	mV	Det1 = Det2 = 0V
DETOS2		-30	0	30	mV	Det1 = Det2 = 0.5VPP, f = 46.2kHz
DET1	Detector Output	-300	-350	-400	mV	Det1 = 0.5VPP, f = 46.2kHz Det2 = 0.0V
DET2		300	350	400	mV	Det2 = 0.5VPP, f = 46.2kHz Det1 = 0.0V
VGCA0	VGCA Gain (0dB)	2	4	6	dB	PBIN = 1.0VPP, 3.2MHz, 0dB
VGCA1		0.7	1	1.6	dB	PBIN = 1.0VPP, 3.2MHz, 1dB
VGCA2		1.7	2	3	dB	PBIN = 1.0VPP, 3.2MHz, 2dB
VGCA4		3.5	4	5	dB	PBIN = 1.0VPP, 3.2MHz, 4dB
VGCA8		6.5	8	9.5	dB	PBIN = 1.0VPP, 3.2MHz, 8dB
VDD	Power Supply Voltage	4.75	5	5.25	V	
IDDR	Power Supply Current		6.5		mA	Record Mode, Gain = 0
IDDPB			8.5		mA	Playback Mode, Gain = 0
PBIN	Input Pilot Signal Level	10	30	50	mVPP	
	Input Composite Signal Level	150	800	1500	mVPP	
	Recpilot Output DC Level	2.3	2.5	2.7	V	
	Recpilot Output AC Level		2.1		VPP	
	Recpilot Output Impedence		1.2	2.5	KΩ	
VDDHLF	AC Ground Input	2.4	2.5	2.6	V	VDD = 5.0V
VREF	Reference Voltage	2.1	2.2	2.3	V	
AGND	AC Ground Output	2.4	2.5	2.6	V	VDD = 5.0V
OPOS	Opamp Offset	-50	20	50	mV	Vin- = Vout
	VGCA Bandwidth	5	7		MHz	3dB Bandwidth
Compref	Compref DC Level	1	1.2	1.6	V	VDD = 5.0V
Envout	Envout DC Level	1	1.2	1.6	V	PBIN = 0V, VGCA = 0dB

DIGITAL CONTROL INPUTS

PILOT FREQUENCY CONTROL

S2	S1	f	F1-F4 Frequency (NTSC)	f0/N
0	0	f4	148689 Hz	40
0	1	f3	165210 Hz	36
1	0	f2	118951 Hz	50
1	1	f1	102544 Hz	58

CLOCK FREQUENCY CONTROL

CLKSEL	Clock Frequency (NTSC)	Clock Frequency (PAL)
1	5.95 MHz	5.86 MHz
0	11.9 MHz	11.72 MHz

OTHER CONTROL SIGNALS

HDSEL	VGCA Input	R/PB	Operation Mode
0	SPIN	0	Playback
1	PBIN	1	Record

SERIAL PORT CONTROL SIGNALS

GCA CONTROL SIGNAL

$B_3B_2B_1B_0$	GAIN(dB)	$B_3B_2B_1B_0$	GAIN(dB)	B_3 B_2 B_1 B_0	GAIN(dB)	B_3 B_2 B_1 B_0	GAIN(dB)
0 0 0 0	0	0 1 0 0	4.27	1 0 0 0	8.53	1 1 0 0	12.8
0 0 0 1	1.07	0 1 0 1	5.33	1 0 0 1	9.60	1 1 0 1	13.9
0 0 1 0	2.13	0 1 1 0	6.40	1 0 1 0	10.7	1 1 1 0	14.9
0 0 1 1	3.20	0 1 1 1	7.47	1 0 1 1	11.7	1 1 1 1	16.0

VGCA CONTROL SIGNAL

$B_7B_6B_5B_4$	GAIN(dB)	B_7 B_6 B_5 B_4	GAIN(dB)	B_7 B_6 B_5 B_4	GAIN(dB)	B_7 B_6 B_5 B_4	GAIN(dB)
0 0 0 0	0	0 1 0 0	4.0	1 0 0 0	8.0	1 1 0 0	12.0
0 0 0 1	1.0	0 1 0 1	5.0	1 0 0 1	9.0	1 1 0 1	13.0
0 0 1 0	2.0	0 1 1 0	6.0	1 0 1 0	10.0	1 1 1 0	14.0
0 0 1 1	3.0	0 1 1 1	7.0	1 0 1 1	11.0	1 1 1 1	15.0

OTHER CONTROL SIGNAL

B8	CLK Frequency	B9	RECPILOT OUT
0	5.95MHz	0	Normal*
1	11.9MHz	1	ON

* Normal means ON in Record Mode and OFF in Playback mode.

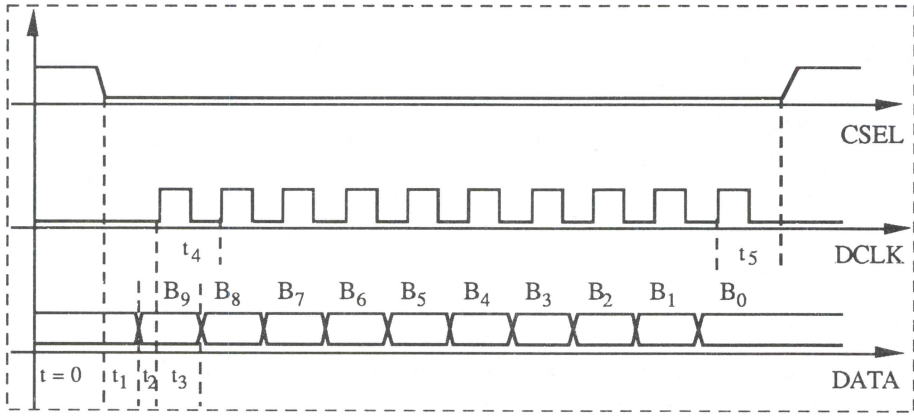


Figure 1. ATF Serial Port Timing Diagram

SERIAL PORT MINIMUM TIMING REQUIREMENT

Name	Time	Unit
t1	500	ns
t2	200	ns
t3	200	ns
t4	1000	ns
t5	500	ns

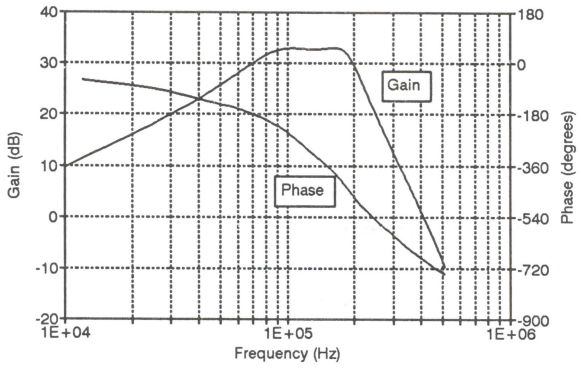


Figure 2. ATF Filter Response

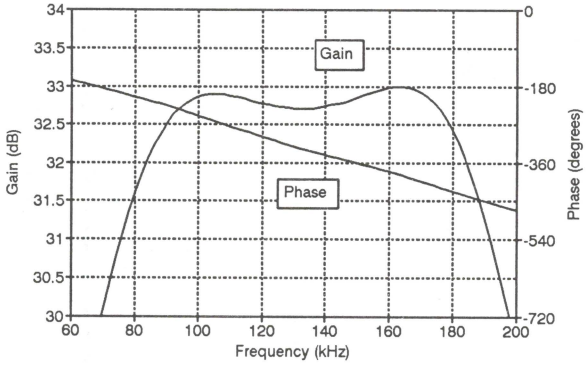


Figure 3. ATF Filter Response (detail)

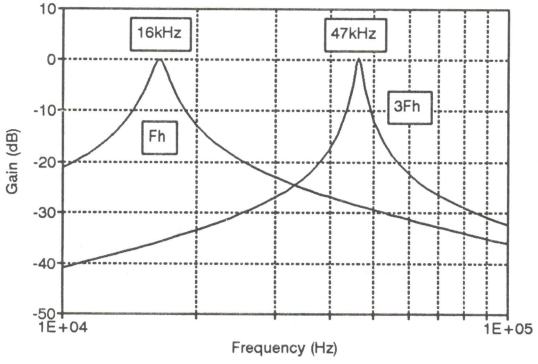


Figure 4. Fh & 3Fh Filter Response

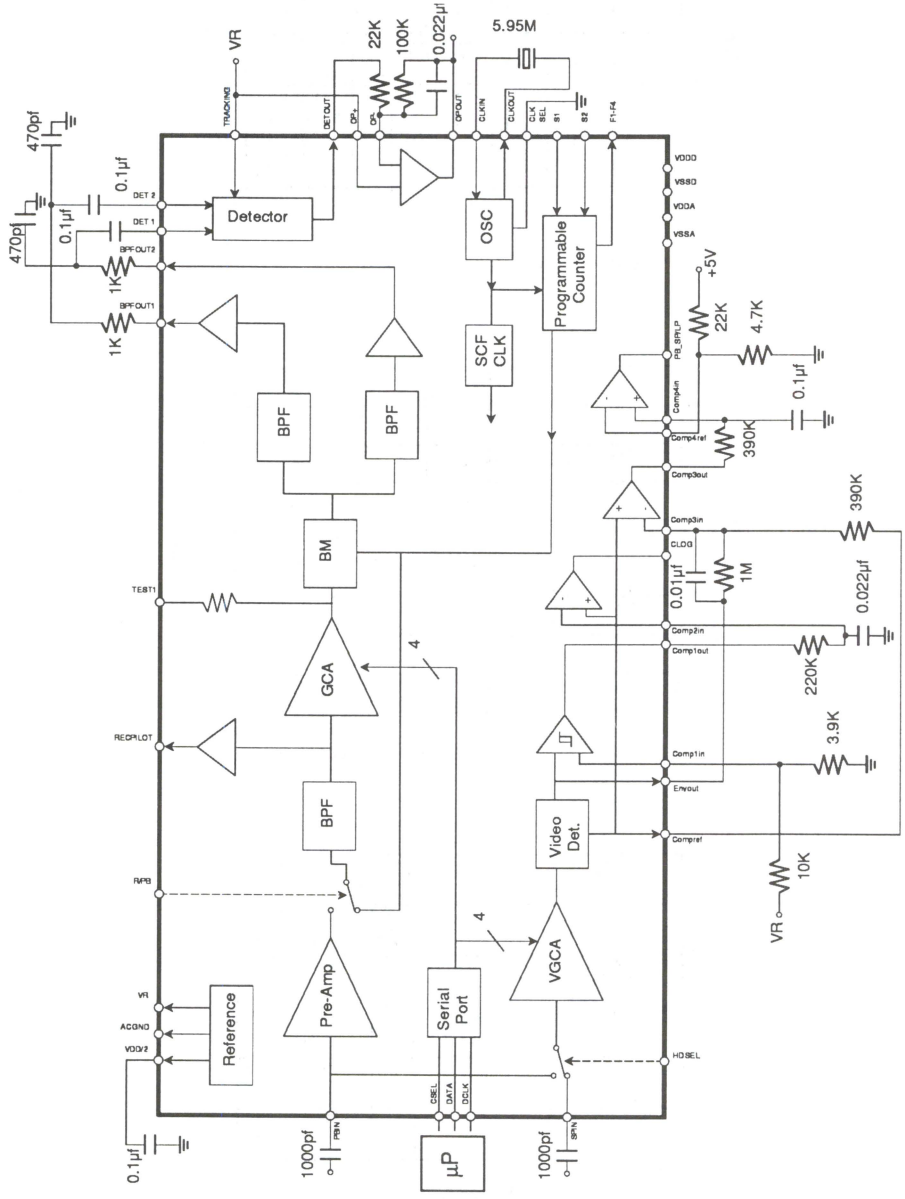


Figure 5. Block Diagram and System Schematic

Microprocessor Support IC

GENERAL DESCRIPTION

The XR-8000 provides simplicity in monitoring of microprocessor controlled systems. The features included in XR-8000 are: on-board 5V/50mA voltage regulator, undervoltage reset, delay reset on powerup, watchdog monitor, short circuit protection and low quiescent current.

The on-board regulator will provide power for all supporting logic and memory circuitry up to 50mA load current. Hence, low power systems will not require a separate voltage regulator IC, which will provide system cost savings.

The low voltage detect level is internally set to 4.4V. It is also externally adjustable with an addition of one external 1MΩ potentiometer. The recommended capacitor value for both external timing capacitors is 0.1uF. With the recommended capacitor values, the nominal turn-on delay time and the oscillation period of the internal oscillator will be 90msec and 65msec, respectively. Both the XR-8000 and XR-8001 (inverted reset) are available in 8 pin PDIP.

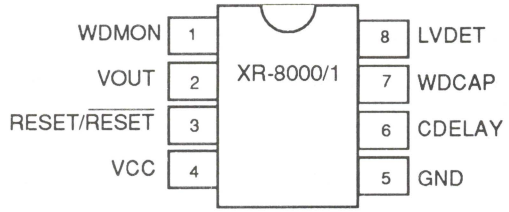
FEATURES

Powerup reset with adjustable delay.
Undervoltage reset with adjustable level.
Watchdog monitor with adjustable timeout period.
5V/50mA on board regulator.
Internal current limit.
7V to 24V supply voltage operating range.
RESET or $\overline{\text{RESET}}$ output.

ABSOLUTE MAXIMUM RATINGS

VCC		-0.3V to 26V
VOUT		-0.3V to 7V
Reset/$\overline{\text{Reset}}$ Output		-0.3V to 26V
Operating Temperature Range		-40°C to +85°C
Package Type		8 PIN PDIP
Power Dissipation	8 PIN PDIP	750mW @ 25°C
		300mW @ 85°C
Storage Temperature Range		-65°C to +160°C
Lead Temperature (soldering 10 sec.)		300°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8000IP	8 pin PDIP	-40°C to +85°C
XR-8001IP	8 pin PDIP	-40°C to +85°C

SYSTEM DESCRIPTION

Fig.1 shows the block diagram for the XR-8000, Fig. 2 shows the timing diagram for the pins of interest and Fig. 3 shows an applications circuit. Whenever the regulator output drops below 4.4 volts, the RESET pin is pulled high. At the same time, the delay and the watchdog oscillator capacitors are discharged (reset). When the regulator output voltage returns above 4.5 volts, the delay capacitor starts charging up and provides 90msec delay time before the RESET pin is returned to its low state. At the same time when the RESET switches from high to low, the WDCAP capacitor starts charging. The microprocessor has 90msec to provide a positive going pulse on the WDMON pin before a reset signal is issued. In absence of the pulse on the WDMON pin, the RESET pin will continue to issue reset pulses (controlled by the watchdog oscillator) until the microprocessor issues a pulse on the WDMON pin. The microprocessor needs to issue at least one pulse every 65msec to prevent the RESET pin from issuing a reset signal. The RESET pin is also delayed by 90msec during powerup. See Fig. 2 for timing diagrams.

ELECTRICAL SPECIFICATIONS:

Vin=14V, Iout=5mA, CDELAY=0.1µF, WDCAP=0.1µF, CL=1µF, T_A=25°C unless otherwise specified. RESET output specs apply to RESET output.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
REGULATOR						
VOUT	Output Voltage	4.65	5.0	5.35	V	IL = 50MA
IOUT	Output Current	50	75		MA	VOUT>4.65V
ICC	Supply Current		600	800	µA	IL=0
IMAX	Short Circuit Current Limit	50	120	200	MA	VOUT=0V
WATCHDOG						
VLDT	Low Voltage Detect Threshold	4.25	4.40	4.55	V	RL(RESET)=10K
VLDH	Low Voltage Detect Hysteresis		20		MV	RS(RESET)=10K
IWD	WDMON Input Current		350	500	µA	VWDMON=5V
			120	175	µA	VWDMON=2.4V
			12	17	µA	VWDMON=.8V
VWD	WDMON Threshold	0.8	1.6	2.4	V	
V_{reset}	VRESET		.25	0.4	V	IRESET=1MA
I_{reset}	IRESET	1.0	2.0		MA	VRESET=.4V
I_{leak}	IRESET (LEAKAGE)		.05	1.0	µA	VRESET=5V

AC SPECIFICATIONS:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
WATCHDOG						
tPUD	Powerup Reset Delay		90		MSEC	VWDMON=5V
TOSC	Reset Oscillation Period		65		MSEC	VWDMON=.8V
tRPW	Reset Pulse Width		2.0		MSEC	VWDMON=.8V
t_f	Reset Fall Time		0.8		µSEC	RL(RESET)=10K
t_r	Reset Rise Time		0.5		µSEC	RL(RESET)=10K
t_{reset}	Reset Delay		90		MSEC	PW=5USEC
tWDPW	WDMON Pulse Width	5			µSEC	(NOTE 1)
TWD	WDMON Period			90	MSEC	PW=5USEC

NOTE 1: Pulse widths less than 5µsec, down to 1µsec, can be used with at least two pulses issued in one RESET oscillation period.

SYSTEM DESCRIPTION (cont.)

For systems with power supply rise time greater than 90msec, the powerup delay time (DELAY cap.) should be increased to allow the supply to reach its final value before the RESET pin is released.

The delay time on powerup is set by an external capacitor (CDELAY) and an internal current source. Similarly, the oscillator frequency is set by an external capacitor and two internal current sources. Thus, the powerup reset delay and the watchdog oscillation frequency can be set by selecting proper external capacitor values to conform to the system requirements. The following equations define the relationship between the external component values and the desired parameters:

Powerup Delay Time(nominal) = K1CDELAY,
where K1 = 900msec/μF

Watchdog Oscillator Period(nominal) = K2CWD,
where K2 = 650msec/μF

Reset Pulse Width = K3CWD
where K3 = 20msec/μF

K1, K2 and K3 constants will have manufacturing tolerances associated with standard IC fabrication techniques. The low voltage threshold level will also have a tolerance proportional to the internal bandgap reference. The nominal value of the bandgap reference is 1.2V ± 40mV. As a result, the low voltage threshold level will have ± 3.3% tolerance (neglecting resistor matching tolerance). To obtain better accuracy, a 1 MegΩ trim pot, connected between regulated output and ground with the wiper arm connected to the LVDET pin, can be used and adjusted until the desired threshold voltage level is obtained.

The watchdog monitor pulse width (issued by a microprocessor) is restricted by the WDCAP discharge time and will be proportional to the WDCAP capacitor value. The WDCAP voltage waveform, shown in Fig. 2, shows the WDCAP being discharged to its reset level during each WDMON pulse. This will be true if WDMON pulse widths are 5μsec or greater with WDCAP capacitor value of 0.1μF. As the WDMON pulse width is reduced, the WDCAP low voltage level will start to rise. Therefore, the WDMON pulse frequency needs to be increased to prevent the WDCAP voltage from reaching its upper threshold level. Inversely, if the WDMON capacitor value is increased, the WDMON pulse width needs to be increased proportionally. The following equation defines the relationship between the WDCAP capacitor value and minimum WDMON pulse width.

PW(min) = K4WDCAP
where K4 = 50 μsec/μF

Due to propagation delay times, the minimum pulse width is restricted to 500nsec. When the pulse width becomes significant with respect to the RESET OSCILLATION PERIOD, the WDMON period can be increased by the same amount as the pulse width. For example, with the nominal capacitor values and 20 msec WDMON pulse width, the WDMON period can be increased by 20 msec. One should keep in mind that when a long WDMON pulse width is used, the total RESET DELAY time will be increased by the amount of the pulse width. This feature provides an advantage for obtaining an increase in the RESET DELAY time without increasing the WDCAP capacitor value.

The XR-8000 can be used in any system that requires voltage level monitoring, with or without microprocessor controller. The XR-8001 has identical specifications as the XR-8000 with the RESET pin providing an inverted RESET function. The watchdog function can be defeated by connecting the WDMON pin through a 10K resistor to the VOUT pin on either the XR-8000 or XR-8001 IC.

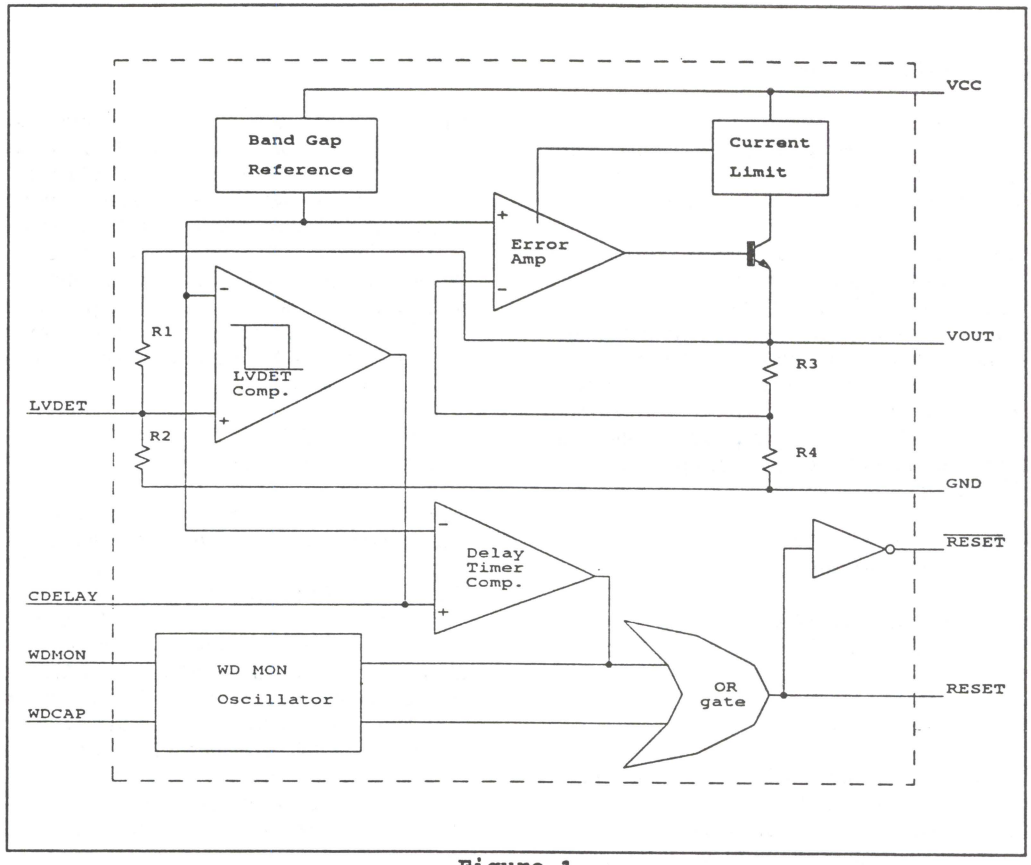

VCC
Band Gap
Reference
Current
Limit
Error
Amp
R1
LVDET
Comp.
VOUT
R3
LVDET
R2
R4
GND
Delay
Timer
Comp.
RESET
CDELAY
WDMON
WD MON
Oscillator
OR
gate
RESET
WDCAP

Figure 1

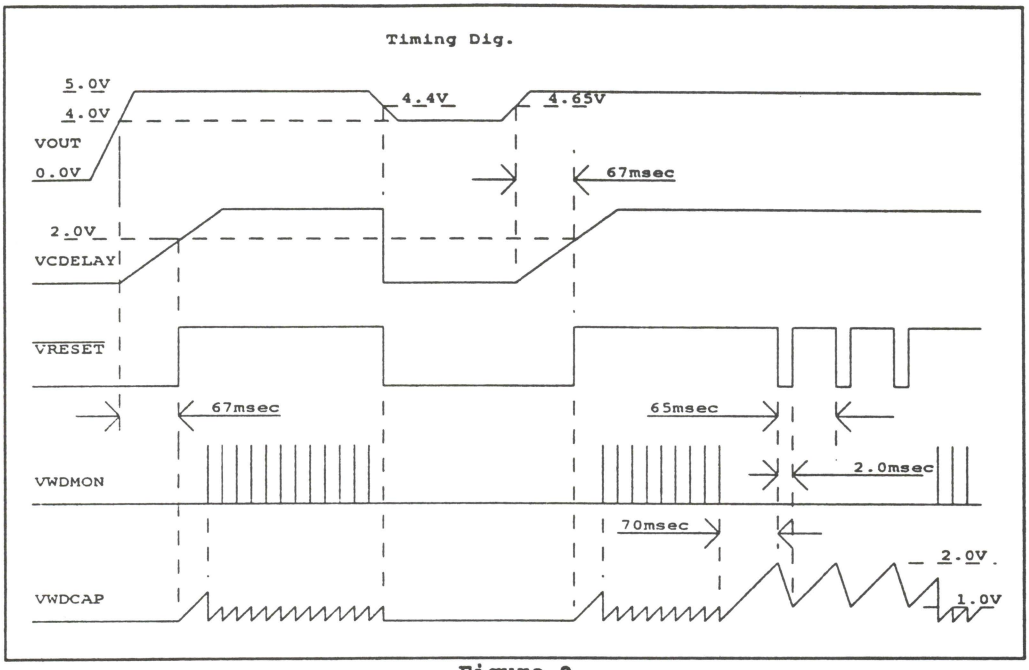


Figure 2

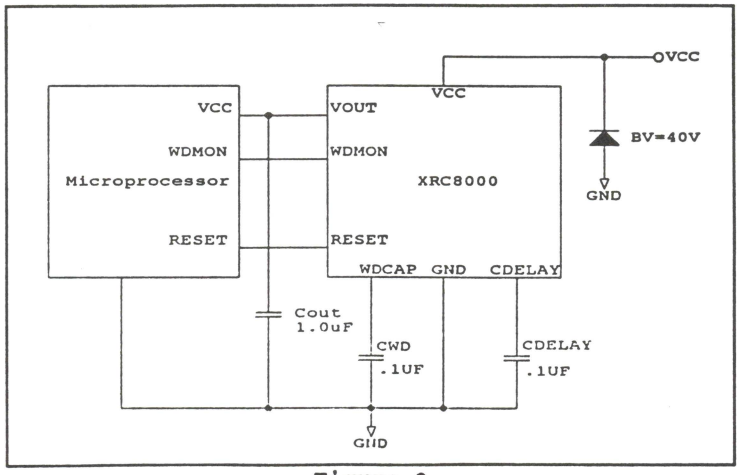


Figure 3



NOTES



Preliminary Information

Micropower Step-up Switching Regulator

GENERAL INFORMATION

The XR-8073 is a bipolar micropower switching regulator designed specifically for low voltage battery powered instruments where high efficiency and minimum size are crucial. The extremely low minimum input voltage gives the device the unique ability to boost single-cell battery voltages. The XR-8073 contains a 172mV temperature compensated voltage reference, a voltage comparator, a gated oscillator, low voltage detection circuitry, and an internal 250mA switch transistor required to make a complete low power switching regulator.

The XR-8073 regulator is available in 8-pin plastic SO and DIL packages for use over the commercial and industrial temperature ranges.

FEATURES

- No Design Required
- +0.9V to +20V Operation
- 100µA Quiescent Current
- Low Component Count
- Remote Shutdown / Power-Down Capability
- On-Board Low Battery Detector
- Adjustable Output Voltage Level
- Same Pin Assignment as Raytheon 4191/2/3

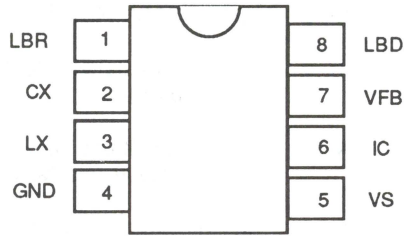
APPLICATIONS

- Battery Powered Systems
- Single-Cell or Multi-Cell Portable Equipment
- Pagers, Cameras, & Cellular Telephones
- Laptop, Palmtop, & Pocket Computers
- High Efficiency DC to DC Converters

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	20V
Power Dissipation (package limitation)	
8 Pin PDIP package	400mW
8 Pin SO package	300mW
Storage Temperature	-65°C to +150°C
Maximum Input Voltage	VS +0.3V
Minimum INput Voltage	GND -0.3V

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8073CP	8 Pin DIP	0°C to +70°C
XR-8073CD	8 Pin SO	0°C to +70°C
XR-8073IP	8 Pin DIP	-25°C to +85°C
XR-8073ID	8 Pin SO	-25°C to +85°C

SYSTEM DESCRIPTION

The XR-8073 is a gated-oscilliator implementation of the standard step-up switching regulator architecture. The benefit of this implementation is low supply current since the switch is gated off much of the time.

Operation of the XR-8073 can be understood by examining the voltage regulating loop of Fig.1. A fraction of the output voltage divided by resistors R4 and R5 is compared to the 172mV reference by comparator A1. When this voltage is lower than Vref, the comparator activates the oscillator by turning on its bias current. Output pulses from the oscillator are passed through a driver stage to the base of the power switch Q1 which drives inductor L1 with a series of pulses at the frequency and duty cycle of the oscillator. During the closed time of switch Q1, L1 stores energy as magnetic flux within its core. When Q1 opens, the energy is transfered through diode D1 to capacitor C2 where it is stored in the form of charge. As the stored charge on C2 increases with subsequent pulses, output voltage rises. When the output voltage reaches a level such that comparator A1 sees a voltage greater than the 172mV reference, bias current to the oscillator is disconnected and Q1 is left open. During this time, capacitor C2 provides current to the load. When voltage across C2 eventually drops below the regulated value, the cycle will be repeated.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
1	LBR	I	**Low Battery Set Resistor.** A voltage less than 170mV at LBR wil activate the LBD output
2	CX	I	**Oscillator Timing Capacitor.** An external capacitor connected between OX and ground sets the frequency of oscillation.
3	LX	O	**External Inductor.** Open collecter output of the internal power switch transistor.
4	GND	P	**Ground.**
5	VS	P	**Supply Voltage.**
6	IC	I	**Bias Set Current (10μA).** Current into this pin activates the regulator. With supply voltages less than 1.5V, connect directly to VS.
7	VFB	I	**Feedback Voltage.** A DC voltage less than 170mV at this pin enables the oscillator and switch driver.
8	LBD	O	**Low Battery Detector Output.** Open collector output of the low battery detector. Active low.

BIAS GENERATOR

The bias generator generates two voltages to bias various internal current mirrors at a current level independent of supply voltage and temperature. The generator is activated by a current into the IC (pin 6) input. This current is determined by an external resistor connected between IC and VS (pin 5). The minimum value for the current is 5mA, the maximum 50mA, and the optimum value 10mA. The correct value for the external resistor is calculated from:

$$R_6 = \frac{V_S - 1.5V}{10\mu A}\ \Omega$$

IC (pin 6) can be connected directly to the supply voltage if VS is less than orequal to +1.5V.

POWER DOWN MODE

IC can also be used as a power-down control input. Removing the current to IC disables the regulator and current consumption is dropped to 15μA.

BANDGAP VOLTAGE REFERENCE

A temperature compensated reference voltage of 172mV is generated by the bandgap voltage reference. This voltage is used as reference voltage at the output voltage feedback and low battery comparators.

COMPARATOR

A fraction of the regulated output voltage at VFB (pin 7) determined by external resistors R4 and R5 is compared to the internal reference voltage by comparator A1. When the VFB voltage is lower than the reference voltage, the output of the comparator is high and the bias current of the oscillator is on. Otherwise, the comparator output is low and the oscillator bias current is switched off, disabling the oscillator. In this way R4 and R5 are used to control the output voltage level according to:

$$V_{OUT} = (1 + R4 / R5) (0.172) V$$

ELECTRICAL CHARACTERISTICS : VS = +1.25VDC, T_A = +25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GENERAL CHARACTERISTICS						
VS	Supply Voltage	0.9		20	V	Operating
		1			V	Start-up
I_S	Supply Current		100		µA	I_{switch} = 0
			15	40	µA	Disabled
V_{REF}	Internal Reference Voltage		172		mV	
eff	Efficiency		TBD		%	
$\Delta V_O/\Delta VS$	Line Regulation		TBD		mV/V	
$\Delta V_O/\Delta I_O$	Load Regulation		TBD		mV/MA	0 to 50 mW load
OSCILLATOR						
F_O	Operating Frequency			75	kHz	
%On	Switch Duty Cycle	75		85	%	
$-I_{CX}$	Capacitor Charcing Current		3		µA	
$+I_{CX}$	Capacitor Discharging Current		12		µA	
$-V_{TH}$	CX-Threshold Voltage		0.20		V	
$+V_{TH}$	CX+Threshold Voltage		0.32		V	
BIAS / SWITCH / FEEDBACK / LB CURRENT						
I_{IC}	IC Input Bias Current	5	10	50	µA	
I_{SW}	Switch Current	150			mA	V_3=250mV
I_{fb}	Feedback Input Current			0.05	µA	
I_1	Low Battery Bias Current			0.1	µA	V_7=170mV
I_{LBO}	Low Battery Output Current	100	300		µA	

5

OSCILLATOR

The oscillator consists of two comparators, a threshold voltage generator, and a charging / discharging current generator. The voltage of external capacitor C3 connected to CX (pin 2) is compared to an internal threshold voltage of VTH. When the voltage at CX is lower than VTH, the capacitor is charged by a current of approximately 3mA. When the voltage of the capacitor reaches VTH, the threshold voltage is switched to a lower value and the capacitor is discharged by a current of 12mA. Discharging goes on until the capacitor voltage reaches VTH which is then switched back to the higher value, and a new cycle begins. Voltage difference between the low and high threshold values is approximately 0.12V. The 1:4 ratio of the charging and discharging currents results in an oscillator duty cycle of 4:1 (switch-on/switch-off). Approximate frequency of the oscillation can be calculated from:

$$F_{OSC} = \frac{1}{50000\ (C3)}\ H_Z$$

DRIVER

The output pulses of the oscillator are passed to a driver stage which providesthe output power transistor with sufficient base current to ensure saturation at all current levels. The driver stage is adaptive in such a way that the power transistor is always only saturated to a point where its current gain drops approximately to 50. This results in a good efficiency since no current is wasted for unnecessarily hard driving of the output transistor.

LOW BATTERY DETECTOR

The low battery detector consists of a comparator which compares the voltage at LBR (pin 1) to the internal reference voltage and, when the voltage at LBR is lower, outputs a logic "0" at the open-collector output LBD (pin 8). The low battery voltage limit is set by two external resistors, R1 and R2, to a value calculated from:

$$V_{LB} = (\ 1 + R1 / R2\ )\ (0.172)\ V$$

The low battery indicator has a large hysteresis dependent of R1. With R1 = 330k, the hysteresis is approximately 1V.

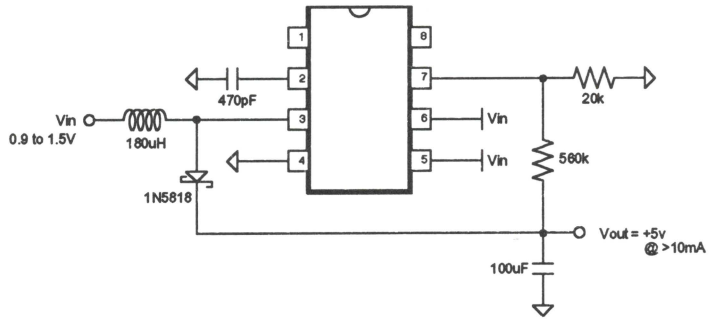


Figure 1. Typical Application Schematic

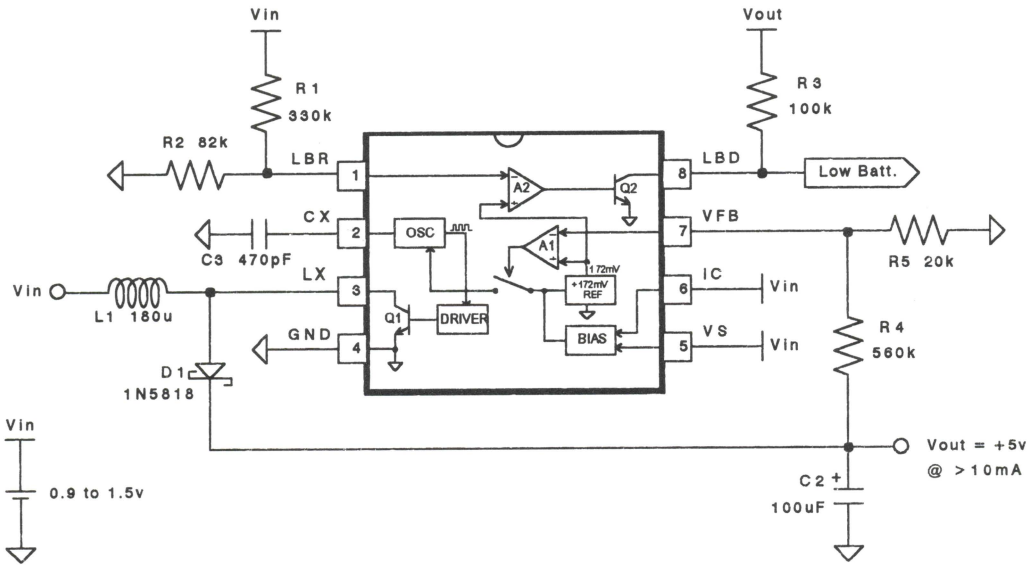


Figure 2. Block Diagram and System Schematic



NOTES



A Square Wave to Sine Wave Converter Using the XR-1015

Application Note

INTRODUCTION

In the world of microprocessors and digital logic control, there is still the need for a synchronized sinusoidal source. For many applications, this was done using a digital-to-analog converter and EPROM with the sine values sequentially selected. This required microprocessor time, as well as two relatively large components to be added to the system.

A synchronized sine wave can be obtained with an XR-1015 Seventh Order Elliptic Low Pass Filter and a single 74LS390 dual divide-by-10 counter. A single clock controls the frequency of the sine output, which can be controlled by the microprocessor using an on-chip timer, or with a digitally programmable counter accessed by the microprocessor data bus. The total harmonic distortion obtained in such a system is less than –60dB (0.1%) from 20Hz to 20kHz, excluding the sampling clock frequency.

PRINCIPLES OF OPERATION

The XR-1015 is a seven pole, six-zero elliptic low pass switched capacitor filter. With its greater than 70dB of stop band rejection, the XR-1015 has the capability of reducing the amplitude of all out-of-band harmonics by a substantial amount.

The 74LS390 is a dual divide-by-10 counter. With the intermediate divide-by-5 and divide-by-2 points made available on the device, it can be wired to perform the divide-by-50 function needed for the dividie-by-2 output of the XR-1015, to create the square wave at the frequency of interest.

Figure 1 shows the basic circuit with its single clock input from the microprocessor applied to the XR-1015. The divide-by-2 output of the XR-1015 is then clamped to –0.7V to +5V and applied to the input of the 74LS390. This divider provides the divide-by-50 clock that is applied to the filter input of the XR-1015.

The clock-to-corner ratio of the XR-1015 is set at 100:1 which allows the corner frequency of the low pass filter to track the square wave input signal. The seven pole, six-zero elliptic low pass filter response of the XR-1015 reduces any harmonics from the applied signal providing a low distortion audio range sine wave at the output.

Figure 2 shows the harmonic content of the sine output at the XR-1015 when clocked at 2kHz (sine output at 20Hz). The total harmonic distortion is –53dB. The lower side band created by the sampled system is –40dB below the fundamental, and should not be a factor in most applications. If needed, an inprecise RC continous-time active filter could be added to the output with the corner controlled by switching in different resistor values.

Figure 3 shows the harmonic content of the sine output with the XR-1015 clocked at 2MHz (sine output at 20kHz). The total harmonic distortion is near –60dB. This low distortion signal allows the sine output to be used for microprocessor controlled test equipment for the evaluation of distortion on tape recorders or telephone lines.

When single supply +5 VDC operation is desired, Figure 5 should be used. This circuit still performs the square wave to sine wave conversion. The harmonics in this case are attenuated by –50dB (0.3%) allowing the circuit to be used for tone generation for the evaluation of telephone lines.

CONCLUSION

The phase relationship, which can be important in many applications (network analysis) is shown in Figure 4. The phase shift from the input of the XR-1015 to the output is a constant –50 degrees, as would be expected, since the corner frequency of the filter moves with the input frequency of the filter. Because of this, the system can be used for phase measurements for test instrumentation. With this circuit, a simplified synchronized sine wave can be provided where before a complicated digital-to-analog converter and EPROM was needed.

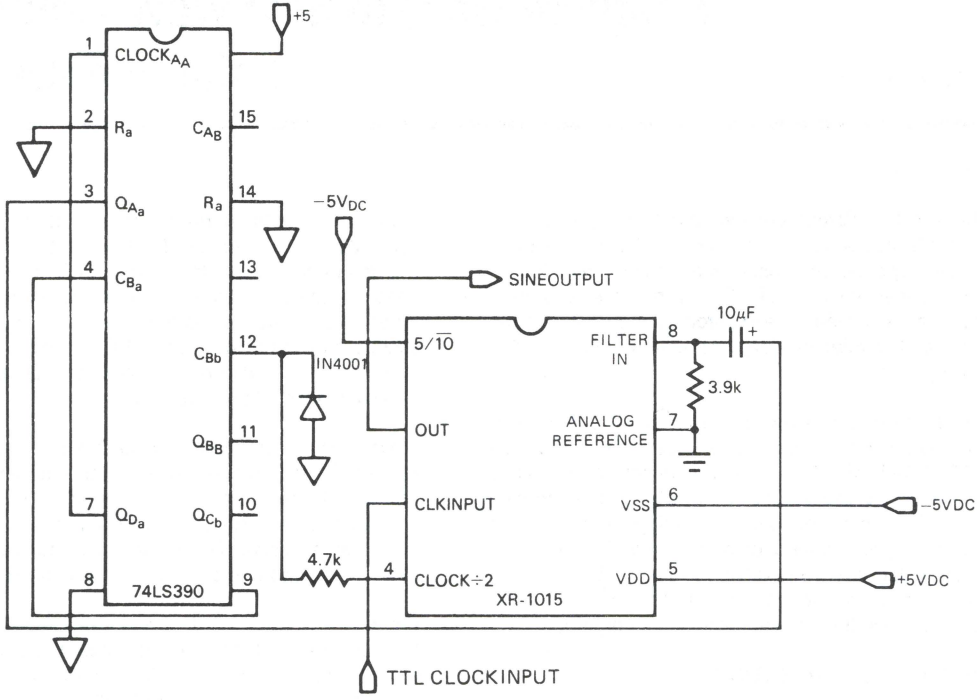


Figure 1. Basic Circuit — Single Clock Input

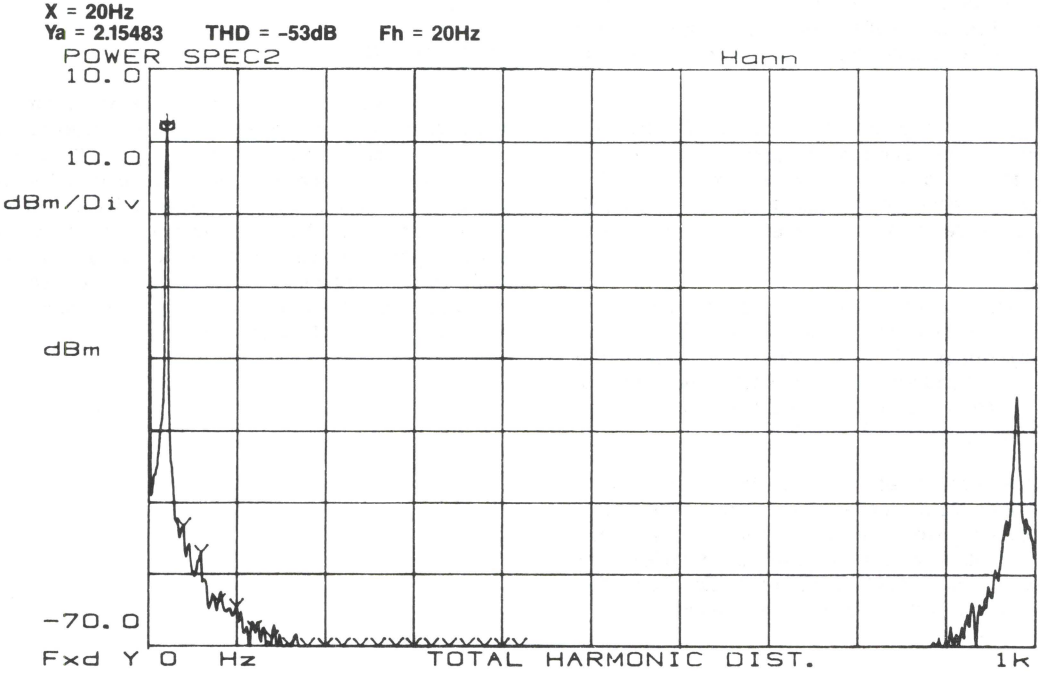


Figure 2. Harmonic Content of Sine Output

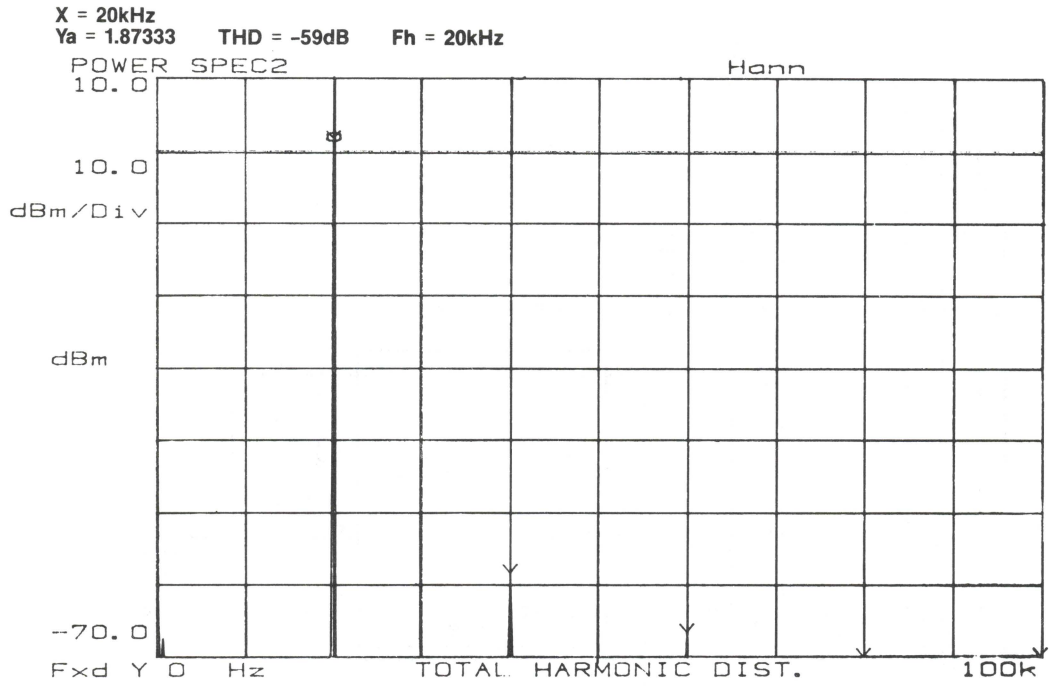


Figure 3. Harmonic Content of Sine Output

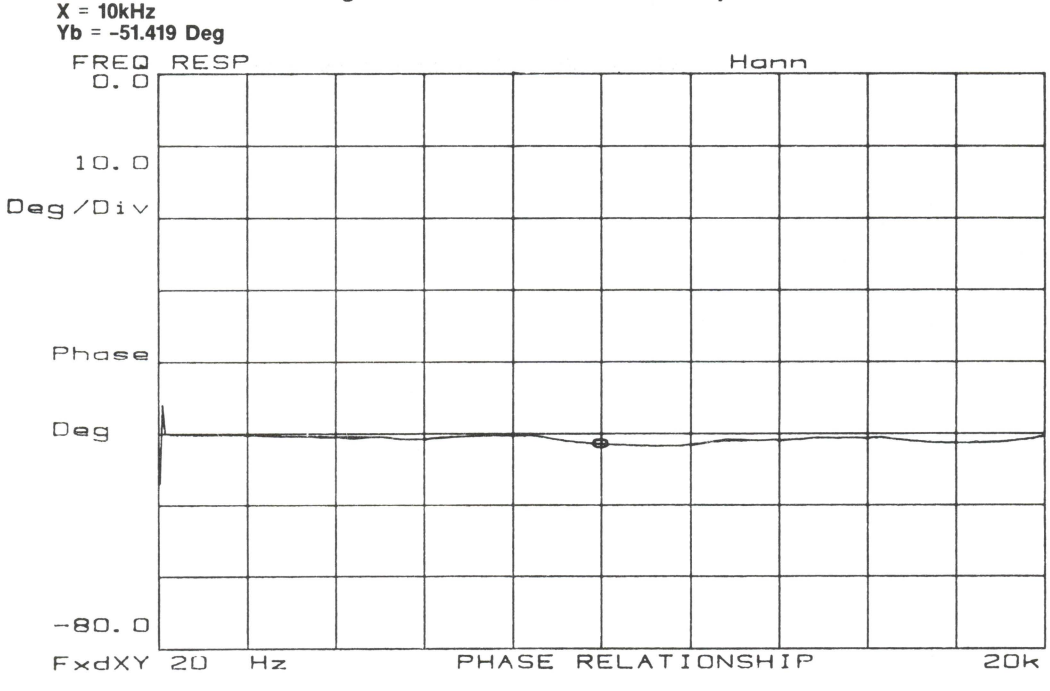


Figure 4. Phase Relationship Input to Output from 20Hz to 20kHz

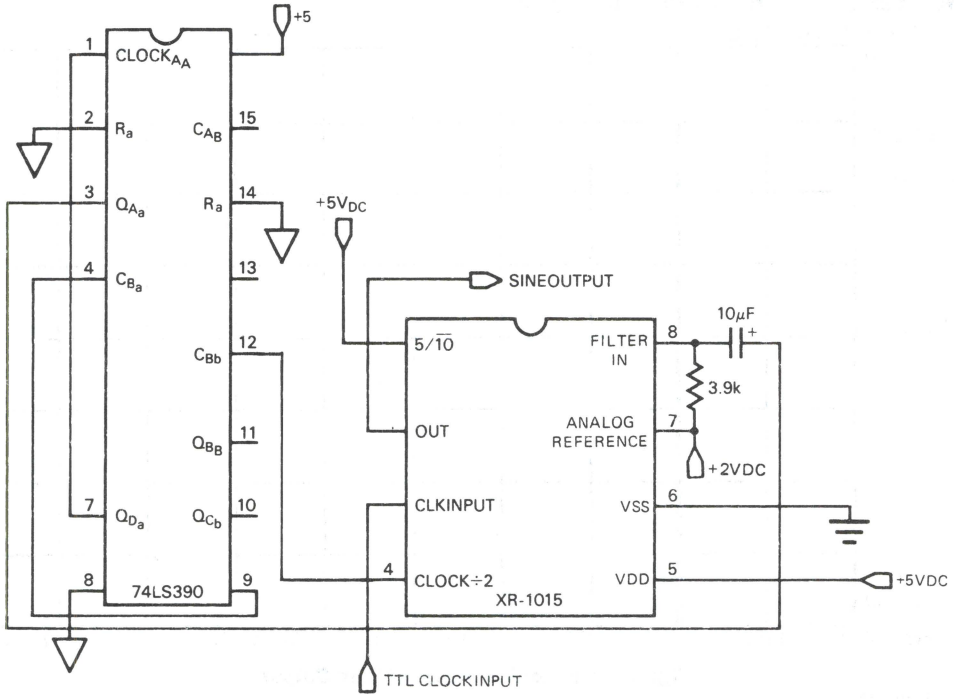


Figure 5. Basic Circuit — Single Clock Input, Single Supply

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STRATEGIC CAPABILITIES

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SECTION 6

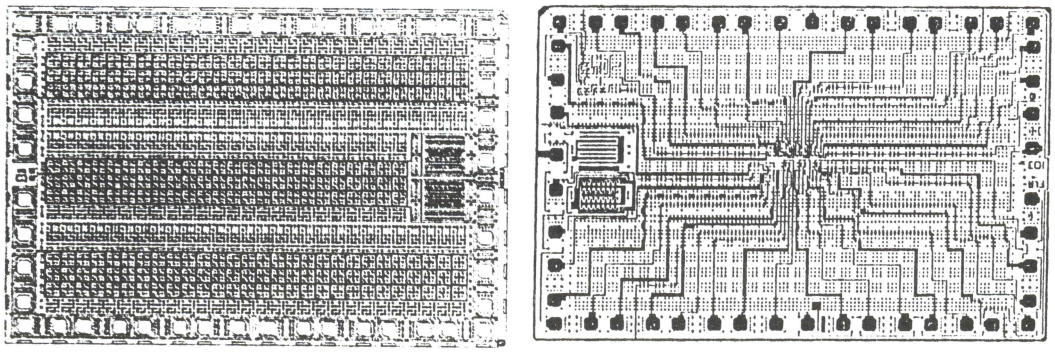
BIPOLAR SEMI-CUSTOM DESIGN CONCEPT

Traditionally, the development of custom IC's has been a long and costly undertaking. The development time would normally run in excess of one year, design changes were slow and costly, and it usually took a long time to get from the prototype stage to full production. Because of these difficulties, the use of custom IC's could be economically justified only when a very large quantity of circuits, i.e., several hundred-thousand units, were required during the life of the end product. In the past, these drawbacks have severely limited the use of custom monolithic IC's.

The bipolar semi-custom design concept, pioneered by EXAR, now overcomes this traditional problem. EXAR makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection, which metalizes all selected components together in the required circuit configuration. This enables an engineer to design a metal mask which will interconnect the uncommitted components on the prefabricated wafers, and thus convert them into customized chips . This allows one to develop an almost unlimited variety of custom linear or digital integrated circuits at very substantial cost savings.

The semi-custom program is intended for those customers seeking cost effective methods of reducing component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks, at approximately 10% to 20% of the development costs for tooling associated with conventional full custom designs. The semi-custom design concept is an interactive or cooperative development effort between EXAR and the customer. In most cases, the cost and development time for the program can be reduced even further if the customer designs and breadboards their own semi-custom IC, using EXAR design kits, instruction manuals, layout sheets, and/or CAD tools.

The semi-custom design approach is based on a number of standardized arrays with fixed component locations. These arrays contain a large number of undedicated active and passive components (i.e., transistors, resistors, etc.). These integrated components can be interconnected in thousands of different ways with a customized interconnection pattern. Each different metal interconnection pattern creates a new custom IC. The figures below show a magnified photograph of a Flexar array, both in its prefabricated form and after its customization. This method is called semi-custom rather than full custom since only the last layer of tooling is changed to customize an IC chip the rest of the layers are standard. As a result, the development phase is very short and far less expensive compared to conventional full or dedicated custom IC's. Similarly, if a design change or iteration is necessary, it can be readily accommodated within a matter of weeks by simply generating a new or modified interconnection pattern.



Magnified Photograph of a Linear Flexar Beta Chip Before and After Customizing.

STRATEGIC CAPABILITIES

THE FIRST STEP

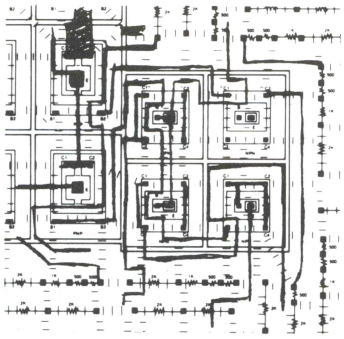
The first step at the start of a semi-custom program, is for the customer to contact EXAR for a preliminary analysis and discussion of needs. This can be done even while the program is still at the thought stage. This initial review by EXAR is performed at no cost to the customer and is essential to the success of the program. It avoids any possible design pitfalls or misunderstandings. This early interaction also allows the customer to find out some of the options or variations available in EXAR's semi-custom programs and choose the ones which are best suited for the design.

The following is required by EXAR's technical staff to provide the customer with an accurate feasibility study of the project, and a budgetary estimate of the development costs, timetables and production pricing.

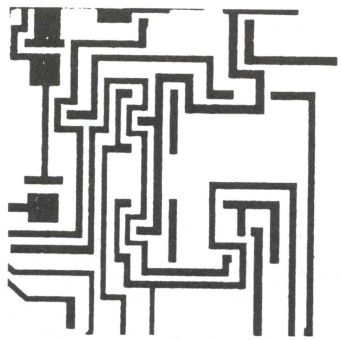
- A block diagram of the circuit function and input/output interface requirements.
- A circuit schematic or logic diagram of your circuit.
- Preliminary or objective performance specifications and limits on critical circuit parameters (also, possible tradeoffs which may be allowed).
- Test specifications
- Packaging requirements.
- Production quantity requirements.
- Desired development and production timetables.
- An indication of how much of the breadboarding, layout, etc., can be done by the customer, using EXAR's Kit Parts or Soft Macros.

Once this data package is submitted, EXAR will review it and respond within a few days.

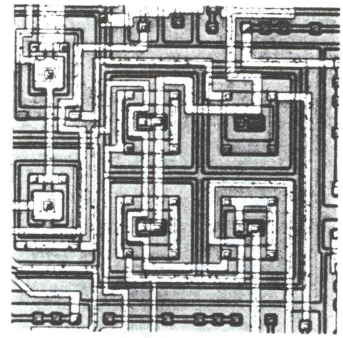
Normally, the test system development effort is initiated in parallel with chip development. EXAR has a complete computer controlled IC test facility and offers complete IC testing capability for production units.



CUSTOMER LAYOUT



METAL MASK



FINISHED CHIP

Steps of Semi-Custom Design

FREQUENTLY ASKED QUESTIONS AND THEIR ANSWERS

Based on EXAR's long experience with semi-custom arrays, a comprehensive glossary of the most often asked questions concerning the program has been compiled. The following is a list of these questions and their answers.

•WHAT IS THE COST OF THE BASIC PROGRAM?

The cost of the semi-custom development program is dependent on the amount of designing and layout completed by the customer. In a basic semi-custom program the customer completes the design, breadboard evaluation and layout on the Flexar worksheet, while the IC tooling and prototype fabrication are completed by EXAR. This is the most economical and cost effective approach.

For bipolar semi-custom designs, the development cost ranges from $15,000 to $30,000. This cost applies for layout and integration of designs submitted by the customer. The customer receives ten prototypes at the completion of the development program.

•WHAT IS THE DEVELOPMENT TIME?

Typical development time for the basic bipolar semi-custom program is four weeks, starting with the customer's layout and ending with the monolithic prototypes. If EXAR is required to do the IC layout or breadboarding evaluation, several additional weeks may be required to complete the development program.

•WHAT IF ADDITIONAL DESIGN CYCLES ARE NEEDED?

If the customer would like to make a modification to the design or layout after evaluation of the initial prototypes, a new design iteration cycle can be completed within 4-6 weeks. Cost for this iteration is dependent on the complexity of the modification.

•WHAT ABOUT PRODUCTION PRICING?

The production pricing of monolithic IC's is dependent upon a number of important factors such as:

a) Flexar array type.

b) Circuit complexity (i.e., yield).

c) Device performance and test requirements.

d) Special environmental screening requirements (burn-in, hermeticity tests, etc.).

e) Package type required.

f) Quantity required.

In the case of a custom IC, it is impossible to anticipate the impact of these factors without detailed knowledge of the circuit and its application. Each custom IC, by definition, has some unique requirement or feature associated with it. After reviewing specific needs, particularly with regard to the circuit performance and quality requirements, EXAR can provide a detailed proposal outlining the development costs and production pricing for a particular circuit.

•WHAT ABOUT THE TESTING OF SEMI-CUSTOM IC's?

EXAR will develop test software and fixtures to provide fully tested production IC's. All production devices receive 100% electrical test and screening to a mutually agreed upon device specification. In addition to the complete electrical testing, all of the production devices are screened by EXAR's Quality Assurance department to assure compliance with the agreed upon Acceptable Quality Level (AQL) standards.

•WHAT ARE THE MINIMUM PRODUCTION QUANTITIES

EXAR also offers turn-key design services for the Beta array series. The minimum annual revenue for Beta array turn-key design projects is $250,000.

STRATEGIC CAPABILITIES

ECONOMICS OF SEMI-CUSTOM DESIGN

In developing either linear or digital custom circuits, one is always confronted with the following key question: for a given product type and production requirement, is it more cost effective to develop a semi-custom IC or full custom IC? Since the functional requirements of each custom IC program vary greatly, there is no general answer to the above question. However, based on EXAR's long experience in both full and semi-custom IC design and the overall production requirements involved, it is possible to establish some sound economic guidelines for choosing the most cost effective approach.

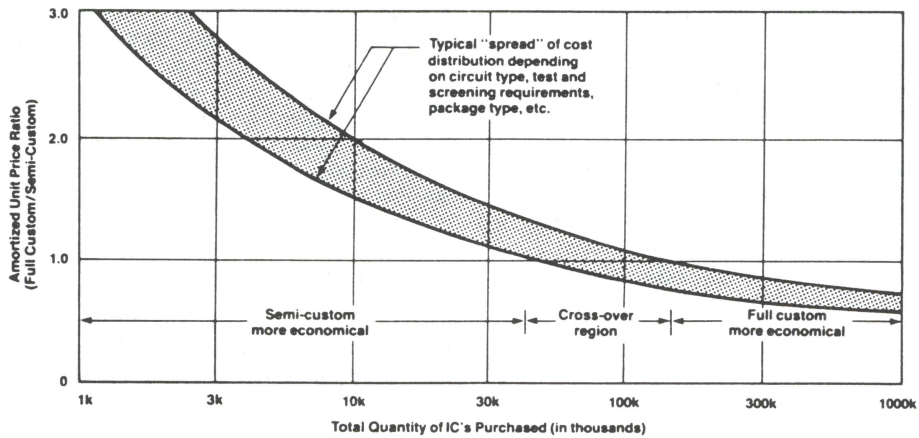
COST FACTORS INVOLVED

Any custom IC development, whether full or semi-custom, involves similar types of cost factors. These a re:

1. Non recurring engineering (NRE) or development costs.
2. Cost or unit price of the product in production quantities.

In the case of monolithic IC's, particularly those which have relatively limited production volume, the development costs may be a significant factor in the cost of the end product. Therefore, when discussing the economics of custom IC's for medium to low production quantities, it is best to consider the cost tradeoffs in terms of the amortized unit price of the IC at a given production volume. This amortized unit price is defined as the actual cost of each unit including its share of the development cost. As an example, a full custom IC may cost $50,000 to develop, and may be priced at $2.90 each at a 50,000 piece total production level. In this case, the actual amortized unit price including development costs would be $2.90 plus $1.00, or $3.90. Similarly, an equivalent semi-custom IC may cost $5,000 to develop and be priced at $3.20 each, with the same 50,000 piece production level. Here the amortized per unit price would be $3.30, or approximately 20% less than a full custom unit price.

The figure below is a comparative graph of the amortized unit price for a typical full custom design, versus the equivalent in semi-custom form at various production quantities. For comparison purposes, the relative ratio of the amortized unit price is plotted along the vertical axis. If this ratio is greater than 1.0 then the semi-custom method is the more cost effective solution.



TYPICAL COST VS. QUANTITIY COMPARISON OF FULL CUSTOM AND SEMI-CUSTOM DESIGNS

NO TWO IC's ARE THE SAME

By definition, each custom IC type is unique. Therefore, the cost comparison curve on the previous page is shown as a spread rather than a single line. This is because, in addition to the production quantity, the cost of monolithic IC's is also dependent upon the circuit complexity, special test requirements and the IC package type.

The key information contained in the relative cost vs. quantity figure can be summarized as follows:

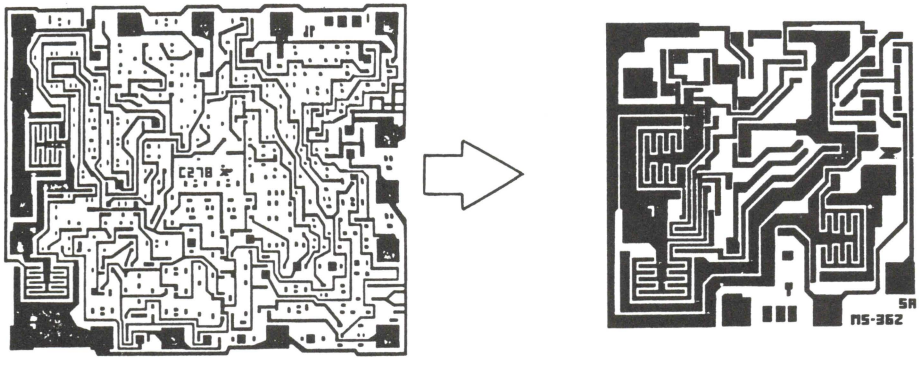
1. For a total production requirement of 50,000 pieces or less, the semi-custom approach is definitely the most economical.

2. For a production requirement of 200,000 pieces or more, the full custom design is more cost effective.

3. For production quantity requirements in the 50,000 to 200,000 piece range, the crossover point for the most economical approach will depend strongly on the specifics of a particular IC function. i.e., special testing, environmental screening, and package requirements.

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

EXAR can offer you the combined advantages of semi-custom and full custom design programs. This is because EXAR has complete semiconductor manufacturing facilities. This unique capability allows EXAR to start a custom development program using a combination of semi-custom arrays during the initial phases of a customer's product. This method allows the customer to take full advantage of the low tooling cost and short development cycle. As the product matures and its market expands (resulting in higher volume production run rates), EXAR can convert the multiple semi-custom chip approach into a single custom IC, thus achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced. This IC design approach has been proven; production is "debugged" and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC can be phased out while the full custom IC is being phased in.



SEMI-CUSTOM DESIGN AND ITS FULL CUSTOM EQUIVALENT

STRATEGIC CAPABILITIES

SEMI- AND FULL CUSTOM COMBINATION: THE TWO-STEP DEVELOPMENT

In many custom development programs one is faced with very short development times and a rapid transfer into high volume production. Such a requirement does not leave room for lengthy development and design changes, or iteration cycles associated with conventional full custom IC design.

EXAR provides a complete custom solution by offering full and semi-custom design capabilities and a complete wafer fabrication facility.

With the combination of these two technologies, the customer has the best of both worlds . The quick turnaround advantage of semi-custom arrays provide prototypes and initial production units, while the subsequent full custom design provides cost savings at high volume production. During this transition, the customer is assured of a continuous flow of product through his production line.

In such a two-step development, the semi-custom prototypes often serve as a monolithic breadboard to optimize and debug the final design. This allows design iterations or changes to be made quickly and inexpensively. In fact, the only difference between a semi-custom and full custom chip is the actual size of the silicon chip.

Once the design is satisfactory, conversion of a semi-custom to a full custom chip is very straight forward and relatively risk free. EXAR simply removes the unused electrical components from the chip to reduce the chip size and passes the resulting cost savings on to the customer in the form of a reduced unit price.

The two-step development capability, i.e., start as semi-custom and finish as full custom, is a very powerful design technique. It avoids the risks associated with a conventional black box type of custom design where one does not know until the very last day of development whether the circuit works or if it can be manufactured.

The two-step program is faster and less expensive than the conventional full custom development, it avoids costly, lengthy design iterations and modification cycles. In addition, it gives the customer a very high degree of assurance that the final full custom unit will work the first time.

ADVANTAGES OF SEMI-CUSTOM DESIGN	
Significant lower costs	Hybrids and discretes are quite expensive as compared to semi-custom ICs. Inventory cost, decrease .
Higher reliability	Greater reliability than hybrids and discretes because one semicustom IC replaces many components.
Quick turnaround	Semi-custom protos are delivered in less than seven (7) weeks.
Lower development cost	Less than 50% cost of a full custom program .
Iterations	Faster and more cost effective than full custom because only one mask needs to be changed.
Reduced real estate & power	Because one IC is replacing many components the PC board may shrink 60-80%, as a result less power consumption will be required.
Quick production ramp up	Need 200,000 units in less than 12 weeks? EXAR can deliver using its semi-custom arrays approach.
Product security	A semi-custom IC is specifically designed for the customer it is not available to competitors as an off-the-shelf ITEM.
Reduced inventory cost, and production cost	One custom IC replaces many discrete components.

STRATEGIC CAPABILITIES

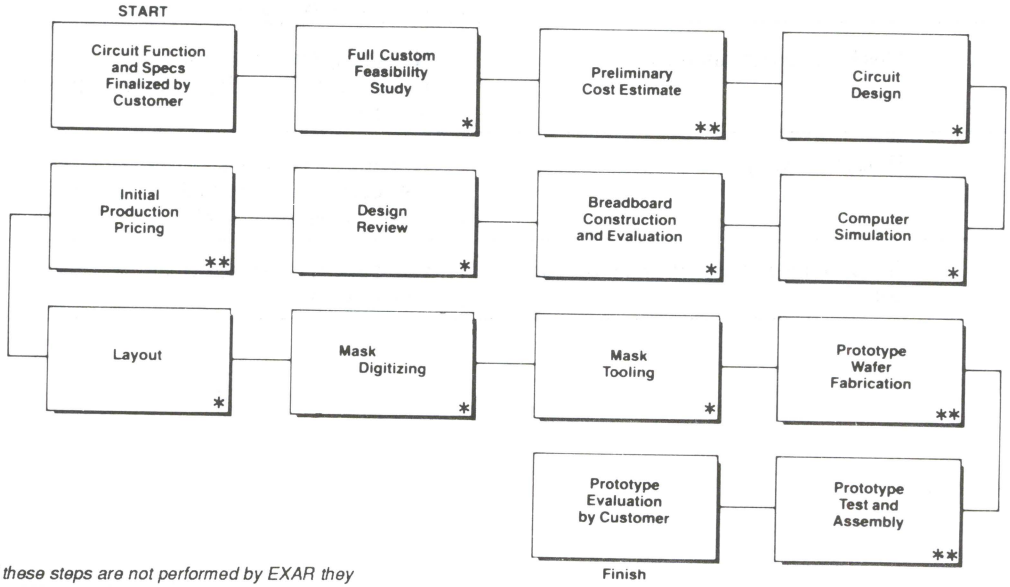
FULL CUSTOM DEVELOPMENT

EXAR offers complete design and production capability for full custom IC development. This provides an excellent complement to EXAR's unique semi-custom capability. EXAR's full custom IC development and production capabilities offer complete flexibility to accommodate the customer's changing needs or design problems. EXAR can develop a complete custom IC starting from your box specifications, or reduce a working breadboard prototype to a monolithic chip. Alternatively, if the customer has the facilities and resources to complete the IC design and layout, EXAR will provide device characteristics and IC layout rules for the particular process suitable to the customers design, and review his IC layout for him. EXAR can then generate the IC tooling and fabricate IC prototypes.

THE FIRST STEP FOR FULL CUSTOM DESIGN

The following technical data package is required in order for EXAR to provide a quotation for full custom development programs:

1. Circuit block diagram with subblocks.
2. Circuit schematic or logic diagram.
3. Description of circuit operation and pertinent application information.
4. Preliminary or objective device specification indicating min/max conditions and limits for the critical parameters; i.e., input/output voltage and current levels, operating frequency, timing diagrams, input/output impedances, power dissipation, etc.5. Production requirements and the desired develop-ment timetable.
5. Production requirements and the desired development timetable.
6. Packaging requirements.
7. Level of screening required.



* *If these steps are not performed by EXAR they should be completed in consultation with EXAR*

** *These steps must be completed by EXAR*

FLOW CHART OF TYPICAL FULL CUSTOM DEVELOPMENT

IC FABRICATION FROM CUSTOMER'S TOOLING

EXAR has a complete in-house silicon wafer fabrication and processing line at its main manufacturing plant in Sunnyvale, California. This facility currently runs 4-inch silicon wafers and is also available for manufacturing custom IC's directly from a set of customer supplied IC tooling, in coordination with EXAR's Mask Design department.

If the customer has a set of IC tooling (masks and composite overlays) or is contemplating having one designed, EXAR's technical staff will be glad to review it to assure compatibility with EXAR's technology and layout tolerances. EXAR's wafer processing technology and capabilities are compatible with the industry standards, and with the technologies of other leading IC manufacturers.

For additional information on EXAR's wafer fabrication services, contact EXAR directly. We pride ourselves in our flexibility and quick response to your needs.

TESTING OF SEMI-CUSTOM IC's

All semicustom IC production units are 100% electrically tested in accordance with specifications that have been mutually agreed upon between EXAR and the customer. Standard electrical screening consists of DC screening at room temperature. AC testing and testing over hot and cold temperature ranges is available at an added cost.

In addition, EXAR's Quality Assurance department performs an independent set of electrical tests on randomly selected samples of production units, prior to shipment, to assure conformity with EXAR's Acceptable Quality Level (AQL) standards.

EXAR provides 100% electrical testing of IC chips in wafer form using automated wafer probe stations, and in packaged form using automatic handlers. EXAR's test facility currently has fifteen independent computer controlled test systems, with more being added as we grow. EXAR's automated test system compliment is comprised of:

* Teradyne A311
* Teradyne A312
* Teradyne A360
* Sentry

Testing is one of the most critical steps in IC production. Therefore, to insure efficient and cost effective testing of production IC's, it is essential that a preliminary test plan be prepared jointly between the customer and EXAR at an early stage of the custom development. This preliminary test plan will lead to the final detailed test specifications once the development prototypes are fully evaluated, characterized, and the circuit is ready to release to production.

TEST INTERFACE DEVELOPMENT

Test hardware and software is developed based upon the performance and characterization data derived from careful prototype evaluation. EXAR and the customer will jointly determine the performance expectations to be placed on the new IC, and once these specifications are agreed upon, EXAR will proceed with test development.

Test development involves the design and construction of a test interface circuit, probe card and automatic handler hardware, as well as writing the software which allows EXAR's test system to perform the desired electrical tests. All these elements are then brought together under actual production conditions for evaluation and system debugging. This process can take from four to six weeks to complete depending on the sophistication and complexity of the test plan under development. Test development begins concurrently with the start of production wafers.

SPECIFICATION AGREEMENT LETTER

With each new custom IC design EXAR issues a Specification Agreement Letter. This specification precisely states the requirements that each production IC must meet before it can leave our factory, including test conditions, performance levels and environmental considerations. This document is also the signed agreement upon which acceptability of the IC is judged. It is issued in duplicate and signed by responsible representatives from both companies prior to the beginning of production. One copy is retained by the customer, the other is returned to EXAR.

If, for some reason, changes in the IC's specification are required, a new Specification Agreement Letter will be issued by EXAR reflecting these changes. However, no change will be put into effect until both companies have signed the new agreement. This new document will then supercede all prior agreements and remain in effect until replaced by yet another agreement.

STRATEGIC CAPABILITIES

LINEAR SEMI-CUSTOM DESIGN CYCLE: SIX SIMPLE STEPS

The basic linear semi-custom design program is comprised of 6 single steps. Beginning with circuit design and ending with the completion of monolithic prototypes. The first four steps can be completed either by EXAR, or by the customer in consultation with EXAR. The last two steps are performed by EXAR.

	STEP 1
Circuit design and breadboard using Linear Design Kit.	Customer purchases EXAR's Linear IC Design Kit, made up of a comprehensive designer manual and monolithic kit parts. Using these kit parts, the cirucit is designed, breadboarded and its performance evaluated. The electrical characteristics of the kit parts are virtually identical to the component which will be on the finished IC chip. Thus, this step provides a true simulationn of the final IC performance.
	STEP 2
Circuit layout is prepared	After breadboard evaluation is complete, a layout of the circuit on the selected array is prepared based on layout rules given in the design manual. The layout is done simply by interconnecting appropriate device terminals with pen or pencil lines on oversize drawings of the FLEXAR® arrays supplied with the kit.
	STEP 3
Layout review	EXAR reviews the circuit layout and schematic to check the following: a) That basic circuit function is feasible b) No layout rules are violated c) Circuit layout accurately represents the circuit schematic. *NOTE: EXAR offers consulting service and design advice during these first three steps.*
	STEP 4
EXAR generates custom interconnection	Using the completed FLEXAR ® layout sheet, EXAR generates a custom interconnection pattern, or metal mask to be applied to pre-fabricated FLEXAR® wafers.
	STEP 5
EXAR fabricates customized IC wafers	EXAR applies the custom interconnection patterns to pre-fabricated FLEXAR® wafers. During this customization process, the hardware and software necessary to test the prototypes is prepared.
	STEP 6
EXAR assembles and delivers monolithic prototypes	The customized IC wafers are scribed, or cut into individual IC chips. After a visual inspection, several die are assembled in cerdip packages. These packaged devices are then bench tested again before shipment. Ten asembled IC's are sent to the customer.

FULL CUSTOM DESIGNS

While EXAR offers direct full custom designs to customers, we also recognize the risks, costs, and longer turn-around times associated with a full custom development program. For this reason, EXAR also offers full custom conversion programs.

Full custom conversion is a two-step approach that provides the best of both worlds; a quick turn-around time, and the efficient use of silicon, which invariably means reduced unit costs.

The first step is to implement the customer's design on one of EXAR's Flexar arrays. This allows the customer to take advantage of the fast integration times, as well as a fast, easy, and low risk design iteration cycle in comparison to a full custom design approach. This approach enables customers to design their product and penetrate the market in a shorter time-frame, thus qualifying the product for production more rapidly. In addition, any application or production problems that may require design iterations can be implemented quickly and at a low cost. With this method all production oriented problems are fully debugged and the device is production proven in semi-custom form.

The second step,consists of a straightforward full custom conversion to minimize the chip size and hence the unit cost when the device is in full production. This ensures a risk free and a very smooth transition to shipping cost effective, high volume products.

THREE STEPS TO SUCCESS

Get EXAR To Work For You

Step 1: Discuss Your Needs With EXAR

EXAR is proud of its quick and flexible response to the customers needs. During the conception stage of a project, EXAR's highly talented design engineers will discuss the technical options and variations that are available. This is done at absolutely no cost to the customer.

Step 2: Get a Quotation From EXAR

To ensure an accurate and complete quotation quickly, the following information should be included when submitting a request for quotation (RFQ) :

- ❑ A block diagram of the application
- ❑ A schematic, at discrete or transistor level
- ❑ Circuit specifications
- ❑ Volume requirements

The more information supplied, the sooner EXAR can respond. EXAR can also assist in compiling this information.

Step 3: Let EXAR technology work for you

Having successfully completed over 1000 user specific projects (automotive, industrial control, telecom, modems, computer peripherals, medical and switch capacitor filter applications), EXAR's engineering staff has the necessary expertise to participate at any level of the customers design. Either in the system design, the IC design, layout or at the integration level. The amount of involvement is determined by the requirements of the customer. In any case, throughout the development process, a close contact is maintained between EXAR and the customer.

In addition to EXAR's extensive engineering expertise in user specific applications, EXAR also has accumulated years of engineering know-how and expertise as a standard IC manufacturer. EXAR's product lines include telecommunications, mass storage, data communications (including switch capacitor filters and modems), industrial control, and instrumentation markets. All this design expertise is available, and the customer should make use of EXAR's valuable engineering resources.

SERVICES OFFERED

Depending on the customers annual volume requirements and the selectivity criteria, EXAR offers a wide variety of Engineering services, These services are briefly outlined:

STRATEGIC CAPABILITIES

1. System Design: This service evolves from the conceptual system description and specification. It requires EXAR to generate the system design using a block diagram approach. It requires definition of the functional blocks and system implementation with discrete IC blocks to verify the performance as per the objective specs. Discrete IC implementation of each functional block and determination of the product or circuit specifications required to meet the system performance, concludes the System Design.

2. Circuit Design: In this type of service, the system is well defined by the customer in block diagrams and at the discrete IC level. EXAR determines the partitioning of the system and the definition of the product and objective specs. The transistor level circuit is then implemented to meet the IC specs. For circuit simulation, EXAR's Flexar models with SPICE programs are also available.

The circuit is breadboarded and fully evaluated. The finalized breadboard together with the evaluation results and performance characteristics is then submitted to the customer for approval.

3. Layout: After the transistor level circuit schematic of the breadboard is finalized, the 200X layout sheets or electronic layout sheets are used to do the interconnect. The interconnections of the circuit on the array is an integral part of the design and can have a significant effect on the performance of the circuit, therefore, all critical paths and matched circuit components must be identified and taken into consideration in achieving an optimum layout. This layout sheet along with the test specification of the circuit, provided by the customer, and the pin-out (bonding diagram) constitute the integration package.

4. Integration: This service involves generating silicon from the layout sheet. After the integration package is ready, EXAR will take the layout sheet and digitize it. At this stage, EXAR will check the digitized plots versus the transistor level circuit schematic. After digitization, Design Rule Check (DRC) is performed to eliminate any violations. The final digitized plots are then used to generate masks (working plates) using automated techniques.

Finally, metalization and passivation (glass or nitride) masking steps are performed on EXAR's premises to finish fabrication of the Flexar wafers. After the wafer fabrication is completed, prototypes are built at EXAR's in-house Hi-Rel assembly facility.

The prototypes are then fully evaluated and sent to the customer with binder that contains all pertinent information. These prototypes are for electrical evaluation purposes only.

5.Wafer Foundry In addition to all the services mentioned above, EXAR offers wafer foundry services utilizing its in-house state-of-the-art wafer fabrication line which includes all diffusion processes, epi, ion implantation, and a wide variety of deposition processes. Technologies offered include all bipolar processes, including I^2L and high voltage. Services are also available for partial or full processing of wafers using customer owned emulsion or chrome tooling.

MODELS AVAILABLE

SPICE model parameters (AC/DC) are available for the Flexar process.

EXAR LINEAR ARRAYS

The following section profiles the available EXAR Linear Arrays.

BI-FET ARRAYS (36V)	U-100	V-100	W-100
Transistors			
NPN, small	94	140	192
Supermatched small NPN's			16
NPN, 100mA	2		
NPN, 200mA		4	4
J-FET (P-channel)	4	4	8
PNP,dual collector	40	56	60
PNP,(med vertical)	2	4	4
PNP,vertical	8	4	10
Base Resistors			
280Ω	40	40	24
450Ω	158	112	100
900Ω	56	72	100
1.8KΩ	32	64	88
3.6KΩ	32	56	72
Total Base Resistance	305K	443K	559K
Implant Resistors			
1KΩ			32
5KΩ	16	32	32
10KΩ	16	32	32
20KΩ	16	32	32
50KΩ	16	32	28
Total Implant Resistance	1.36M	2.72M	2.55M
Cross Unders			
15Ω XU	9	4	
5Ω XU		8	
30Ω LVXU (5V max)		8	
15Ω LVXU	4	4	
Capacitors			
MOS capacitors (10pF max)	4	4	8
Pads	28	28	40
Die Size (mils)	110x110	146x113	163x133

NOTE: LV-low voltage (5V max. to substrate) XU-N + cross under

HIGH VOLTAGE (75V) ARRAY	X-100
Transistors	
NPN, small	30
NPN, 100mA	
NPN, 200mA	4
PNP, dual collector	16
20Ω XU	1
Base Resistors	
500Ω	64
1KΩ	27
2KΩ	58
5KΩ	12
Total Base Resistance	234K
N+ Resistors	
5 Ω	14
10 Ω	7
20Ω	7
Pinch Resistors	
100K Ω Pinched	3
30K ΩPinched	3
Pads	18
Die Size (mils)	115x95

STRATEGIC CAPABILITIES

KIT PARTS

Please Note: *Large NPN200 ma*
Medium NPN 100 ma
Small NPN 10 ma
** Absolute maximum ratings*

Item	Kit Part No.	Description	Max Voltage	Applicable for Miister-Chip
1.	XR-W101	5 small NPNs	36V	U-100,V-100,W-100
2.	XR-W108	Four 200 ma NPNs	36V	U-100,V-100,W-100
3.	XR-W111	4 small NPNs	36V	U-100,V-100,W-100
4.	XR-W206	4 lateral PNPs dual coilector	36V	U-100,V-100,W-100
5.	XR-W213	5 small, 2 large vertical PNPs	36V	U-100,V-100,W-100
6.	XR-W421	4 P channel, JFets	36V	U-100,V-100,W-100
7.	XR-X101	5 small NPNs	75V	X-100
8.	XR-X108	Four 200 ma NPNs	75V	X-100
9	XR-X206	4 lateral PNPs dual collector	75V	X-100

FLEXAR®

THE FLEXIBLE LINEAR BIPOLAR ARRAYS

EXAR adds a new dimension to its wide variety of linear arrays, NEVER BEFORE AVAILABLE in semi-custom design. EXAR introduces "FLEXAR®", the Programmable Linear Array. For the first time a designer can select either a NPN or PNP transistor from a specific location by using only a single layer of metal. This means that a circuit can be layed out for the total number of transistors without regard to polarity. For example, if the chip has space for 100 transistors, the designer could use 100 PNP's or 100 NPN's or any combination of NPN's and PNP'S. In addition, unused bonding pads may be converted to active or passive components giving greater than 100 percent utilization and a chip size and cost approaching full custom.

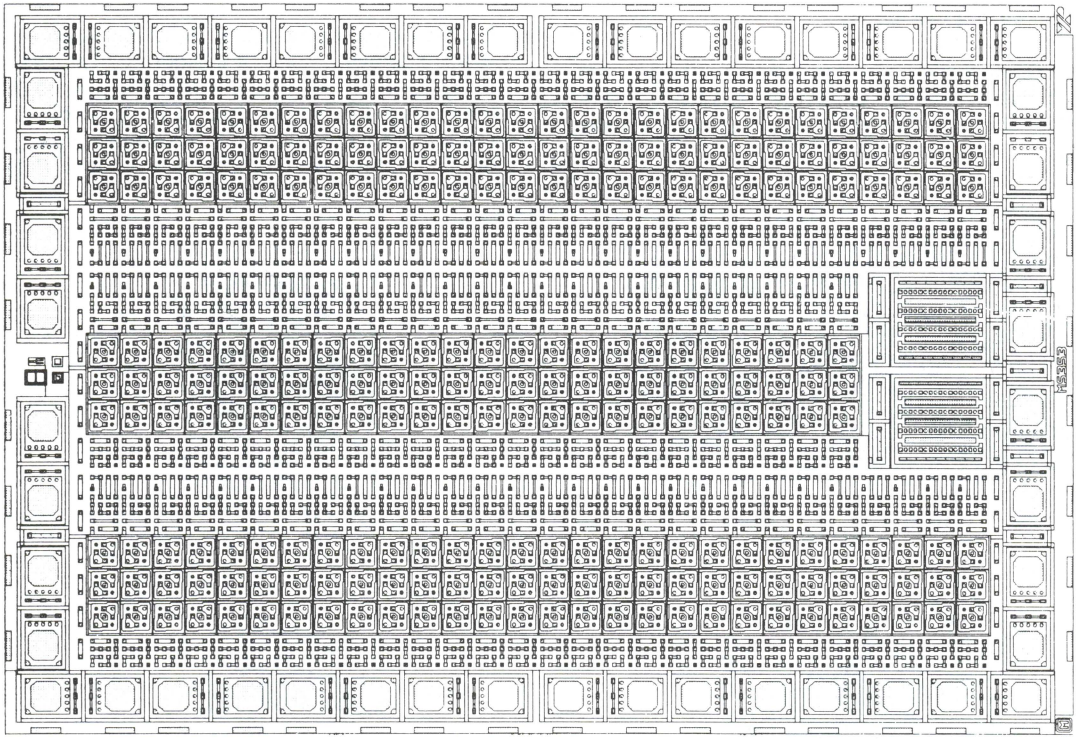


Figure 1. The BETA 240 Array Topography and Component Count

STRATEGIC CAPABILITIES

The FLEXAR® topology is perfectly suitable for mixed-signal technology designs. Now you can truly design both linear and digital circuitry on the same chip–another first in the industry!

EXAR is developing an extensive "SOFT MACRO" Library of already proven circuits. Designing from this library will greatly simplify the schematic capture tasks and minimize the time required to get from working schematic to the final IC.

Any user designed function can also be made into a circuit building block and, like EXAR soft macro library, can be transferred to various locations on the chip or to other chips in the FLEXAR family.

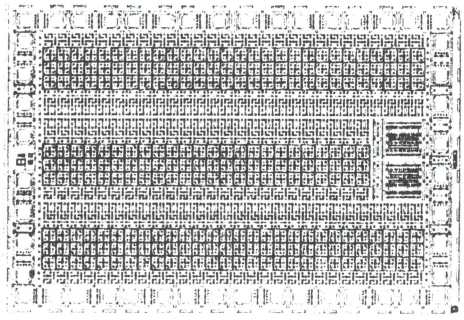
The new FLEXAR® family is designed with the same layout architecture. All applications are covered with only three different arrays.

Four types of "Kit Parts" are required to breadboard the circuit. These are the TWINSTOR (NPN, PNP), PADSTOR, and TWINBOOSTOR (patent applied for).

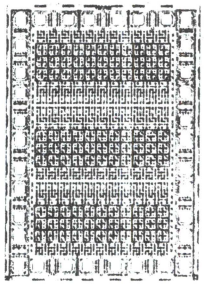
FLEXAR® BETA ARRAY CELL ARCHITECTURE

The architecture of the FLEXAR® Beta array is built around a flexible CELL which is repeated throughout the array and on the other arrays of the family (see figure 3). This enables a circuit to be duplicated anywhere within an array or transferred from one array to another with unchanged characteristics. The designer's tack becomes greatly simplified because the same layout may be placed in any location and on any array in the family, giving a major reduction in design cycle. This is far superior to the typical semi-custom IC which does not have this cell structure. Prior to the introduction of FLEXAR®, a new layout would have been required if the same circuit was to be transferred from one array to another or even to a different location on the same array.

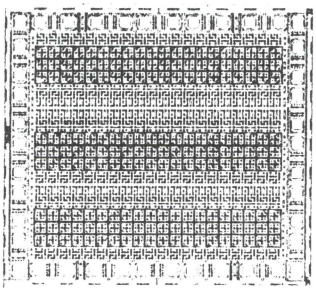
Each cell contains three TWINSTORS flanked by two resistor arrays as shown in figure 3. The resistor arrays are part of the four independent resistor islands (see figure 1) Resistor Array A, in figure 3 on the left, contains 3K ohms base resistance, 10K ohms implant resistance, a 40 ohms P-type



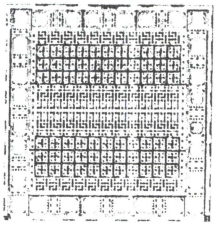
MS353 BETA 240



MS365 BETA 100



MS366 BETA 180



MS409 BETA 66

Figure 2

crossunder and a low current bias contact to V+ (the most positive supply). Resistor Array B, in figure 3 on the right, contains 5.5K ohms base resistance, 35K ohms implant resistance, two P-type crossunders (40 and 45 ohm), an independent bias contact, a low current substrate and a wide preassigned V+ track running perpendicular to the 1.5K ohm resistors. Interconnections between CELLS become simple and make the layout compact and efficient.

When the TWINSTORS are not used as active elements, each TWINSTOR may be used either as a 90 ohm crossunder or as a 500 ohm matched resistance pair conveniently close to the active elements.

FLEXAR ® BETA ARRAY TOPOLOGY

The V+ metal is preassigned to run perpendicular to the 1.5K ohm resistors. A wide substrate metal (most negative supply) around the perimeter of the die is easily accessible to every CELL, regardless of location. Within each CELL, a low current direct V+ tap is provided in resistor Array A and a low current V- tap in resistor Array B.

In case of multiple supplies, the designer should pay careful attention to the biasing of the four independent resistor tubs. To avoid latch-up during power on of the power supplies, it is recommended to keep resistors to each supply in a separate tub or to bias all the tubs to the highest Vcc used.

Every bonding pad, being a multifunction PADSTOR, is located at the perimeter of the die. The grid format is set at a constant pitch, designed especially for compatibility of EXAR's routing software. This reduces the digitizing time and shortens the overall mask design time.

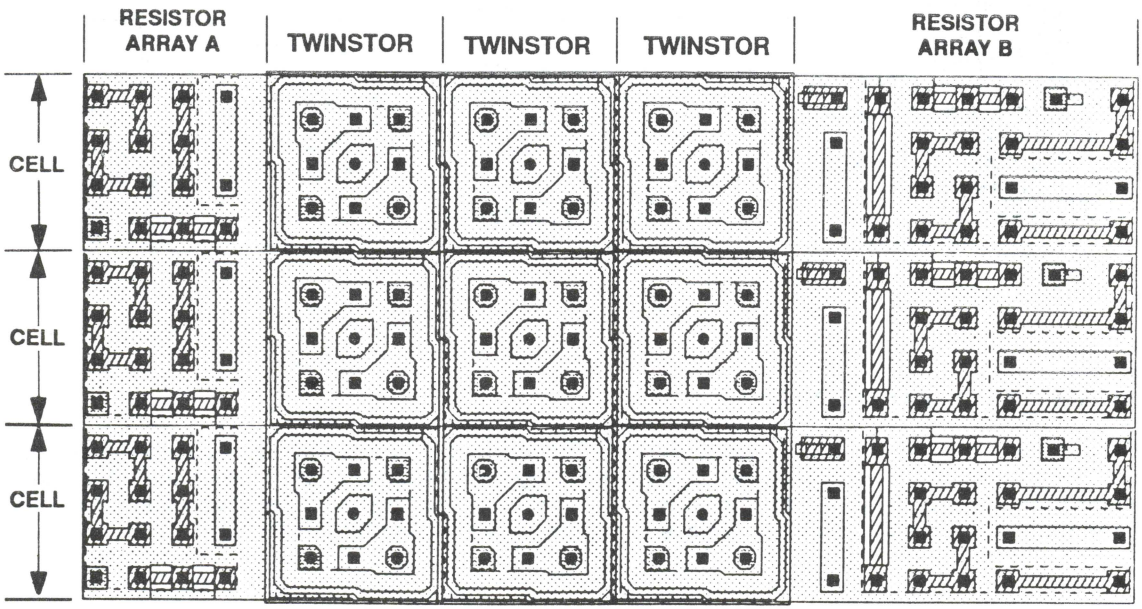


Figure 3.

STRATEGIC CAPABILITIES

FLEXAR®BETA ARRAYS

COMPONENT COUNT

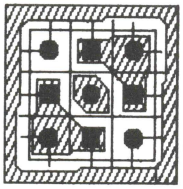
	BETA-240	BETA-180	BETA-100	BETA-66
CELLS	80	60	33	22
TWINSTOR NPR OR PNP	240	180	99	66
PADSTOR OR PADSTOR AS				
NPN	48	42	34	28
PNP	48	42	34	28
Resistor	48	42	34	28
Capacitor	48	42	34	28
Bonding Pad	48	42	34	28
Twinbooster NPN PR PNP	2	0	0	0
Base Resistors				
500 ohm	880	660	363	242
1.5K ohm	160	120	66	44
Total Base Resistance	680KΩ	510KΩ	28OKΩ	190KΩ
Ion Implant Resistors				
5K ohm	320	240	132	88
25K ohm	80	60	33	22
Total Implant Resistance	3.6MΩ	2.7MΩ	1.5MΩ	1MΩ
P+ Crossunder Resistors				
(XU1) 500 ohm	480	360	216	132
(XU4) 45 ohm	86	66	39	26
(XU3) 40 ohm	184	150	96	64
(XU5) 20 ohm (PADSTOR)	48	42	34	28
N+ Crossunder Resistors				
(XU7) 90ohm	240	180	99	66
(XU2) 20 ohm (PADSTOR)	96	84	68	44
(XU6) 15 ohm	15	4	0	0
DIE DIMENSION	110x160 mils	110x121 mils	110x78 mils	78x82 mils

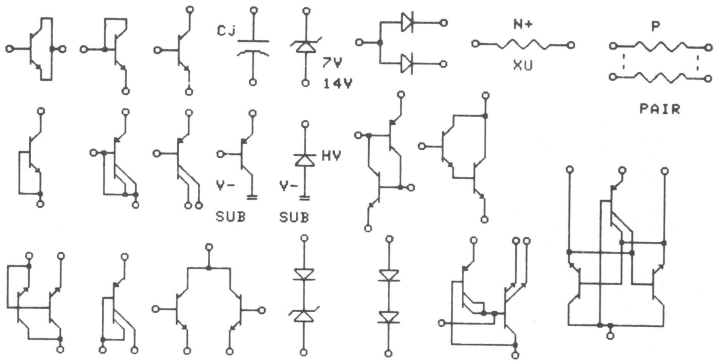
FLEXAR®BETA ARRAY COMPONENTS

Three multifunction components (TWINSTOR, PADSTOR, and TWINBOOSTER) in FLEXAR® Beta array family of linear/digital arrays and the continuity of the topology of the FLEXAR® series are unique to the industry. For the first time, each component can be programmed to serve as one of many active or passive functions. The designer defines the desired function by proper connections with the single metal layer.

TWINSTOR - MULTIFUNCTION AND MULTIPURPOSE

The TWINSTOR is the star of the family its versatility comes from its composite structure: a dual collector PNP (common base) merged with a two common collector NPN. With the 9 available contacts, you have a choice of over 20 active or passive functions from a single TWINSTOR.



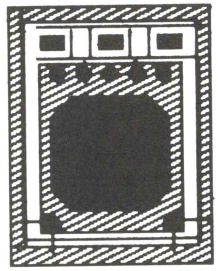


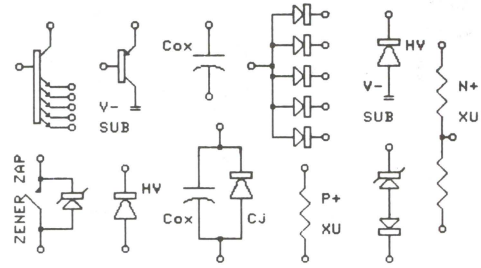
TWINSTOR AS NPN (2X)	Min	Typical	Max	Units
Breakdown voltage BVCEO, Ic = 1 mA	26	35		Volts
Current gain, Ic = 1 mA, VCE = 5V	80	180	360	
Current gain, Ic = 15 mA, VCE = 5V	30	60		
Saturation resistance (two collectors)		50	100	Ohms
Collector Current			15	mA
f_T NPN at Ic = 3 mA, VCE =, 5V		800		MHz
TWINSTOR AS PNP				
Breakdown voltage, Ic = 0.1 mA	26	45		Volts
Current gain, Ic = 10 µA, VEC = 5V		50	140	300
Current gain, Ic = 1 mA, VEC = 5V		10	20	
Saturation resistance		200	300	Ohms
Collector Current		9	3	mA
f_T PNP at Ic = 100 µA, VEC = 5V				MHz
TWINSTOR AS RESISTOR				
Resistance	400	500	650	Ohms

STRATEGIC CAPABILITIES

PADSTOR - A BUSY BONDING PAD

With the bonding pad merged with a five emitter NPN and a large vertical substrate PNP, the PADSTOR complements the TWINSTOR. Not only can it drive loads as NPN or PNP, but it can stabilize your design by acting as a large compensation capacitor (both MOS and junction). It can also trim design parameters as a zener zap, provide pad protection as a high voltage and a high current clamping diode and even serve as a dual series resistor network for sink/source output stages.

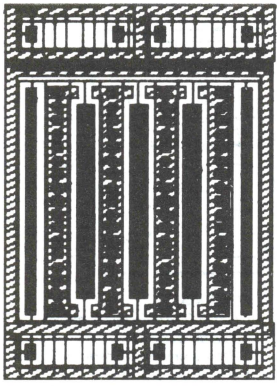


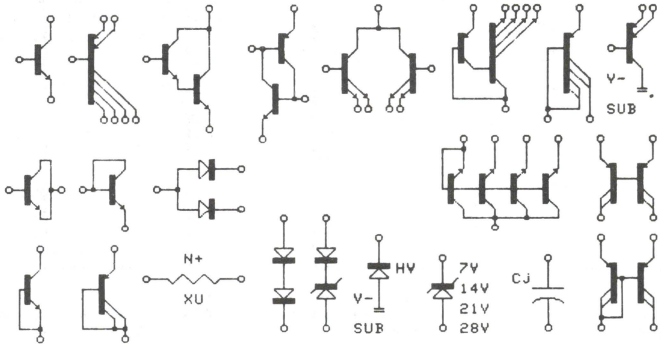


PADSTOR AS NPN	Min	Typical	Max	Units
Breakdown voltage BVCEO, Ic = 1 mA	26	40		Volts
Current gain, Ic = 5 mA, VCE = 5V	80	250		
Current gain, Ic = 50 mA, VCE = 5V	30	60		
Saturation resistance at 50 mA		20		Ohms
Collector Current			50	mA
PADSTOR AS PNP				
Breakdown voltage BVCEO, Ic = 1 mA	26	70		Volts
Current gain, Ic = 1 mA, VCE = 5V	200	400	550	
Collector Current			25	mA
PADSTOR AS CAPACITOR				
Junction capacitor, Vj = ov		3.8		pF
Oxide/Nitride capacitor, tox. = 0.22 μ		2.5		pF
PADSTOR AS N + RESISTOR (2 in series)				
Resistor value (each)		20		Ohms
PADSTOR AS P+ RESISTOR				
Resistance		20		Ohms
PADSTOR AS BONDING PAD	–	–		

THE TWINBOOSTER - "THE SLEDGEHAMMER"

The TWINBOOSTOR has a 32 emitter NPN merged with a four collector and a three large emitter lateral PNP. It can handle up to 500 mA loads as a NPN and 25 mA loads as a PNP.



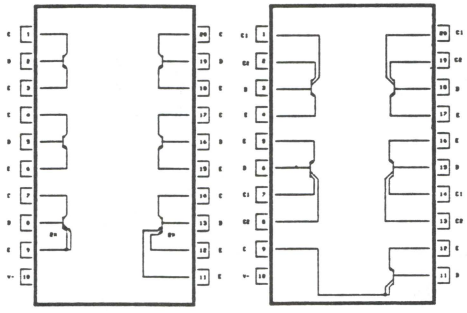


TWINBOOSTOR AS NPN	Min	Typical	Max	Units
Breakdown voltage BVCEO, Ic = 10mA	26	35		Volts
Current gain, Ic = 20 mA, VCE = 5V	80	250	430	
Current gain, Ic = 30 mA, VCE = 5V	80	200		
Saturation resistance		4		Ohms
Collector Current			500	mA
TWINBOOSTOR AS PNP				
Breakdown voltage BVCEO, Ic = 1mA	26	55		Volts
Current gain, Ic = 500 µA, VCE = 5V	35	45		
Current gain, Ic = 10 mA, 5V	5	15		
Saturation resistance		25		Ohms
Collector Current			25	mA

STRATEGIC CAPABILITIES

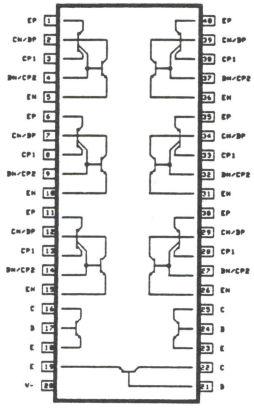
FLEXAR® BETA ARRAY KIT PARTS

The simplicity and ease of designing with FLEXAR® BETA-arrays is demonstrated by the fact that only four different types of KIT PARTS are required to breadboard and check your design.

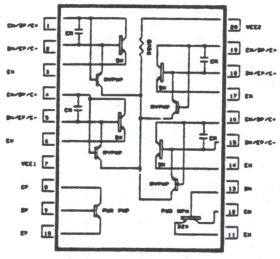


FLA-101
6 TWINSTORS Programmed
as NPNs

FLA-102
5 TWINSTORS Programmed
as PNPs
as NPNs



FLA-103
6 TWINSTORS- Programmable
3 TWINSTORS- Programmed



FLA-104A
4 PADSTORS-Programmable
1 TWINBOOSTOR-
Programmed as Power PNP
1 TWINBOOSTOR -
Programmed as Power NPN

DESIGNING WITH SOFT MACROS

A Softmacro is a predesigned, fully characterized circuit that is ready to be implemented on any of the FLEXAR® BETA-arrays. The Softmacro approach makes IC design simple. An engineer who is unfamiliar with IC design can, for the first time, reduce a working circuit to an IC just by following these simple steps:

1 . Draw a block diagram of the system.

2. Choose the appropriate Softmacro(s) for each block, using the extensive library of Softmacros provided by EXAR.

3. Connect the Softmacro(s), forming the desired circuit.4. Simulate the circuit, on your computer or on EXAR's.

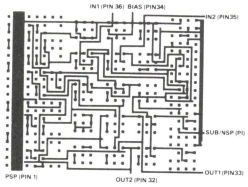
5. Layout the circuit, or let EXAR do the layout for you.

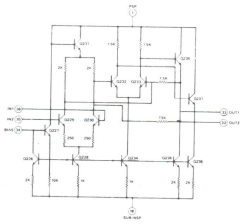
6. EXAR-always ready to support you-will pick up the project at any stage, including at your building block concept.

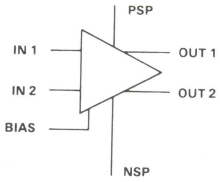
7. EXAR will provide functionally tested prototypes ⟶ FAST!

TYPICAL SOFT MACRO

BTA-AMP-01 is a wideband, differential input-output amplifier. It is similar to the industry standard 733 except that the gain is fixed. The optional circuit bias permits additional versatility. This circuit is capable of operating from either a single or a split power supply.







BTA—AMP—01

FEATURES		MAXIMUM RATINGS	
GAIN	20dB	PSP-NSP	26V
BANDWIDTH	UP T0 30MHz	IN (DIFF)	7V
SLEW RATE	160V/μS	I OUT	10mA

6

PARTIAL LIST OF SOFT MACRO LIBRARY.

Low Level Full-wave Rectifier
Full-wave Rectifier with Ground Reference
Inductive Coupled Rectifier
Precision Full wave Rectifier
Single-ended Full-wave Rectifier
Simple Rectifier
Transconductance Amplifier
Low Voltage Output Amplifier
Current Source With Low TC
Voltage to Current Converter
Voltage to Current Pump
Current Source, With Multiple Outputs
Ground Sensing V-1 Converter
High Accuracy Current Source
Differential-voltage Controlled Current Generator
Low Voltage Bandgap Referenced Current Source
Frequency Divider
D Latch
AND Gate
Exclusive OR Gate
NOR Gate
Phase Detector
Peak Detector
Zero Crossing Detector
Sample-and-Hold

FLEXAR® BETA ARRAY SUPPORT

User-support for FLEXAR® BETA-arrays is available on PC/AT personal computers. With the FLEXAR Integrated Development System (FIDS) your PC/AT can be equipped with a schematic entry system, circuit simulation and layout software. This allows you to design a circuit, capture the schematic, check the circuit simulation, make modifications if necessary, and resimulate as often as desired. When the circuit has been sufficiently verified, a net list can be printed out. EXAR will pick up the development at any stage, and fabricate your design into an integrated circuit. You can maintain full control of your system-and complete privacy-when you perform the entire design at your facility. Of course, EXAR engineering and applications personnel are always available for technical support.

By special arrangement schematic capture may be performed at EXAR.

STRATEGIC CAPABILITIES

PACKAGING

EXAR provides all standard dual-in-line packages in plastic, cerdip, and side braze. The list below describes some of the surface mount packages available. Contact EXAR for a complete discussion of your package requirements.

SIZE	PACKAGE TYPE		
	SO	QFP	PLCC
16	√		
18	√		
20	√		
22	√		
24	√		
28	√		√
32	√	√	
44	√	√	√

Note: *Dimensions for these packages are listed in the section 9 of this book.*

FLEXAR INTEGRATED DESIGN SYSTEM

Get Acquainted with FIDS

The FLEXAR Integrated Design System (FIDS) is the industry- first, fully-integrated CAD/CAE tool. FIDS converts 386-based personal computers into complete analog IC workstations for FLEXAR Beta-arrays.

*User-friendly FIDS Executive Shell interfaces with all resources
*Schematic entry (OrCAD/SDT III^TM V3.2, OrCAD Systems Corporation)
*Simulation(PSpice^TM^V4.0, MicroSim Corporation)
*Graphic layout editing (EXAR-proprietary SW)
*Design-Rule-Check (DRC)
*Electrical-Rule-Check (ERC)
*Layout-Versus-Schematic checking (LVS)
*Pattern Generation (PG) output in David Mann 3000 format

Get a Growing Library of Softmacros

Schematics and layouts for 65 building block circuits: industry standards, special designs, are being developed. Layouts are easily ported across all four Beta-arrays.

Use a Popular Low Cost PC Design Platform
Minimum hardware requirements:

*PC/386 with DOS 3.0
*387 Math co-processor
*4Mbyte RAM
*EGA color capability
*1.2Mbyte 5.25" floppy drive
*20Mbyte hard drive
*1 serial port (COM1)
*1 parallel port
*Mouse Systems^TM Mouse (MSC Technologies Inc.)

Optional additions:

*2nd serial port (COM2)
*HPGL plotter
*dot matrix printer

Documentation and Training

FIDS comes with a comprehensive users manual and free registration for two participants in our 3-day training class. Classes are offered quarterly. Additional registrations are available at a cost of $1000.

Dedicated Follow Up

EXAR issues software upgrades and additions to the Softmacro library, quarterly, as they are developed. Nominal cost per release.

Hotline Support

A 24-hour answering service has been established for FIDS users. Call our west coast headquarters at 408-434-6400, ext. 3650. Inquiries acknowledged promptly in your timezone, anywhere in the world.

Packaging Options

Choose one of four packages, according to whether the site has OrCAD, PSpice, both or neither. Manuals can be ordered separately.



NOTES



XR-N1600 STANDARD CELLS

XR-N1600 Standard Cells

The N1600 series of standard cells from EXAR Corporation is manufactured using an advanced 1.6 micron, double Poly, double metal, CMOS with E^2, BiCMOS process. This process is unmatched in its versatility and performance, providing the user with fast digital switching, precise analog functions, and dense memory, including EEPROM. This access to highly integrated, digital and analog solutions assures the associated system advantages that VLSI provides. The N1600 standard cell library offers high noise immunity and very low power consumption typical of CMOS technology. All inputs and outputs may be selected to be compatible with either TTL or CMOS logic levels or any analog signal from 0 to 50 Volts. The small geometries allow over 150 I/O signals and integration complexities up to 10,000 equivalent gates.

The digital portion of the Standard Cell library consists of cell primitives, Macro-cells and Mega-cells, implementing functions ranging from simple NAND gates to high speed multipliers. The 1.6 micron drawn feature size permits very fast clock rates and very high levels of integration.

XR-N1600 analog cells reflect EXAR's extensive experience in linear design. These cells allow the merging of digital processing with the analog world of motors, sensors and communications. Basic analog functions available include op-amps, comparators, voltage references, and oscillators. In addition, the library includes high level analog functions, such as A/D and D/A converters, phase-locked loops, and switched capacitor filters. Of course, all these cells take full advantage of the capabilities offered by EXAR's advanced analog CMOS process including various types of trimming for even higher performance.

FEATURES

1.6 micron CMOS
3 to 16.5 Volt supply voltages
Over 150 input/output pads
Fast generation of user specific functions

* Digital synthesis
* Analog custom product experience
* Memory configurations up to256K

Extensive 100 cell digital library
* Toggle frequencies to 75 MHZ
* Clock frequencies to 50 MHz

Expanding 20 cell EEPROMLibrary
* 0.8 nS typical 2 input NAND delay
* Output drivers to 48 mA
* Up to 10,000 equivalent gates

Comprehensive 50 cell analog library
* Op amps, comparators, oscillators
* A/D, D/A switched capacitor filters, phase lock loops, voltage references

Reconfigurable memory macros
* EEPROM,RAM,ROM

MAXIMUM RATINGS

Storage Temperature	-65 to+ 150°C
Operating Temperature	-55 to +125°C
Supply Voltage, VDD	+3.0V to +16.5V
Voltage on any pin	VSS -.3V to VDD +.3V
ESD	3000V at 100pF thru 1.5k Ohms

STRATEGIC CAPABILITIES

DC OPERATING CHARACTERISTICS

VDD = 5.0V ± 10%, Temperature = -55 to +125°C

Parameter	Condition	Limit	Value	Unit
IOH, Output High Current	VOH = 2.4V	MIN	4.0	mA
IOL, Output Low Current	VOL = 0.40	MIN	4.0	mA
VIH, Input High Voltage	TTL Interface	MIN	2.0	V
	CMOS Interface	MIN	3.5	V
VIL, Input Low Voltage	TTL Interface	MAX	0.8	V
	CMOS Interface	MAX	1.5	V
IIN, Input Current	CMOS/TTL	MAX	±0.1	µA
IDD, Supply Current	Active/Cell/MHz	TYP	1.5	µA
	Quiescent/Chip	TYP	±1.0	µA
Capacitance				
Chip input	DIP Package	TYP	4.0	pF
Chip output	DIP Package	TYP	6.0	pF
Cell input		TYP	0.1	pF

AC OPERATING CHARACTERISTICS DIGITAL CELLS

VDD = 5.0V, Temperature = 25°C, 2µ Transistor Lengths

Parameter	Condition	Limit	Value	Unit
Propagation Time				
Inverter	0.5 pF Load	MAX	0.8	ns
2-input NAND	0.5 pF Load	MAX	1.0	ns
2-input NOR	0.5 pF Load	MAX	1.3	ns
Output Buffer	15 pF Load	MAX	3.7	ns
Frequency				
Flip Flop Toggle		MIN	100	MHz
Oscillator		MIN	50	MHz

AC OPERATING CHARACTERISTICS MEMORY CELLS

VDD = 5.0V, Temperature = 25°C

Parameter	Condition	Limit	Value	Unit
Access Time				
256 x 8 EEPROM		MAX	100	ns
256 x 8 RAM		MAX	80	ns
256 x 8 ROM		MAX	60	ns

AC OPERATING CHARACTERISTICS ANALOG CELLS

VDD = 10.0V, Temperature = 25°C

Parameter	Condition	Limit	Value	Unit
Opamp				
Gain Bandwidth		MIN	3.5	MHz
PSRR	1 KHz	MIN	80	dB
A/D Converter	8 Bits			
Resolution	MAX	=	LSB	
Conversion Time		MAX	100	µs
D/A Converter	8 Bits			
Resolution	MAX	=	LSB	
Settling Time	MAX	10	µS	

DIGITAL CELL DATA

Cell Name	Function
A2202	AND-OR-COMBINATION
AND2	2-INPUT AND GATE
AND3	3-INPUT AND GATE
AND4	4-INPUT AND GATE
AND5	5-INPUT AND GATE
CINBUF2	CMOS INPUT LEVEL SHIFTER
CISBUF2	CMOS INPUT SHMIDT TRIGGER
CRIP4	4 BIT RIPPLE COUNTER
CRIPT4	4 BIT RIPPLE COUNTER WITH TRISTATE
BUF2	MEDIUM-DRIVE BUFFER
BUF4	HIGH-DRIVE BUFFER
BUFT2	MEDIUM DRIVE TRI-STATE BUFFER
BUFT4	HIGH DRIVE TRI-STATE BUFFER
D20N12V	MEDIUM-DRIVE BUFFER WITH DELAY
DF	D-TYPE FLIP-FLOP
DFR	D-TYPE FLIP-FLOP WITH RESET
DFRU	D-TYPE FLIP-FLOP WITH RESET (UNBUFFERED)
DFS	D-TYPE FLIP-FLOP WITH SET
DFSR	D-TYPE FLIP-FLOP WITH SET AND RESET
DFU	D-TYPE FLIP-FLOP (UNBUFFERED)
DFSU	D-TYPE FLIP-FLOP WITH SET (UNBUFFERED)
DFSRU	D-TYPE FLIP-FLOP WITH SET AND RESET (UNBUFFERED
EXN2	2-INPUT EXCLUSIVE NOR
EXO2	2-INPUT EXCLUSIVE OR
INV2	MEDIUM-DRIVE INVERTING BUFFER
INV4	HIGH-DRIVE INVERTING BUFFER
INVT2	MEDIUM DRIVE INVERTING TRI-STATE BUFFER
INVT4	HIGH DRIVE INVERTING TRI-STATE BUFFER
LD	D-TYPE LATCH
LDR	D-TYPE LATCH WITH RESET
LDS	D-TYPE LATCH WITH SET
LDSR	D-TYPE LATCH WITH SET AND RESET
LNAND	CROSS COUPLED NAND LATCH
LNOR	CROSS COUPLED NOR LATCH
LVSH	COMPLEMENTARY INPUT LEVEL SHIFTER
MDFRU	D-TYPE FLIP-FLOP WITH MULTIPLEXED INPUT AND RESET (UNBUFFERED)
MUX21	2 TO 1 DIGITAL MULTIPLEXER
MUX21U	2 TO 1 UNBUFFERED DIGITAL MULTIPLEXER
MUX41	4 TO 1 DIGITAL MULTIPLEXOR
MUX81	8 TO 1 DIGITAL MULTIPLEXOR
NAND3	2-INPUT NAND GATE
NAN3	3-INPUT NAND GATE
NAND4	4-INPUT NAND GATE
NAND5	5-INPUT NAND GATE

(DIGITAL CELLS CONTINUED)

CELL NAME	FUNCTION
	NOR2 2-INPUT NOR GATE
NOR3	3-INPUT NOR GATE
NOR4	4-INPUT NOR GATE
O22A2	OR-AND-INVERT
OR2	2-INPUT OR GATE
OR3	3-INPUT OR GATE
OR4	4-INPUT OR GATE
PD50K,100K	50K,100K Ohm PULLDOWN
POR	POWER ON RESET (Vt=1.0V)
POR4HV	POWER ON RESET (Vt=4.0V)
PU50K, 100K	50K, 100K Ohm PULLUP
RDF4,8	4,8 BIT DF REGISTER
RDFR4,8	4,8 BIT DF REGISTER WITH RESET
RDFR4S,8S	4,8 BIT DF REGISTER WITH RESET AND SERIAL SHIGT
RDFRT4,8	4,8 BIT DF REGISTER WITH RESET AND TRISTATE
RDFT4,8	4,8 BIT DF REGISTER WITH TRISTATE
RSHF4,8	4,8 BIT SHIFT REGISTER
RSHFR4,8	4,8 BIT SHIFT REGISTER WITH RESET
TINBUF2	TTL INPUT LEVEL SHIFTER
TINSBUF2	TTL INPUT SHMIDT TRIGGER
TRI4,8	4,8 BIT TRISTATE DRIVER

EEPROM CELLS

CELL NAME	FUNCTION
EELAT	EEPROM ONE BIT LATCH
EENON	EEPROM TWO-PHASE CLOCK
EEOSC	EEPROM CLOCK OSCILLATOR
EEPOR	EEPROM POWER-ON-RESET
EEPSFHV	EEPROM PROGRAMMING VOLTAGE SWITCH
EEPUM	EEPROM HIGH VOLTAGE GENERATOR
EERAMPHV	EEPROM RAMP VOLTAGE GENERATOR
EEREF	EEPROM HIGH VOLTAGE REFERENCE
EEWRTL	EEPROM WRITE/RECALL LOGIC
EE64X16	EEPROM ARRAY 64 WORK X 16 BIT

I/O PAD CELLS

CELL NAME	FUNCTION
CIN2,W	CMOS BUFFERED INPUT PAD
CIS2,W	CMOS SCHMITT TRIGGER INPUT PAD
EEVPPAD,W	EEPROM EXTERNAL HIGH VOLTAGE PAD
INP,W	UNBUFFERED INPAD (SERIES R)
INPA,W	UNBUFFERED INPUT PAD
OB1,W	1mA OUTPUT PAD
OB4,W	4mA OUTPUT PAD
OB7,W	7mA OUTPUT PAD
OBBCI4,W	4mA TRI-STATE BIDIRECTIONAL PAD
OBN4,W	4mA OPEN-DRAIN OUTPUT PAD (SINK)
OBP4,W	4mA OPEN-DRAIN OUTPUT PAD(SOURCE)
OBT4,W	4mA TRI-STATE OUTPUT PAD
OSC4,W	SINGLE PAD OSCILLATOR
OSRC4,W	RC OSCILLATOR (2 PAD)
OSX4,W	CRYSTAL OSCILLATOR (1-100KHz)
OSX16,W	CRYSTAL OSCILLATOR (10KHz-1MHz)
OSX32,W	CRYSTAL OSCILLATOR (1-40MHz)
TIN2,W	TTL BUFFERED INPUT PAD
TIS 2,W	TTL SCHMITT TRIGGER INPUT PAD

COMPLEMENTARY BIPOLAR

FUNCTION
High Speed VCA's
Wide Bandwidth Op-Amps, BUFFERS
High Speed COMPARATORS
High Speed PEAK-DETECTORS
High Speed S/H AMPLIFIERS
High Speed GROUND SENSING CIRCUITS
Video Amplifiers
High Speed amplifiers/BUFFERS
High Slew Rate Amplifiers

CMOS

FUNCTION
PEAK DETECTOR
BAND GAP
5 BIT D/A
8 BIT A/D
OP AMP
INTEGRATOR
HIGH GAIN COMPARATOR
VCO
DIGITAL CELLS with
ECL FRONT END & CMOS BACKEND

ANALOG CELL DATA

BIAS GENERATORS

(with power down (MIRRor for 20µ/8µ NTX))

CELL NAME	BIAS1	BIAS2
MIRR	10µA	10µA
TEMPCO	0±.05%	0,.25,-.25±/0.5%
VOLTCO	3000ppm	3000ppm
SUPPLY V	4.5 - 16.5	4.5 - 16.5
CURRENT	50µA	75µA

OPERATIONAL AMPLIFIERS

(with power down (external bias))

CELL NAME	OP1HV	OP1LV	OP2HV	OP2LV	OPB1HV	OPB1LV
OFFSET	15mV	15mV	10mV	10mV	10mV	10mV
GBW	4MHz	2MHz	2MHz	1MHz	2MHz	1MHz
PSSR	70dB	70dB	70dB	70dB	70dB	70dB
CMRR	70dB	70dB	70dB	70dB	70dB	70dB
CMVOLT	0,VDD-2	0,VDD-2	0,VDD-2	0,VDD-2	0,VDD-2	0,VDD-2
CL	10pF	10pF	10pF	10pF	100pF	100pF
RL	10K	10K	10K	10K	1K	1K
SUPPLY V	7.0 - 16.5	4.5 - 7.0	7.0 - 16.5	4.5 - 7.0	7.0 - 16.5	4.5 - 7.0
CURRENT	200µA	100µA	100µA	100µA	400µA	400µA

COMPARATORS

(with power down (RESponse for 10mV overdrive using BIAS1))

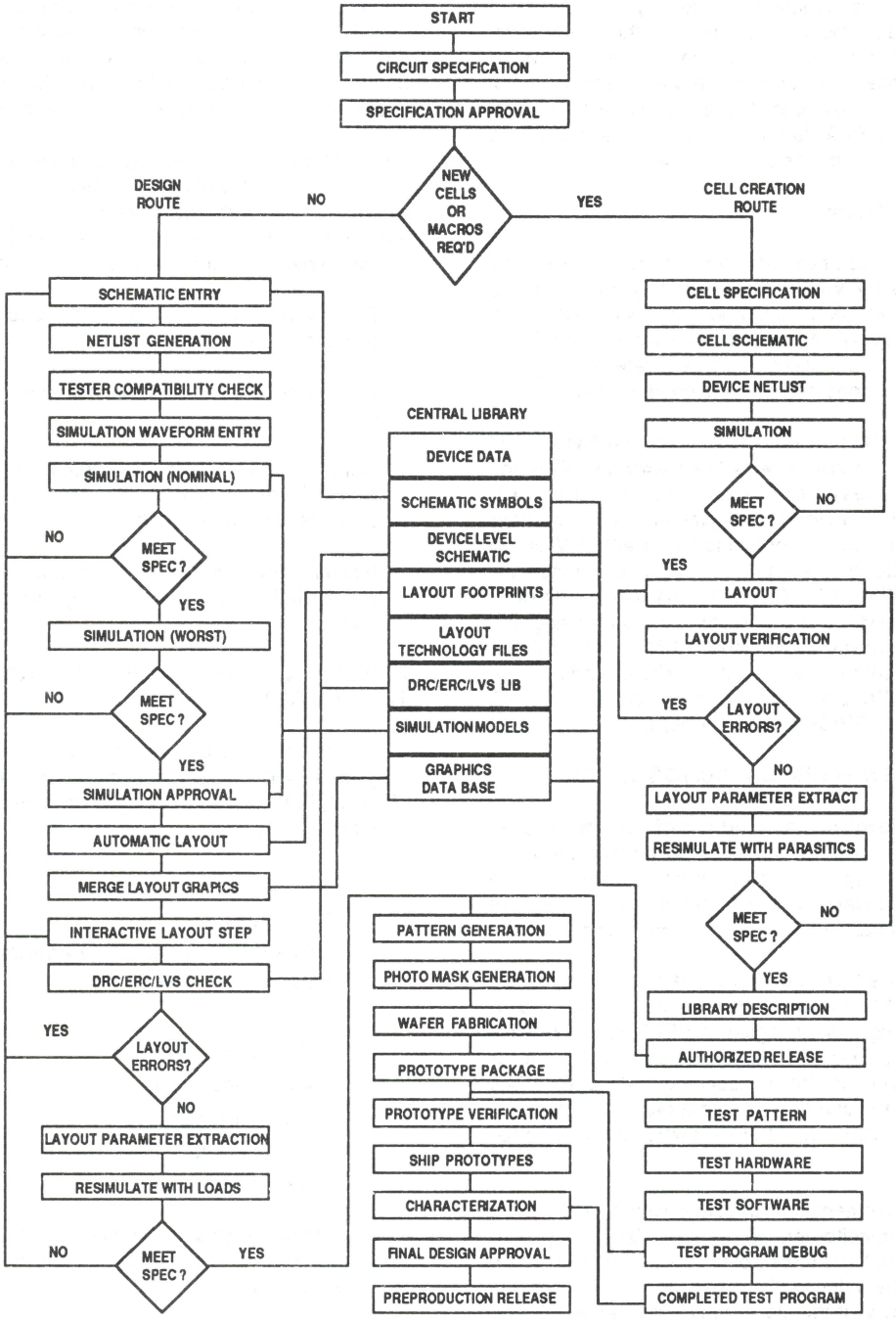
CELL NAME	CMP1LV	CMP1	CMP2LV	CMP2
OFFSET	10mV	10mV	5mV	5mV
RESP	200ns	200ns	400ns	400ns
CMVOLT	0,VDD-2	0,VDD-2	0,VDD-2	0, VDD-2
CL	1pF	1pF	1pF	1pF
RL	100K	100K	100K	100K
SUPPLY V	4.5 - 7.0	4.5 - 16.5	4.5 - 7.0	4.5 - 16.5
CURRENT	125µA	125µA	75µA	75µA

BANDGAP VOLTAGE REFERENCES:

(with power down (internal bias))

CELL NAME	BGP1V2	BGP1V2H	BGP1V2LV	BGP1V2T	BGP1V2HT	BGP1V2LT
TRIM	NO	NO	NO	4BIT	4BIT	4BIT
VOLTAGE	1.23±6%	1.23±6%	1.23±6%	1.23±1%	1.23±1%	1.23±1%
TEMPCO	100ppm	100ppm	100ppm	200ppm	200ppm	200ppm
VOLTCO	1000ppm	1000ppm	1000ppm	1000ppm	1000ppm	1000ppm
SUPPLY V	4.5 - 16.5	7.0 - 16.5	4.5 - 7.0	4.5 - 16.5	7.0 - 16.5	4.5-7.0
CURRENT	250µA	250µA	250µA	250µA	250µA	250µA

N1600 Design Flow



STRATEGIC CAPABILITIES

WORKSTATION SUPPORT

EXAR supports customer design by providing true mixed mode simulation libraries for the Viewlogic™ CAE environments. This includes schematic entry symbols, intelligent simulation models, environmental configuration files, and design database translation programs to EXAR's internal format. Hardware and software requirements are as follows:

Viewlogic Designs

Hardware Requirements: Any hardware presently supported by Viewlogic. Currently this includes 80386 PC AT compatible and Sun™ workstations. A multitasking system is required for simultaneous mixed mode simulation but separate analog and digital simulations can be done on any system.

Software Requirements: The Workview^TM environment software with the Viewdraw, Viewsim, and Viewwave options. Also required for simultaneous analog and digital simulation is either PSPICE or HSPICE combined with either Viewsim A/D PSPICE or Viewsim A/D HSPICE respectively plus the XR VIEWLOGIC/AD N1600 cell library. Additional software required for separate analog and digital simulation is either PSPICE or HSPICE combined with either the XR PSPICE model file or the XR HSPICE model file respectively, plus the XR VIEWLOGIC/SPICE N1600 cell library.

CUSTOM SWITCHED CAPACITOR CIRCUITS

Exar has developed a broad line of custom switched capacitor circuits that are used to perform all of the classical signal processing functions in datacommunications, telecommunications, spectrum analysis, sonar, and general purpose applications.

Exar process technology includes a 2 micron double poly, double metal CMOS process capable of implementing analog, digital and EEPROM. With this technology, Exar can implement switched capacitor circuits with bandwidths exceeding 1 MHz. Exar has developed the first IF filter with a center frequency of 455 KHz utilizing CMOS switched capacitor technique.

The basic element of a switched capacitor filter is a switched capacitor integrator that utilizes a capacitor and a pair of transistors (forming a switch) to act as a resistor. The value of this "resistor" is dependent on the frequency of the clock controlling the switch and the value of capacitor. The transfer function ultimately depends on the ratio of that capacitor to the feedback capacitor connected across an opamp. In MOS technology, this ratio can be very accurately controlled. Overall, switched capacitor technology brings with it savings in silicon area, less complexity in design, and stability over time and temperature.

Switched capacitor technology is used to implement the basic filter types of lowpass, bandpass, highpass, allpass and notch (band reject). Mathematical approximations are used to make filter functions in real life. There are four basic approximations:

Butterworth: Maximally flat with good overshoot response and medium roll off.

Chebyshev: Equiripple in passband with steep roll off.

Elliptical: Equiripple in both the passband and the reject band with monotonically decreasing characteristics after cutoff.

Bessel: Droopy amplitude response in passband but with linear phase and good overshoot response.

APPLICATIONS OF SWITCHED CAPACITOR TECHNOLOGY

Exar has successfully developed many custom programs utilizing switched capacitor technology. Major application areas that utilize switched capacitor circuits are as follows:

* Modems
* Videophones
* Disk drive/VCR servomechanisms
* Cellular telephones
* Sensors
* Speech Processing
* Audio/Video filters
* DSP front ends
* Cordless telephones
* Data converters

All of the above applications make use of Exar's switched capacitor expertise to develop mixed-mode integrated circuits.

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DATA COMMUNICATION PRODUCTS 3

MASS STORAGE PRODUCTS 4

ADVANCED CONSUMER PRODUCTS 5

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MILITARY GRADE PRODUCTS 7

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EXAR ...the analog plus™company

MILITARY GRADE PRODUCTS

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XR-2209 Precision Oscillator 7-43
XR-2211 FSK Demodulator/Tone Decoder 7-45
XR-2212 Precision Phase-Locked Loop 7-47
XR-2240 Programmable Timer Counter 7-49
XR-2567 Dual Monolithic Tone Decoder 7-51
XR-8038 Precision Waveform Generator 7-53
XR-88C681/68C681 DUART 7-59
XR-82C684 QUART 7-67

PRODUCT ORDERING INFORMATION

Part Identification

XX	XXXXX	X	X	883
Manufacturer's Prefix Type	Basic Outline	Case Finish	Lead	Screening

Case Outline (See MIL-M-38510H, Figure C-1)

P = 8 Lead Ceramic DIP
E = 16 Lead Ceramic DIP
C = 14 Lead Ceramic DIP
Q = 40 Lead Ceramic DIP
L = 24 Lead Ceramic DIP
Y = 28 Lead Ceramic DIP
X = 44 Lead Ceramic Leadless Chip Carrier
Z = 32 Lead Ceramic Leadless Chip Carrier

Lead Finish (See MIL-M-38510H,)

A = Hot Solder DIP
C = Gold Plate (used for LCC packages only)

Screening

Per = MIL-STD-883, Method 5004 Class B Devices which includes Burn-in and electrical test at -55°C to +125°C.

Example: XR146EA883

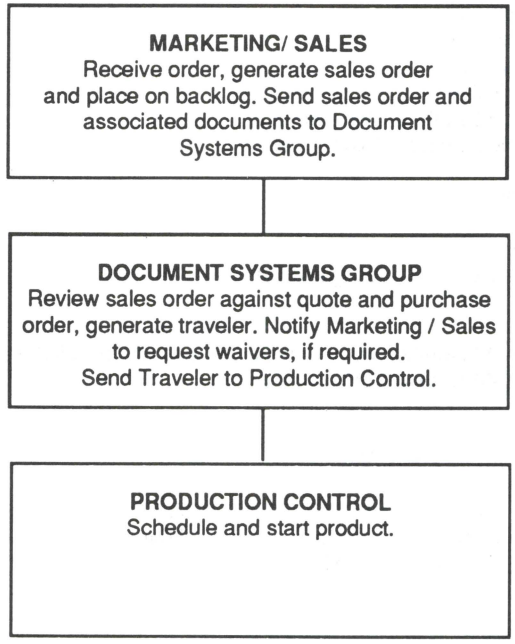
XR	146	E	A	883
Manufacturer's Prefix Type	Basic Outline	Case Finish	Lead	Screening

XR = EXAR Corporation

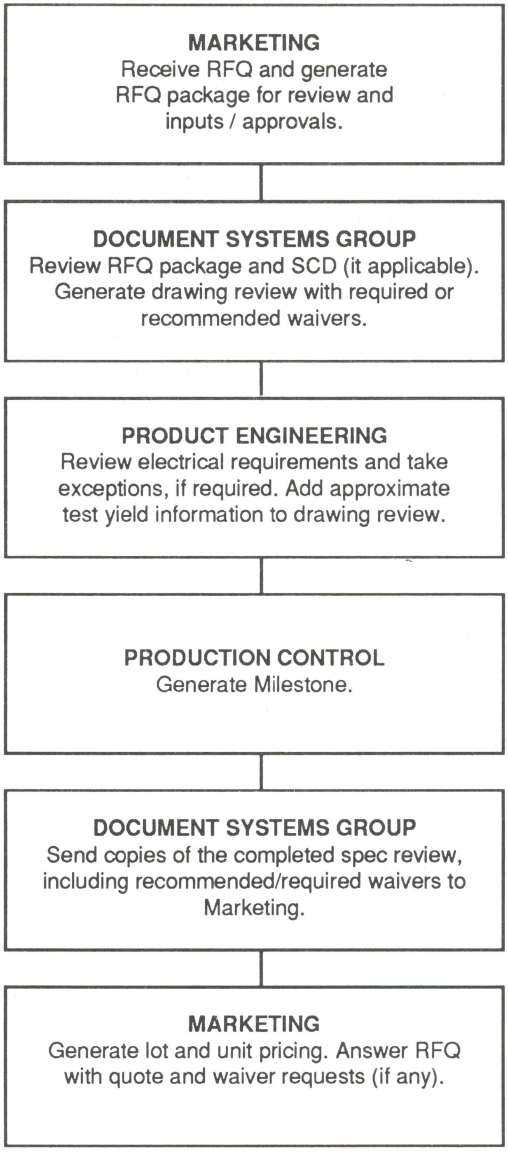
DOCUMENTATION SYSTEMS

Documentation Systems maintains a program to ensure that the revision level of documents is correct for the design, manufacture and test of product. This program includes change control notification and the maintenance of historical records for documents.

Documentation Systems also reviews customer specifications and purchase orders and generates customized internal travelers to assure compliance to customer requirements.



RFQ FLOW FOR MILITARY PRODUCT



CLASS B 883 SCREENING FLOW



QUALITY CONFORMANCE INSPECTION MIL-STD-883, METHOD 5005, GROUPS A, B, C AND D

EXAR will be performing Method 5005 Q.C.I. in accordance with MIL-M-38510. Group A consists of sample electrical testing and is performed on each lot. Group B consists of assembly related construction testing and is also performed on each lot. Group C is primarily a test of die reliability. Group C is performed on one lot of each microcircuit group for each twelve months of wafer fabrication. Group D is performed on one lot of each package type for twelve months of production. The twelve month time period for Group D is based on date of seal. The date of seal also determines the date code for the lot.

EXAR will maintain Group A and Group B attributes data for each lot of 883 devices. EXAR will also have generic test data for Group C and Group D for each lot of 883 devices. Generic Group C and Group D attributes data may not be from the same lot as the production (shippable) parts. However, generic Group C attributes data will be from a device lot in the same microcircuit group as the production lot. The data will fall within the 12 month time frame. Similar generic Group D generic test data will be from a lot with the same package type as the production lot. The data will fall within the 12 month time frame.

Group A and B attributes data as well as generic Group C and D generic attributes will be available at a nominal charge for all EXAR 883 product. Customer requirements for QCI testing or attributes are best negotiated at the time of RFQ. Please consult your EXAR distributor, sales representative or the factory for details.

SOURCE INSPECTION

Source inspection is the surveillance by a customer's quality representative at the manufacturer's plant of devices being screened by the manufacturer. There are several points in the screening process where customers may request source inspection. The most popular is a final source inspection which typically includes a review of all the documentation for the lot and witnessing electrical test on a sample basis. Other points for source inspection, can be pre-cap visual inspection, post-cap visual inspection, burn-in and environmental testing.
It is Exar policy to charge for all source inspections per source point and per lot. It is advisable to request source inspection at the time a purchase order is placed or before.

DATA CAPABILITY

With each shipment of Exar 883 product the customer will receive a Certificate of Conformance. An example of this Certificate is shown on page 6-11. Also upon request, Method 5005 Group A and B attributes data is available at no charge. 100% Attributes data indicates the total number of devices subjected to and passing or failing the various screening steps. Generic attributes data is available for Method 5005, Group C and D upon request at a nominal charge.

Variables data, commonly known as read and record data, gives actual parametric values measured for each device. Variables data is not available unless specifically requested prior to placing an order. There is an extra charge for variables data.

For devices built to a customer's source control drawing Group A and B attributes data is available upon request at no charge. However if Group C and D attributes data is required for a customer's specific lot and generic data is not sufficient or available then an extra charge will be assessed. Again, customers are asked to clarify all data requirements prior to placing an order. Please consult the factory for further details.

MIL-STD-883D

GROUP A electrical tests for classes S and B Devices. 1/

Subgroups 2/ Quantity/accept no. = 116/0 3/ 4/ 5/
Subgroup 1
Static tests at 25°C
Subgroup 2
Static tests at maximum rated operating temperature
Subgroup 3
Static test at minimum rated operating temperature
Subgroup 4
Dynamic tests at 25°C
Subgroup 5
Dynamic test at maximum rated operating temperature
Subgroup 6
Dynamic tests at minimum rated operating temperature
Subgroup 7
Functional tests at 25°C
Subgroup 8A
Functional tests at maximum rated operating temperature
Subgroup 8B
Functional tests at minimum rated operating temperature
Subgroup 9
Switching test at 25°C
Subgroup 10
Switching tests at maximum rated operating temperature
Subgroup 11
Switching tests at minimum rated operating temperature

MIL-STD-883D

GROUP A electrical tests for classes S and B Devices. 1/ *(continued)*

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table I), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified.

3/ The sample plan (quantity) and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in 2/, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub) lot size is less than the required sample size, each and every device in the (sub) lots shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests.subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class S only, if this testing results in a percent defective greater that 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of test/subgroups, as applicable, using a 116/0 sample.

MIL-STD-883D

Table IIb. GROUP B TEST FOR CLASS B. 1/ 2/

Test	MIL-STD-883		Quantity/(accept no) or LTPD
	Method	Condition	
Subgroup 2 3/ a. Resistance to solvents	2015		4(0)
Subgroup 3 a. Solderability 4/	2022 or 2003	Soldering temperature of 245°C ± 5°C	10
Subgroup 5 a. Bond strength 5/ (1) Thermocompression (2) Ultrasonic or wedge (3) Flip-chip (4) Beam lead	2011	 (1) Test condition C or D (2) Test condition C or D (3) Test condition F (4) Test condition H	15

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electricals and provided the rejects are exposed to the full temperature/ time exposure of burn-in.

2/ Subgroups 1,4,6,7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.

3/ Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.

4/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall be less than 3 devices be used to provide the number of leads required.

5/ Test samples for bond strength may, at all manufacturers option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection, specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

MIL-STD-883D

GROUP C (DIE-RELATED TEST) (FOR CLASS B ONLY)

Test 1/	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 1 a. Steady state life test b. End-point electrical parameters	1005	Test condition to b specified (1,000 hours at 125°C or equivalent) in accordance with table 1 of method 1005	5

MIL-STD-883D

GROUP D (PACKAGE RELATED TEST) (FOR ALL CLASSES)

Test 1/	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 1 2/			
a. Physical dimensions	2016		15
Subgroup 2 2/			
a. Lead integrity 3/	2004	Test condition B_2 (lead fatigue)	5
b. Seal 4/			
(1) Fine	1014	As applicable	
(2) Gross			
Subgroup 3 5/			
a. Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum.	15
b. Temperature cycling	1010	Test condition C, 100 cycles minimum.	
c. Moisture resistance 6/	1004		
d. Visual examination		In accordance with visual criteria of method 1004 and 1010	
e. Seal	1014	As applicable	
(1) Fine			
(2) Gross 7/			
(f) End-point electrical parameters 8/		As specified in the applicable device specification	
Subgroup 4 5/			
a. Mechanical shock	2002	Test condition B minimum	15
b. Vibration, variable frequency	2007	Test condition A minimum	
c. Constant acceleration	2001	Test condition E minimum (see 3), Y1 orientation only	
d. Seal	1014	As applicable	
(1) Fine			
(2) Gross			
e. Visual examination	9/		
f. End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5 2/			
a. Salt atmosphere 6/	1009	Test condition A minimum	15
b. Visual examination		In accordance with visual criteria of method 1009	
c. Seal	1014	As applicable	
(1) Fine			
(2) Gross			

see footnotes at end of table.

MIL-STD-883D

GROUP D (PACKAGE RELATED TEST) (FOR ALL CLASSES)

Test 1/	MIL-STD-883		Quantity/(accept no.) or LTPD
	Method	Condition	
Subgroup 6 2/ a. Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1) 10/
Subgroup 7 2/ a. Adhesion of lead finish 11/ 12/	2025		15
Subgroup 8 a. Lid torque 2/ 13/	2024		5(0)

1/. In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitors sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot (s) represented (accepted or rejected) by the data.

2/. Electrical reject devices from that same inspection lot may be used for samples.

3/.The LPTD of 5 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of Subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads use method 2028. For leadless chip carrier packages only, use test condition D and an LTPD of 15 based on the number of pads tested taken from 3 devices minimum.

4/. Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/. Devices used in subgroup 3. "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

6/. Lead bend stress initial conditioning is not required for leadless chip carrier packages.

7/ After completion of the required visual examinations and prior to submittal to method 1014 seal test, the devices may have the corrosion by-products removed by using a bristle brush.

8/. At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

9/. Visual examination shall be in accordance with method 1010 or 1011.

10/. Test three devices; if one fails, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices. from the same lot.

11/. The adhesion of lead finish lest shall not apply for leadless chip carrier packages.

12/. LTPD based on number of leads.

13/. Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., whenever frit seal establishes hermeticity or package integrity).

EXAR
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QUALITY CONTROL
DELIVERABLE DOCUMENTATION CHECKLIST
AND
CERTIFICATE OF CONFORMANCE

PART NO. AND REV.	SALES ORDER NO:	QUANTITY SHIPPED:
CUSTOMER NAME:	PURCHASE ORDER NO:	PRODUCT I.D. CODE:
ADDRESS:		
CUSTOMER DETAIL DWG. NO. AND REV.	CUSTOMER PART NO:	DATE CODE:
CUSTOMER GENERAL DWG. NO. AND REV.	LOT NUMBER/WAFER RUN NO:	TRAVELOG NO:
PRODUCT ASSURANCE LEVEL:		

SAMPLE

DOCUMENTATION ITEM	Req'd	N/A	See Remark	DOCUMENTATION ITEM	Req'd	N/A	See Remark
CUSTOMER WAIVER(S)				SEM PHOTOS AND REPORT			
CUSTOMER SOURCE INSPECTION (CSI)				X-RAY PHOTOS AND REPORT			
GOVERNMENT SOURCE INSPECTION (GSI)				DESTRUCT UNIT SAMPLES			
TEST DATA				ADDITIONAL SAMPLES			
GENERIC DATA				SPECIAL PACKAGING			
QUALITY CONFORMANCE TESTS (GRP A, B, C & D)				SPECIAL MARKING ON PARTS			
FAILURE ANALYSIS REPORT				SPECIAL LABELING ON CONTAINER			
FORM DD 250 & 1149							

REMARKS:

CERTIFICATE OF CONFORMANCE

We certify that the articles and/or services listed and shipped herewith under your purchase order mentioned above have been inspected and are in full requirements of said purchase order and the drawings and specifications applicable to that order. We certify that inspection evidence, including test data, necessary to substantiate this certification is available from our files.

EXAR Corporation

QUALITY CONTROL _____ STAMP _____ SHIPPING DATE _____

200336

MICROCIRCUIT GROUP ASSIGNMENTS
PER 38510 APPENDIX E

Microcircuit Group 49 - 146 (bipolar op amps)

Microcircuit Group 54 - 2240 (timers)

Microcircuit Group 52 - 1524, 1543 (regulators)

Microcircuit Group - Tone Decoders - 567, 567A, L567, 2567

Microcircuit Group - Function Generator - 2206, 2207, 2209, 8038

Microcircuit Group - Phase Locked Loops - 210, 2211, 2212, 2208

Microcircuit Group - UARTs - 68C681, 88C681, 82C684



NOTES



Programmable Quad Operational Amplifiers

GENERAL DESCRIPTION

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op-amps on a monolithic chip. The use of external bias setting resistors permit the user to program gain-bandwidth product, supply current, input bias current, input offset current, input noise and the slew rate.

The basic XR-146 family of circuits offer partitioned programming of the internal op-amps where one setting resistor is used to set the bias levels in the three op-amps, and a second bias setting is used for the remaining op-amp.

FEATURES

Programmable
Micropower operation
Low noise
Wide power supply range
Class AB output
Ideal pin out for biquad active filters
Overload protection for input and output
Internal frequency compensation

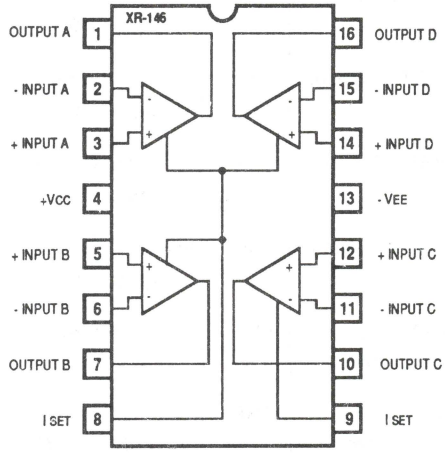
APPLICATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ~= 50 nA (I_{SET}/10 μA)

I_{SET} = Current into pin 8, pin 9 (see schematic)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-146	±22V
Differential Input Voltage	
XR-146	±30V
Common Mode Input Voltage	
XR-146	±15V
Power Dissipation	
XR-146	900 mW
Output Short Circuit Duration	
XR-146	Indefinite
Maximum Junction Temperature	
XR146	+150°C
Storage Temperature Range	
XR-146	–65°C to + 150°C

Rev-A

7

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-146

TEST	SYMBOL	CONDITIONS	TEMPERATURE	MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	I_{CC}	Vs =±15V	T_A = +25°C		2.00	mA	1
		I_{SET} = 10µA	-55°C≤T_A≤+125°C		2.00	mA	2,3
Supply Current	I_{CC}	Vs = ±22V I_{SET} = 10µA	T_A = +25°C		4.00	mA	1
Input Offset Voltage	Vos	Vs=±15V, Rs=50Ω	T_A = +25°C		5.00	mV	1
		I_{SET} = 10µA	-55°C≤T_A≤+125°C		6.00	mV	2,3
Input Bias Current	Ib	Vs=±15V, Rs=10KΩ	T_A = +25°C		100	nA	1
		I_{SET} = 10µA	-55°C≤T_A≤ + 125°C		100	nA	2,3
Input Offset Current	Ios	Vs=±15V, Rs=100KΩ	T_A = +25°C		20	nA	1
		I_{SET} = 10µA	-55°C≤T_A≤ +125°C		25	nA	2,3
Power Supply Rejection Ratio	PSRR	Rs = 10KΩ ±10V≤ Vs≤ ±15V	T_A = +25°C -55°C≤T_A≤+125°C	76	100	uV/V dB	1 2,3
Common Mode Rejection Ratio	CMRR	VCM = ±13.5V Vs=±15V, RL=10KΩ	T_A = +25°C -55°C≤T_A≤+125°C	80 70		dB dB	1 2,3
Large Signal Voltage Gain	AVO	Vo=±10V, Rs =50Ω Vs=±15V, R_L=10KΩ Vo=±10V Vs=±15V, RL=10KΩ	T_A = +25°C -55°C≤T_A≤+125°C	100 50		V/mV V/mV	4 5,6
Output Voltage - Swing	Vo	RL = 10KΩ Vs=±15V, Rs =125Ω Vs=±15V, RL=10KΩ	T_A = +25°C -55°C≤T_A≤+125°C	±12 ±12		V V	4 5,6
Short Circuit Current	Isc	Vs=±15V, Rs=50Ω	T_A = +25°C	5	30	mA	1
Supply Current	Icc	Vs=±15V, I_{SET}=1µA	T_A = +25°C		250	µA	1
Input Offset Voltage	Vos	Rs = 50Ω, Vs=±15V I_{SET} = 1µA	T_A = +25°C		5.00	mV	1
Input Bias Current	Ib	Rs=10 KΩ, Vs=±15V I_{SET} = 1µA	T_A = +25°C		20	nA	1
Input Offset Voltage	Vos	Rs=50Ω, Vs=±15V I_{SET} = 10µA	T_A = +25°C		5.00	mV	1
Common Mode Rejection Ratio	CMRR	Rs = 50Ω, Vs = 1.5V VCM = ±0.7V	T_A = +25°C	60		dB	1
Output Voltage - Swing	Vo	RL=10KΩ, Rs=50Ω Vs=±1.5V,I_{SET}=10µA	T_A = +25°C	10.6		V	4

FSK Modulator/Demodulator

GENERAL DESCRIPTION

The XR-210 is a highly versatile monolithic phase-locked loop system, especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters, and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accommodate analog signals between 300μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range	0.5 Hz to 20 MHz
Wide Supply Voltage Range	5V to 26V
Digital Programming Capability	
RS-232C Compatible Demodulator Output	
DTL, TTL and ECL Logic Compatibility	
Wide Dynamic Range	300μV to 3V
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	±1% to ±50%
Good Temperature Stability	200 ppm/°C
High-Current Logic Output	50 mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

APPLICATIONS

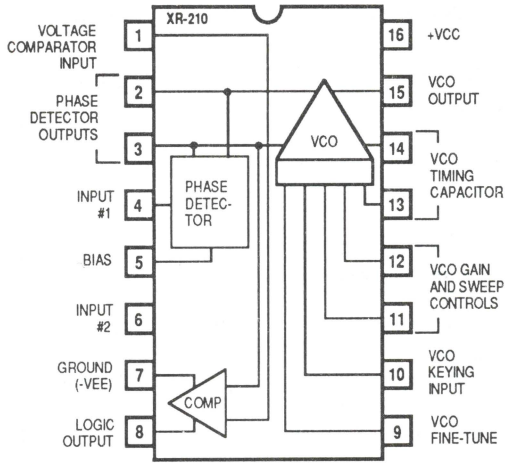
Data Synchronization
Signal Conditioning
FSK Generation
Tone Decoding
Frequency Synthesis
FSK Demodulation
Tracking Filter
FM Detection
FM and Sweep Generation
Wideband Discrimination

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate Above +25°C	6.0 mW/°C
Storage Temperature	- 65°C to + 150°C

Rev-C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-210 is made up of a stable wide-range voltage- controlled oscillator (VCO), exclusive OR gate type phase detector, and an analog voltage comparator. The VCO, which produces a square wave as an output, is either used in conjunction with the phase detector to form a phase-locked loop (PLL) for FSK demodulation and tone detection or as a generator in FSK modulation schemes. The phase detector when used in the PLL configuration produces a differential output voltage with a 6 KΩ output impedance, which when capacitively loaded forms a single pole loop filter. The voltage comparator is used to sense the phase detector output and produces the output in the FSK demodulation connection.

7

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-210

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	I_{CC}	V_{CC} = ±6V	T_A = +25°C	5.0	16.0	mA	1
			-55°C≤T_A≤+125°C	5.0	20.0	mA	2,3
Supply Current	I_{CC}	V_{CC} = ±13V	T_A = +25°C		26.0	mA	1
			-55°C≤T_A≤+125°C		26.0	mA	2,3
VCO Power Supply Stability	PSR	±6V≤V_{CC}≤±12V	T_A =+25°C		0.5	%/V	9
			-55°C≤T_A≤+125°C		1.0	%/V	10,11
VCO Sweep Range	FSW		T_A = +25°C	5:1			9
			-55°C≤T_A≤+125°C	3:1			10,11
VCO Duty Cycle Asymmetry	DC		T_A = +25°C		±3	%	9
			-55°C≤T_A≤+125°C		±10	%	10,11
Phase Detector Output Offset Voltage		Measured Across Pin 1 and Pin 3,VIN =0	T_A = +25°C		±150	mV	1
			-55°C≤T_A≤+125°C		±150	mV	2,3
Logic Output Leakage Current	I_{OH}	V_{CC} = ±12V	T_A = +25°C		10.0	µA	1
		V_{CC} = ±6V	-55°C≤T_A≤+125°C		100.0	µA	2,3
Logic Output Low Voltage	V_{OL}	I_L = 10 mA	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.7	V	2,3
Logic Output Sink Current	I_{SINK}	V_O≤1V	T_A =+25°C	30		mA	1
			-55°C≤T_A≤+125°C	25		mA	2,3

Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01 Hz to 500 kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enables the system to distinguish between the presence or absence of an input signal at the center frequency.

FEATURES

Bandwidth adjustable from 0 to 14%.
Logic compatible output with 100 mA current sinking capability
High stable center frequency.
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false signals
High rejection of out-of-band signals and noise
Frequency range adjustable over 20:1 range by external resistor.

APPLICATIONS

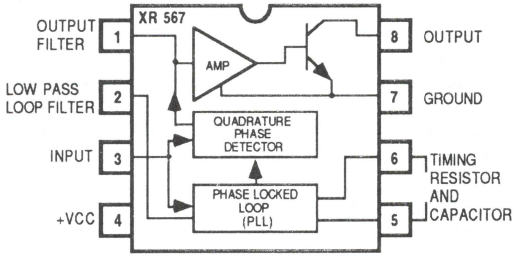
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Derate Above +25°C	2.5 mW/°C
Temperature	
Storage	-65°C to + 150°C

Rev-B

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-567 monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependent upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is + VCC (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

In applications requiring two or more 567-type devices, consider the XR-2567 dual tone decoder. Where center frequency accuracy and drift are critical, compare the XR-567A. Investigate emplopying the XR-L567 in low power circuits.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-567

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	TA = +25°C		8.00	mA	1
			-55°C≤TA≤+125°C		9.80	mA	2,3
Supply Current Quiescent	Icc	Vcc = +9v	TA = +25°C		20.00	mA	1
			-55°C≤TA≤+125°C		18.00	mA	2,3
Highest Center Frequency	Fc	Vcc = +9V Vin = 300 mVrms	TA = +25°C	100		KHz	9
			-55°C≤TA≤+12E°C	100		KHz	10,11
Center Frequency Drift with Supply	DRFT	4.75V≤Vcc≤6.75V	TA = +25°C		1.00	%/V	9
			-55°C≤TA≤+125°C		6.00	%/V	10,11
Output Saturation Voltage	VSAT	Ic = 30 mA Vin = 30 mVrms	TA = +25°C		0.4	V	1
			-55°C≤TA≤+125°C		0.4	V	2,3
Output Saturation Voltage	VSAT	Ic = 100 mA Vin = 30 mVrms	TA = +25°C		1.0	V	1
			-55°C≤TA≤+125°C		1.2	V	2,3
Output Leakage Current	IOL	Vin = 7.5 mVrms	TA = +25°C		25	µA	1
			-55°C≤TA<+125°C		50	µA	2,3
Largest No Output Input Voltage	VIL		TA= +25°C	10		mVrms	7
			-55°C≤TA≤+125°C	5		mVrms	8
Smallest Detectable Input Voltage	VIS		TA = +25°C		25	mVrms	7
			-55°C≤TA≤+125°C		50	mVrms	8
Largest Detection Bandwidth	LDEW		TA = +25°C	12.0	16.0	%	4
			-55°C≤TA≤+125°C	7.0	19.0	%	5,6
Largest Detection Bandwidth Skew	SKEW		TA = +25°C		2.0	%	4
			-55°C≤TA≤+125°C		4.0	%	5, 6
Supply Current Activated	ICC	Vcc = +5V	TA = +25°C		13.0	mA	1
			-55°C≤TA≤+125°C		14.5	mA	2,3

Precision Tone Decoder

GENERAL DESCRIPTION

The XR-567A provides all the necessary circuitry for constructing a variety of tone detectors and frequency decoders. Phase-locked loop circuit techniques are used to provide operation from 0.01 Hz tp 500 kHz. The circuit also features an input preamp, a high-current logic output, and programmable output delay.

The XR-567A, available in an 8-Pin DIL package, is designed to offer improved frequency accuracy and drift characteristics over the standard industry 567. These changes offer improved overall circuit performance, while reducing initial circuit adjustments.

FEATURES

Programmable Detection Bandwidth	0% to 14%
Logic Output	100 mA
Wide Center Frequency Range	0.01 Hz to 500 kHz
High Rejection of Out-of-Band Signals and Noise	
Direct Replacement for standard 567	
Inherent immunity to out-of-band signals & noise	

APPLICATIONS

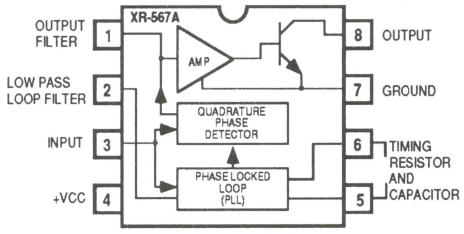
Tone Detection
Touch-Tone ® Decoding
Communications Paging
Ultrasonic Remote Control
Precision Oscillator
Wireless Intercom
Carrier-Tone Transceiver
FSK Demodulation
Dual Time Constant Tone Detector

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation	
Ceramic Package	385 mW
Derate above 25°C	2.5 mW/°C
Storage Temperature Range	-65°C to + 150°C

REV-B

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-567A is an improved version of the popular 567 tone decoder. Center frequency accuracy is guaranteed by design modifications and testing to 5%, and is typically better than 2%. Temperature drift of the center frequency is also improved. Thus, in most applications, no trimming is required.

The XR-567A monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Band- width is adjustable from 0% to 14% of the center frequency. Pin 4 is + VCC (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in band signal triggers the device.

ELECTRICAL PERORMANCE CHARACTERISTICS - XR-567A

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C -55°C≤T_A≤+125°C		8.00 9.80	mA mA	1 2,3
Supply Current Quiescent	Icc	Vcc = +9V	T_A = +25°C -55°C≤T_A≤+125°C		20.00 18.00	mA mA	1 2,3
Supply Current Activated	Icc	Vcc =+5V VIN = 300 mVrms	T_A = +25°C -55°C≤T_A≤+125°C		13.00 14.50	mA mA	1 2,3
Highest Center Frequency	Fc	Vcc = +5V	T_A = +25°C -55°C≤T_A≤+125°C	100 100		KHz KHz	9 10,11
Center Frequency Drift with Supply	DRFT	4.75V≤Vcc≤6.75V	T_A = +25°C -55°C≤T_A≤+125°C		1.00 6.00	%/V %/V	9 10,11
Output Saturation Voltage	VSAT	Ic = 30 mA Vin = 30 mVrms	TA = +25°C -55°C≤T_A≤+125°C		0.4 0.4	V V	1 2,3
Output Saturation Voltage	VSAT	Ic = 100 mA Vin = 30 mVrms	T_A = +25°C -55°C≤T_A≤+125°C		1.0 1.20	V V	1 2,3
Output Leakage Current	I_{OL}	Vin = 7.5 mVrms	T_A = +25°C 55°C≤T_A≤+125°C		25 50	µA µA	1 2.3
Largest No Output Input Voltage	V_{IL}		T_A= +25°C -55°C≤T_A≤+125°C	10 5		mVrms mVrms	7 8
Smallest Detectable Input Voltage	V_{IS}		T_A = +25°C -55°C≤T_A≤+125°C		25 50	mVrms mvrms	7 8
Largest Detection Bandwidth	LDBW		T_A = +25°C -55°C≤T_A≤+125°C	12.0 7.0	16.0 19.0	% %	4 5,6
Largest Detection Bandwidth Skew	SKEW		T_A = +25°C -55°C≤T_A≤+125°C		2.0 4.0	% %	4 5, 6

Micropower Tone Decoder

GENERAL DESCRIPTION

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the XR-L567 can replace the popular 567- type decoder with only minor component value changes. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4 mW at 5 volts. It operates over a wide frequency band of 0.01 Hz to 60 kHz and contains a logic compatible output which can sink up to 10 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

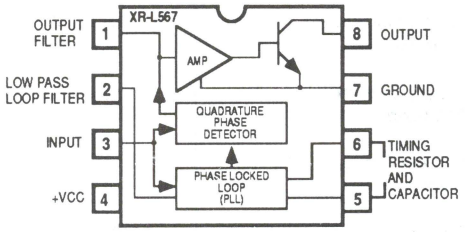
FEATURES

Very Low Power Dissipation (≈ 4 mW at 5V).
Bandwidth Adjustable from 0 to 14%.
Logic Compatible Output with 10 mA Current Sinking Capability
Highly Stable Center Frequency.
Center Frequency Adjustable from 0.01 Hz to 60 kHz.
Inherent Immunity to False Signals.
High Rejection of Out-of-Band Signals and Noise.
Frequency Range Adjustable Over 20:1 Range by External Resistor.

APPLICATIONS

Battery-Operated Tone Detection
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Storage Temperature	-65°C to + 150°C

Rev-A

SYSTEM DESCRIPTION

The XR-L567 monolithic circuit consists of a phase detector low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependant upon the circuitry here. Pin 4 is + VCC (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The XR-L567 is pin-for-pin compatible with the standard XR-567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-L567

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C		1000	µA	1
			-55°C≤T_A≤+125°C		1000	µA	2,3
Supply Current Quiescent	Icc	Vcc = +8V	T_A = +25°C		2000	µA	1
Supply Current Activated	Icc	Vcc = +5V	T_A = +25°C		1400	µA	1
			-55°C≤T_A≤+125°C		2000	µA	2,3
Highest Center Frequency	Fc		T_A = +25°C	10		KHz	9
			-55°C≤T_A≤+125°C	10		KHz	10,11
Center Frequency Drift with Supply	DRFT	4.75V≤Vcc≤8V	T_A = +25°C		2.0	%/V	9
			-55°C≤T_A≤+125°C		3.0	%/V	10,11
Output Saturation Voltage	VSAT	Ic = 2 mA Vin = 25 mVrms Vcc = +5V	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.4	V	2,3
Output Saturation Voltage	VSAT	Ic = 10 mA Vin = 25 mVrms Vcc = +5V	T_A = +25°C		0.6	V	1
			-55°C≤T_A≤+125°C		0.6	V	2,3
Output Leakage Current	I_{OL}	Vin = 7.5 mVrms Vcc = 15V	T_A = +25°C		25	µA	1
			-55°C≤T_A≤+125°C		25	µA	2,3
Largest No Output Input Voltage	V_{IL}	Vcc = +5V	T_A = +25°C	10		mVrms	4
			-55°C≤T_A≤+125°C	10		mVrms	5,6
Smallest Detectable Input Voltage	V_{IS}		T_A = +25°C		25	mVrms	4
			-55°C≤T_A≤+125°C		25	mVrms	5,6
Largest Detection Bandwidth	LDBW		T_A = +25°C	10	18	%	4
			-55°C≤T_A≤+125°C	10	20	%	5,6
Largest Detection Bandwidth Skew	SKEW		T_A = +25°C		3.0	%	4
			-55°C≤T_A≤+125°C		3.0	%	5,6

Pulse-Width Modulating Regulator

GENERAL DESCRIPTION

The XR-1524 family of monolithic integrated circuits contain all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16- pin dual-in-line package is the voltage reference. error. amplifier, oscillator. pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity. transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The XR-1524 is specified for operation over the full military temperature range of -55°C to +125°C.

FEATURES

Pin-for-Pin Replacement for SG-1524/2524/3524
Complete PWM power control circuitry
Single ended or push-pull outputs
Line and load regulation of 0.2%
Total supply current less than 10 mA
Operation beyond 100 kHz

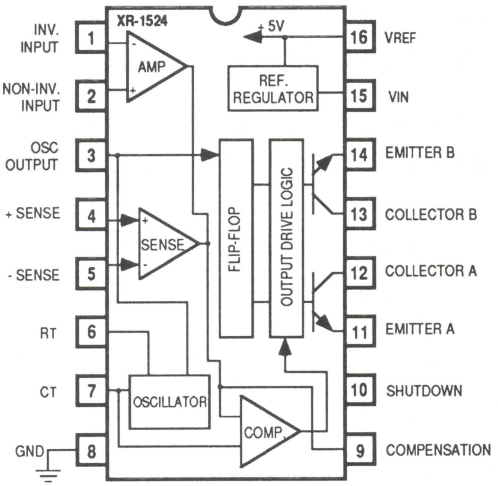
APPLICATIONS

Switching Regulators
Pulse-width Modulated Power Control Systems

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Output Current (each output)	100 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	8 mW/°C
Operating Temperature Range	
XR-1524	-55°C to + 125°C
Storage Temperature Range	-65°C to + 150°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-1524 pulse width modulating regulator is a complete monolithic switching regulator. An internal 5V reference, capable of supplying up to 50 mA to external loads, provides an on-board operating standard. The oscillator frequency and duty cycle are adjusted by an external RC network. Regulation is controlled by an error amplifier which, combined with the sense amplifier, also allows current limiting and remote shutdown functions. The outputs of the XR-1524 are two identical NPN transistors with both emitters and collectors uncommitted. Each output transistor has antisaturation circuitry for fast response and local current limiting set at 100mA.

XR-1524 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	MIN	MAX		
REFERENCE SECTION							
Output Voltage	VREF	VIN = 20V	TA = 25°C	4.8	5.2	V	1
			-55°C≤TA≤+125°C	4.8	5.2	V	2,3
Line Regulation	V_{RLINE}	8V≤V_{IN}≤40V	TA = 25°C		20	mV	1
			-55°C≤TA≤+125°C		20	mV	2,3
Load Regulation	V_{RLOAD}	0mA≤I_L≤20mA	TA = 25°C		50	mV	1
			-55°C≤TA≤+125°C		50	mV	2,3
Short Circuit Current Limit	I_{OS}	V_{REF} = 0	TA = 25°C		150	mA	1
			-55°C≤TA≤+125°C		150	mA	2,3
OSCILLATOR SECTION							
Voltage Stability	Δf_{OSC}	8V≤V_{IN}≤40V	TA = 25°C		1	%	1
			-55°C≤TA≤+125°C		1	%	2,3
ERROR AMPLIFIER SECTION							
Input Offset Voltage	V_{IO}		TA = 25°C		5	mV	1
			-55°C≤TA≤+125°C		5	mV	2,3
Input Bias Current	I_{IB}		TA = 25°C		10	µA	1
			-55°C≤TA≤+125°C		10	µA	2,3
Open Loop Gain	A_{VS}		TA = 25°C	72		db	4
			-55°C≤TA≤+125°C	72		db	5,6
Common Mode Rejection Ratio	CMRR	1.8≤$_{CM}$≤3.4V	TA = 25°C	46		db	4
			-55°C≤TA≤+125°C	46		db	5,6
Output High Level	V_{HI}		TA = 25°C	3.8		V	1
			-55°C≤TA≤+125°C	3.8		V	2,3
Output Low Level	V_{LO}		TA = 25°C		0.5	V	1
			-55°C≤TA≤+125°C		0.5		2,3
CURRENT LIMITING SECTION							
Sense Voltage	V_{SEN}		TA = 25°C	190	210	mV	1
OUTPUT SECTION							
Emitter Output Voltage	V_{EO}	V_{IN} = 20V	TA = 25°C	17		V	1
			-55°C≤TA≤+125°C	17		V	2,3
Saturation Voltage	V_{CE}(SAT)	I_C = 50mA	TA = 25°C		2	V	1
			-55°C≤TA≤+125°C		2	V	2,3
Collector Leakage Current	I_{CEX}	V_{CE} = 40V	TA = 25°C		50	µA	1
			-55°C≤TA≤+125°C		50	µA	2,3
Standby Current	I_{IN}	V_{IN} = 40V	TA = 25°C		10	mA	1
			-55°C≤TA≤+125°C		10	mA	2,3

Power Supply Output Supervisory Circuit

GENERAL DESCRIPTION

The XR-1543 is a monolithic integrated circuit that contains all the functions necessary to monitor and control the output of a power supply system. Included in the 16-pin dual-in-line package is a voltage reference, an operational amplifier, voltage comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage sensing, under-voltage sensing and current limiting, with provisions for triggering an external SCR "crow-bar".

The internal voltage reference on the XR-1543 is guaranteed for an accuracy of 11% to eliminate the need for external potentiometers. The entire circuit may be powered from either the output that is being monitored or from a separate bias voltage.

FEATURES

Over-Voltage Sensing Capability	
Under-Voltage Sensing Capability	
Current Limiting Capability	
Reference Voltage Trimmed	±1%
SCR "Crowbar" Drive	300 mA
Programmable Time Delays	
Open Collector Outputs and Remote Activation Capability	
Total Standby current	Less than 10 mA

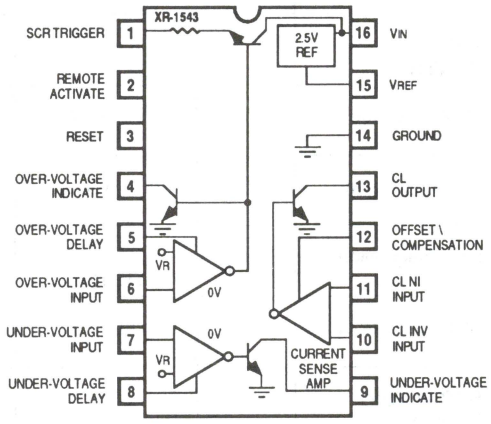
APPLICATIONS

DC/DC Converters
Switch Mode Power Supplies
Power Line Monitors
Linear Power Supplies

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage. VIN	40V
Sense Inputs	VIN
SCR Trigger Current (Note 1)	300 mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50 mA
Power Dissipation (Ceramic)	1000 mW
Derate Above TA = + 25°C	8 mW/°C
Operating Junction Temperature (TJ)	+150°C
Storage Temperature Range	-65°C to + 150°C

FUNCTIONAL BLOCK DIAGRAM



Note 1: At higher input voltages, a dissipation limiting resistor, RG, is required.

SYSTEM DESCRIPTION

An output supervisory circuit, such as the XR-1543, is used to control and monitor the performance of a power supply. In many systems, it is crucial that the supply voltage is always within some minimum and maximum level, to guarantee proper performance, and to prevent damage to the system. It the supply voltage is out of tolerance. it is often desirable to shut down the system or to have some form of indication to the operator or system controller. As well as protecting the system, the power supply sometimes reeds to be protected under short circuit and current overload situations. By providing an SCR "crowbar" on the output of a power supply, it can be shut off under certain fault conditions as well.

The over-voltage sensing circuit (O.V.) can be used to monitor the output of a power supply and provide triggering of an SCR, when he output goes above the prescribed voltage level. The under-voltage sensing circuit (U.V.) can be used to monitor either the output of a power supply or the input line voltage.

XR-1543 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	MIN	MAX		
Supply Current		V_{IN} = 40V	TA = 2°C -55°C≤TA≤+125°C		10 10	mA mA	1 2, 3
Reference Section							
Output Voltage		V_{IN} = 10V	TA = 25°C -55°C≤TA≤+125°C	2.48 2.45	2.52 2.55	V V	1 2, 3
Line Regulation		V_{IN} = 5Vto30V	TA = 25°C -55°C≤TA≤+125°C		5 5	mV mV	1 2, 3
Load Regulation		i_{REF} = 0 to 10mA	TA = 25°C -55°C≤TA≤+125°C		10 10	mV mV	1 2, 3
Short Circuit Current		V_{REF} = 0V	TA = 25°C -55°C≤TA≤+125°C	12 12	40 40	mA mA	1 2, 3
SCR Trigger Section							
Peak Output Current		Tested Go-No Go	TA = 25°C -55°C≤TA≤+125°C		400 400	mA mA	1 2, 3
Peak Output Voltage		V_{IN} = 5V Io = 100mA	TA = 25°C -55°C≤TA≤+125°C	12 12		V V	1 2, 3
Output on Voltage		V_{IN} = 40V	TA = 25°C -55°C≤TA≤+125°C		0.1 0.1	V V	1 2, 3
Remote Activate Current			TA = 25°C -55°C≤TA≤+125°C		800 800	µA µA	1 2, 3
Remote Activate Voltage			TA = 25°C -55°C≤TA≤+125°C		6.0 6.0	V V	1 2, 3
Reset Current			TA = 25°C -55°C≤TA≤+125°C		800 800	µA µA	1 2, 3
Reset Voltage			TA = 25°C -55°C≤TA≤+125°C		6.0 6.0	V V	1 2, 3

COMPARATOR SECTIONS

Input Threshold		Tested Go-No Go Only	TA = 25°C -55°C≤TA≤+125°C	2.45 2.40	2.55 2.60	V V	1 2, 3
Input Bias Current			TA = 25°C -55°C≤TA≤+125°C		1.0 1.0	µA µA	1 2, 3
Delay Saturation			TA = 25°C -55°C≤TA≤+125°C		0.5 0.5	V V	1 2, 3
Delay High Level			TA = 25°C -55°C≤TA≤+125°C	5.0 5.0	8.0 8.0	V V	1 2, 3
Delay Charging Current			TA = 25°C -55°C≤TA≤+125°C	200 200	300 300	µA µA	1 2, 3
Indicate Saturation		I_L = 10MA	TA = 25°C -55°C≤TA≤+125°C		0.5 0.5	V V	1 2, 3
CURRENT LIMIT AMPLIFIER SECTION							
Input Voltage Range		V_{IN} = 10V	TA = 25°C -55°C≤TA≤+125°C		V_{IN} -3V	V	1 2, 3
Input Bias Current			TA = 25°C -55°C≤TA≤+125°C		1.0 1.0	µA µA	1 2, 3
Input Offset Voltage			TA = 25°C -55°C≤TA≤+125°C		10 10	mV mV	1 2, 3
Input Offset Voltage		P_{IN}12 = 10K to GND	TA = 25°C -55°C≤TA≤+125°C	80 80	120 120	mV mV	1 2, 3
CMRR			TA = 25°C -55°C≤TA≤+125°C	60 60		dB dB	1 2, 3
Open Loop Gain			TA = 25°C -55°C≤TA≤+125°C	72 72		dB dB	1 2, 3
Output Saturation Voltage		I_L = 10mA	TA = 25°C -55°C≤TA≤+125°C		0.5 0.5	V V	1 2, 3
Output Leakage Current		V_{OUT} = 40V	TA = 25°C -55°C≤TA≤+125°C		1.0 1.0	µA µA	1 2, 3
Indicate Leakage Current		V_{OUT} = 40V	TA = 25°C -55°C≤TA≤+125°C		1.0 1.0	µA ≤µA	1 2, 3

7

Monolithic Function Generator

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high- stability and accuracy The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range, with an external control voltage, having a very small affect on distortion.

FEATURES

Low-Sine Wave Distortion	0.5%, Typical
Excellent Temperature Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Low-Supply Sensitivity	0.01%V, Typical
Linear Amplitude Modulation	
TTL Compatible FSK Controls	
Wide Supply Range	10V to 26V
Adjustable Duty Cycle	1% to 99%

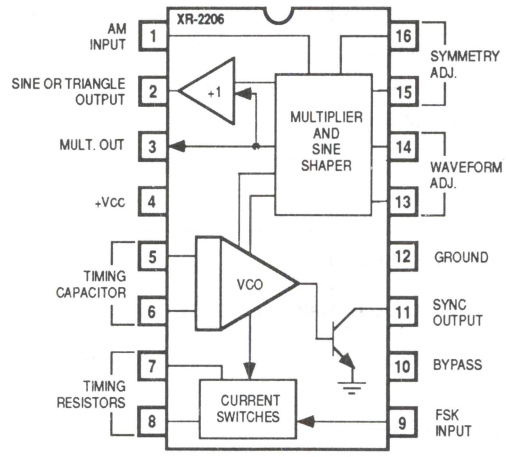
APPLICATIONS

Waveform Generation
Sweep Generation
AM/FM Generation
V/F Conversion
FSK Generation
Phase-Locked Loops (VCO)

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Total Timing Current	6 mA
Storage Temperature	-65°C to + 150°C
Rev-A	

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO actually produces an output frequency proportional to an input current, which is produced by a resistor from the timing terminals to ground. The current switches route one of the timing pins current to the VCO controlled by an FSK input pin, to produce an output frequency. With two timing pins, two discrete output frequencies can be independently produced for FSK Generation Applications.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2206

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	Icc1	Vcc = 12V	TA = +25°C		17.0	mA	1
			-55°C≤TA≤+125°C		17.0	mA	2, 3
Supply Current	Icc2	Vcc = 26V	TA = +25°C		25.0	mA	1
			-55°C≤TA≤+125°C		25.0	mA	2, 3
Squarewave Leakage Current	IL	V11 =26V	TA = +25°C		20	µA	1
			-55°C≤TA≤+125°C		20	µA	2, 3
Squarewave Saturation Voltage	VSAT	IL=2mA	TA = +25°C		0.4	V	1
			-55°C≤TA≤+125°C		0.6	V	2, 3
Reference Bypass Voltage	VREF	AT Pin 10	TA = +25°C	2.9	3.3	V	1
			-55°C≤TA≤+125°C	2.5	3.5	V	2, 3
FSK Input Threshold	VINKEY	Vcc = 12V	TA = +25°C	0.8	2.4	V	1
			-55°C≤TA≤+125°C	0.8	2.4	V	2, 3
Max. Frequency	FMAX	RT = 1Kohm	TA = +25°C	500		KHz	9
		CT = 1000PF	-55°C≤TA≤+125°C	500		KHz	10, 11
Frequency Accuracy	Fo	Vcc = 12V	TA = +25°C	.96	1.04	KHz	9
		CT = 0.01µF	-55°C≤TA≤+125°C	.96	1.04	KHz	10, 11
		RT = 100Kohm					
Frequency Accuracy	Fo	Vcc = 12V	TA = +25°C	9.0	11.0	KHz	9
		CT = 0.01µF	-55°C≤TA≤+125°C	9.0	11.0	KHz	10, 11
		RT = 1OKohm					
Frequency Accuracy Low Voltage		Vcc = 10V	TA = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤TA≤+125°C	4.0	6.0	KHz	10, 11
		CT =.01µF					
		VINKEY = 2.4V					
Frequency Accuracy Low Voltage		Vcc = 10V	TA = +25°C	4.0	6.0	KHz	9
		CT =.01µF	-55°C≤TA≤+125°C				10, 11
		VINKEY = 0.8V					
Frequency Accuracy High Voltage		Vcc = 26V	TA = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤TA≤+125°C	4.0	6.0	KHz	10, 11
		CT =.01µF					
		VINKEY = 2.4V					
Frequency Accuracy High Voltage		Vcc = 26V	TA = +25°C	4.0	6.0	KHz	9
		RT = 20Kohm	-55°C≤TA≤+125°C	4.0	6.0	KHz	10, 11
		CT =.01µF					
		VINKEY = 0.8V					
Supply Sensitivity	PSRR	Vcc = 10 to 20V	TA = +25°C		0.1	%/V	9
		RT = 20Kohm	-55°C≤TA≤+125°C		0.1	%/V	10, 11
		CT = 0. 01 µF					
		VINKEY =2.4V					

Supply Sensitivity	PSRR	Vcc 10 to 20V RT = 20Kohm CT = 0.01µF VINKEY = 0.8V	TA = +25°C -55°C≤TA≤+125°C		0.1 0.1	%/V %/V	9 10, 11
Low Timing Resistor	FMAX	RT = 1 KΩ CT = 100pF	TA = +25°C -55°C≤TA≤+125°C	500 500		KHz KHz	9 10, 11
High Timing Resistor	FMIN	RT = 2MΩ CT = 1000pF	TA = +25°C -55°C≤TA≤+125°C	400 400	600 600	Hz Hz	9 10, 11
Sweep Range		FMAX/FMIN	TA = +25°C -55°C≤TA≤+125°C	1000 1000			9 10, 11
Sine Wave Amplitude		RT = 100KΩ CT =.01µF	TA = +25°C -55°C≤TA≤+125°C	40 20	80 120 Kohm	mV/ Kohm mV/	4 5, 6
AM Sine Wave Amplitude		RT= 100KΩ VAM = 3V CT =.01µF	TA = +25°C -55°C≤TA≤+125°C	30 10	60 100 Kohm	mV/ Kohm mV/	4 5, 6
AM Sine Wave Amplitude		AT = 100KΩ VAM = 9V CT =.01µF	TA = +25°C -55°C≤TA≤+125°C	30 10	60 100 Kohm	mV/ Kohm mV/	4 5, 6
AM Sine Wave Amplitude Symmetry			TA = +25°C -55°C≤TA≤+125°C		10 10	mV mV	4 5, 6
Symmetry Adjust Resistor	R15	Pin 15	TA = +25°C -55°C≤TA≤+125°C	1.7 1.5	2.6 3.0	Kohm Kohm	4 5, 6
Symmetry Adjust Resistor	R16	Pin 16	TA = +25°C -55°C≤TA≤+125°C	1.7 1.5	2.6 3.0	Kohm Kohm	4 5, 6
Symmetry Adjust Balance		R16-R15	TA = +25°C -55°C≤TA≤+125°C	-0.1 -0.2	0.1 0.2	Kohm Kohm	4 5, 6

Voltage-Controlled Oscillator

GENERAL DESCRIPTION

The XR-2207 is a monolithic voltage-controlled osciliator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (3000:1 Typical)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.1%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

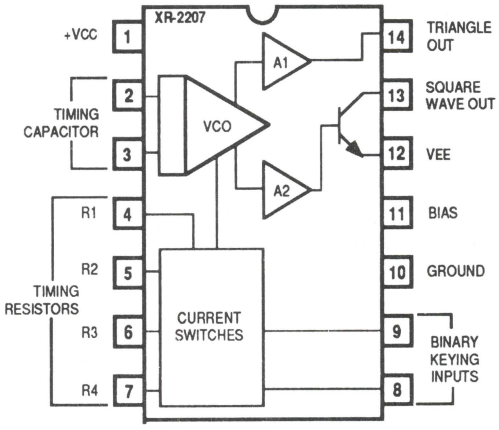
FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Storage Temperature Range	-65°C to + 150°C

Rev-B

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2207 utilizes four main functional blocks for frequency generation. These are a voltage controlled oscillator (VCO), four current switches which are activated by binary keying inputs, and two buffer amplifiers for triangle and squarewave outputs. The VCO is actually a current controlled oscillator which gets its input from the current switches. As the output frequency is proportional to the input current, the VCO produces four discrete output frequencies. Two binary input pins determine which timing currents are channelled to the VCO- These currents are set by resistors to ground from each of the four timing terminals.

The triangle output buffer provides a low impedance output (10Ω) TYP) while the squarewave is an open-collector type. A programmable reference point allows the XR-2207 to be used in either single or slip supply configurations.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2207

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	
Supply Current	Icc1	Positive, Vcc = ±6V	TA = +25°C -55°C≤TA≤+125°C		7.0 12.0	mA mA	1 2,3
Supply Current	IEE1	Negative, Vcc = ±6V	TA = +25°C -55°C≤TA≤+125°C	-6.0 -11.0		mA mA	1 2,3
Supply Current	Icc2	Positive, Vcc = ±13V	TA = +25°C -55°C≤TA≤+125°C		19.0 20.0	mA mA	1 2,3
Supply Current	IEE2	Negative, Vcc = ±13V	TA = +25°C -55°C≤TA≤+125°C	-19.0 -20.0		mA mA	1 2,3
Squarewave Output Leakage Current	IL	Vcc = ±13V Vcc = ±10V	TA = +25°C -55°C≤TA≤+125°C		100 200	µA µA	 2,3
Sqarewave Output Low Voltage	VOL	Referenced to VEE Vcc = ±6V	TA = +25°C -55°C≤TA≤+125°C		0.40 1.00	V V	1 2,3
Squarewave Output Amplitude	Vo	Vcc = ±6V	TA = +25°C -55°C≤TA≤+125°C	11.0 11.0		V V	4 5,6
Frequency Accuracy	fSTD	CT =5000pF RT = 20 Kohm	TA = +25°C -55°C≤TA≤+125°C	9.70 9.50	10.30 10.50	KHz KHz	9 10,11
Power Supply Stability		±6V≤Vcc ≤±13V	TA = +25°C -55°C≤TA≤+125°C		10.0 11.0	% %	9 10,11
Frequency Matching	fXX	VKEYA = 1.4V VKEYB = 1.4V f = 10 KHz	TA = +25°C Only		5	%	9
Frequency Matching	fXX	VKEYA = 2.8V VKEYB = 1.4V f = 10 KHz	TA = +25°C Only		5	%	9
Frequency Matching	fXX	VKEYA = 2.8V VKEYB = 2.8V f = 20 KHz	TA = +25°C Only		5	%	9
Frequeney Matching	fXX	VKEYA = 1.4V VKEYB = 2.8V f = 20 KHz	TA = +25°C Only		5	%	9
Upper Frequency	fH	CT =500pF RT = 2 Kohm	TA = +25°C -55°C≤TA≤+125°C	500 500		KHz KHz	9 10,11
Sweep Linearity	SWLIN	CT = 5000pF RT = 200 Kohm vs FSTD	TA = +25°C -55°C≤TA≤+125°C		2 4	% %	9 10,11
Minimum Timing Resistor	TMIN	CT =5000pF RT = 1.5 Kohm	TA = +25°C -55°C≤TA≤+125°C	90 85		KHz KHz	9 10,11

Maximum Timing Resistor	T_{RMAX}	CT = 5000pF RT = 2 Mohm R_T = 200KΩ	 T_A = +25°C -55°C≤T_A≤+125°C	 80 800	 120 1200	 Hz	 9 10,11
Sweep Range	S_{WRNG}	T_{RMIN}/T_{RMAX}	T_A = +25°C -55°C≤T_A≤+125°C	1000 100			9 10,11
Triangle Wave Output Amplitude	T_{VPP}[1]	Vcc ±6V CT = 5000pF RT = 20 Kohm	T_A = +25°C -55°C≤T_A≤+125°C	4 2		V	4 5,6
Triangle Wave Output Amplitude	T_{Vpp}[2]	Vcc = ±13V CT = 5000pF RT = 20 Kohm	T_A = +25°C -55°C≤T_A≤+125°C	7 7		V	4 5,6
Triangle Wave	T_{WLIN}	Vcc = ±6V CT = 5000 pF RT = 20 Kohm	T_A = +25°C -55°C≤T_A≤+125°C		5.0 5.0	% %	9 10,11



NOTES



Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/ buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability.

FEATURES

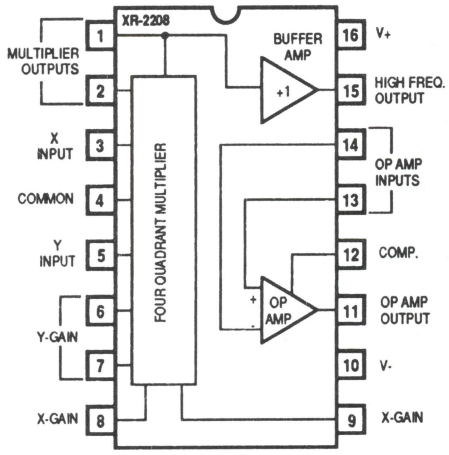
Maximum Versatility
  Independent Multiplier, 0p Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB B.W.-8 MHz typ,
  3^0^ Phase Shift B.W-1.2 MHz typ.
  Transconductance B.W-100 MHz typ.
Simplified Offset Adjustments
Wide Supply Voltage Range (+4.5V to ±16V)

APPLICATIONS

Analog Computation
  Multiplication
  Division
  Squaring
  Square-Root
Signal Processing
  AM Generation
  Frequency Doubling
  Frequency Translation
  Synchronous AM Detection
Triangle-to-Sine wave Converter
AGC Amplifier
Phase Detector
Phase-Locked Loop (PLL) Applications
Motor Speed Control
Precision PLL
Carrier Detection
Phase-Locked AM Demodulation

Rev-B

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply V^+	+18 Volts
V^-	-18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25° C	6mW/°C
Storage Temperature Range	-65°C to + 150°C

SYSTEM DESCRIPTION

The XR-2208 operational multiplier contains a four-quadrant multiplier with a buffer amplifier for one of the differential outputs for applications requiring high frequency applications. The inputs have a dynamic response of 4 MHz (8 MHz for the X input) and a transconductance bandwidth of 100 MHz for phase detector applications. The fully independent operational amplifier features high gain and a large common mode rejection ratio (90 dB). The device can be powered by voltages from ±4.5 VDC to ±16 VDC.

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ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2208

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	Icc	Vs = ±4.5V	TA = +25°C		7.0	mA	1
			-55°C≤TA≤+125°C		7.0	mA	2,3
Supply Current	Icc	Vs = ±16.0V	TA = +25°C		7.0	mA	1
			-55°C≤TA≤+125°C		7.0	mA	2,3
Multiplier Output Voltage	Mvo	Pin 1	TA = +25°C	12.2	13.7	V	1
			-55°C≤TA≤+125°C	12.2	13.7	V	2,3
Multiplier Output Voltage	Mvo	Pin 2	TA = +25°C	12.2	13.7	V	1
			-55°C≤TA≤+125°C	12.2	13.7	V	2,3
Multiplier Output Offset Voltage	Mvos		TA = +25°C	-80	80	mV	1
			-55°C≤TA≤+125°C	-80	80	mV	2,3
Feedthrough	VFT	Vx = -10V, Vy = 0	TA = +25°C	-150	150	mV	4
			-55°C≤TA≤+125°C	-150	150	mV	5,6
Feedthrough	VFT	Vx = 0, Vy = -10V	TA = +25°C	-150	150	mV	4
			-55°C≤TA≤ +125°C	-150	150	mV	5,6
Feedthrough	VFT	Vx = 0, Vy = 10V	TA = +25°C	-150	150	mV	4
			-55°C≤TA≤+125°C	-150	150	mV	5,6
Feedthrough	VFT	Vx = 0, Vy = 10V	TA = +25°C	-150	150	mV	4
			-55°C≤TA≤+125°C	-150	150	mV	5,6
Nonlinearity	NLIN	Vx = 10V	TA = +25°C	-0.5	0.5	%	9
		-1OV≤Vy≤10V	-55°C≤TA≤+125°C	-1.0	1.0	%	10,11
Nonlinearity	NLIN	Vx = -10V	TA = +25°C	-0.5	0.5	%	9
		-10V≤Vy≤10V	-55°C≤TA≤+125°C	-1.0	1.0	%	10,11
Nonlinearity	NLIN	Vy = +10V	TA = +25°C	-0.5	0.5	%	9
		-10V≤Vx≤10V	-55°C≤TA≤+125°C	-1.0	1.0	%	10,11
Nonlinearity	NLIN	Vy =10V	TA = +25°C	-0.5	0.5	%	9
		-10V≤Vx≤10V	-55°C≤TA≤+125°C	-1.0	1.0	%	10,11
Input Bias Current	IBX	XINPUT	TA = +25°C	-6.0	6.0	µA	1
			-55°C≤TA≤+125°C	-6.0	6.0	µA	2,3
Input Bias Current	IBY	YINPUT	TA = +25°C	-6.0	6.0	µA	1
			-55°C≤TA≤+125°C	-6.0	6.0	µA	2,3
Input Bias Current	IBC	Common Input	TA = +25°C	-12.0	12.0	µA	1
			-55°C≤TA≤+125°C	-12.0	12.0	µA	2,3
Buffer Voltage Gain	BG		TA = +25°C	0.8	1.1		4
			-55°C≤TA≤+125°C	0.8	1.1		5,6
Buffer Output Voltage High	BVO	Vx = 10V, Vy = -10v	TA = +25°C	10.0	13.0	V	1
			-55°C≤TA≤+125°C	10.0	13.0	V	2,3

Buffer Output Voltage Difference	B_{VOD}	Vx = -10V, Vy = 10V	T_A = +25°C -55°C≤T_A≤+125°C	-2.1 -2.1	-0.55 -0.55	V V	1 2,3
Input Offset Voltage	V_{OS}		T_A = +25°C -55°C≤T_A≤+125°C	-3.0 -3.0	3.0 3.0	mV mV	1 2,3
Input Offset Voltage	I_{OS}		T_A = +25°C -55°C≤T_A≤+125°C	-75.0 -75.0	75.0 75.0	nA nA	1 2,3
Input Bias Current	I_B		T_A = +25°C -55°C≤T_A≤+125°C	-200 -200	200 200	nA nA	1 2.3
Common Mode Rejection Ratio	CMRR		T_A = +25°C -55°C≤T_A≤+125°C	70 70		dB dB	1 2.3
Voltage Gain	A_{VOL}		T_A = +25°C -55°C≤T_A≤+125°C	70 70		dB dB	4 5,6
Power Supply Rejection	PSR R		T_A = +25°C -55°C≤T_A≤+125°C	70 70		dB dB	1 2,3
Output Voltage Swing Positive	V_{OSWP}		T_A = +25°C -55°C≤T_A≤+125°C	10.0 10.0		V V	4 5,6
Output Voltage Swing Negative	V_{OSWN}		T_A = +25°C -55°C≤T_A≤+125°C		-10.0 -10.0	V V	4 5,6
Short Circuit Current Negative	I_{SCN}		T_A = +25°C -55°C≤T_A≤+125°C	-30.0 -30.0	-5.0 -5.0	mA mA	1 2.3
Short Circuit Current Positive	I_{SCP}		T_A = +25°C -55°C≤T_A≤+125°C	5.0 5.0	30.0 30.0	mA mA	1 2.3

NOTES

Precision Oscillator

GENERAL DESCRIPTION

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. It is ideally suited for frequency modulation. voltage to frequency or current to frequency conversion. sweep or tone generation as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR- 2208

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Wide Sweep Range (1000:1 Min)
Wide Supply Voltage Range (± 4V to ± 13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

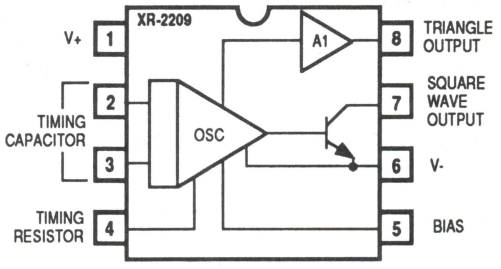
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Derate above +25°C	8.3 mW/°C
Operating Temperature Range	
XR-2209M	-55°C to + 125°C
Storage Temperature Range	-65°C to + 150°C

Rev-B

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2209 precision oscillator is comprised of three functional blocks: a variable frequency oscillator which generates the basic periodic waveforms and two buffer amplifiers for the triangle and the squarewave outputs. The oscillator frequency, set by an external capacitor, C, and the timing resistor, R, operates over 8 frequency decades, from 0.01 Hz to 1 MHz. With no sweep signal applied, the frequency of oscillation is equal to 1/RC.

The XR-2209 has a typical drift specification of 20 ppm/°C. Its frequency can be linearly swept over a 1000:1 range with an external control signal. Output duty cycle is adjustable from less than 1% to over 99%. The device may operate from either single or split supplies from 8 V to 26 V (±4 V to ±13 V).

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2209

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	I_{CC1}	Positive V_{CC} = ±6V	T_A = +25°C		8.00	mA	1
			-55°C≤T_A≤+125°C		12.00	mA	2,3
Supply Current	I_{EE1}	Negative V_{CC} = ±6V	T_A = +25°C	-7.00		mA	1
			-55°C≤T_A≤+125°C	-11.0		mA	2,3
Supply Current	I_{CC2}	Positive V_{CC} = ±13V	T_A = +25°C		17.00	mA	1
			-55°C≤T_A≤+125°C		20.00	mA	2,3
Supply Current	I_{EE2}	Negative V_{CC} = ±13V	T_A = +25°C	-17.0		mA	1
			-55°C≤T_A≤+125°C	-20.0		mA	2,3
Squarewave Output Leakage Current	I_L	V_{CC} = ±13V	T_A = +25°C		100	µA	1
			-55°C≤T_A≤+125°C		200	µA	2, 3
Squarewave Output Low Voltage	V_{OL}	Referenced to V_{EE}	T_A = +25°C		0.4	V	1
		V_{CC} = ±6V	-55°C≤T_A≤+125°C		1.00	V	2,3
Squarewave Output Amplitude	V_O	V_{CC} = ±6V	T_A = +25°C	11.0		V	4
			-55°C≤T_A≤+125°C	11.0		V	5,6
Frequency Accuracy	f_{STD}	C_T = 5000 pF, V_{CC} = ±6V, R_T = 20KΩ	T_A = +25°C	9.70	10.30	KHz	9
			-55°C≤T_A≤+125°C	9.50	10.50	KHz	10,11
Power Supply Stability		±6V≤Vcc≤±13V	T_A = +25°C		10.0	%	9
			-55°C≤T_A≤+125°C		11.0	%	10,11
Upper Frequency	f_H	C_T = 500 pF, R_T = 2KΩ, V_{CC} = ±6V	T_A = +25°C	500		KHz	9
			-55°C≤T_A≤+125°C	500		KHz	10,11
Sweep Linearity	S_{WLIN}	C_T = 5000 pF, R_T = 20OKΩ vs. f_{STD}	T_A = +25^0^C		2.0	%	9
			-55°C≤T_A≤+125°C		4.0	%	10,11
Minimum Timing Resistor	T_{RMIN}	C_T = 5000 pF R_T = 1.5KΩ	T_A = +25°C	90		KHz	9
			-55°C≤T_A≤+125°C	85		KHz	10,11
Maximum Timing Resistor	T_{RMAX}	C_T = 5000 pF R_T = 2MΩ	T_A = +25°C Only	80	120	Hz	9 10,11
		R_T = 20OKΩ	-55°C≤T_A≤+125°C	800	1400	Hz	
Sweep Range	S_{WRNG}	T_{RMIN}/T_{RMAX}	T_A = +25°C	90			9
			-55°C≤T_A≤+125°C				10,11
Triangle Wave Output Amplitude	T_{VPP1}	V_{CC} = ±6V C_T = 5000 pF R_T = 20KΩ	T_A = +25°C	4		V	4
			-55°C≤T_A≤+125°C	2		V	5,6
Triangle Wave Output Amplitude	T_{VPP2}	V_{CC} = ±13V C_T = 5000 pF R_T = 20KΩ	T_A = +25°C	7		V	4
			-55°·C≤T_A≤+125°C	7		V	5,6
Triangle Wave Linearity	T_{WLIN}	C_T = 5000 pF RT = 2OKΩ	T_A = +25°C Only		5	%	9 10,11
		V_{CC} = 16V	-55°C≤T_A≤+125°C		5	%	

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides ratio metric operation for low system performance variations with power supply changes.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20 V
HCMOS / TTL / Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2 mV to 3 V rms
Adjustable Tracking Range (11% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

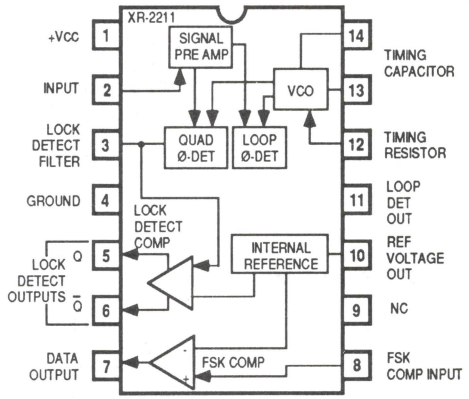
FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	900 mW
Ceramic Package	750 mW
Derate Above TA = + 25°C	8mW°C

Rev-A

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The output of the phase detector produces sum and difference frequencies of the input and the VCO (internally connected). When in lock, these frequencies are fIN + fVCO (2 times fIN when in lock) and fIN - FVCO (0HZ when lock). By adding a capacitor to the phase detector output, the 2 times fIN component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

7

XR-2211 ELECTRICAL PERFORMANCE CHARACTERISTICS

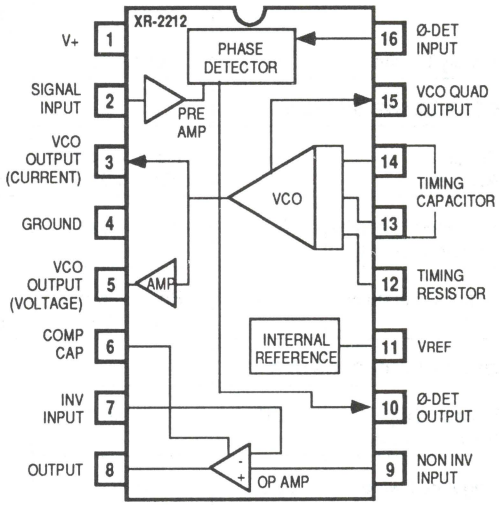
TEST	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
	CONDITIONS	TEMPERATURE	MIN	MAX		
GENERAL CHARACTERISTICS						
Supply Voltage	Vcc = 4.5V RT = 30Kohm CT = 0.033UF	TA = 25°C -55°C≤TA≤+125°C	900 900	1100 1100	Hz Hz	9 10, 11
	Vcc = 20V RT = 30Kohm CT = 0.033UF	TA = 25°C -55°C≤TA≤+125°C	900 900	1100 1100	Hz Hz	9 10, 11
Supply Current	Vcc = 12V	TA = 25°C -55°C≤TA≤+125°C		7 11	mA mA	1 2, 3
	Vcc = 20V	TA = 25°C -55°C≤TA≤+125°C		14 20	mA mA	1 2, 3
OSCILLATOR SECTION						
Frequency Accuracy	RT = 30Kohm Vcc = 12V CT = 0.033UF	TA - 25°C -55°C≤TA≤+125°C	970 900	1030 1100	Hz Hz	9 10, 11
Frequency Stability vs Power Supply	Vcc = 12V 11V	TA - 25°C		0.5	%	9
Maximum Frequency	Vcc = 12V RT = 8.2Kohm CT = 400pf	TA = 25°C	100		KHz	9
Minimum Timing Resistor	RT = 15Kohm CT = 0.03UF	TA = 25°C	1600	2400	Hz	9
LOOP PHASE DETECTOR SECTION						
Peak Output Current	Vcc =12V Measured at Pin 11	TA = 25°C -55°C≤TA≤+125°C	1150 1100	1300 1300	µA µA	1 2, 3
Maximum Swing	Vcc = 12V Referenced to Pin 10	TA = 25°C -55°C≤TA≤+125°C	14.0 12.8		V V	1 2, 3
QUADRATURE PHASE DETECTOR						
Peak Output Current	Vcc = 12V Measured at Pin 3	TA = 25°C -55°C≤TA≤+125°C	100 50		µA µA	1 2, 3
INPUT PREAMP SECTION						
Input Signal Voltage Required to cause Limiting	Vcc = 12V, fo = 1 KHz VIN = 10mVrms Measured "Q" output Pin 5	TA = 25°C -55°C≤TA≤+125°C		0.6 0.8	V V	7 8
INTERNAL REFERENCE						
Voltage Output	Vcc = 12V Measured at Pin 10	TA = 25°C -55°C≤TA≤+125°C	4.9 3.8	5.7 6.95	V V	1 2, 3

Precision Phase-Locked Loop

GENERAL DESCRIPTION

The XR-2212 is an ultra-stable monolithic phase-looked loop (PLL) system especially designed for data communications and control system applications. Its on board reference and uncommitted operational amplifier, together with a typical temperature stability of better than 20 ppm/°C, make it ideally suited for frequency synthesis, FM detection, and tracking filler applications. The wide input dynamic range, large operating voltage range, large frequency range, and HCMOS, and TTL compatibility contribute to the usefulness and wide applicability of this device.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
TTL/ HCMOS Compatible	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range	(±1% to ± 80%)
Excellent Temp. Stability	20 ppm/°C, Typ.

APPLICATIONS

Frequency Synthesis
Data Synchronization
FM Detection
Tracking Filters
FSK Demodulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Input Signal Level	3 Vrms
Power Dissipation	
Ceramic Package:	750 mW
Derate Above TA = + 25°C	6 mW/°C

Rev-A

SYSTEM DESCRIPTION

The XR-2212 is a complete PLL system with buffered inputs and outputs, an internal reference, and an uncommitted op amp. Two VCO outputs are pinned out; one sources current, the other sources voltage. This enables operation as a frequency synthesizer using an external programmable divider. The op amp section can be used as an audio preamplifier for FM detection or as a high speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth, and tracking range of the PLL are controlled independently by external components. The PLL output is directly by compatible with CMOS, HCMOS and TTL logic families as well as microprocessor peripheral systems.

7

XR-2212 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNITS	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	LIMIT	MAX		
Supply Current	Icc	Vcc = 12V	TA = 25°C -55°C≤TA≤+125°C		10.00 12.00	mA	1 2, 3
Supply Current	Icc	Vcc = 15V	TA = 25°C		15.00	mA	1
OSCILLATOR SECTION							
Frequency Accuracy	Fo	Ro = 30Kohm Co = 0.03µF	TA = 25°C -55°C≤TA≤+125°C		3.0 5.0	% %	9, 11 1
Frequency Stability vs Power Supply	Fd	Vcc = 12±1V	TA = 25°C -55°C≤TA≤+125°C		0.5 1.2	%/V %/V	9, 11 1
Upper Frequency Limit	Fmax	Ro = 8.2Kohm Co = 400pF	TA = 25°C -55°C≤TA≤+125°C	100 100		Khz Khz	9 10, 11
OSCILLATOR OUTPUTS							
Voltage Output Positive Swing	VOH	At Pin 5	TA = 25°C -55°C≤TA≤+125°C	9.50 9.50		V V	1 2, 3
Negative Swing	VOL	At Pin 5	TA = 25°C -55°C≤TA≤+125°C		0.4 0 4	V V	1 2, 3
Current Output Peak Current Swing		At Pin 3	TA = 25°C -55°C≤TA≤+125°C	100 100		µA µA	1 2, 3
LOOP PHASE DETECTOR SECTION							
Peak Output			TA = 25°C -55°C≤TA≤+125°C	150 100	300 300	µA µA	1 2, 3
Maximum Swing			TA = 25°C -55°C≤TA≤+125°C	4.00 4.00		V V	1 2
OP AMP SECTION							
Voltage Gain			TA = 25°C -55°C≤TA≤+125°C	55 50		dB dB	4 5, 6
Input Bias Current	IB		TA = 25°C -55°C≤TA≤+125°C		1 1	µA µA	1 2, 3
Offset Voltage	Vos		TA = 25°C -55°C≤TA≤+125°C		20 20	mV mV	1 2, 3
INTERNAL REFERENCE							
Voltage Level	VREF		TA = 25°C -55°C≤TA≤+125°C	4.90 4.75	5.70 5.85	V V	1 2, 3

Programmable Timer/Counter

GENERAL DESCRIPTION

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to five days. Two timing circuits can be cascaded to generate time delays up to three years.

As shown in Figure 1, the circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter and a control flip-flop. The time delay is set by an external R-C network and can be programmed to any value from 1 RC to 255 RC.

In astable operation, the circuit can generate 256 separate frequencies or pulse-patterns from a single RC setting and can be synchronized with external clock signals. Both the control inputs and the outputs are compatible with TTL and DTL logic levels.

FEATURES

Timing from micro-seconds to days
Programmable delays: 1 RC to 255 RC
Wide supply range; 4V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
External Sync and Modulation Capability
Excellent Supply Rejection: 0.2 %N

APPLICATIONS

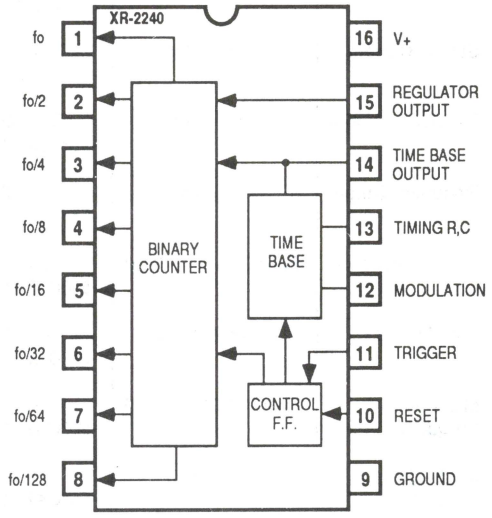
Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	
Ceramic Package	750 mW
Derate above + 25°C	6 mw/°C
Operating Temperature XR-2240	-55°C to + 125°C
Storage Temperature	-65°C to + 150°C

Rev-B

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2240 is a combination timer/counter capable of generating accurate timing intervals ranging from microseconds through several days. The time base works as an astable multivibrator with a period equal to RC. The eight bit counter can divide the time base output by any integer value from 1 to 255. The wide supply voltage range of 4.5 to 15 V, TTL and DTL logic compatibility, and 0.5% accuracy allow wide applicability. The counter may operate independently of the time base. Counter outputs are open collector and may be wire- OR connected.

The circuit is triggered or reset with positive going pulses. By connecting the reset pin (Pin 10) to one of the counter outputs, the time base will halt at timeout. If none of the outputs are connected to the reset, the circuit will continue to operate in the astable mode. Activating the trigger terminal (Pin 11) while the timebase is stopped will set all counter outputs to the low state and start the timebase.

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2240

TEST	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current	V+ = 5V	T_A = +25°C		6	mA	1
		-55°C≤T_A≤+125°C		8	mA	2, 3
Supply Current	V+ = 15V	T_A = +25°C		16	mA	1
		-55°C≤T_A≤+125°C		20	mA	
Regulator Output	V+ = 5V	T_A = +25°C	4.1		V	1
		-55°C≤T_A≤+125°C	3.7		V	2, 3
Regulator Output	V+ = 15V	T_A = +25°C	6.0	6.6	V	1
		-55°C≤T_A≤+125°C	5.2	7.0	V	2, 3
Timing Accuracy	R =10KΩ, C = 0.1µF	T_A = +25°C		2.0	%	9
		-55°C≤T_A≤+125°C		6.0	%	10, 11
Supply Drift	8V≤V+≤15V	T_A = +25°C		0.2	%/V	9
		-55°C≤T_A≤+125°C		0.4	%/V	10, 11
Maximum Frequency	R=1 KΩ,C= 0.007µF	T_A = +25°C	100		KHz	9
		-55°C≤T_A≤+125°C	85		KHz	10, 11
Modulation Voltage Level	V+ = 5V	T_A = +25°C	3	4	V	1
		-55°C≤T_A≤+125°C	3	4	V	2, 3
Trigger Threshold		T_A = +25°C		2.0	V	1
		-55°C≤T_A≤+125°C		2.3	V	2, 3
Reset Threshold		T_A = +25°C		2.0	V	1
		-55°C≤T_A≤+125°C		2.3	V	2, 3
Max Toggle Rate		T_A = +25°C	0.5		MHz	9
Input Threshold	V+ = 5V	T_A = +25°C	1.0		V	1
		-55°C≤T_A≤+125°C	0.5		V	2, 3
Output Sink Threshold	V_{OL}≤0.4V	T_A = +25°C	3		mA	1
	V_{REG} = V+ = 5V	-55°C≤T_A≤+125°C	2		mA	2, 3
Output Leakage Current	V_{OH} = 15V	T_A = +25°C		8	µA	1
		-55°C≤T_A≤+125°C		8	µA	2, 3

Dual Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-2567 is a dual monolithic tore decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-'tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Suoply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free- running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

FEATURES

Replaces two 567-type decoders
Excellent temperature tracking between decoders
Bandwidth adjustable from 0 to 14 %
Logic compatible outputs with 100 mA sink capability
Center frequency matching (1% typ.)
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false triggering
Frequency range adjustable over 20:1 range by external resistor.

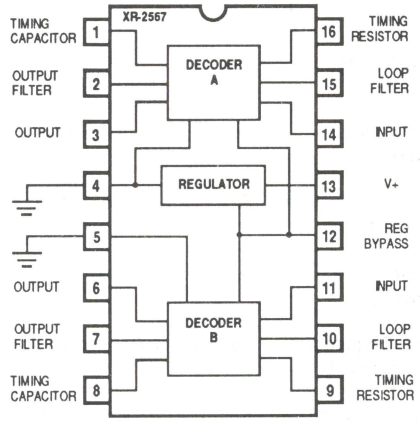
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Dual-Tone Decoding/ Encoding
Communications Paging
Ultrasonic Remote-Control and Monitoring
Full-Duplex Carrier-Tone Transceiver
Wireless Intercom
Dual Precision Oscillator
FSK Generation and Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	
With Internal Regulator	14V
Without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	
Ceramic Package	750 mW
Derate Above + 25°C	6 mW/°C
Storage Temperature	-65°C to +150°C
Rev-B	

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2567 dual monolithic tone decoder consists of two independent 567-type circuits and an on board voltage regulator. Each decoder has a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. Both devices have normally high open collector outputs capable of sinking 100 mA.

The input signal is applied to Pin 14 (device A) or Pin 11 (device B), both with 20 kΩ nominal input resistance. Free running frequency is controlled by an RC network at Pins 1 and 16 (device A) or Pins 8 and 9 (device B). A capacitor on Pin 2 (A), or Pin 7 (B) serves as the output filler and eliminates out-of-band triggering. PLL fillering is accomplished with a capacitor on Pin 15 (A), or Pin 10 (B) bandwidth and skew are also dependent upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 13 is +Vcc (4.75 to 12V nominal, 14V maximum): Pin 7 is ground; and Pin 3 (A) or Pin 6 (B) is the open collector output, pulling low when an in-band signal triggers the device.

Voltage supplies below 7V necessitate bypassing the internal regulator. This is accomplished by shorting Pin 12 to Vcc, for supplies over 7V, a bypass capacitor of at least 1 μF should AC ground Pin 12.

7

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-2567

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT	GROUP A SUBGROUP
Supply Current Quiescent	Icc	Vcc = +5V	T_A = +25°C		16.0	mA	1
			-55°C≤T_A≤+125°C		16.0	mA	2, 3
Supply Current Quiescent	Icc	Vcc = +12V	T_A = +25°C		40.0	mA	1
			-55°C≤T_A≤+125°C		40.0	mA	2, 3
Supply Current Activated	Icc	Vcc = +5V	T_A = +25°C		26.0	mA	1
			-55°C≤T_A≤+125°C		26.0	mA	2, 3
Highest Center Frequency	Fc	Vcc = +12V	T_A = +25°C	100		KHz	9
			-55°C≤T_A≤+125°C	**90**		KHz	10, 11
Highest Center Frequency	Fc	Vcc = +5V	T_A = +25°C	100		KHz	9
			-55°C≤T_A≤+125°C	100		KHz	10, 11
Center Frequency Drift with Supply	Fo	4.75V≤Vcc≤6.75V	T_A = +25°C		1.00	%/V	9
			-55°C≤T_A≤+125°C		3.00	%/V	10, 11
Output Saturation Voltage	VSAT	IL = 30 mA Vin = 25 mV	T_A = +25°C		0.4	V	1
			-55°C≤T_A≤+125°C		0.6	V	2, 3
Output Saturation Voltage	VSAT	IL = 100 mA Vin 25 mV	T_A = +25°C		1.0	V	1
			-55°C≤T_A≤+125°C		1.0	V	2, 3
Output Leakage Current	I_{OL}	**VIN** = 7.5mV Vcc = +5v	T_A = +25°C		25	µA	1
			-55°C≤T_A≤+125°C		35	µA	2, 3
Largest No Output Input Voltage	V_{IL}	Vcc = +5V IL = 100mA	T_A = +25°C	10		mVrms	4
			-55°C≤T_A≤+125°C	10		mVrms	5, 6
Smallest Detectable Input Voltage	V_{IS}	Vcc = +5V IL = 100mA	T_A = +25°C		25	mVrms	7
			-55°C≤T_A≤+125°C		50	mVrms	8
Largest Detection Bandwidth	LDBW	Vcc = +5V Vin = 300 mV	T_A = +25°C	12	1 6	%	4
			-55°C≤T_A≤+125°C	10	27	%	5, 6
Largest Detection Bandwidth Skew	SKEW	Vcc = +5V Vin = 300 mV	T_A = +25°C		2.00	%	4
			-55°C≤T_A≤+125°C		3.00	%	5, 6

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038 is a precision waveform generator IC capable of producing sine. square, triangular, sawtooth and pulse waveforms with a minimum number of external components and adjustments. Its operating frequency can be selected over eight decades of frequency, from 0.001 Hz to 200 KHz by the choice of external R-C components. The frequency of oscillaticn is highly stable over a wide range of temperature and supply voltage changes. Both full frequency sweeping as well as smaller frequency variations (FM) can be accomplished with an external control voltage. Each of the three basic waveforms, i.e., sinewave, triangle and square wave outputs are available simultaneously, from independent output terminals.

The XR-8038 monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance It can be readily interfaced with a monolithic phase-detector circuit, such as, the XR-2208, to form stable phase-locked loop circuits.

FEATURES

With Improved Sweep Range, Frequency Drift
and Max. Operating Frequency
Simultaneous Sine. Triangle and Square-Wave Outputs
Low Sine Wave Distortion-THD
High FM and Triangle Linearity
Wide Frequency Range
Variable Duty-Cycle

APPLICATIONS

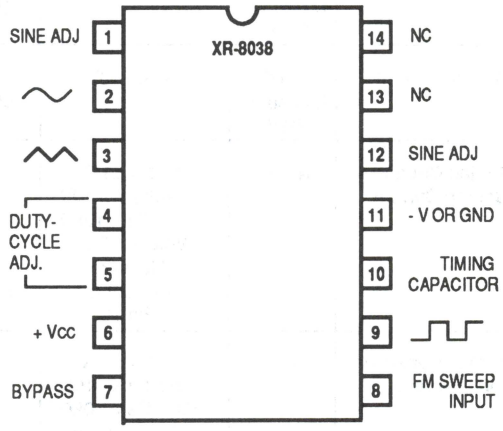
Precision Waveform Generation: Sine. Triangle, Square,
Pulse
Sweep and FM Generation
Tone Generation
Instrumentation on and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW°C
Storage Temperature Range	-65°C to + 150°C

Rev A

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-8038 precision waveform generator produces highly stable and sweepable square, triangle, nd sine waves across eight frequency decades. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, buffers, and a sine wave converter. Three identical frequency waveforms are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7%, with Pin 1 open and 82 kΩ from Pin 12 to Pin 11 (- V or ground). Sine wave distortion may be improved by including two 100 kΩ potentiometers between Vcc and - V (or ground), with one wiper connected to Pin 1 and the other connected to Pin 12.

Small frequency deviation (FM) is accomplished by applying modulation voltage to Pins 7 and 8; large frequency deviation (sweeping) is accomplished by applying voltage to Pin 8 only Sweep range is typically 1000:1.

The square wave output is an open collector transistor, output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typirally 13 of, the supply, and sine wave output reaches 0.22 of the supply voltage.

7

XR-8038 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS (SEE NOTE 1)		LIMITS		UNIT	GROUP A SUBGROUP
		CONDITIONS	TEMPERATURE	MIN	MAX		
Supply Current	I_{CC} HI Measure Pin 6	V_{CC} = ±18V	T_A = 25°C -55°C≤T_A≤+125°C		60.0 80.0	mA mA	1 2, 3
Supply Current	I_{CC} LO Measure Pin 6	V_{CC} ±10V	T_A = 25°C -55°C≤T_A≤+125°C	3.0 2.0	15.0 25.0	mA mA	1 2, 3
Timing Capacitor Source Current	I_{+CAP}	V_{CC} = ±15V V_{SWEEP} = +10V R_A = R_B = 10kΩ V_{CAP} = 15.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	450 400	550 600	µA1 µA	 2, 3
Timing Capacitor Sink Current	I_{-CAP}	V_{CC} = ±15V V_{SWEEP} = +10V R_A = R_B = 10kΩ V_{CAP} = -5.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	550 -600	-450 -400	µA µA	1 2, 3
Timing Capacitor Source Current	I_{+HIGH}	V_{CC}= ±15V V_{SWEEP} = +12V R_A = R_B = 1kΩ V_{CAP} = +5.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	2.50 2.00	3.50 4.00	mA mA	1 2, 3
Timing Capacitor Sink Current	I_{-HIGH}	V_{CC} = ±15V V_{SWEEP} = +12V R_A = R_B = 1kΩ V_{CAP} = +5.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	-3.50 -4.00	-2.50 -2.00	mA mA	1 2, 3
Timing Capacitor Source Current	I_{+LOW}	V_{CC} = ±15V V_{SWEEP} = +10V R_A = R_B = 1MΩ V_{CAP} = +5.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	2.20 -2.00	15.00 50.00	µA µA	1 2, 3
Timing Capacitor Sink Current	I_{-LOW}	V_{CC} = ±15V V_{SWEEP} = +10V R_A = R_B = 1MΩ V_{CAP} = -55V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	-15.00 -50.00	-2.20 2.0	µA µA	1 2, 3

Timing Capacitor Sink Current	I_{-IN}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B = \infty$ V_{CAP} = +5.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	-8.0 -20.00	1.00 -2.00	µA µA	1 2, 3
Timing Capacitor Source Current	I_{+LEAK}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B$ V_{CAP} = +4.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	-1.00 -10.00	1.00 10.00	µA µA	1 2, 3
Timing Capacitor Sink Current	I_{-LEAK}	V_{CC} = ±15V V_{SWEEP} = +10V $R_A = R_B = \infty$ V_{CAP} = -4.5V Measure Current at Pin 10	T_A = 25°C -55°C≤T_A≤+125°C	-1.00 -10.00	1.00 10.00	µA µA	1 2, 3
FM Sweep Bias Current	V_{BIAS}	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B$ =10KΩ V_{CAP} = GND Measure current at Pin 8	T_A = 25°C -55°C≤+T_A≤+125°C	-1.00 -10.00	1.00 10.00	µA µA	1 2, 3
FM Bias Voltage	V_{BIAS}	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B$ = 10K V_{CAP} = GND Measure Voltage at Pin 7	T_A = 25°C -55°C≤T_A≤+125°C	8.30 3.00	9.70 10.00	V V	1 2, 3
Square Wave Output Saturation Voltage	SQ_{LOW}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} = +5.5V I_{PIN9} = 2mA Measure Voltage at Pin 9	T_A = 25°C -55°C≤T_A≤+125°C	-15.00 -15.00	-14.60 -14.00	V V	1 2. 3
Square Wave Output Leakage Current	SQ_{HIGH}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$= 10KΩ V_{CAP} = +55V IPIN9 = +15V Measure Current at Pin 9	T_A = 25°C -55°C≤T_A≤+125°C	-2.5 -4.0	20.0 300.0	µA µA	1 2, 3

Sine Output Offset Voltage	V_{OSSIN}	V_{CC}- ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} = GND Measure Voltage at Pin 2	T_A = 25°C -55°C≤T_A≤+125°C	-100 -600	100 600	mV mV	1 2, 3
Sine Output Voltage	V_{OUT+}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10kΩ V_{CAP} = +5V Measure Voltage at Pin 2	T_A = 25°C -55°C≤T_A≤+125°C	2.50 1.70	3.90 4 70	V V	1 2, 3
Sine Output Voltage	V_{OUT-}	V_{CC} = ±15V V_{SWEEP} = GND $R_A = R_B$ = 10KΩ V_{CAP} = -5V Measure Voltage at Pin 2	T_A = 25°C -55°C≤T_A≤+125°C	-3.90 -4.70	-2.50 -1.70	V V	1 2, 3
Sine Adjust Voltage	V_{ADJ+}	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B = \infty$ V_{CAP} = GND Measure Voltage at Pin 1	T_A = 25°C -55°C≤T_A≤+125°C	2.50 1.70	3.90 4.70	V V	1 2, 3
Sine Adjust Voltage	V_{ADJ-}	V_{CC} = ±15V No V_{SWEEP} $R_A = R_B = \infty$ V_{CAP} = GND Measure Voltage at Pin 12	T_A = 25°C -55°C≤T_A≤+125°C	-3.90 -4.70	-2.40 -1 70	V V	1 2, 3

Frequency	F_o	V_{CC} = ±10V CT = 3000pF $R_A = R_B$ = 10KΩ Connect Pin 7 to Pin 8 R_L = 10KΩ Measure Frequency at Pin 9	T_A =25°C -55°C≤T_A≤+125°C	8.600 3.400	10.000 10.100	KHz KHz	9 10, 11
Sine Wave Distortion Unadjusted	THD	V_{CC} = ±10V CT = 3000pF $R_A = R_B$ = 100KΩ R_L = 10KΩ Connect Pin 7 to Pin 8 Measure Distortion at Pin 2	T_A =25°C -55°C≤T_A≤+125°C	0.0 0.0	5.5 25.0	% %	9 10, 11
Sine Wave Distortion adjusted	THD ADJ	V_{CC} = ±10V CT = 3000pF $R_A = R_B$ = 100KΩ RL = 10KΩ Connect Pin 7 to Pin 8 Adjust R_A +R_B to get 50% Duty Cycle at Pin 9 Measure Distortion at Pin 2	T_A =25°C -55°C≤T_A≤+125°C	0.0 0.0	2.1 20.0	% %	9 10, 11

Note 1 - 82KΩ between Pin 11 and Pin 12

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NOTES



CMOS Dual Channel UART (DUART)

GENERAL DESCRIPTION

The EXAR Dual Univeral Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communications channels in a single package. The DUART is designed for use in micrprocessor based systems and may be used in a polled or interrupt driven environment.

Two basic versions of the DUART are available, each optimized for use with various microprocessor families: XR- 88C681 for 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx family based systems, and the XR-68C681 for 68000 family based systems. A programmable mode of the XR- 88C681 version provides an interrupt daisy chain capabiiity for use in Z80 and Z8000 based systems. However, the bus interfaces are general enough to allow interfacing with other microprocessors and microcontrollers. The XR- -88C681 and XR-68C681 are enhanced versions of the Signetics, Motorola 2681 and 68681 respectively, and are pin and function compatible with those devices,

The DUART is fabricated using advanced two-layer metal high density CMOS process to provide high performance and low power consumption and is packaged in a 40 pin DIP or a 44 pin LCC. The XR-88C861 is also available in a 28 pin DIP.

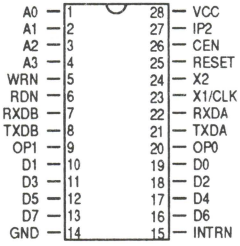
FEATURES

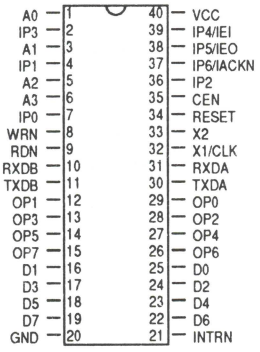
Full Duplex, Dual Channel, Asynchronous Receiver and Transmitter
Quadruple-Buffered Receiver, Dual-Buffered Transmitter
Stop Bits Programmable in 1/16-bit Increments
Internal Bit Rate Generator with 23 Sit Rates
Independent Bit Rate Selection for Each Receiver and Transmitter
Maximum Bit Rate: 1x Clock - 1 Mb/Sec, 16x Clock - 125Kb/Sec
Normal, Autoecho, Local Loopback, and Remote Loopback Modes
Multi-Function 16-Bit Counter/Timer
Interrupt Output with Eight Maskable Interrupting Cond.
Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
Up to 15 I/O Pins (Depending on Package and Version)
Change of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On-Chip Oscillator for Crystal
Standby Mode to Reduce Operating Power
Advanced CMOS Low Power Technology

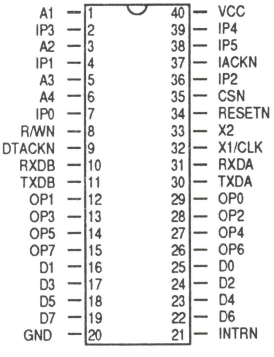
ABSOLUTE MAXIMUM RATINGS

Storage Temperature-65°C to +150°C
All Voltages with Respect to Ground-0.5 V to +7.0 V

PACKAGE OUTLINE DIAGRAMS







ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-68C681

TEST	SYMBOL (See Note 1)	CONDITIONS	LIMITS TEMPERATURE	MIN	MAX	UNIT	GROUP A SUBGROUP
Input Low Voltage	VIL		TA = +25°C	-0.5	0.8	V	1
			-55°C≤TA≤+125°C	-0.5	0.8	V	2, 3
Input High Voltage	VIH		TA = +25°C	2.2		V	1
			-55°C≤TA≤+125°C	2.2		V	2, 3
Input High Voltage (x1/CLK)	VIH1		TA = +25°C	4.0	Vcc	V	1
			-55°C≤TA≤+125°C	4.0	Vcc	V	2, 3
Output Low Voltage	VOL	IOL = 2.4 mA	TA = +25°C		0.4	V	1
			-55°C≤TA≤+125°C		0.4	V	2, 3
Output High Voltage (Except Open Drain Outputs)	VOH	IOH = -400µA	TA = +25°C	2.4		V	1
			-55°C≤TA≤+125°C	2.4		V	2, 3
Input - Leakage Current (Except x1/CLK,x2)	IIL	VIN = 0 to Vcc	TA = +25°C	-10	10	µA	1
			-55°C≤TA≤+125°C	-10	10	µA	2, 3
Data Bus 3 - State Leakage Current	ILL	Vo = 0 to Vcc	TA = +25°C	-10	10	µA	1
			-55°C≤TA≤+125°C	-10	10	µA	2, 3
Open Drain Output Leakage Current	Ioc	Vo = 0 to Vcc	TA = +25°C	-10	10	µA	1
			-55°C≤TA≤+125°C	-10	10	µA	2, 3
Power Supply Active Current	ICCA		TA = +25°C		15	mA	1
			-55°C≤TA≤+125°C		15	mA	2, 3
Power Supply Standby Current	ICCS		TA = +25°C		10	mA	1
			-55°C≤TA≤+125°C		10	mA	2, 3
Reset Pulse Width	tRES		TA = +25°C	1.0		µS	9
			-55°C≤TA≤+125°C	1.0		µS	10, 11
Port Input Set Up TimeTo RDN/CSN Low	tPS		TA = +25°C			nS	9
			-55°C≤TA≤+125°C	0		nS	10, 11
Port Input Hold Time From RDN/CSN High	tPH		TA = +25°C	0		nS	9
			-55°C≤TA≤+125°C	0		nS	10, 11
Port Output Valid From WRN/CSN High	tPD		TA = +25°C		400	nS	9
			-55°C≤TA≤+125°C		400	nS	10, 11

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-68C681

TEST	SYMBOL (See Note 1)	CONDITIONS	TEMPERATURE	LIMITS MIN	MAX	UNIT	GROUP A SUBGROUP
INTRN or OP3-OP7 When used as Interrupts High from: Clear ofInterrupt Status Bit inISR or IPCR	tIR		TA = +25°C -55°C≤TA≤+125°C		300 300	nS nS	9 10, 11
Clear of Interrupt Mask Bit in IMR			TA = +25°C -55°C≤TA≤+125°C		300 300	nS nS	9 10, 11
X1/CLK (External) High or Low Time	TCLK		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
X1/CLK Crystal or External Frequency	fCLK		TA = +25°C -55°C≤TA≤+125°C	2.0 2.0	4.0 4.0	MHz MHz	9 10, 11
Counter/Timer External Clock High or Low Time	tCTC		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Counter/Timer External Clock Frequency	fCTC		TA = +25°C -55°C≤TA≤+125°C	0.0 0.0	4.0 4.0	MHz MHz	9 10, 11
RXC and TXC (External) High or Low Time	tRTX		TA = +25°C -55°C≤TA≤+125°C	220 220		nS nS	9 10, 11
RXC and TXC (External) Frequency 16X	fRTX		TA = +25°C -55°C≤TA≤+125°C	0.0 0.0	2.0 2.0	MHz MHz	9 10, 11
RXC and TXC (External) Frequency 1X	fRTX		TA = +25°C -55°C≤TA≤+125°C	0.0 0.0	1.0 1.0	MHz MHz	9 10, 11
TXD Output Delay From TXC (External) Low	tTXD		TA = +25°C -55°C≤TA≤+125°C		350 350	nS nS	9 10, 11
TXD Output Delay From TXC (Internal) Output Low	tTCS		TA = +25°C -55°C≤TA≤+125°C	0 0	150 150	nS nS	9 10, 11
RXD Data Set Up Time to RXC (External) High	tRXS		TA = +25°C -55°C≤TA≤+125°C	240 240		nS nS	9 10, 11
RXC Data Hold Time From RXC (External) High	tRXH		TA = +25°C -55°C≤TA≤+125°C	200 200		nS nS	9 10, 11
DTACKN High From CSN or IACKN High	tDAH		TA = +25°C -55°C≤TA≤+125°C		100 100	nS nS	9 10, 11

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ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-68C681

TEST	SYMBOL	CONDITIONS	LIMITS TEMPERATURE	MIN	MAX	UNIT	GROUP A SUBGROUP
DTACKN High Impedance From	tDAT		TA = +25°C -55°C≤TA≤+125°C		125	nS	
CSN or IACKN Set UpTime to CLK High	tCSC		TA = +25°C -55°C≤TA≤+125°C	90 90		nS nS	9 10, 11
A1-A4 Set Up Time Time to CSN Low	tAS		TA = +25°C -55°C≤TA≤+125°C	10 10		nS nS	9 10, 11
A1-A4 Hold Time From CSN High	tAH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RWN Set Up Time To CSN Low	tRWS		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RWN Hold Time To CSN High	tRWH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
CSN High Pulse Width	tCSW		TA = +25°C -55°C≤TA≤+125°C	90 90		nS nS	9 10, 11
CSN or IACKN High From DTACKN Low	tCSD		TA = +25°C -55°C≤TA≤+125°C	20 20		nS nS	9 10, 11
Data Valid From CSN or IACKN Low	tDD		TA = +25°C -55°C≤TA≤+125°C		175 175	nS nS	9 10, 11
Data Bus Floating From CSN or IACKN High	tDF		TA = +25°C -55°C≤TA≤+125°C	10 10	100 100	nS nS	9 10, 11
Data Set Up Time To CLK High	tDS		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Data Hold Time From CSN High	tDH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
DTACKN Low From Read Data Valid	tDAL		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
DTACKN Low (Read Cycle) From CLK High	tDCR		TA = +25°C -55°C≤TA≤+125°C		125 125	nS nS	9 10, 11
DTACKN Low (Write Cycle) From CLK High	tDCW		TA = +25°C -55°C≤TA≤+125°C		125 125	nS nS	9 10, 11

Notes:

1. Vcc = 5.0 V -+ 10%

ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-88C681

TEST	SYMBOL (See Note 1)	CONDITIONS	LIMITS TEMPERATURE	MIN	MAX	UNIT	GROUP A SUBGROUP
INTRN or OP3-OP7 When used as Interrupts High from: Clear of interrupt Status Bit inISR or IPCR	tIR		TA = +25°C -55°C≤TA≤+125°C		300 300	nS nS	9 10, 11
Clear of Interrupt Mask Bit in IMR	tIR		TA = +25°C -55°C≤TA≤+125°C		300 300	nS nS	9 10, 11
X1/CLK (External) High or Low Time	tCLK		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
X1/CLK Crystal or External Frequency	fCLK		TA = +25°C -55°C≤TA≤+125°C	2.0 2.0	4.0 4.0	MHz MHz	9 10, 11
Counter/Timer External Clock High or Low Time	tCTC		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Counter/Timer External Clock Frequency	fCTC		TA = +25°C -55°C≤TA≤+125°C	0.0 0.0	4.0 4.0	MHz MHz	9 10, 11
RXC and TXC (External) High or Low Time	tRTX		TA = +25°C -55°C≤TA≤+125°C	220 220		nS nS	9 10, 11
RXC and TXC (External) Frequency 16X	fRTX		TA = +25°C -55°C≤TA≤+125°C	0.0 0.0	2.0 2.0	MHz MHz	9 10, 11
RXC and TXC (External) Frequency IX	fRTX		TA = +25°C -55°C≤TA≤+125°C	0.0 0.0	1.0 1.0	MHz MHz	9 10, 11
TXD Output Delay From TXC (External) Low	tTXD		TA = +25°C -55°C≤TA≤+125°C		350 350	nS nS	9 10, 11
TXD Output Delay From TXC (Internal) OutPut Low	tTCS		TA = +25°C -55°C≤TA≤+125°C	0 0	150 150	nS nS	9 10, 11
RXD Data Set Up Time to RXC (External) High	tRXS		TA = +25°C -55°C≤TA≤+125°C	240 240		nS nS	9 10, 11
RXC Data Hold Time From RXC (External) High	tRXH		TA = +25°C -55°C≤TA≤+125°C	200 200		nS nS	9 10, 11

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ELECTRICAL PERFORMANCE CHARACTERISTICS. XR-88C681

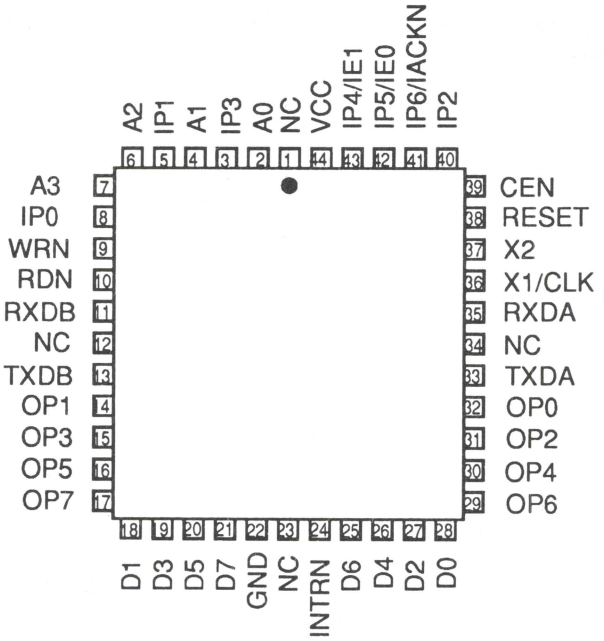
TEST	SYMBOL (See Note 1)	CONDITIONS	LIMITS TEMPERATURE	MIN	MAX	UNIT	GROUP A SUBGROUP
Input Low Voltage	VIL		TA = +25°C -55°C≤TA≤+125°C	-0.5 -0.5	0.8 0.8	V V	1 2, 3
input High Voltage	VIH		TA = +25°C -55°C≤TA≤+125°C	2.2 2.2		V V	1 2, 3
Input High Voltage (x1/CLK)	VIH1		TA = +25°C -55°C≤TA≤+125°C	4.0 4.0	Vcc Vcc	V V	1 2, 3
Output Low Voltage	VOL	IOL = 2.4 mA	TA = +25°C -55°C≤TA≤+125°C		0.4 0.4	V V	1 2, 3
Output High Voltage (Except Open Drain Outputs)	VOH	IOH = -400 µA	TA = +25°C -55°C≤TA≤+125°C	2.4 2.4		V V	1 2, 3
Input Leakage Current (Except x1/CLK,x2)	IIL	VIN = 0 to Vcc	TA = +25°C -55°C≤TA≤+125°C	-10 -10	10 10	µA µA	1 2, 3
Data Bus 3 - State Leakage Current	ILL	Vo = 0 to Vcc	TA = +25°C -55°C≤TA≤+125°C	-10 -10	10 10	µA µA	1 2, 3
Open Drain Output Leakage Current	Ioc	Vo = 0 to Vcc	TA = +25°C -55°C≤TA≤+125°C	-10 -10	10 10	µA µA	1 2, 3
Power Supply Active Current	ICCA		TA = +25°C -55°C≤TA≤+125°C		15 15	mA mA	1 2, 3
Power Supply Standby Current	ICCS		TA = +25°C -55°C≤TA≤+125°C		10 10	mA mA	1 2, 3
Reset Pulse Width	tRES		TA = +25°C -55°C≤TA≤+125°C	1.0 1.0		µS µS	9 10, 11
Port Input Set Up TimeTo RDN/CSN Low	tPS		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
Port Input Hold TimeFrom RDN/ CSN High	tPH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
Port Output Valid From WRN/CSN High	tPD		TA = +25°C -55°C≤TA≤+125°C		400 400	nS nS	9 10, 11

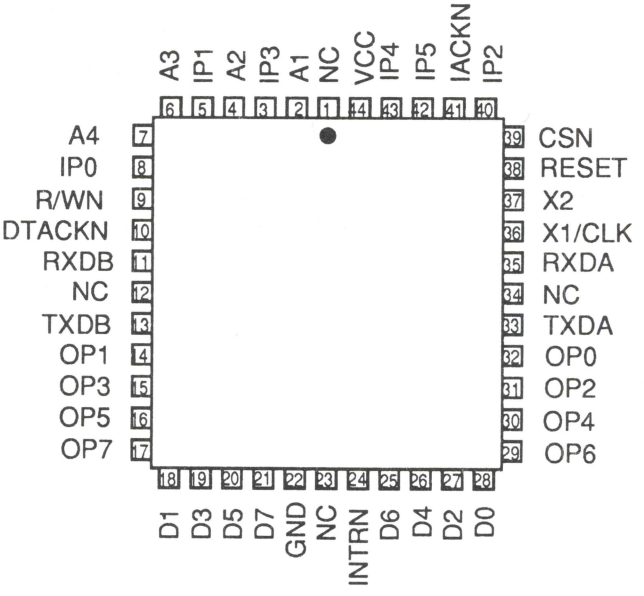
ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-88C681

TEST	SYMBOL (See Note 1)	CONDITIONS	LIMITS TEMPERATURE	MIN	MAX	UNIT	GROUP A SUBGROUP
IEI Set Up Time to RDN Low	TEIS		TA = +25°C -55°C≤TA≤+125°C	50 50		nS nS	9 10, 11
IEO Delay Time from INTRN Low	TEOD		TA = +25°C -55°C≤TA≤+125°C		100 100	nS nS	9 10, 11
A0-A3 Set Up Time to RDN, WRN Low	tAS		TA = +25°C -55°C≤TA≤+125°C	10 10		nS nS	9 10, 11
A0-A3 Hold Time fromRDN, WRN High	tAH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
CEN Set UP Time from RDN, WRN High	tCS		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
CEN Hold Time to RDN,WRN Low	tCH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RDN, WRN Pulse Width	tRW		TA = +25°C -55°C≤TA≤+125°C	225 225		nS nS	9 10, 11
Data Valid from RDN Low	tDD		TA = +25°C -55°C≤TA≤+125°C		175 175	nS nS	9 10, 11
Data Bus Floating RDN High	tDF		TA = +25°C -55°C≤TA≤+125°C	10 10	100 100	nS nS	9 10, 11
Data Set Up Time To WRN High	tDS		TA = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Data Hold Time From WRN High	tDH		TA = +25°C -55°C≤TA≤+125°C	5 5		nS nS	9 10, 11
High Time Between Reads and/or Writes	tRWD		TA = +25°C -55°C≤TA≤+125°C	200 200		nS nS	9 10, 11
IEO Delay Time From IEI	tDIO		TA = +25°C -55°C≤TA≤+125°C		100 100	nS nS	9 10, 11
IACKN Hold Time From RDN High	tIAH		TA = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11

Notes:

1. Vcc = 5.0 V 1 10%


A2 6
IP1 5
A1 4
IP3 3
A0 2
NC 1
VCC 44
IP4/IE1 43
IP5/IE0 42
IP6/IACKN 41
IP2 40
A3 7
IP0 8
WRN 9
RDN 10
RXDB 11
NC 12
TXDB 13
OP1 14
OP3 15
OP5 16
OP7 17
39 CEN
38 RESET
37 X2
36 X1/CLK
35 RXDA
34 NC
33 TXDA
32 OP0
31 OP2
30 OP4
29 OP6
18 D1
19 D3
20 D5
21 D7
22 GND
23 NC
24 INTRN
25 D6
26 D4
27 D2
28 D0


A3 6
IP1 5
A2 4
IP3 3
A1 2
NC 1
VCC 44
IP4 43
IP5 42
IACKN 41
IP2 40
A4 7
IP0 8
R/WN 9
DTACKN 10
RXDB 11
NC 12
TXDB 13
OP1 14
OP3 15
OP5 16
OP7 17
39 CSN
38 RESET
37 X2
36 X1/CLK
35 RXDA
34 NC
33 TXDA
32 OP0
31 OP2
30 OP4
29 OP6
18 D1
19 D3
20 D5
21 D7
22 GND
23 NC
24 INTRN
25 D6
26 D4
27 D2
28 D0

CMOS Quad Channel UART (QUART)

PRELIMINARY

GENERAL DESCRIPTION

The EXAR Quad Universal ASynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full duplex asynchronous communications channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR-82C684 offers a single IC solution for various microprocessor families. The 88 and 68 modes can be selected by tying SEL pin to VDD or VSS.

The QUART is fabricated using advanced two layer metal, with a high density EPI/CMOS process to provide high performance and low power consumption.

FEATURES

Four Full Duplex, Independent Channels, Asynchronous Receiver and Transmitter
Quadruple Receive and Transmit Buffer
Programmable Stop Bits in 1/16 Bit Increments
Pin Selectable 88 and 68 mode
Four Independent Internal Bit Rate Generator with more than 33 Bit Rates
Independent Bit Rate Selection for each Transmitter and Receiver
External Clock Capability
Normal, Autoecho, Local Loop Back and Remote Loopback Modes
Two Multifunction 16-Bit Counter/Timer
Interrupt Output with Sixteen Maskable Interrupt Conditions
Prioritized Interrupt Vector Output on Acknowledge
Programmable Interrupt Daisy Chain
16 General Purpose Outputs
16 General Purpose Inputs with Eight Charge of State Detectors on Inputs
Multidrop Mode Compatible with 8051 Nine-Bit Mode
On Chip Oscillator for Crystal
Stand-by Mode to Reduce Operating Power

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
All Voltages with respect to ground	-0.5V to +7 V

Consult Factory for Package Information.

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XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS		UNIT	GROUP A SUBGROUP
		SEE NOTE 1	TEMPERATURE	MIN	MAX		
Input Low Voltage	V_{IL}		T_A = +25°C -55°C < T_A < + 125°C	-0.5 -0.5	0 8 0.8	V V	1 2,3
Input High Voltage	V_{IH}		T_A = +25°C -55°C < T_A < + 125°C	2 0 2.2		V V	1 2,3
Input High Voltage (x1 / CLK)	V_{IH1}		T_A = +25°C -55°C < T_A < + 125°C	4.0 4.0	VCC VCC	V V	1 2,3
Output Low Voltage	V_{OL}	I_{OL} = 2.4mA	T_A = +25°C -55°C < TA < + 125°C		0.4 0.4	V V	1 2,3
Output High Voltage (Except pen Drain Outputs)	V_{OH}	I_{OH} = -400µA	T_A = +25°C -55°C < T_A < + 125°C	2.4 2.4		V V	1 2,3
Input Leakage Current	I_{IL}	V_{IN} = 0 to Vcc	T_A = +25°C -55°C < T_A < + 125°C	-15 -25	15 25	µA µA	1 2,3
Data Bus 3-State Leakage Current	I_{IL}	V_O =0 to Vcc	T_A = +25°C -55°C < T_A < + 125°C	-10 -10	10 10	µA µA	1 2,3
Open Drain Output Leakage Current	I_{OC}	V_O = 0 to Vcc	T_A = +25°C -55°C < T_A < + 125°C	-10 -10	10 10	µA µA	1 2,3
Power Supply Active Current	I_{CCA}		T_A = +25°C -55°C < T_A < + 125°C		15 15	mA mA	1 2,3
Power Supply Standby Current	I_{CCs}		T_A = +25°C -55°C< T_A < + 125°C		10 10	mA mA	1 2,3
Reset Pulse Width	t_{RES}		T_A = +25°C -55°C < T_A < + 125°C	1.0 1.0		µS µS	9 10,11

XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS		LIMITS			GROUP A
		SEE NOTE 1	TEMPERATURE	MIN	MAX	UNIT	SUBGROUP
Port Input Set Up Time To RD/CS Low	t_{PS}		T_A = +25°C -55°C ≤T_A ≤ + 125°C	0 0		nS nS	9 10,11
Port Input Hold Time From RD/CS High	t_{PH}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10,11
Port Output Valid From WR/CS High	t_{PD}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	400 400		nS nS	9 10,11
Inter or OP3-OP7/ OP10-OP15 When Used as Interpt High From: Clear of Interrupt Status Bit in ISR or IPCR	t_{IR}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	300 300		nS nS	9 10,11
Clear of Interrupt Mask In IMR	t_{IR}		T_A = +25°C -55°C < T_A ≤ + 125°C	300 300		nS nS	 10,11
X1/CLK(external) High or Low Time	t_{CLK}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	100 100		nS nS	9 10,11
X1/CLK Crystal or External Frequency	f_{CLK}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	2.0 2.0	7.372 7.372	MHz MHz	9 10,11
Counter / Timer External Clock High or Low Time (1P2/1P10)	t_{CTC}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	100 100		nS nS	9 10,11
Counter / Time External Clock Frequency	f_{CTC}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	0.0 0.0	7.372 7.372	MHz MHz	9 10,11
RXC and TXC (External) High or Low Time	t_{RTX}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	220 220		nS nS	9 10,11

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XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

RXC nd TXC (External) Frequency 16X	f_{RTX}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	0.0 0.0	16.0 16.0	MHz MHz	9 10, 11
RXC and TXC (External) Frequency 1X	f_{RTX}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	0.0 0.0	1.0 1.0	MHz MHz	9 10, 11
TXD Output Delay from TXC (External) Low	t_{TXD}		TA = +25°C -55°C ≤ T_A ≤ + 125°C		350 350	nS nS	9 10, 11
TXD Output Delay from TXC (Internal) Output Low	t_{TCS}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C	0 0	150 150	nS nS	9 10, 11
RX[) Data Setup Time to RXC External High	t_{RXS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	240 240		nS nS	9 10, 11
RXD Data Hold Time from RXC External High	t_{RXH}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	200 200		nS nS	9 10,11
IEI Setup Time to RD Low	T_{EIS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	 50	50 	 nS	nS 9 10,11
IEO Delay Time from Internal Low	T_{EOD}		T_A = +25°C -55°C ≤ T_A ≤ + 125°C		100 100	nS nS	9 10,11
A0-A4 Setup Time to RD, WR Low	t_{AS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	10 10		nS nS	9 10,11
A0-A4 Hold Time from RD, WR Low	t_{AH}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10,11
CS Setup Time to RD, WR Low	t_{CS}		TA = +25°C -55°C ≤ T_A ≤ + 125°C	0 0		nS nS	9 10,11

XR-82C684 ELECTRICAL PERFORMANCE CHARACTERISTICS

CS Hold Time from RD, WR High	t_{CH}		T_A = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11
RD, WR Pulse Width	t_{RW}		T_A = +25°C -55°C≤TA≤+125°C	225 225		nS nS	9 10, 11
Data Valid from RD Low	t_{DD}		T_A = +25°C -55°C≤TA≤+125°C		175 175	nS nS	9 10, 11
Data Bus Floating from RD High	t_{DF}		T_A = +25°C -55°C≤TA≤+125°C	10 10	100 100	nS nS	9 10, 11
Data Setup Time to WR High	t_{DS}		T_A = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
Data Hold Time from WR High	t_{DH}		T_A = +25°C -55°C≤TA≤+125°C	5 5		nS nS	9 10, 11
High Time Between Reads and/or Writes	t_{RWD}		T_A = +25°C -55°C≤TA≤+125°C	100 100		nS nS	9 10, 11
IEO Delay Time from IEI	t_{DIO}		T_A = +25°C -55°C≤TA≤+125°C		100 100	nS nS	9 10, 11
IACK Hold Time from RD High	t_{IAH}		T_A = +25°C -55°C≤TA≤+125°C	0 0		nS nS	9 10, 11

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QUALITY ASSURANCE AND RELIABILITY

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QUALITY ASSURANCE

INTRODUCTION

The practice of Quality Assurance (QA) at Exar revolves around the use of active controls in the purchase of materials, the fabrication of wafers, the assembly of die, test and shipment of finished parts. This requires that all materials and processes be properly documented and that audits and inspections be used to insure that the written specifications are available and being followed. Adherence to written specifications is the foundation of consistent and repeatable processes. This provides the "basis" upon which more elegant statistical control procedures may be used.

The Exar QA program also contains those key elements necessary to process to MIL-STD-883 and MIL-M-38510, Appendix A. These elements include control of equipment maintenance and calibration, control of cleanliness and atmosphere in the wafer fab area, personnel training and certification, and corrective action programs.

Vendor Control

All critical purchased materials are documented so that Exar vendors know exactly what is expected. critical material vendors are qualified prior to accepting material. Qualified vendors are periodically audited and those consistently meeting these requirements are preferred by placing them on the approved vendor list (AVL). Use of vendors who are not on the AVL requires the prior approval of Exar QA (there may be new vendors who are being qualified prior to placing on the AVL, for example). Incoming QA (IQA) inspection is performed either on a sample or 100% basis. IQA results are monitored by statistical process control (SPC) charts to monitor the ability of the vendor to control critical processes. Vendors who consistently utilize statistical control receive less frequent audits and IQA inspections making them more cost effective for Exar operations. Exar vendors are rated accordingly with orders being placed with the best ones.

Wafer Fabrication Process Control

All critical wafer fabrication processes are documented and those specifications are followed by Exar processing personnel. For this reason, Exar QA signs off on the approval of all process specifications and audits all wafer fabrication processes on a periodic basis. The audits enforce the adherence to those specifications and indicate when updating is required. All major process changes require that a process qualification be run prior to acceptance of material from the changed process. Any deviations from specifications for production wafer lots requires the approval of Exar QA. Critical process steps are monitored by use of in-process inspections and SPC charting which enables process adjustment by statistical criteria only. Each wafer must pass thorough in-process inspections. This enables the ability to control state of the art processes within very tight tolerances. Critical process steps which consistently exhibit control are candidates for less frequent collection of data for SPC purposes. The emphasis is upon the capability of given processes to exhibit statistical control (uniformity).

Assembly Process Control

Assembly vendors are selected on the basis of their ability to control the packaging process. Each vendor is placed on the AVL after successful completion of a vendor qualification. This includes the use of vendor internal written specifications and audits by Exar of those processes. Exar QA audits each assembly house a minimum of once per year. Additionally, Exar QA pulls lot samples for destructive incoming inspections of assembled product. The sample inspection results are monitored by SPC charts to assess the vendors ability to control the processes. Vendors who consistently utilize statistical control receive less frequent audits making them more cost effective for Exar operations.

Exar also maintains an onshore assembly facility with well documented processes. The area is audited and monitored with SPC charts to assess the control over the process.

Test and Shipping Process Control

All handling of finished product through final test and shipping is per written specification. These areas are periodically audited to assure adherence to specifications. The handling specifications include ESD protection for all Exar products.

After final test, every lot goes through a sample test using LTPD 2(0) at room temp by final Q.C to assure that all final tests and handling of the material has been performed to specification. Any lot which fails the sample criteria is re-screened to make sure that no defective product gets shipped. Plant clearance inspection is performed to assure that all customer specifications have been met prior to shipment. This insures that the test traveller is correct and that all steps have been accomplished according to customer requirements.

SPC Program

In order for Exar to maintain a competitive edge in the manufacturing of integrated circuit products, we need to minimize the production of defective material in fabrication, assembly and test.

The traditional approach to ensuring quality is for the production group to manufacture material and the quality group to inspect and/or lest the product to sort out any defects prior to shipment.

The definition of what is acceptable is provided either by the customer or by the design and manufacturing specifications. However, the use of after-the-fact inspection is not a very effective strategy because the damage (of producing defective material) has already been done. In order to improve Exar products overall, systematically eliminating the causes of defective production is crucial; it is clearly necessary to maximize the production of good material and minimize the production of unuseable material.

The major indication of production of defective unuseable material is excessive variation in manufacturing. SPC is an effective method to continuously monitor the variation in key process steps, and to provide the criteria for making adjustments to the process, when necessary, to maintain control. As the product is sampled repeatedly, the mark of a process under (statistical) control is that over time, each critical process parameter is proven to follow one statistical distribution with one mean (average) and one standard deviation. When a process is not under control, the distributions of key process parameters will tend to wander (having more than one mean and/or standard deviation).

When all critical processes are in control, never-ending quality improvement can take place. Customers will benefit by improved levels of quality and reliability of products received from Exar.

The implementation of such a program is not a simple task, given the vast number of process steps (and the inherent complexity of those steps) required by Exar's semiconductor products. An SPC plan has been written and implementation is in progress.

If you or any of your customers are interested in our progress in implementation of SPC, please contact Exar Quality Assurance.

OUTGOING QUALITY MONITOR

Introduction

One task of Exar Quality Assurance is to monitor outgoing quality, or estimate the defective parts a customer is likely to observe in the inspection or application of parts produced by Exar.

Outgoing electrical quality estimates are given in parts per million (PPM) defective. Outgoing lots are sampled and inspected/tested by the Quality Control (QC) group in Quality Assurance using the QC test program and visual criteria. Reslts of the QC sampling are used to estimate the outgoing electrical/mechanical quality. The QC program tests all critical parameters and functions to the data sheet or specification. All Exar parts are 100% functionally and parametrically tested prior to the QC sample electrical test, with the QC sample, the final guarantee that the lot conforms to the specification. The QC electrical sample, unless otherwise specified, is run at room temperature (25°C). The visual criteria are provided in Exar's external visual inspection specification.

It is important to note that Exar guarantees an acceptable quality level (AQL) of less than 0.1% (1000 PPM) for electrical parameters and visual criteria. With current Exar QC electrical sample plan (of 116 devices tested per lot, accept with no defectives, reject on one or more defectives), the sample AQL is actually 0.04% (approximately 400 PPM defective) for all lots. AQL implies nothing about the average outgoing quality (AOQ) that Exar currently ships. Exar track AOQ values on a monthly basis.

DEFINITIONS

Before getting into further details, some definitions are called for as follows:

p : Process average PPM defective, the PPM defective observed in the QC electrical test and visual samples or simply the number defective divided by the number sampled.

Pa(p) : Probability of acceptance for a given lot sample based on the lot sample plan which includes sample acceptance/rejection criteria. For instance, a popular plan is to pull a sample of 116 parts from a lot and run the QC electrical test and visual inspection. If one or more parts fail, the lot from which the sample came is rejected and goes back for a complete screen to sort out all defectives. Pa(p) is simply the probability that a lot with a given process average PPM defective, p, will pass the 116 piece sample test with no defectives.

AQL : Acceptable quality level, that value of p for which we have Pa(p) = 0.95, or that PPM defective for which we have a 95% chance of passing the QC sample test/inspection for a given lot.

LTPD : Lot tolerance percent defective, that value of p for which we have Pa(p) = 0.10, or that PPM defective for which we have a 10% chance of passing the QC sample testlinspection for a given lot.

Rectifying Sample Inspection Plan: A sample plan for which a lot failing to pass the sample acceptance criteria is re-screened thereby sorting out all defectives.

AOQ : Average outgoing quality, the average PPM defective which we are shipping when we use rectifying sample inspection. It is important to know that there is some very low rate of defectives that exists in lots which pass the acceptance criteria when rectifying sample inspection is used. We use a method to estimate AOQ which uses results from a series of lots. This estimator is calculated as follows:

$$\text{AOQ (estimate)} = \frac{A}{A+B}$$

Where A = the number of lots in the series with one defective in the QC sample test/inspection divided by the lot sample size and B = the number of lots in the series with no defectives in the QC electrical sample test.

AOQL : Average outgoing quality limit, the absolute maximum level of PPM defective that can be shipped based on use of rectifying sample inspection plan. This recognizes that as we produce lots, the PPM defective varies. For p values that are high, we tend to reject the lot samples and screen lots so that shipments of the screened lots are defect free. For p values that are low, we tend to pass lots which have very few defectives. AOQL tells us what the worst PPM defective is under that sample plan regardless of how much p varies from lot to lot.

EXAR uses a rectifying sample inspection scheme in which lots failing the sample acceptance criteria are re-screened 100% prior to lot acceptance. This implies that lots which fail the sample acceptance criteria are considered defect free after screening and lots which pass the sample criteria have a very low defective rate. Therefore even after the QC electrical sample test, some defects (very few) may still exist in the lot. It is necessary to estimate what the rate of defective is for lots shipped. This requires collection of QC electrical sample results for a series of lots in order to estimate the average PPM defective value AOQ (average outgoing quality). Results can be assembled in a way that the sumof the lot sizes for lot samples in the series that were defect free, and the sum of lot sizes for samples containing one defective. For example, suppose a series of 100 lots are processed with a QC sample test/inspection of 116 pieces per lot. Further suppose that 94 lots were defect free and 3 lots had one defective, 2 lots had two defectives and 1 lot had three defectives, we would compute AOQ as follows:

$$AOQ = \frac{3/116}{3/116 + 94} = 10^6 = 275 \text{ PPM}$$

Any questions regarding Exar PPM defective levels or the methods of AOQ estimation should be addressed to the Quality Assurance Department.

RELIABILITY ASSURANCE

INTRODUCTION

EXAR Reliability Assurance begins with product design and continues throughout the life of the product.

During the design phase of a new product Reliability Engineering reviews the design rules, and the processes and material to be used. The review insures that at least the minimum requirements of MIL-M-38510.

A reliability evaluation or qualification is performed on all new design rules, processes and materials.

When the design is frozen, but before the product is released to production, Reliability Engineering performs an extensive physical analysis and stress tests to verify the reliability of the design. The physical analysis includes internal and external visual, bonding and die attach evaluation, passivation integrity and SEM. Stress tests includes mechanical, environmental and electrical stresses. The results of the stress tests are used to predict the life of the product and to identify the prevalent failure mechanisms.

Once the product is released to production Reliability Engineering performs qualification in accordance with MIL-STD-883 method 5005, establishes a reliability data base for the product tests. The reliability data base includes data from qualification and extended lifetime tests. The data base is reviewed periodically to identify reliability trends and to establish reliability statistics.

Reliability Engineering analyzes all qualification and field failures and provides feedback into the system to enhance the reliability of EXAR product.

FAILURE ANALYSIS CAPABILITY

After EXAR has performed all of the environmental stress testing on the product any failures that have occurred during the stress need to be analyzed to determine the cause of failure.

EXAR has a full complement of tools available to perform extensive failure determination. The results of the analysis are then relayed to the appropriate groups to determine any corrective action for improving the product. Also any customer requested failure analysis can be handled by EXAR's failure analysis group. Reports are generated and the information is provided to the customer for his analysis. The following is a short description of EXAR's failure analysis capability.

Procedure

Exar can analyze a failure starting with an initial electrical examination all the way through to a detailed structural and internal visual examination pinpointing the exact physical element on the die that has failed. The failure analysis group uses a variety of analysis equipment to perform this determination.

Curve Tracer

The curve tracer is a simple but essential tool to perform the first level of analysis on a failing device. The current-voltage characteristics are taken on every pin of the device to determine electrical opens, shorts or anomalous behavior at the dc level. At this point it may be possible to limit the analysis to particular pin. Some of the types of failures isolated at this stage may be electrical overstress, ESD (Electrostatic discharge) failures, leakage failures bonding problems or other assembly related issues.

Package Decapsulation

Almost all failures require decapsulating the device to perform an internal visual examination of the die. Ceramic and cerdip packages are decapsulated mechanically while plastic packages may require chemical methods. A plastic package is usually decapsulated using either sulfuric acid or fuming nitric acid. In some cases plastic packages can also be mechanically decapsulated. In the normal situation a "Jet Etcher" is used to quickly but carefully remove the plastic over the die surface. The die is then exposed and a visual examination can be performed.

High Power Optical Microscope

A high power optical microscope is used to examine the die surface and the bonding and assembly quality of the device. The microscope is equipped to perform phase contrast and dark field analysis to enhance any topographical features during visual examination. At this point in the analysis failure mechanisms which exhibit any visual change may be observed. A multitude of failure mechanisms may show up now due to physical changes caused by the failure process. The exact location of the failure may now be determined and correlated to previous electrical data. Process induced failures are also evident at this point. Some failure mechanisms that are observed may be electromigration, electrostatic discharge damage, junction or oxide failure, metal corrosion among many others.

Electrical Microprobing

When the visual examination via the optical microscope shows no anomalies then it may be necessary to do electrical microprobing to determine the location of the failing element on the die. This is done by physically measuring electrical characteristics on the individual elements of the die itself. Probing may entail a sequential cutting and electrical measuring on the metal interconnects between transistors until the failure location is determined.

Liquid Crystal Analysis

This technique can be used in lieu of or in conjunction with microprobing. It uses temperature sensitive liquid crystal that changes color when a spot on the die draws excessive power. This may be a way to determine areas which are damaged but show no visual evidence during the optical microscope analysis. Oxide shorts and junction damage are quite often apparent during use of this procedure.

Selective Deprocessing

When there is a need to look at different layers of the die surface then various selective deprocessing techniques are used. Plasma enhanced etching along with wet chemical etching removes layer after layer of the die surface with visual examination being performed after each removal. This allows the failure site to be examined in more detail and to pin point the precise layer at which failure has occurred. Gate oxide ruptures and pin holes in the interlayer oxides can be usually found during this procedure. Deprocessing allows previously hidden fail sites to to become apparent.

Scanning Electron Microscope

One of the final methods to obtain a detailed look at a failure site is to use a Scanning Electron Microscope. This method allows extremely high (300,000x) magnification of the fail site. Very fine detail can be obtained which is possible in no other way. The failure mechanisms can be studied and a cause can be assigned based on the morphology of the fail site. Metallurgical problems can be studied at this level of magnification and process issues become very evident. An additional feature that is possible with the help of the SEM is the use of Voltage Contrast and Electron Beam Induced Current techniques. Voltage contrast allows one to electrically exercise the device and observe voltage levels as they propagate along the internal conducting lines. When an unexpected break in the voltage level occurs a fail site has been identified. Electron Beam Induced Current (EBIC) analysis allows one to find degraded or damaged junctions which would otherwise not be visible optically.

Cross-Sectioning Analysis

Cross-Sectioning is performed on both die failures and assembly failures. This technique allows one to see the entire profile of the process and to delineate areas which are at or below the silicon surface. Assembly failures, in particular, are brought out very clearly with this technique. In addition, staining can show the depth of and damage to diffused junction below the silicon surface. Electrical shorts between multiple level conductors can be seen using cross-sectioning and interlevel oxide quality can be determined.

Electron Dispersive X-Ray Analysis

This technique (EDX) is used in conjunction with the SEM and determines the elemental (Periodic Table) composition of the material being observed. It allows one to find the identity of contaminants that may cause specific failures. These contaminants may have been introduced during the fabrication of the die or possibly during the assembly operation. Corrective action may then be taken at the appropriate manufacturing site based on the EDX finding.

FAILURE RATE CALCULATIONS

Failure rate prediction calculations are based on what is known as the Arrhenius Model. This model assumes that most failures are due to component degradation that follow the laws of Reaction-rate kinetics. This model has been shown to work quite well for most types of failure mechanisms.

Each failure mechanism is observed to have its own characteristic Acceleration Factor when doing Temperature accelerated environmental stress testing. By performing environmental testing at elevated temperatures one can then use this factor to predict failure rates at actual application temperatures. In practice the acceleration factor is obtained from an Activation Energy of the failure mechanism. The Activation Energy (in Electron Volts) is an average value that is determined from experimental data taken over an extended period of time. Activation Energy is a rough measure of the thermal energy that is required for an electrochemical reaction (failure mechanism) to occur.

The formula for the Acceleration Factor is given as:

$$\text{ACCELERATION FACTOR} = \frac{R1}{R2} = e^{\frac{Ea}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)}$$

where:

R1 = Failure rate at junction temperature T1
R2 = Failure rate at junction temperature T2
e = Base for Natural Logarithms - 2.71818....
Ea = Activation Energy in electron volts

K = Boltsmann's Constant ($8.625 \times 10^{-5} ev/o_K$)

T1 is taken as the Accelerated test temperature
T2 is taken as the Operating temperature

Also once failure rate is known MTBF (Mean Time Between Failures) can be calculated as:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

To calculate the failure rate the total Device Hours (No. of devices on test times the total hours on test) is multiplied by the Acceleration Factor to give the Total Equivalent Device hours at the operating temperature. Then the following formula gives the failure rate (at a particular Confidence Level).

$$\text{Failure Rate} = \frac{CHI^2}{2t}$$

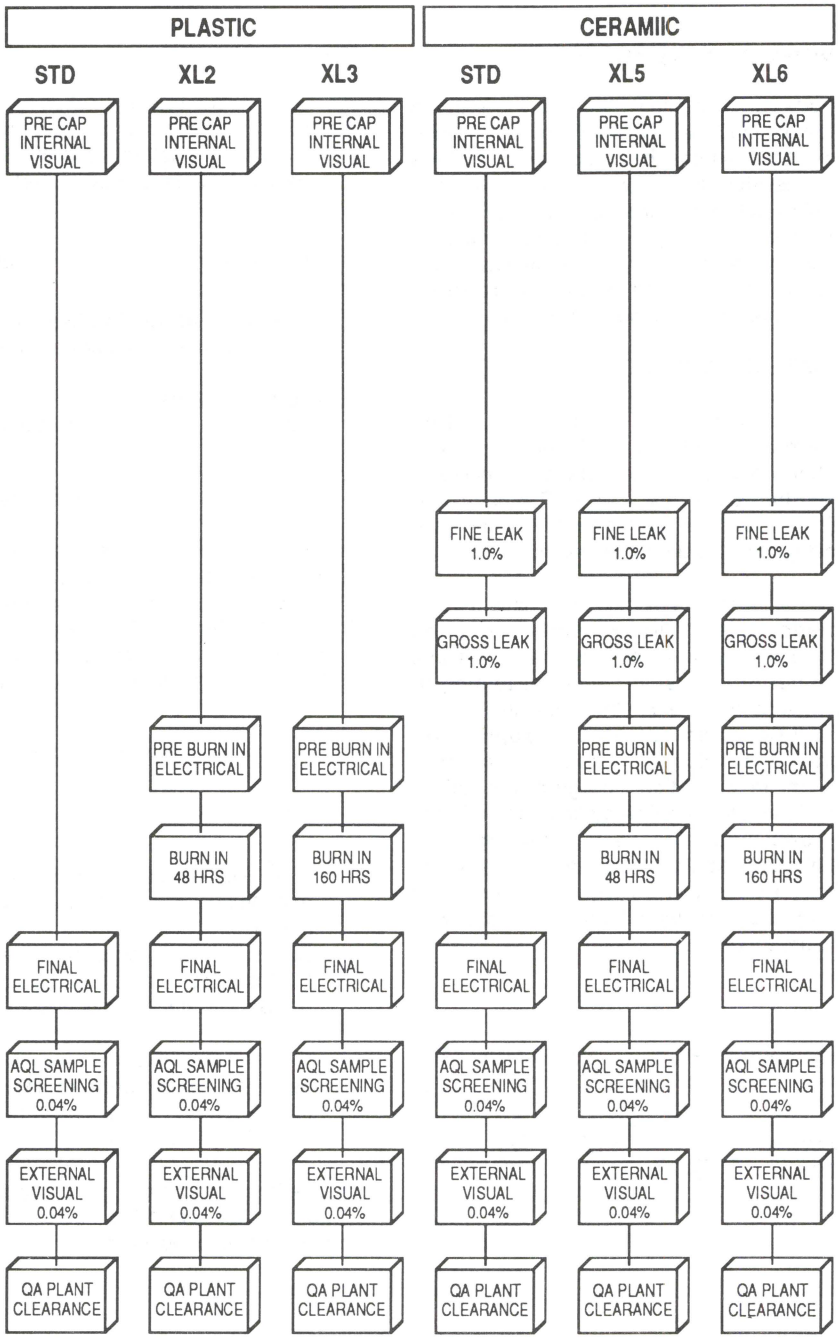
where:

CHI^2 = CHI Square distribution (available from mathematics handbooks) with confidence level and DF
DF = Degrees of freedom = 2 x number of failures +2
t = Total Equivalent Device Hours
α = Statistical error expected in the failure rate

$1 - \alpha$ = is the confidence level we have (i.e. 90 percent or 60 percent sure) that the ACTUAL failure rate is no worse than the above CALCULATED failure rate.

The failure rates are generally expressed in either percent fails per 1000 hours or in FITS (1 fail in 1 billion hours of operation).

8



NOTE: ALL OPERATIONS ARE 100% UNLESS OTHERWISE SPECIFIED.

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PACKAGING INFORMATION

Section 9 - Packaging Information **9-1**

Package Outlines

Plastic Dual In Line (P) 9-3

Shrink Plastic Dual In Line (P) 9-4

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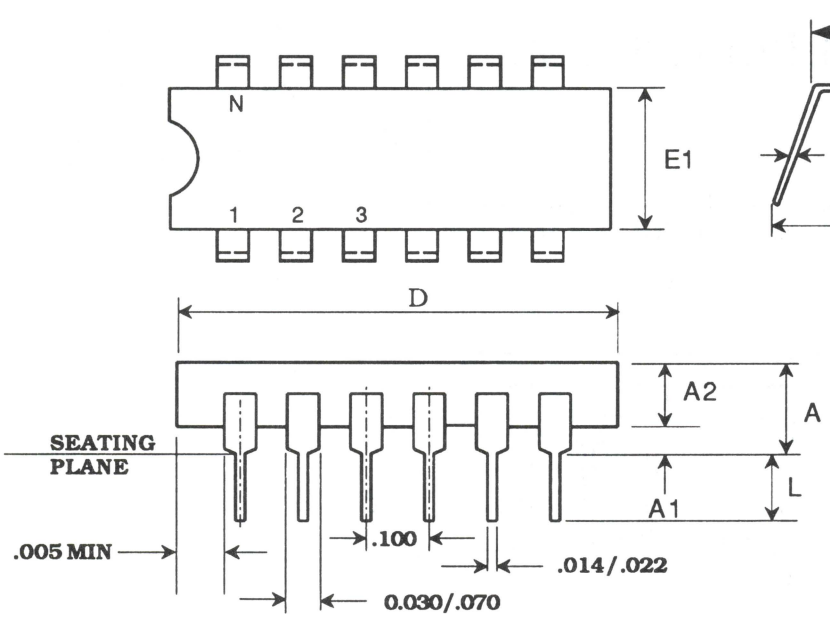
48 LD Very Small Quad Flat Pack (V) 9-13

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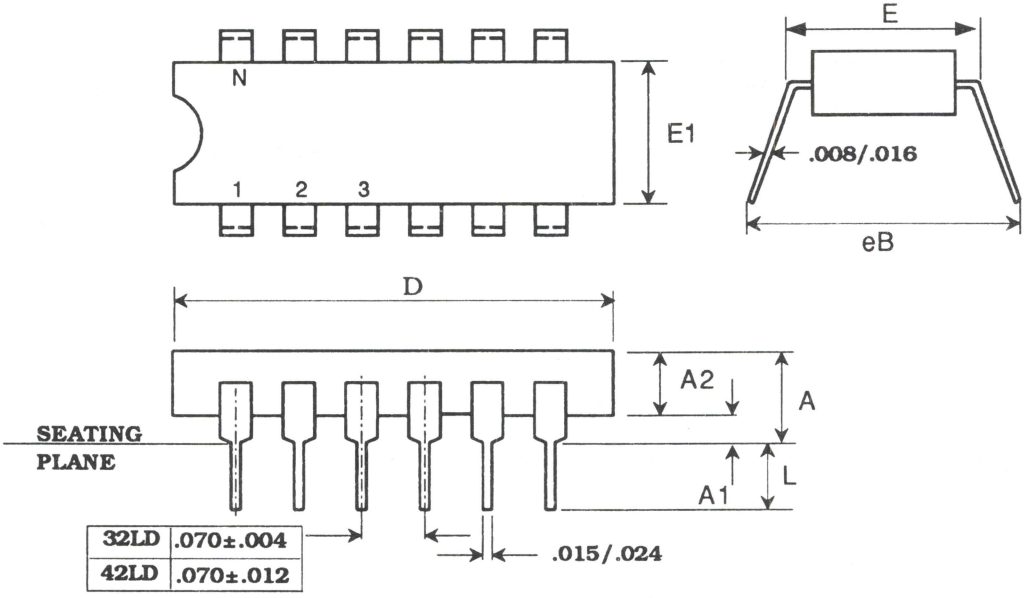
Plastic Dual In Line Package ("P" Package)



LEAD COUNT	A MIN/MAX	A1 MIN/MAX	A2 MIN/MAX	D MIN/MAX	E MIN/MAX	E1 MIN/MAX	eB MIN/MAX	L MIN/MAX
8LD	.145/.210	.015/.070	.115/.195	.348/.430	.300/.325	.240/.280	.310/.430	.115/.160
14LD	.145/.210	.015/.070	.115/.195	.725/.795	.300/.325	.240/.280	.310/.430	.115/.160
16LD	.145/.210	.015/.070	.115/.195	.745/.840	.300/.325	.240/.280	.310/.430	.115/.160
18LD	.145/.210	.015/.070	.115/.195	.845/.925	.300/.325	.240/.280	.310/.430	.115/.160
20LD	.145/.210	.015/.070	.115/.195	.925/1.060	.300/.325	.240/.280	.310/.430	.115/.160
22LD(.300)	.145/.210	.015/.070	.115/.195	1.000/1.070	.285/.315	.240/.280	.310/.430	.115/.160
22LD(.400)	.145/.210	.015/.070	.125/.195	1.050/1.120	.390/.425	.330/.380	.400/.500	.115/.160
24LD(.300)	.145/.210	.015/.070	.115/.195	1.125/1.275	.300/.325	.240/280	.310/.430	.115/.160
24LD(.600)	.160/.250	.015/.070	.125/.195	1.150/1.290	.600/.625	.485/.580	.600/.700	.115/.200
28LD	.160/.250	.015/.070	.125/.195	1.380/1.565	.600/.625	.485/.580	.600/.700	.115/.200
40LD	.160/.250	.015/.070	.125/.195	1.980/2.095	.600/.625	.485/.580	.600/.700	.115/.200
48LD	.160/.250	.015/.070	.125/.195	2.385/2.480	.600/.625	.485/.580	.600/.700	.115/.200

***ALL DIMENSIONS ARE IN INCHES**

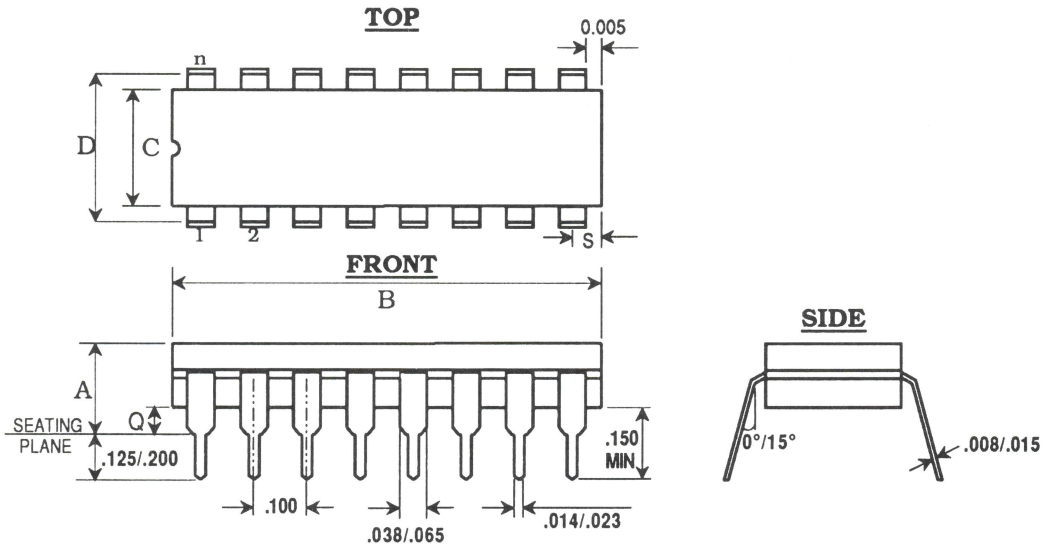
Shrink Plastic Dual In Line Package ("P" Package)



LEAD COUNT	A MIN/MAX	A1 MIN/MAX	A2 MIN/MAX	D MIN/MAX	E MIN/MAX	E1 MIN/MAX	eB MIN/MAX	L MIN/MAX
32LD	.173/.197	.038/.049	.133/.149	1.099/1.123	.388/.412	.318/.342	.429/.469	.118/.134
42LD	.169/.185	.020/.032	.150/.154	1.461/1.469	.543/.551	.587/.610	.630/.669	.114/.138

*ALL DIMENSIONS ARE IN INCHES

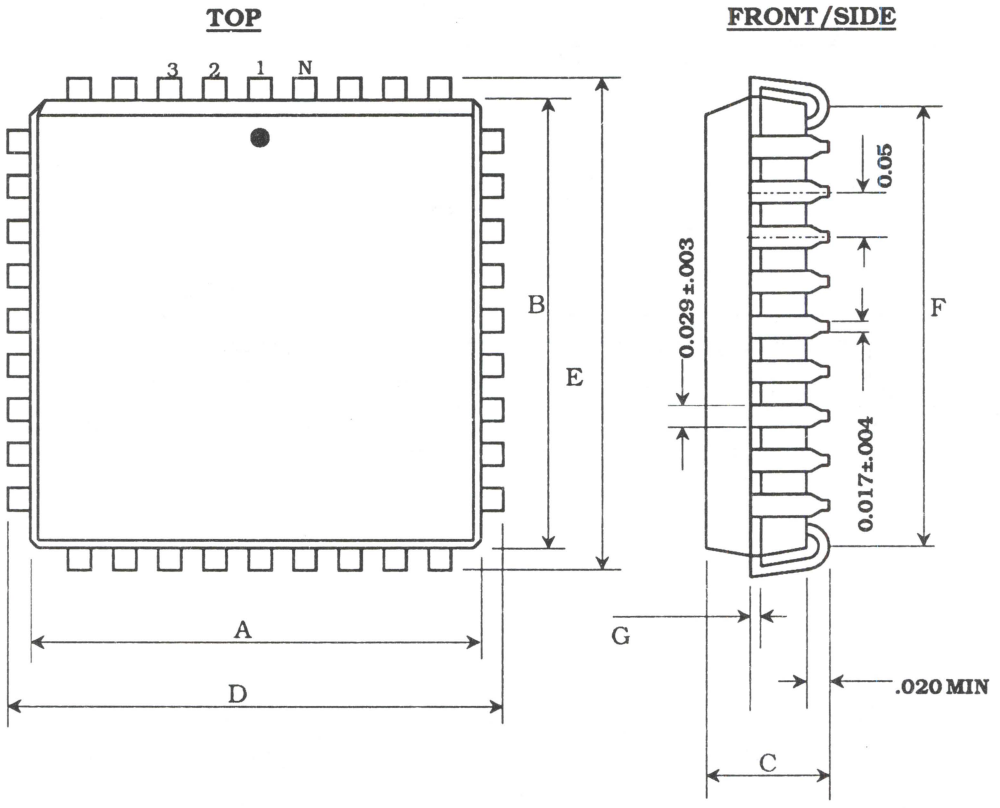
Ceramic Dual In Line Package ("N" Package)



LD COUNT	A	B	C	D	Q	S
	MAX	MAX	MIN/MAX	MIN/MAX	MIN/MAX	MAX
08LD	0.200	0.376/0.405	.220/.310	.290/.320	.015/.060	0.055
14LD	0.200	0.754/0.785	.220/.310	.290/.320	.015/.060	0.098
16LD	0.200	0.754/0.840	.220/.310	.290/.320	.015/.060	0.080
18LD	0.200	0.882/0.960	.220/.310	.290/.320	.015/.070	0.098
20LD	0.200	0.942/1.060	.220/.310	.290/.320	.015/.070	0.080
22LD	0.225	1.062/1.111	.350/.410	.390/.420	.015/.070	0.080
24LD(.300)	0.200	1.240/1.260	.220/.310	.290/.320	.015/.060	0.098
24LD(.400)	0.225	1.240/1.280	.350/.410	.380/.420	.015/.060	0.070
24LD(.600)	0.225	1.240/1.290	.500/.610	.590/.620	.015/.075	0.098
28LD	0.232	1.440/1.490	.500/.610	.590/.620	.015/.060	0.100
40LD	0.225	2.040/2.096	.510/.620	.590/.630	.015/.070	0.098

***ALL DIMENSIONS ARE IN INCHES.**

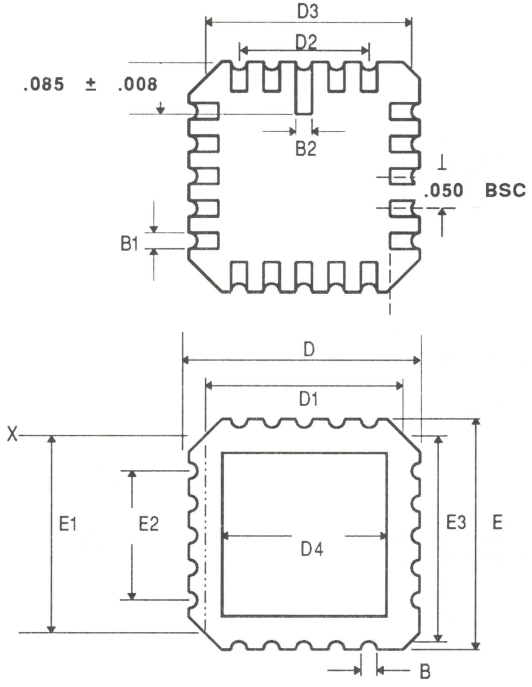
Plastic Leaded Chip Carrier ("J" Package)



LD COUNT	A	B	C	D	E	F	G
	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX
20LD	.350/.356	.350/.356	.165/.180	.385/.395	.385/.395	.290/.330	.0097/.0103
28LD	.450/.456	.450/.456	.165/.180	.485/.495	.485/.495	.390/.430	.0097/.0103
44LD	.650/.656	.650/.656	.165/.180	.685/.695	.685/.695	.590/.630	.0097/.0103
52LD	.750/.756	.750/.756	.165/.200	.785/.795	.785/.795	.690/.730	.0097/.0103
68LD	.950/.958	.950/.958	.165/.200	.985/.995	.985/.995	.890/.930	.0077/.0083
84LD	1.150/1.158	1.150/1.158	.165/.200	1.185/1.195	1.185/1.195	1.090/1.130	.0077/.0083

*ALL DIMENSIONS ARE IN INCHES.

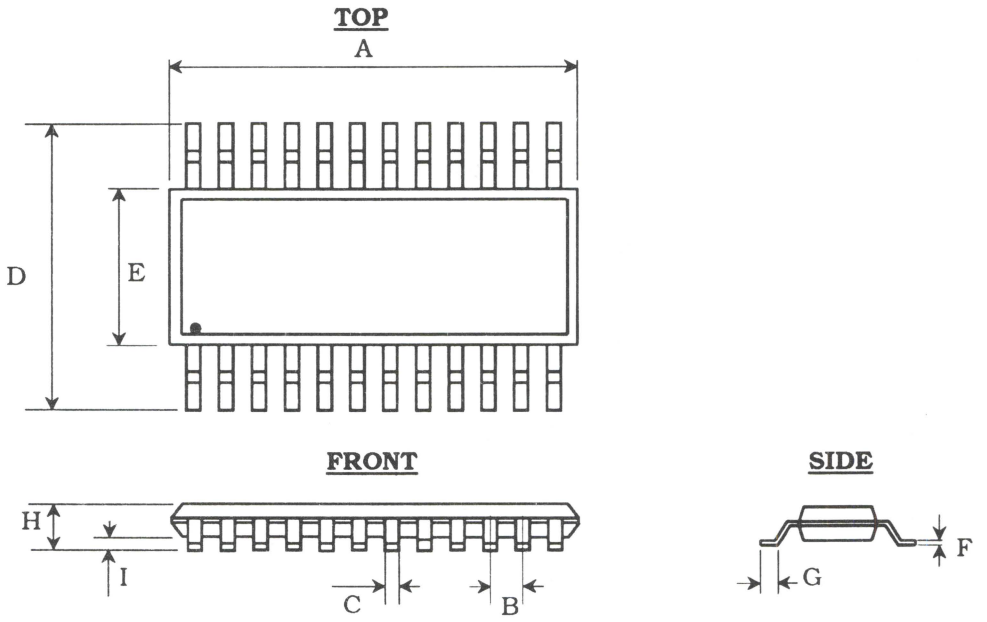
Leadless Ceramic Chip Carriers ("L" Package)



	24LC		28LC		44LC		52LC		68LC		84LC	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	.017	.088	.017	.088	.037	.088	.037	.088	.037	.088	.037	.088
A1	.064	.100	.064	.100	.069	.120	.082	.120	.082	.120	.082	.120
A2	.007	.075	.007	.075	.007	.080	.007	.080	.007	.080	.007	.080
B	-	-	-	-	.033	.039	.033	.039	.033	.039	.033	.039
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.022	.041	.022	.041	.022	.041	.022	.041	.022	.041	.022	.041
D	.395	.410	.442	.458	.640	.660	.739	.761	.938	.962	1.135	1.165
D1	.358	.367	.404	.415	.600	.620	.699	.721	.898	.922	1.095	1.125
D2	.250		.300		.500		.600		.800		1.000	
D3	.370 REF.		.420 REF.		.620 REF.		.720 REF.		.920 REF.		1.120 REF.	
D4	.352	.408	.406	.458	.495	.560	.495	.560	.495	.862	.495	1.065
E	.395	.410	.442	.458	.640	.660	.739	.761	.938	.962	1.135	1.165
E1	.358	.367	.404	.415	.600	.620	.699	.721	.898	.922	1.095	1.125
E2	.250		.300		.500		.600		.800		1.000	
E3	.370 REF.		.420 REF.		.620 REF.		.720 REF.		.920 REF.		1.120 REF.	
E4	.352	.408	.406	.458	.495	.560	.495	.560	.495	.862	.495	1.065

***ALL DIMENSIONS ARE IN INCHES**

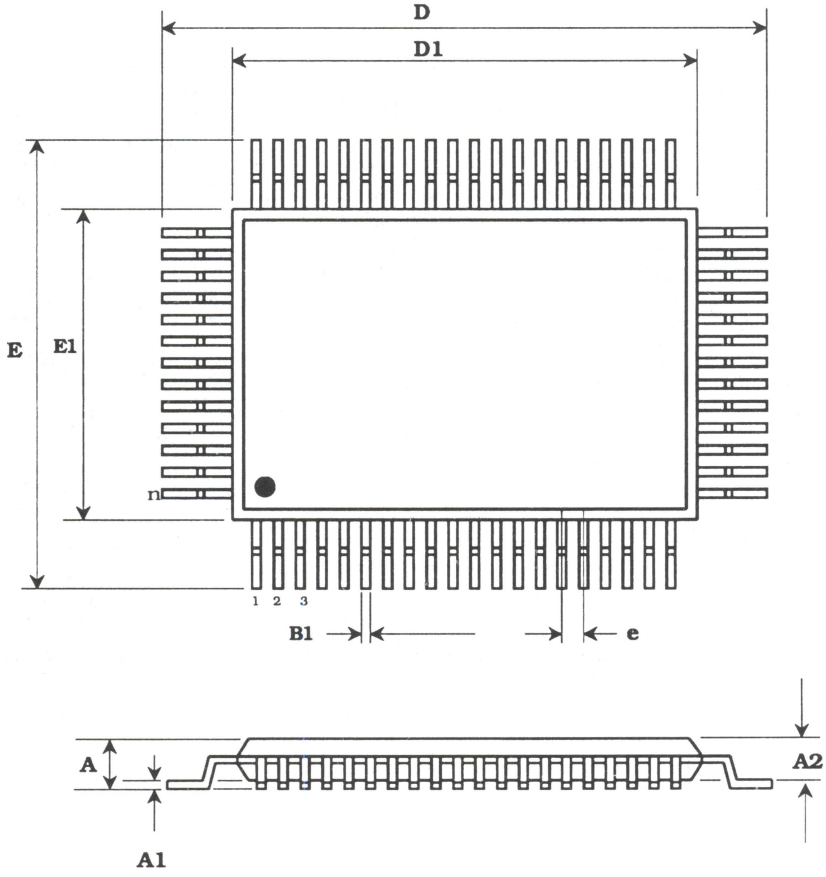
JEDEC Small Outline Package ("D" Package)



LD COUNT	A	B	C	D	E	F	G	H	I
	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX
8LD	.189/.197	0.050	.014/.019	.228/.244	.150/.157	.007/.010	.016/.050	.053/.069	.004/.010
14LD	.336/.344	0.050	.014/.019	.228/.244	.150/.157	.007/.010	.016/.050	.053/.069	.004/.010
16LD(.150)	.385/.394	0.050	.014/.019	.228/.244	.150/.157	.007/.010	.016/.050	.053/.069	.004/.010
16LD(.300)	.397/.413	0.050	.014/.019	.394/.419	.291/.299	.009/.012	.016/.050	.092/.104	.004/.012
18LD	.446/.462	0.050	.014/.019	.394/.419	.291/.299	.009/.012	.016/.050	.092/.104	.004/.012
20LD	.496/.511	0.050	.014/.019	.394/.419	.291/.299	.009/.012	.016/.050	.092/.104	.004/.012
24LD	.598/.614	0.050	.014/.019	.394/.419	.291/.299	.009/.012	.016/.050	.092/.104	.004/.012
28LD	.696/.712	0.050	.014/.019	.394/.419	.291/.299	.009/.012	.016/.050	.092/.104	.004/.012
32LD	.800/.815	0.050	.014/.019	.493/.519	.390/.398	.009/.012	.016/.050	.092/.104	.004/.012
34LD	.697/.713	0.040	.014/.019	.393/.419	.291/.299	.009/.012	.016/.050	.092/.104	.004/.012

***ALL DIMENSIONS ARE IN INCHES.**

Plastic Quad Flat Pack Drawing ("Q" Package)



EIAJ Plastic Quad Flat Package Dimension Table ("Q" Package)

LEAD	32LD			44LD			56LD			64LD			80LD		
COUNT	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35 (0.053)	–	1.60 (0.063)	2.05 (0.081)	–	2.30 (0.090)	2.05 (0.081)	–	2.30 (0.090)	2.05 (0.081)	–	2.30 (0.090)	2.60 (0.102)	–	2.85 (0.112)
A1	0.00 (0.000)	–	0.05 (0.002)	0.00 (0.000)	–	0.05 (0.002)	0.00 (0.000)	–	0.05 (0.002)	0.00 (0.000)	–	0.05 (0.002)	0.00 (0.000)	–	0.05 (0.002)
A2	1.35 (0.053)	1.45 (0.057)	1.55 (0.061)	2.05 (0.081)	2.15 (0.084)	2.25 (0.088)	2.05 (0.081)	2.15 (0.084)	2.25 (0.088)	2.05 (0.081)	2.15 (0.084)	2.25 (0.088)	2.60 (0.102)	2.70 (0.106)	2.80 (0.110)
D	8.70 (0.342)	9.00 (0.354)	9.30 (0.366)	13.70 (0.539)	14.00 (0.551)	14.30 (0.563)	12.10 (0.476)	12.40 (0.488)	12.70 (0.500)	23.70 (0.933)	24.00 (0.945)	24.30 (0.957)	23.70 (0.933)	24.00 (0.945)	24.30 (0.957)
D1	6.70 (0.263)	7.00 (0.275)	7.30 (0.287)	9.70 (0.382)	10.00 (0.394)	10.30 (0.405)	9.70 (0.382)	10.00 (0.394)	10.30 (0.405)	19.70 (0.776)	20.00 (0.788)	20.30 (0.800)	19.70 (0.776)	20.00 (0.788)	20.30 (0.800)
E	8.70 (0.342)	9.00 (0.354)	9.30 (0.366)	13.70 (0.539)	14.00 (0.551)	14.30 (0.563)	12.10 (0.476)	12.40 (0.488)	12.70 (0.500)	17.70 (0.697)	18.00 (0.709)	18.30 (0.721)	17.70 (0.697)	18.00 (0.709)	18.30 (0.721)
E1	6.70 (0.263)	7.00 (0.275)	7.30 (0.287)	9.70 (0.382)	10.00 (0.394)	10.30 (0.405)	9.70 (0.382)	10.00 (0.394)	10.30 (0.405)	13.70 (0.539)	14.00 (0.551)	14.30 (0.563)	13.70 (0.539)	14.00 (0.551)	14.30 (0.563)
L	0.40 TYP (0.016 TYP)			1.2 TYP (0.047 TYP)			0.5 TYP (0.020 TYP)			1.2 TYP (0.047 TYP)			1.2 TYP (0.047 TYP)		
e	0.8 TYP (0.0315 TYP)			0.8 TYP (0.0315 TYP)			0.55 TYP (0.021 TYP)			0.1 TYP (0.0394 TYP)			0.8 TYP (0.0315 TYP)		
B1	0.30 (0.012)	0.40 (0.016)	0.50 (0.020)	0.30 (0.012)	0.40 (0.016)	0.50 (0.020)	0.30 (0.008)	0.40 (0.012)	0.50 (0.016)	0.30 (0.012)	0.40 (0.016)	0.50 (0.020)	0.30 (0.012)	0.40 (0.016)	0.50 (0.020)
C	0.2 TYP (0.008 TYP)			0.2 TYP (0.008 TYP)			0.2 TYP (0.008 TYP)			0.2 TYP (0.008 TYP)			0.2 TYP (0.008 TYP)		

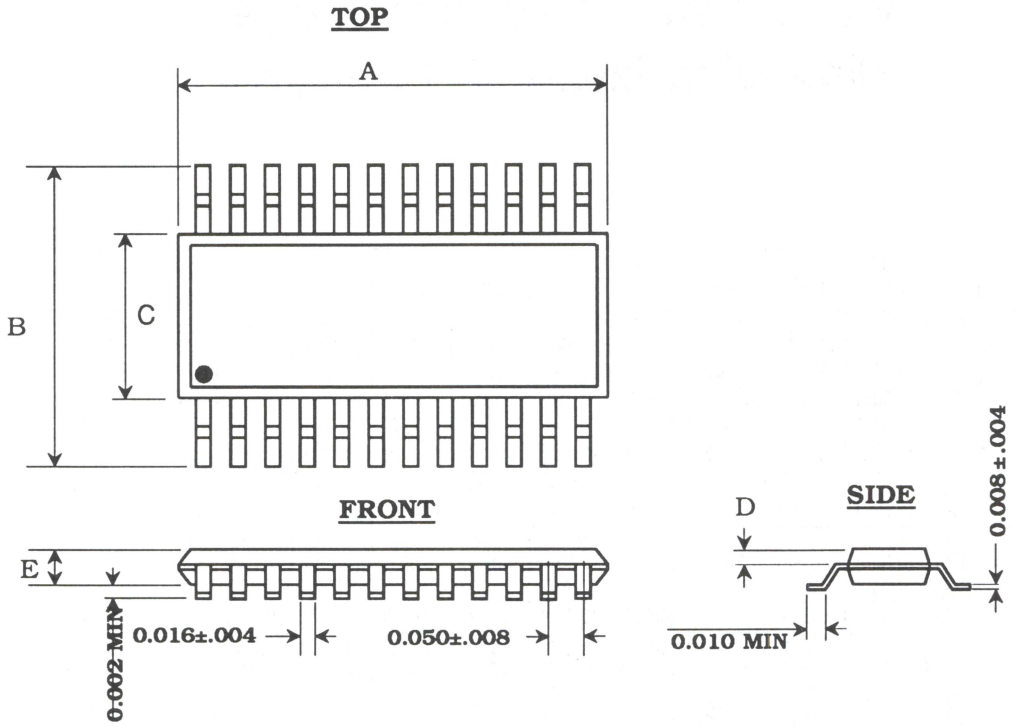
*ALL DIMENSIONS ARE IN MM (INCHES)

JEDEC Metric Quad Flat Package Dimension Table ("Q" Package)

LEAD COUNT	44LD			52LD			64LD			80LD		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	1.81 (0.071)	2.13 (0.084)	2.35 (0.093)	1.81 (0.071)	2.13 (0.084)	2.35 (0.093)	2.55 (0.100)	2.80 (0.110)	3.30 (0.130)	2.68 (0.106)	3.04 (0.120)	3.30 (0.130)
A1	0.00 (0.000)	0.13 (0.005)	0.25 (0.010)	0.00 (0.000)	0.13 (0.005)	0.25 (0.010)	0.00 (0.000)	0.13 (0.005)	0.25 (0.010)	0.00 (0.000)	0.13 (0.005)	0.25 (0.010)
A2	1.95 (0.077)	2.00 (0.079)	2.10 (0.083)	1.95 (0.077)	2.00 (0.079)	2.10 (0.083)	2.55 (0.100)	2.80 (0.110)	3.05 (0.120)	2.55 (0.100)	2.80 (0.110)	3.05 (0.120)
D	12.95 (0.510)	13.20 (0.520)	13.45 (0.530)	12.95 (0.510)	13.20 (0.520)	13.45 (0.530)	16.95 (0.667)	17.20 (0.677)	17.45 (0.687)	22.95 (0.904)	23.20 (0.913)	23.45 (0.923)
D1	9.90 (0.390)	10.00 (0.394)	10.10 (0.398)	9.90 (0.390)	10.00 (0.394)	10.10 (0.398)	13.90 (0.547)	14.00 (0.551)	14.10 (0.555)	19.90 (0.783)	20.00 (0.787)	20.10 (0.791)
E	12.95 (0.510)	13.20 (0.520)	13.45 (0.530)	12.95 (0.510)	13.20 (0.520)	13.45 (0.530)	16.95 (0.667)	17.20 (0.677)	17.45 (0.687)	16.95 (0.667)	17.20 (0.677)	17.45 (0.687)
E1	9.90 (0.390)	10.00 (0.394)	10.10 (0.398)	9.90 (0.390)	10.00 (0.394)	10.10 (0.398)	13.90 (0.547)	14.00 (0.551)	14.10 (0.555)	13.90 (0.547)	14.00 (0.551)	14.10 (0.555)
L	0.65 (0.026)	0.80 (0.031)	0.90 (0.037)	0.65 (0.026)	0.80 (0.031)	0.90 (0.037)	0.65 (0.026)	0.80 (0.031)	0.95 (0.037)	0.65 (0.026)	0.80 (0.031)	0.95 (0.037)
e	0.80 BSC (0.0315 BSC)			0.65 BSC (0.026 BSC)			0.80 BSC (0.0315 BSC)			0.80 BSC (0.0315 BSC)		
B1	0.30 (0.012)	0.35 (0.014)	0.45 (0.018)	0.22 (0.009)	0.26 (0.010)	0.35 (0.014)	0.30 (0.012)	0.35 (0.014)	0.45 (0.018)	0.30 (0.012)	0.35 (0.014)	0.45 (0.018)
C	0.13 (0.005)	–	0.23 (0.009)	0.13 (0.005)	–	0.23 (0.009)	0.13 (0.005)	–	0.23 (0.009)	0.13 (0.005)	–	0.23 (0.009)

* ALL DIMENSIONS ARE IN MM (INCHES)

Japanese Small Outline Package ("K" Package)

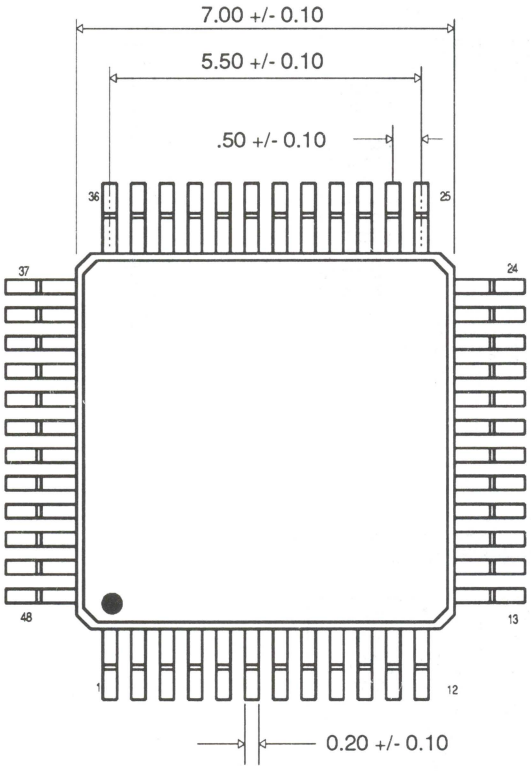


LD COUNT	A	B	C	D	E
	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX
08LD	.185/.209	.232/.256	.165/.181	.026	.055/.063
14LD	.330/.354	.232/.256	.165/.181	.026	.055/.063
16LD	.382/.406	.232/.256	.165/.181	.026	.055/.063
18LD	.429/.452	.295/.319	.205/.221	.031	.066/.074
20LD	.480/.504	.295/.319	.205/.221	.031	.066/.074
22LD	.527/.551	.295/.319	.205/.221	.031	.066/.074
24LD	.578/.602	.295/.319	.205/.221	.031	.066/.074
28LD	.716/.740	.377/.401	.287/.303	.039	.082/.090

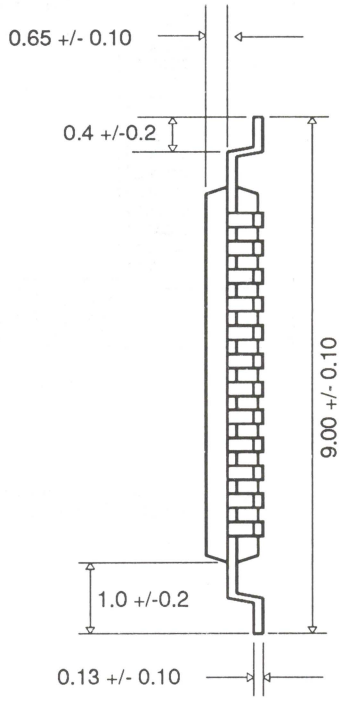
ALL DIMENSIONS ARE IN MM

48LD Very Small Quad Flat Pack ("V" Package)

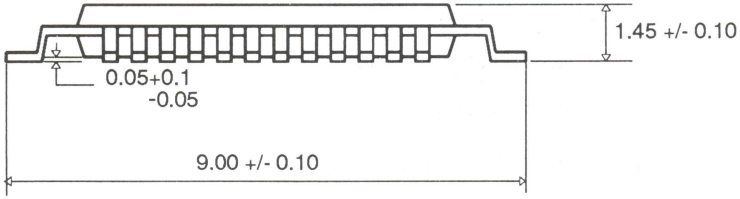
TOP



SIDE



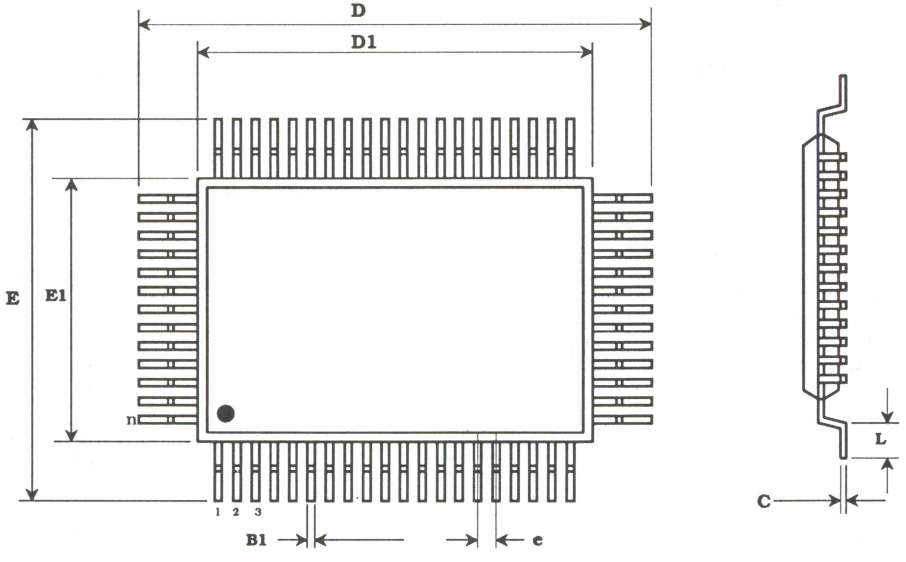
FRONT



*** ALL DIMENSIONS ARE IN MM**

9

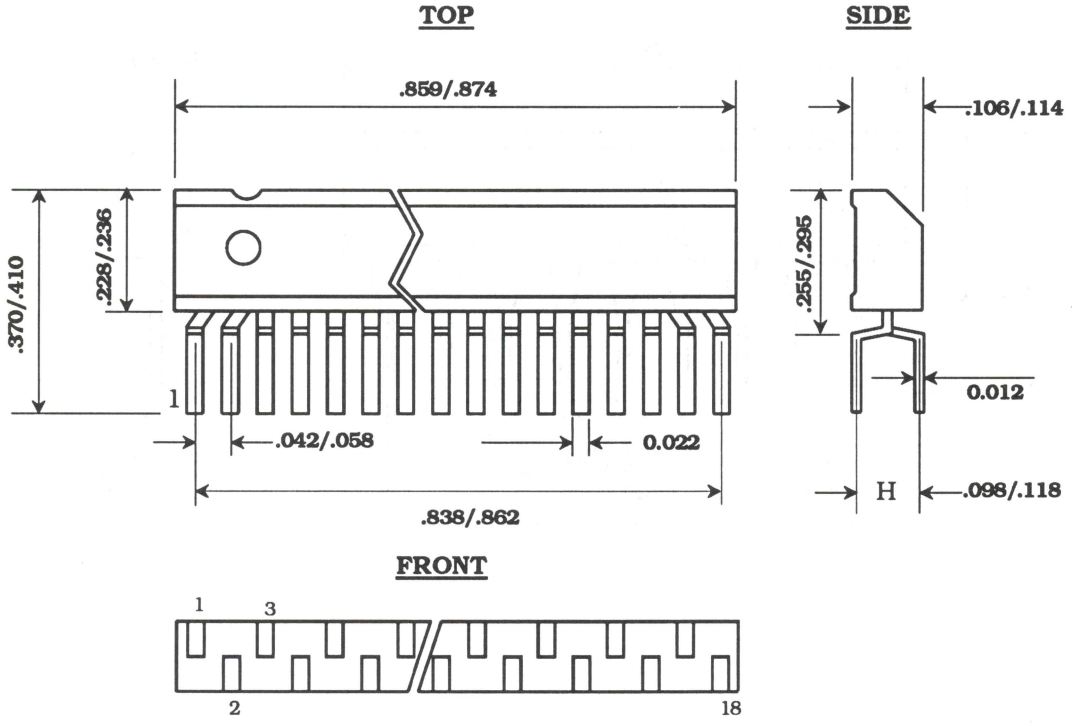
Shrink Quad Flat Pack SQFP ("V" Package)



LEAD COUNT	64LD MIN	NOM	MAX
A1	1.35 (.053)	1.45 (.057)	1.55 (.061)
A1	0.00 (.000)	0.05 (.002)	0.10 (.004)
A2	1.35 (.053)	1.40 (.055)	1.45 (.057)
D	11.70 (.461)	12.00 (.473)	12.30 (.485)
D1	9.80 (.386)	10.00 (.394)	10.20 (.402)
E	11.70 (.461)	12.00 (.473)	12.30 (.485)
E1	9.80 (.386)	10.00 (.394)	10.20 (.402)
L	0.30 (.012)	0.50 (.020)	0.70 (.028)
e	0.50BSC (.0256 BSC)		
B	0.15 (.006)	0.20 (.008)	0.25 (.010)
C	0.120 (.0047)	0.125 (.0049)	0.130 (.0051)

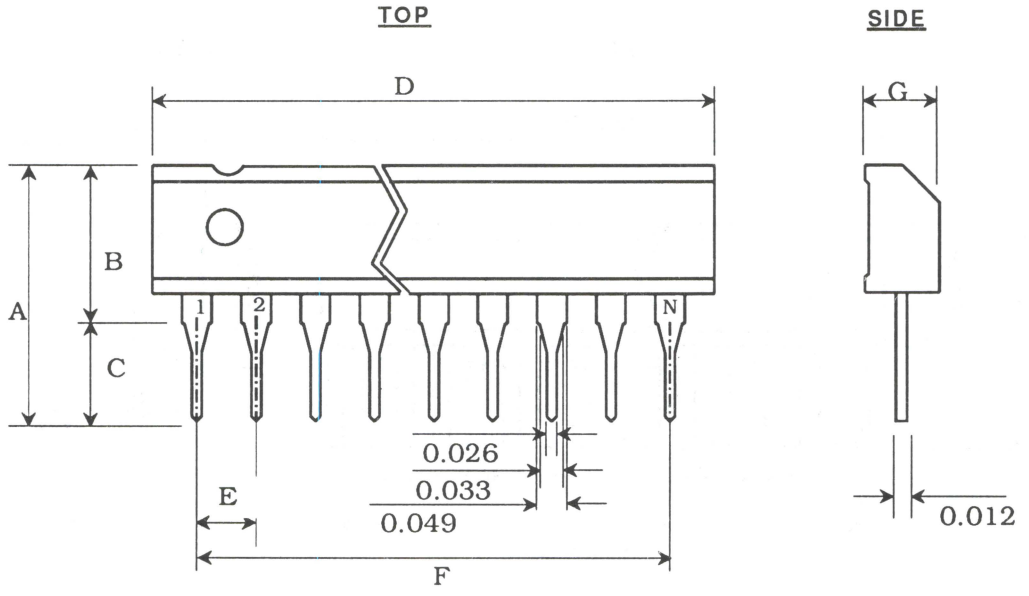
Controlling Dimension in MM (inch)

18LD Staggered In Line Package ("Z" Package)



*ALL DIMENSIONS ARE IN INCHES.

Single In Line Package ("Y" Package)



LD COUNT	A	B	C	D	E	F	G
	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX	MIN/MAX
08LD	.393/.433	.276/.284	.118/.158	.768/.776	.092/.108	.688/.712	.110/.114

ALL DIMENSIONS ARE IN INCHES.

GENERAL INFORMATION 1

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EXAR ...the analog plus™company

AUTHORIZED SALES REPRESENTATIVES AND DISTRIBUTORS

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Authorized Domestic Sales Representatives

ALABAMA

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FAX 205-621-1038

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SYSTEM SALES OF ARIZ.
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2995 Red Hill Ave, Ste 101
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3100 Arapahoe Rd, Ste 404
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FAX 813-442-2234

SEMTRONIC
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2297 E. Blvd
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FAX 317-457-7732

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FAX (319) 393-7224
TWX 910-525-1331

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DLE ELECTRONICS
6572 East Central
Wichita, KS 67206
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FAX 316-683-9367

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LOUISIANA
(See Texas)

MAINE
(See Massachusetts)

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FAX 410-740-0076

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A/D SALES
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Tewksbury, MA 01876
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FAX 508-851-5555

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NEVADA
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Haddonfield, NJ 08033
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2403 San Mateo, NE, #W-5
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Dallas, TX 75248
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BRAVO SALES INC.
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FAX 713-320-0212

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Murray, UT 84107
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Glendale, WI 53217
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(See Minnesota)

WYOMING
(See Colorado)

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FAX 416-840-6091

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Quebec, Canada H9R 4H7
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A-2380 Perchtoldsdorf
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FAX 43-222-863257

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Volta, III Brooklin
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FAX 5511 241-3382

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DK-2970 Horesholm
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FAX 45-42-572299

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Milton Keynes MK 1 1NN
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FAX 44-908-270380

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FAX 43-222-6106610

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0220 Espoo , Finland
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FAX 358-042-8932

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Drentestraat 7 1083HK
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FAX 31-20-423-948

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Shankarpuram, Bangalore
560 004, India
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FAX 91-81-2643495

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VECTRONICS LTD.
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Herzlia B 46120, Israel
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FAX 972-52-556508

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20151 Milano, MI, Italy
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FAX 39-2-38-006789

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FAX 03-3445-5333

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213 Japan
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FAX 044-877-4268
TLX 3842272 CTCEC J

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P.O.Box 7006 Shinjuku Monolith
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Shinjukuku, Tokyo, 163 Japan
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FAX 03-3340-8402
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2020 Skedsmokorset
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Rue Casimiro Freieoa
1900 Lisboa, Portugal
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FAX 351-1-809517

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EXER TECHNOLOGIES
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Tai Thong Hung Industrial Bldg.
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FAX 011-65-741-2971

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UNITRONICS, SA
Plaza España, 18
28008 Madrid, Spain
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FAX 34-1-248-4228

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131 31 Nacka, Sweden
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FAX 46-8-6431195

SWITZERLAND
ASCOM PRIMOTEC AG
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Baden-Dättwil
CH-5405
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TEL 41-56-840171
FAX 41-56-833454

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Taipei 10524, Taiwan
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FAX 011-886-2-768-2517

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FAX (205) 830-5664

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(205) 881-9235

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FAX (205) 722-9348

REPTRON
4835 University Square
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Tempe, AZ 85281
(602) 966-7800
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(602) 968-7140

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9830 S. 51st St, Ste B121
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(602) 496-0290

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Phoenix, AZ 85040
(602) 437-5565
TLX 667317 STERLING PHX

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San Diego, CA 92121
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A.V.E.D.
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Visalia, CA 93291
(209) 734-8661

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FAX 213-258-6932

*BELL INDUSTRIES
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Rocklin, CA 95677
(916) 652-0414

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FAX 408-734-8875

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San Diego, CA 92111
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*BELL INDUSTRIES
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Agoura Hills, CA 91301
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San Jose, CA 95134
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(818) 880-6846

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El Monte, CA 91731-3004
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*MARSHALL
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Irvine, CA 92718-1994
(714) 458-5360

*MARSHALL
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Rancho Cordova, CA
95670
(916) 635-9700

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10105 Carroll Canyon Rd
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(619) 578-9600

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(303) 691-9010

FUTURE ELECTRONICS
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FAX (303) 421-7696

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Englewood, CO 80112
(303) 792-3939

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FAX (203) 269-6527

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Bethel, CT 06801
(203) 743-9594

*MARSHALL
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Barnes Industrial Park
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Wallingford, CT 06492
(203) 265-3822

NU HORIZON
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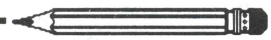


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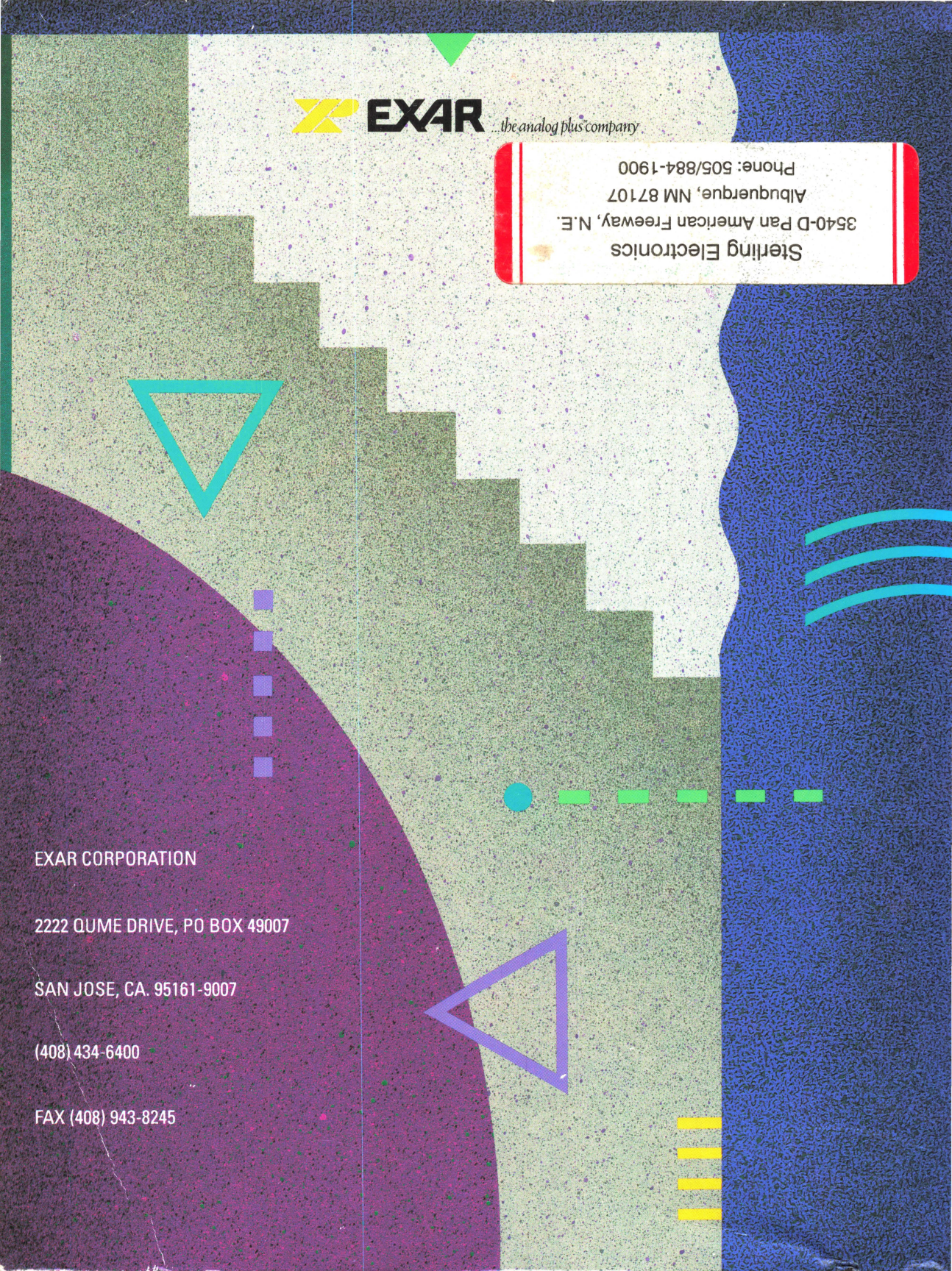
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